50 Micron Pitch Flip Chip Bumping Technology: Processes and Applications

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Outline

- RTI Identity/History
  - Historical development of solder bumping at RTI
- Fine Pitch Solder Bump Technology
  - Fine Pitch Bumping Processes
  - Post Bump Processes
  - Hybridization
- Applications
  - What kinds of devices need fine pitch?
  - Compact Muon Solenoid (CMS)
  - MEDIPIX
- Future directions of fine pitch interconnects
  - 3D integration technology
  - Alternative bump materials
  - VISA-like structures

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Who We Are

Since 1958, our mission has defined us...

- Private, Independent, 501(c)(3), non-profit
- Recognized as the physical and intellectual cornerstone of the Research Triangle Park.
- One of the largest non-profit R&D organizations in the US

RTI International at a Glance

- 2500 employees  
  - half with advanced degrees  
  - multidisciplinary
- FY05 revenues of $467.7M
- Broad array of clients

Select Clients

- Government clients:
  - DOD
  - DOE
  - NASA
  - EPA
  - USAID
  - DHHS

- Commercial clients:
  - Eastman Gasification Services
  - Süd Chemie
  - Air Liquide
  - BOC
  - Chevron-Texaco
  - General Electric
RTI International Practice Areas

- Defense
- Homeland Security
- Education and Training
- Health and Pharmaceuticals
- Energy, Environment, and Natural Resources
- International Development
- Advanced Technology

Who We Used To Be...

- The acquisition of MCNC-RDI was completed in March 2005

RTI International to Acquire Three Divisions of MCNC’s Research and Development Institute

Research Triangle Park, N.C. (Sept. 15, 2004) — As part of a strategy to strengthen its core research and development capabilities, RTI International today announced that it intends to acquire three research divisions of MCNC’s Research and Development Institute (MCNCRDI) later this year.

The research divisions being acquired include MCNC’s Signal Electronics Division, Materials and Electronic Technologies Division and Advanced Network Research Division. MCNC’s Grid Computing and Ventures business units are not included in the RTI acquisition.
A Brief History of Flip Chip Development at RTI

• 1965: IBM introduces Controlled Collapse Chip Connection (C4) process
  - Evaporated high-lead solder bumps onto an evaporated Cr/Cr-Cu/Cu/Au thin-film under bump metallurgy (UBM)
  - Shadow mask manually aligned to the wafer to define pad and bump location
  - Minimum bump pitch ~ 225 µm
  - Typical bump height 100-125 µm
  - Expensive – high end applications
A Brief History of Flip Chip Development at RTI

- In the early 1990’s researchers at MCNC develop electroplated solder deposition processes to replace evaporation
  - Patterned photoresist replaces shadow mask as the bump deposition template
  - Alignment between wafer features and bumps is improved through photolithography
  - Minimum bump size and pitch is now “theoretically” not limited
- 90/10 – 97/3 Pb/Sn solder bump composition
- UBM structure is still based on IBM Cr/Cr-Cu/Cu
- Awarded DARPA contract to further develop this technology for commercial and government use, created the Flip Chip Technology Center

Electroplated Bump Process Flow

Incoming Wafer
With I/O Pads

Repassivation

UBM Deposition

Apply and Define Plating Template

Plate Solder

Strip Resist Template

Reflow

Etch Field
UBM
A Brief History of Flip Chip Development at RTI

- Mid-1990’s: Several changes to base bumping process are made
- Shift from high lead solder to eutectic Sn/Pb
  - Reduction of MP from high lead to eutectic reduces thermal stress on devices
  - Lower reflow temperature (183°C vs. 312°C) allows a shift from ceramic substrates to organic laminate substrates
- Shift from evaporated to sputtered UBM
  - Less complicated structure, fewer metal layers
  - Suitable for high Sn solders
- Adoption of BCB as repassivation material
  - Extremely low moisture absorption
  - Lower cure temperature than PI
  - Lower dielectric constant

A Brief History of Flip Chip Development at RTI

- 1997: MCNC enters the Seamless High Off-Chip Connectivity (SHOCC) Consortium
  - DARPA program aimed at developing technologies to shift design paradigms from single die approaches to a parallel manufacturing approach utilizing yield-optimized IC elements connected to a common substrate
  - Required the development of sub-100 µm pitch area array solder bumps to interconnect ICs on the substrate

- 1998: MCNC spins off Unitive Electronics as a for-profit commercial bumping company
  - MCNC continues fine pitch bumping technology as the basis for its advanced packaging research, proof of concept, and prototyping activities
A Brief History of Flip Chip Development at RTI

- March 2005: RTI acquires the research divisions of MCNC-RDI to add additional research capabilities and directions to the Science & Engineering Group

- Present Day: RTI continues to support prototype, proof of concept, and small volume production for emerging and niche applications and research into new areas of advanced packaging and interconnect

Fine Pitch Bumping Processes
Fine Pitch Solder Bumping

- Formation of fine pitch solder bumps uses essentially the same processes as ‘standard’ flip chip
  - Repassivation
  - UBM Deposition
  - Bumping template application
  - Solder Electroplating
  - UBM Etching
  - Bump Reflow
- The main difference is the degree of process control must be high and the margins for error are low

Repassivation

- BCB (Dow Chemical) is applied to the wafer surface
  - Allows for a consistent base material for the bumping process, regardless of the surface of the incoming wafer
  - Provides a stress buffer under the solder bumps
  - Provides protection to the wafer through subsequent process steps
  - Planarizes the wafer surface, evening out topographical differences
  - Vias are photolithographically opened over device I/O pads
  - Must have high degree of control over photolithography process due to BCB process limits
Repassivation

[Diagram showing a cross-section with labels for BCB, Inorganic Dielectric, and Silicon, along with Aluminum Pad and Dicing Street]

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Repassivation

UBM Deposition

- Sputtered thin film metal UBM system
  - Provides excellent contact resistance and adhesion to both BCB surface and I/O metal
  - Structure is engineered to provide good current carrying characteristics for uniform electroplating, but must be thin enough to mitigate undercut during UBM etch
Bumping Template Application

- Typically a thick spin-on photoresist, some require multiple coats
- New dry-film photoresists (DuPont) for wafer level packaging applications
- Alignment of bump template to I/O is critical and more difficult for fine pitch designs
  - Alignment tolerances reduced from +/- 5 µm for typical WLP to +/- 1-2 µm for fine pitch
  - 1X exposure tools make this more difficult
  - Complete development of the template openings is more difficult due to their size
Bumping Template Application

- Comparison of typical flip chip bump template opening to fine pitch

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**Bumping Template Application**

- Dry film photoresist bumping template

**Solder Electroplating**

- Electroplating is the only practical deposition technology for fine pitch bumping
- Any bump material can be used, so long as it is compatible with the UBM and template material and can be electroplated (Sn/Pb, Pb-free, Au, etc)
- Ni/Au pads are used as solder wettable joining pads on mating parts for Sn/Pb bumps
- Wafer level uniformity for fine pitch designs is achieved through
  - Multiple cathode contact points around the perimeter of the wafer
  - An good current-carrying plane (UBM)
  - Plating cell design, solution flow dynamics
  - Changes to the plating current profile: DC→pulse plating
UBM Etch

- Removal of field UBM metal to electrically isolate the bumps
- Typically achieved through chemical etching, but some metals are removed through dry etching/plasma processes
- Control of bump undercut is extremely important for fine pitch designs
  - 250 μm base diameter with 2 μm undercut on each side → 246 μm effective base diameter, 1.6% loss
  - 25 μm base diameter with 2 μm undercut on each side → 21 μm effective base diameter, 16% loss
  - Loss of bump base contact area = reduced bump strength

Reflow

- Bumps are melted in an inert atmosphere with a reducing agent (usually flux) to form the familiar spherical shape
- Flux residues are removed from the wafer after reflow with solvents
Reflow

Post-Bumping Wafer Thinning

- Wafer thinning is done after bumping to prevent excessive handling and processing of thin wafers
- A protective coating is applied to the wafer to protect the bumps during the taping, thinning, and de-taping processes
- Wafer thinning process consists of two steps
  - Grind: to quickly remove Si from the wafer backside
  - Stress relief: to remove the damaged Si layer and alleviate the stress created in the silicon during the grind
- Protective layer is removed prior to dicing
Dicing Considerations

- Thinned wafers are more susceptible to chipping damage during dicing and require different blades and parameters.
- Dicing kerf must be very close to the active area (50 µm or less) on some devices to allow close placement in multi-chip module assembly.
- Thin, high resistivity silicon sensor wafers are susceptible to chipping and microcracking during dicing, which increases the leakage current.

Poorly Diced Sensor Wafers
ROC Dicing

Cleanly Diced Sensor

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Assembly

- High throughput flip chip assembly tools usually do not have the placement accuracy to reliably place fine pitch bumped devices
  - Need <5 \( \mu \text{m} \) placement accuracy
- MCM assemblies usually have neighboring die edges placed <150 \( \mu \text{m} \) apart
  - Chip placement process must not disturb previously placed devices
- Flux is undesirable in the assembly process
  - Difficult to remove flux residues from under large chips with very small standoff gap

Post-Assembly Chip Standoff Gap

![Graph showing the relationship between bump pitch (micron) and gap between chip and substrate.](image)
Standard Vs. Fine-Pitch Assembly

- Chip-to-substrate gap reduces from 65µm to 22µm for 25µm diameter bumps

Plasma Assisted Dry Soldering (PADS)

- Replaces flux in assembly process
- Solder-bearing parts treated prior to assembly
- Short (10-15 min) treatment time
- Leaves no residues on chip or substrate
- Proven applications in SMT, MEMS, photonics, flip chip packaging
- Patented
Who Needs Fine Pitch Bumping?

ITRS Roadmap For Bump Pitch

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<th>2009</th>
<th>2012</th>
<th>2015</th>
<th>2018</th>
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<td>0.65 mm</td>
<td>0.65 mm</td>
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<td>0.5 mm</td>
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<td>CSP Bump Pitch</td>
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<td>Flip Chip Bump Pitch</td>
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<td>90 μm</td>
<td>80 μm</td>
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From: ITRS 2004 Update
Devices That Require Fine Pitch Bumping

- Pixelated Detector Arrays
  - High energy physics particle detectors
  - X-Ray imaging detectors
- Smart Pixel Arrays
  - Optoelectronic element arrays of VCELS, photodetectors
- MEMS
- High Performance I/C’s & Processors
- 3D Integrated Electronics
  - Focal plane arrays

Characteristics of Fine Pitch Devices

- High interconnect counts, from a few thousand to over 65,000
- Large chip size (~ 1 cm² and larger)
- Many are pixelated devices for imaging and detection
  - Small pixel size gives higher resolution to image
- Mating devices are typically both made of silicon, thus reducing CTE reliability issues
- Wirebond terminals and bumps are commonly needed on the same device
The Compact Muon Solenoid (CMS)

- High energy physics particle detector being built at CERN in Switzerland for the Large Hadron Collider (LHC)
- Goals of CMS
  - Explore physics at the TeV scale
  - Find the Higgs boson, the subatomic particle in the Standard Model theorized to regulate mass
  - Study heavy ion collisions
- RTI is building part of one of the particle detectors that will be at the core of the system by bump bonding readout chips and sensor devices together into MCMs of different sizes

The CMS System

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CMS Detector Modules

- Readout chips are fabricated on full thickness 8-inch silicon wafers and are thinned to 200 µm prior to assembly, 4160 bumps per chip
- Sensor wafers are fabricated on 350 µm thick high resistivity wafers
- Bump size is 25 micron base diameter with a minimum I/O pitch of 50 microns
- 6 different module sizes: 1x1, 1x2, 1x5, 2x3, 2x4, 2x5
- Full detector will require over 800 total modules with about 5000 individual readout chips
- Total number of bumped connections is over 19,000,000

Solder Bumped CMS ROC
Solder Bumped CMS ROC

Solder Bumped ROC and Sensor (US-CMS)
Pixilated Detector Module Assemblies

CMS single and multi-chip sensor modules

2x4 detector module in test fixture

Courtesy: US-CMS FPix Collaboration

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CMS Yield Data

- Recent evaluation of CMS FPix detector modules (61 total modules, 1,626,560 bump connections)
  - Bump bonding yield of 99.66%
  - 60 of 61 modules meet leakage current specifications at 250V
  - 59 of 61 modules meet leakage current specifications at 600V
  - Power consumption on all modules within spec

Courtesy: US-CMS FPix Collaboration

MEDIPLEX Consortium - CERN

- X-ray/gamma ray detector devices working in single photon counting mode
- 55 µm pitch, uniform in both directions
- Detector modules of 1x1 (~1 in²) and 2x2 (~4 in²)
- MEDIPLEX ASIC is used in conjunction with different sensor devices for a number of applications
  - X-ray imaging
  - Biological radiography
  - Neutron detection
MEDIPIX Detector Module
Future Hybridization Technologies

- 3D Integration
- Alternative Bump Materials
- Alternative Singulation Processes

3D Integration

- Through via interconnects (TVI) are formed through bulk silicon in active devices
- Allows multiple device layers to be interconnected front-to-back
- TVIs can be formed before or after devices are physically joined together
  - Significant process differences between vias-first process and vias-last process
  - Process used dictated by device design and process compatibility
- Allows array sizes that are not limited to 1xN or 2xN modules: true area array ROC placement
Benefits of 3D Integration: Pixelated Devices

- 3-D Integration allows massively parallel signal processing
- Dramatically increased electronic functionality in each pixel

Detector/Sensor Arrays
- 3-D Sensor Arrays
  - Large formats with high resolution
  - On-chip signal processing
  - Reduction of size, weight & power

Actuator Arrays
- 3-D Actuator Arrays
  - Large formats with high resolution
  - Low switching energy & latency
  - Reduction of size, weight & power

Test Structure Operability Test

- Demonstrated 99.98% operability in 256x256 arrays with 4 µm vias on 30 µm pitch
Alternative Bump Materials

- Non-collapsible bump materials may be useful for extremely small bump interconnections (~5 µm dia.)

Sn-capped Cu bumps

Alternatives to Saw Dicing

- Silicon etching using Bosch process allows damage-free singulation of ROCs and sensor devices
- Dicing streets must be free of metal

Deposit and pattern photoresist

Bosch etching complete

Bosch etching

Photoresist removal
Conclusion

- RTI has developed the processes for fine pitch bumping and assembly and supports prototype, small volume, and leading edge applications
- A growing infrastructure to support back end processes such as dicing and grinding is in place
- While large volume applications for fine pitch flip chip bumping do not exist yet, there are special applications which are using this technology today

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