Trends in IC Packaging and Multicomponent Packaging

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www.electronic트rendpubs.com
What’s Affecting the Economy

- Cost of transportation of goods — Gasoline costs fluctuate, oil reserves will eventually be consumed
- Housing crisis
- Tightening credit markets / Collapse of the financial markets
- Tightening wallets – lack of consumer confidence
- Collapsing world economies

Thoughts on the Economy

- The first nine months of 2008 were positive
- No excess inventories to burn off this time around; different from the 2000 down turn
- Falling oil prices make the price of all goods less expensive; more money left over for other goods and services
- Lower interest rates should stimulate the economy
- All major countries putting forth a stimulus package
- Financial markets need to be stable; Credit markets need to reliable
- We don’t need a “killer application”, rather just good products the general public wants to purchase
Today’s Demand for Electronics

Worldwide IC Packaging Units by Package Family

2007—151 Billion Units
Worldwide IC Packaging Units by Package Family

2012—262 Billion Units

Worldwide IC Packaging “Revenue” by Package Family

2007—$30.5 Billion
Worldwide IC Packaging “Revenue” by Package Family

- FBGA/DSBGA: 29.8%
- BGA: 32.5%
- QFP: 14.9%
- QFN: 4.1%
- PGA: 2.1%
- WLP: 2.4%
- DIP: 0.9%
- SOT: 0.8%
- TSOP: 4.8%
- DFN: 0.8%
- CC: 0.4%

2012—$47.1 Billion

Worldwide Contractor IC Packaging Units by Package Family

- FBGA/DSBGA: 13.2%
- BGA: 5.3%
- PGA: 0.2%
- QFN: 13.0%
- QFP: 11.0%
- TSOP: 11.9%
- DFN: 2.4%
- CC: 1.4%
- WLP: 3.5%
- DIP: 6.8%
- SOT: 3.2%
- SO: 28.1%

2007—48.7 Billion Units
Worldwide Contractor IC Packaging Units by Package Family

- FBGA / DSBGA: 19.6%
- QFN: 18.2%
- QFP: 10.0%
- TSOP: 8.9%
- SO: 22.0%
- BGA: 6.6%
- PGA: 0.2%
- WLP: 3.9%
- DIP: 4.2%
- SOT: 2.3%
- SO: 22.0%
- TSOP: 8.9%
- BGA: 6.6%
- SO: 22.0%
- TSOP: 8.9%
- SO: 22.0%
- FBGA / DSBGA: 30.1%
- QFP: 15.8%
- QFN: 15.8%
- PGA: 4.9%
- BGA: 25.9%
- DIP: 1.8%
- WLP: 1.8%
- SO: 0.3%
- DFN: 0.3%
- CC: 0.8%
- QFN: 4.9%
- BGA: 25.9%
- QFP: 15.8%
- QFN: 15.8%
- PGA: 4.9%
- BGA: 25.9%
- DIP: 1.8%
- WLP: 1.8%
- SO: 0.3%
- DFN: 0.3%
- CC: 0.8%

2012—84.1 Billion Units

2007—$12.1 Billion
Worldwide Contractor IC Packaging Revenue by Package Family

2012—$22.5 Billion

Developments in IC Packaging

1. The number of stacked packages is increasing; there is a great interest in 3D or through silicon vias (TSV)

2. Increased integration – such as combining an SOC within a SiP, and embedding an active die within the substrate

3. WLPs continue to grow; creating WLPs which are of a standardized size while taking advantage of wafer level processing is the new twist in this technology
What are Multicomponent Packages?

<table>
<thead>
<tr>
<th>Stacked Packages</th>
<th>SiP (System in Package)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple die stacked within a package (die stack), or multiple packages stacked on top of each other (package stack), or a combination of the two.</td>
<td>One or more ICs, can be combined with passives, into a functional block, typically in a JEDEC footprint. Fewer I/O and higher price per I/O when compared with stacked packages</td>
</tr>
</tbody>
</table>

Fab and Fabless Companies with SiPs and Stacked Packages

- Advanced Micro Devices
- Akita Elpida Memory, Inc.
- BeSang, Inc.
- Casio Computer Co., Ltd.
- Elpida Memory, Inc.
- Endicott Interconnect Technologies, Inc.
- Fairchild Semiconductor
- Freescale Semiconductor, Inc.
- Hitachi, Ltd.
- Hynix Semiconductor
- IBM
- IBM Japan, Ltd.
- Infineon Technologies
- Intel Corporation
- Matsushita Electric Industrial Co., Ltd.
- Micron Semiconductor Asia Pte., Ltd.
- Micron Technology, Inc.
- National Semiconductor
- NEC Electronics Corporation
- Nokia
- Nokia Japan Co., Ltd.
- Oki Electric Industry
- Panasonic Electronic Devices Corporation
- Panasonic Factory Solutions
- Philips Electronics
- Renesas Technology Corporation
- Samsung Electronics Co., Ltd.
- Sanyo Electric Co., Ltd.
- Sharp Corporation
- Skyworks Solutions, Inc.
- Spansion /FASL
- STMicroelectronics
- Tezzaron Semiconductor Corporation
- Toshiba Corporation
- Triquint Semiconductor, Inc.
Contract Companies offering SiPs and Stacked Packages

- 3-D Plus
- Advanced Interconnect Technologies, Inc. (AIT)
- Amkor Technology, Inc.
- ASAT, Limited
- ASE Group
- Bridge Semiconductor Corporation
- Carsem
- ChipMOS Technologies, Inc.
- CORWIL
- EEMS Italia SpA
- Engent, Inc.
- Epson Electronics America, Inc./Seiko Epson
- Flextronics
- FlipChip International, LLC
- Fujitsu Microelectronics America, Inc.
- Hana Microelectronics, Inc.
- I2A
- Inapac Technology, Inc.
- Irvine Sensors, Microelectronics Product Division
- Kingspak Technology, Inc.
- Kingston Technology Company
- Mitsui High-tec, Inc.
- Orient Semiconductor Electronics (OSE)
- Payton Technology Corporation
- Shinko Electric Industries Co., Ltd.
- Siliconware Precision Industries Co., Ltd. (SPI)
- SimpleTech
- SMART Modular Technologies, Inc.
- STATS ChipPAC, Ltd.
- Sysflex, Inc.
- Unisem Group
- UTAC
- Valtronic SA
- Vate Technology Co., Ltd.
- VLSIP Technologies, Inc.
- ZyCube Co., Ltd.

IP Companies with SiP or Stacked Package Designs

- Association of Super Advanced Electronics Technologies (ASET)
- CEA-Grenoble—leti
- Center for Power Electronics Systems (CPES)
- Cubic Wafer
- EOL
- Entorian Technologies Inc.
- ERSO
- Fong Chia University
- Fraunhofer Institute for Reliability & Microintegration IZM
- Georgia Institute of Technology / Packaging Research Center
- Hong Kong University of Science and Technology
- Hongik University
- IMEC’s Advanced Packaging and Interconnect Center (APIC)
- Industrial Technology Research Institute (ITRI)
- Institute of Microelectronics (IME)
- KAIST
- Kyushu Institute of Technology
- Los Alamos National Laboratory, Air Force Research Laboratory, General Electric
- Rensselaer Polytechnic Institute
- RTI International
- State University of New York at Binghamton
- Tessera Technologies, Inc.
- Tohoku University
- Tsukuba Research Center
- University of Arkansas
- University of Southampton
- Vertical Circuits
- Ziptronix
Sampling of End Products Using Stacked Packages

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>Units [M]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cell Phones</td>
<td>1,144</td>
<td>1,215</td>
<td>1,410</td>
<td>1,566</td>
<td>1,700</td>
<td>1,875</td>
</tr>
<tr>
<td>PDAs</td>
<td>19</td>
<td>21</td>
<td>22</td>
<td>22</td>
<td>24</td>
<td>26</td>
</tr>
<tr>
<td>MP3 Players</td>
<td>98</td>
<td>105</td>
<td>115</td>
<td>120</td>
<td>130</td>
<td>160</td>
</tr>
<tr>
<td>Camcorders</td>
<td>17</td>
<td>16</td>
<td>18</td>
<td>19</td>
<td>20</td>
<td>22</td>
</tr>
<tr>
<td>Set-Top Boxes/DVRs</td>
<td>110</td>
<td>120</td>
<td>135</td>
<td>140</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>Digital Cameras</td>
<td>122</td>
<td>125</td>
<td>130</td>
<td>145</td>
<td>155</td>
<td>155</td>
</tr>
<tr>
<td>Notebook Computers</td>
<td>103</td>
<td>125</td>
<td>145</td>
<td>155</td>
<td>190</td>
<td>190</td>
</tr>
<tr>
<td>Desktop PCs</td>
<td>162</td>
<td>170</td>
<td>175</td>
<td>190</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Servers</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>13</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td>Workstations</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Total</td>
<td>1,793</td>
<td>1,972</td>
<td>2,158</td>
<td>2,353</td>
<td>2,697</td>
<td>2,908</td>
</tr>
</tbody>
</table>

Application Breakdown for Stacked Packages, 2008
Cellular Handsets vs. Stacked Packages, 2007–2012

- Die Stack — FBGAs
- PoP or Package on Package (package stack)
- PiP or Package in Package
- Stacked TSOPs, or devices stacked within a TSOP, or a combination of the two
- Stacked QFNs, or devices stacked within a QFN, or a combination of the two
- Stacked MCMs
- Folded Stack
- Stacked WLPs
Stacked Package Units, 2007 vs. 2012

Total Memory Devices in FBGAs
Through silicon vias (TSVs) route the electric signal through all the die in the stack – an alternate method of interconnection in relation to wire bonding or flip chip.

The wafer is thinned, and through vias protrude through the wafer which are filled with copper or other electrically conductive material.

If via last technology, vias are filled in plating baths, slowly and carefully so as not to have voids in the vias.

Redistribution layers can be added between the devices so as to mix and match technologies.

Devices are stacked and vias are connected to other die on a different vertical plane.
3-D Integration / Through Silicon Vias

Via First:
- Via First: Vias can be added as part of the front end process
  - Finer via diameters
  - Improved aspect ratios
  - Eliminate a timely and costly process later to create the TSVs
  - If some wafers created differently from the rest, this not the most efficient from a manufacturing perspective

Via Last:
- Via Last: Vias can be added as part of the back-end process, after the wafer is created, either through the top or bottom of the wafer.
  - Thicker via diameters
  - Larger aspect ratios
  - Additional wafer processing
  - Costly, time consuming, yield issues

TSV Market

TSVs began being used in CMOS image sensors in the spring of 2008. ICs stacked with TSVs will be the next market, and include and combine the following:
- Memory
- RF
- Logic
- Analog
- Logic plus baseband
- Mixed signal
- Processor plus cache memory
- Interface (transceivers)

DRAM stacks with TSVs will occur before NOR flash memory is stacked this way, and processor plus memory possibly may be available as early as the 2011/2012 time frame.
3-D Integration / Through Silicon Vias

3D integration offers the shortest interconnect distance, which results in:
- High speed
- High performance
- Low power consumption
- Smallest form factor

Other Factors of New Technology:
- Complex and slow process
- Low yields
- Expensive

Interconnection of Stacked Packages, 2007 vs. 2012
Companies with TSV Designs

- 3-D Plus
- Association of Super-Advanced Electronics Technologies (ASET)
- Elpida Memory
- Epson America/Seiko Epson
- ERSO/ITRI’s Advanced Packaging Technology Center (APC)
- Fraunhofer Institute for Reliability and Microintegration IZM
- Hong Kong University of Science and Technology
- IBM
- IMEC’s Advanced Packaging and Interconnect Center (APIC)
- Institute of Microelectronics (IME)
- Infineon Technologies
- Intel Corporation
- Irvine Sensors (routing on the sides of Neo-Stacks)
- Micron Semiconductor Asia Pte. Ltd.
- NEC Electronics
- Oki Electric Industry
- Rensselaer Polytechnic Institute
- RTI International
- Samsung Electronics Co., Ltd.
- State University of New York at Binghamton
- Tezzaron Semiconductor Corp.
- University of Albany
- Ziptronix
- ZyCube Co., Ltd. (furthering ASET technology)
IMEC

Figure 5-20 Schematic Presentation of Stacked Embedded Dies

Courtesy of IMEC

ITRI and Feng Chia University

Figure 6-12 Process Steps for C-Trio

Courtesy of ITRI and Feng Chia University
ELECTRONIC TREND PUBLICATIONS

3D Plus

1. Chips placement
2. Potting
3. Pads’ redistribution
4. Diecutting & thinning
5. Test
6. Stacking & 3D interconnect

Figure 8-8: Process to Relicd Wafer

NEC ELECTRONICS, ELPIDA MEMORY, AND OKI ELECTRIC

1 Gbit stacked DRAM with TSV
(512 Mbit x 2 strata)

Molded resin
Silicon lid
FTI
CMOS logic
BGA
Conclusions

• A high level of innovation is the key to furthering the advancement of the IC world. This will bring about more desirable and variable end products, from portable electronics for the consumer to medical devices that will save and/or improve lives.

• Advanced IC packaging technologies are key essentials in bringing forth size reduction and performance, which will ultimately lower costs, and allow for a host of new product launches.

• Technological inspirations and innovations should help fuel demand for electronic products, which could result in the technology sector leading the way out of this recession.