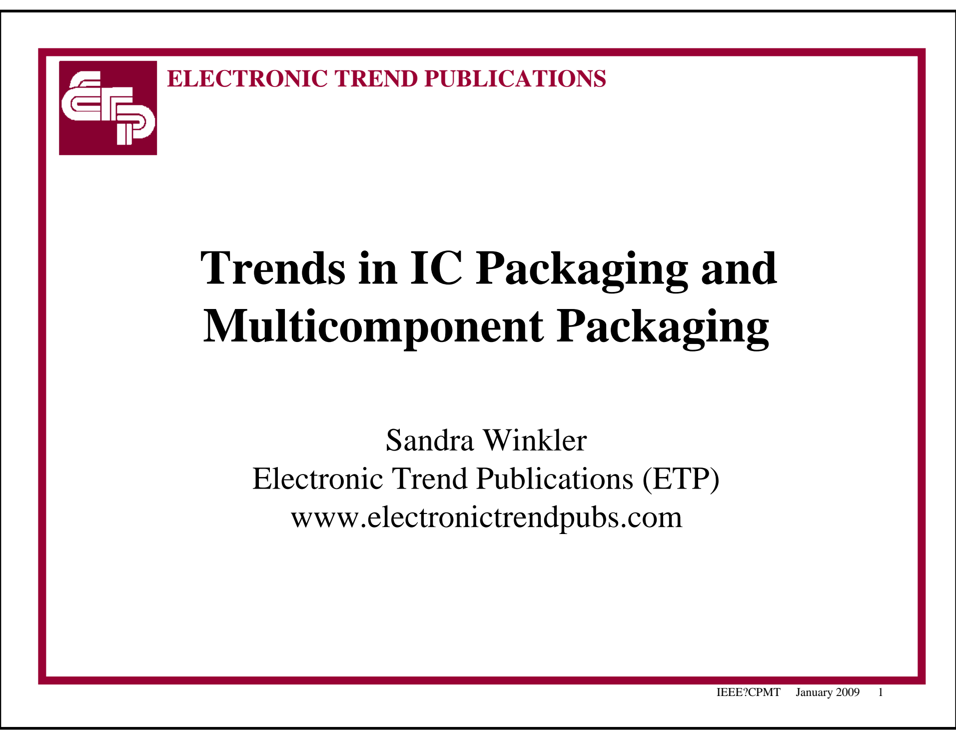
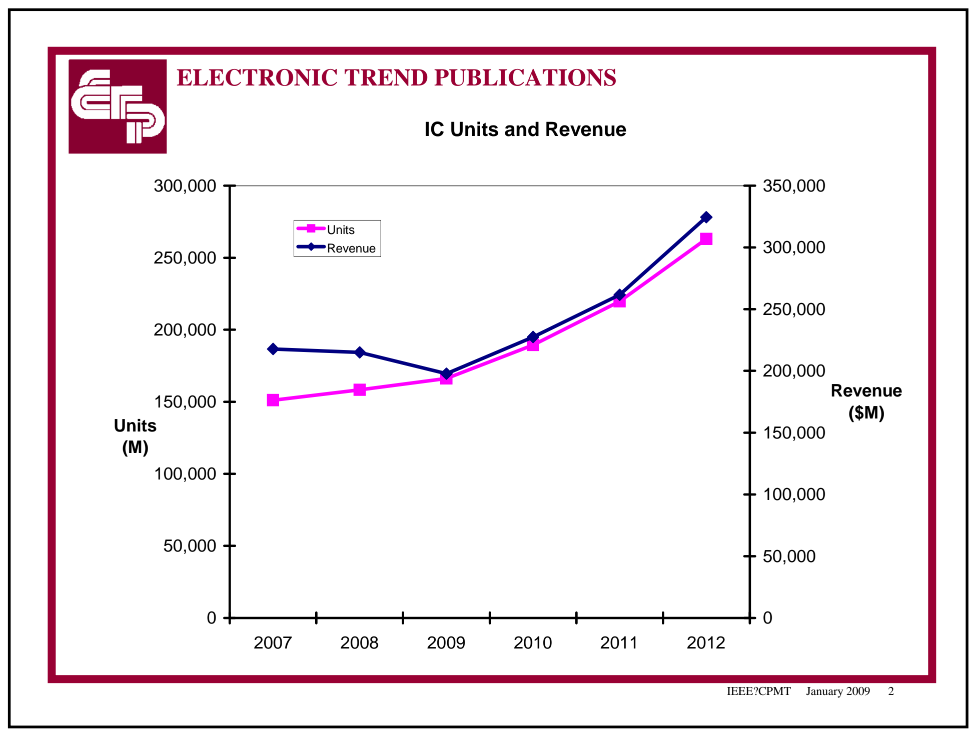

ELECTRONIC TREND PUBLICATIONS
Trends in IC Packaging and Multicomponent Packaging
Sandra Winkler
Electronic Trend Publications (ETP)
www.electronictrendpubs.com
IEEE?CPMT January 2009 1


ELECTRONIC TREND PUBLICATIONS
IC Units and Revenue
Units
Revenue
Units (M)
Revenue ($M)
300,000
250,000
200,000
150,000
100,000
50,000
0
350,000
300,000
250,000
200,000
150,000
100,000
50,000
0
2007
2008
2009
2010
2011
2012
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ELECTRONIC TREND PUBLICATIONS

What's Affecting the Economy

- Cost of transportation of goods — Gasoline costs fluctuate, oil reserves will eventually be consumed
- Housing crisis
- Tightening credit markets / Collapse of the financial markets
- Tightening wallets – lack of consumer confidence
- Collapsing world economies

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Thoughts on the Economy

- The first nine months of 2008 were positive
- No excess inventories to burn off this time around; different from the 2000 down turn
- Falling oil prices make the price of all goods less expensive; more money left over for other goods and services
- Lower interest rates should stimulate the economy
- All major countries putting forth a stimulus package
- Financial markets need to be stable; Credit markets need to reliable
- We don't need a "killer application", rather just good products the general public wants to purchase

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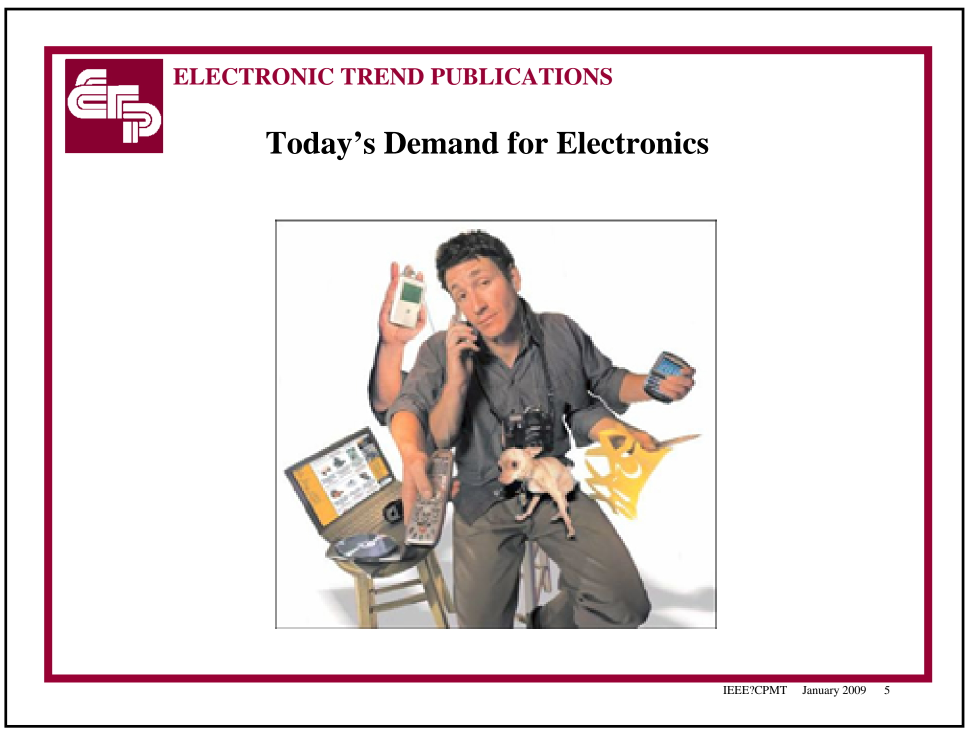
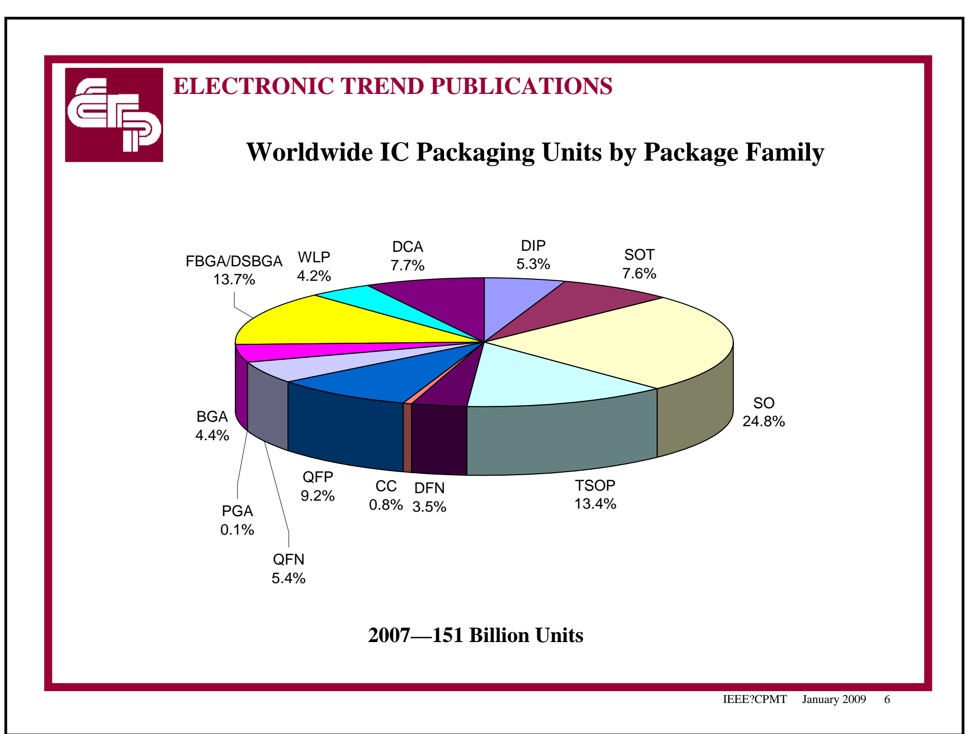

ELECTRONIC TREND PUBLICATIONS
Today's Demand for Electronics
IEEE?CPMT January 2009 5


ELECTRONIC TREND PUBLICATIONS
Worldwide IC Packaging Units by Package Family
FBGA/DSBGA 13.7%
WLP 4.2%
DCA 7.7%
DIP 5.3%
SOT 7.6%
SO 24.8%
TSOP 13.4%
DFN 3.5%
CC 0.8%
QFP 9.2%
QFN 5.4%
PGA 0.1%
BGA 4.4%
2007—151 Billion Units
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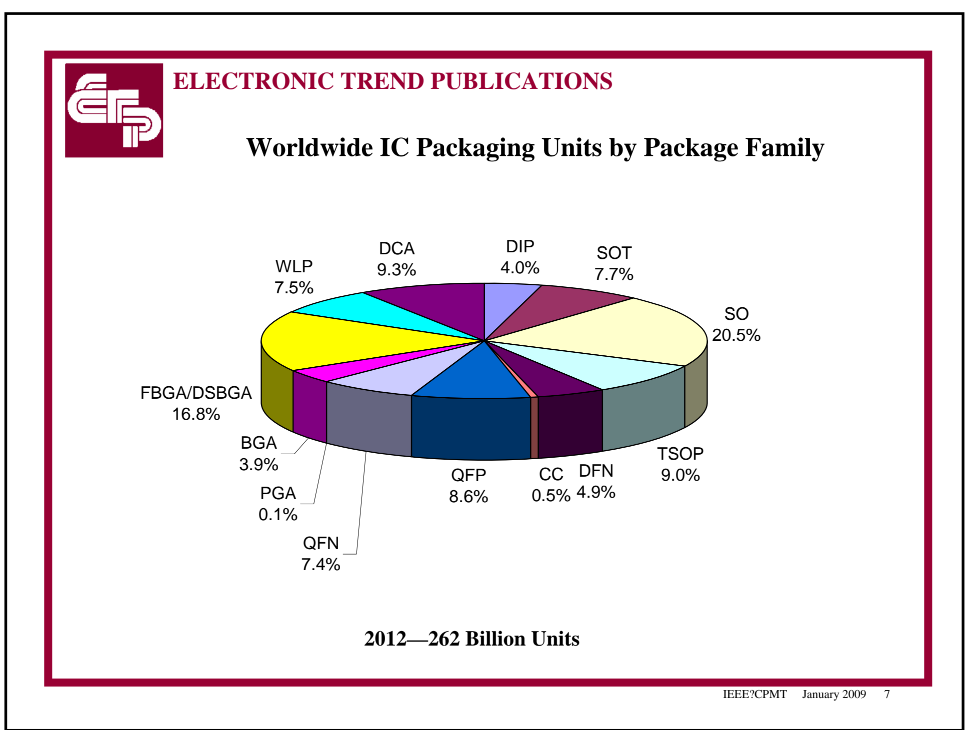
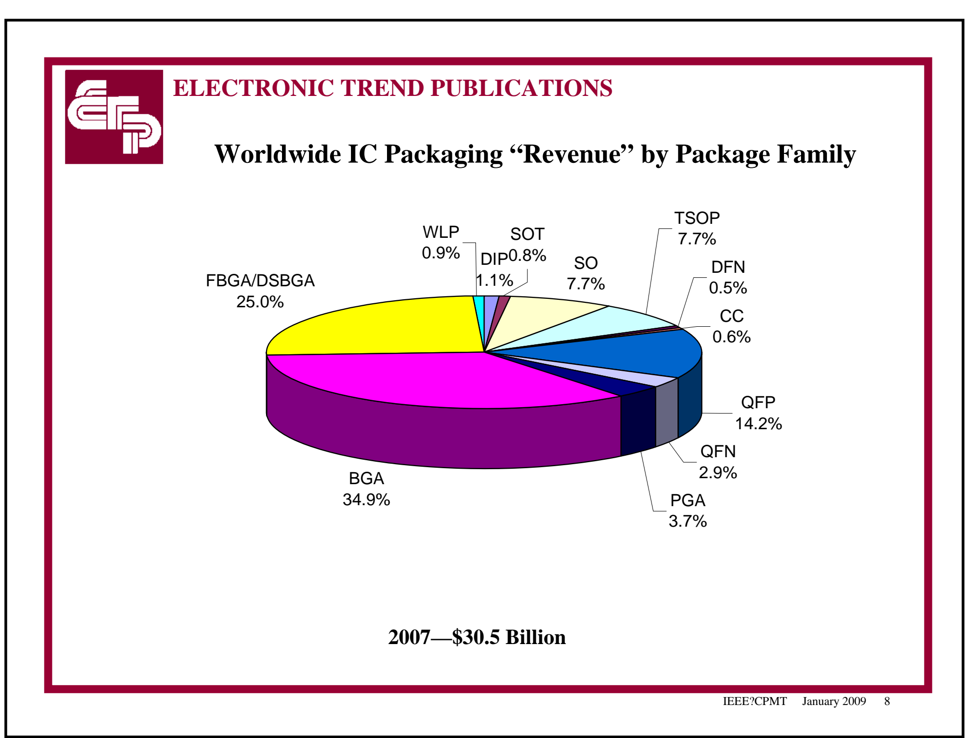
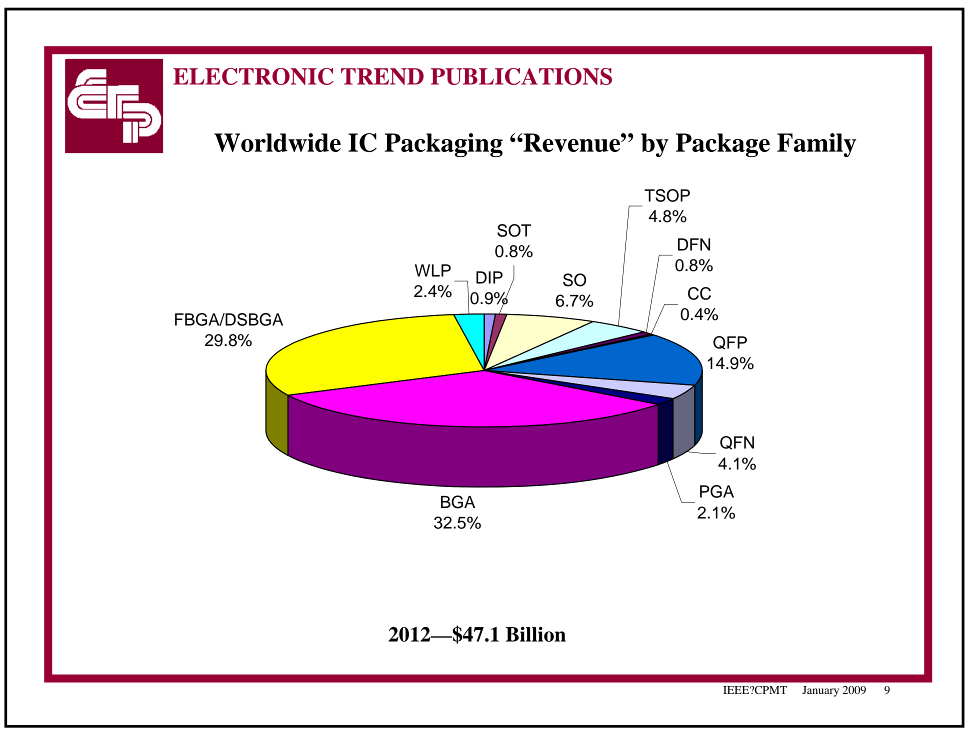

ELECTRONIC TREND PUBLICATIONS
Worldwide IC Packaging Units by Package Family
DIP 4.0%
SOT 7.7%
SO 20.5%
TSOP 9.0%
DFN 4.9%
CC 0.5%
QFP 8.6%
QFN 7.4%
PGA 0.1%
BGA 3.9%
FBGA/DSBGA 16.8%
WLP 7.5%
DCA 9.3%
2012—262 Billion Units
IEEE?CPMT January 2009 7


ELECTRONIC TREND PUBLICATIONS
Worldwide IC Packaging "Revenue" by Package Family
WLP 0.9%
DIP 1.1%
SOT 0.8%
SO 7.7%
TSOP 7.7%
DFN 0.5%
CC 0.6%
QFP 14.2%
QFN 2.9%
PGA 3.7%
BGA 34.9%
FBGA/DSBGA 25.0%
2007—$30.5 Billion
IEEE?CPMT January 2009 8


ELECTRONIC TREND PUBLICATIONS
Worldwide IC Packaging "Revenue" by Package Family
TSOP 4.8%
SOT 0.8%
DFN 0.8%
WLP 2.4%
DIP 0.9%
SO 6.7%
CC 0.4%
FBGA/DSBGA 29.8%
QFP 14.9%
QFN 4.1%
PGA 2.1%
BGA 32.5%
2012—$47.1 Billion
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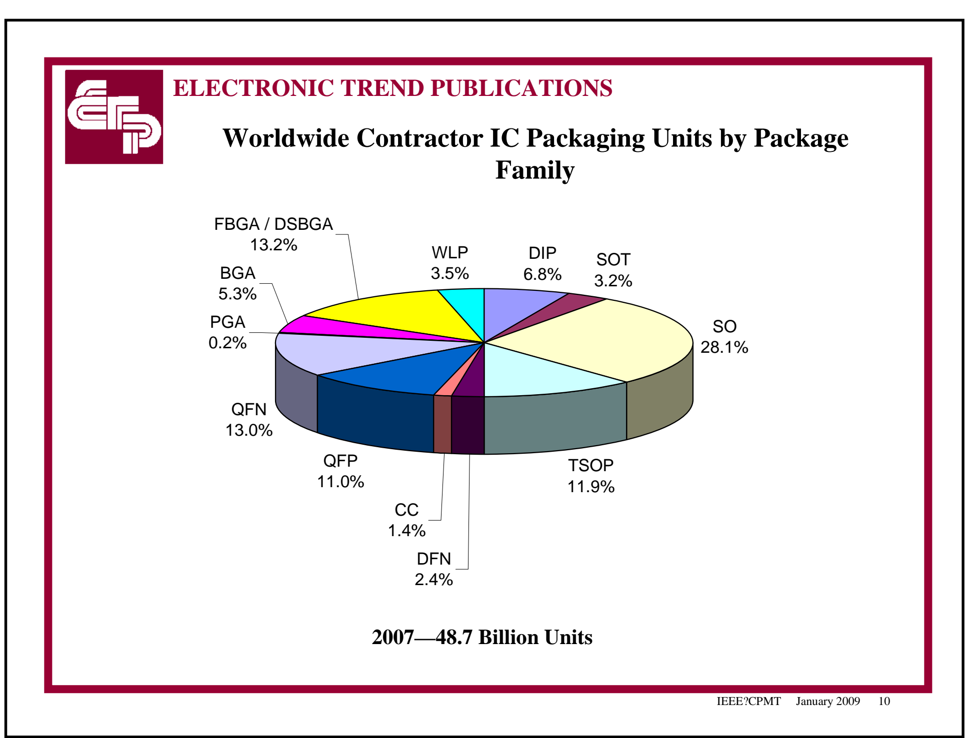
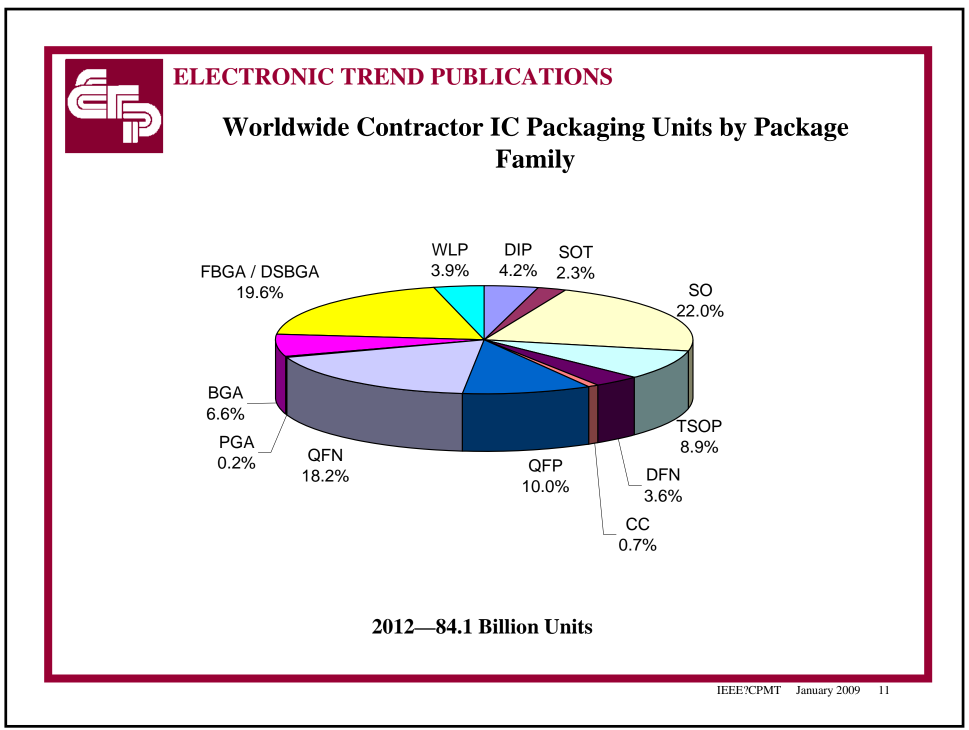
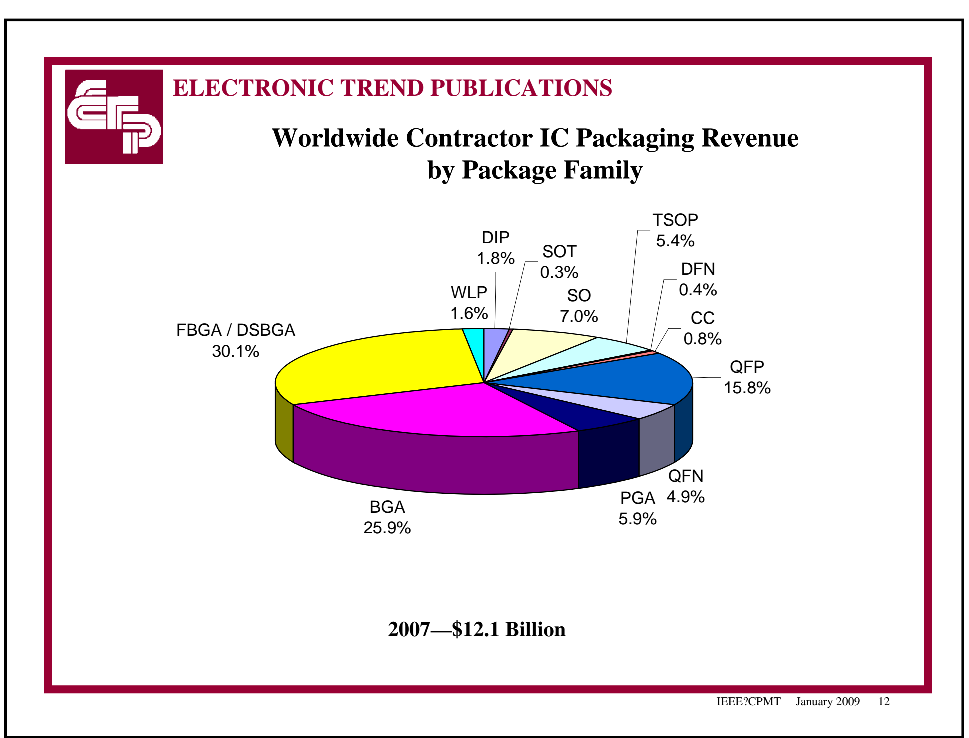
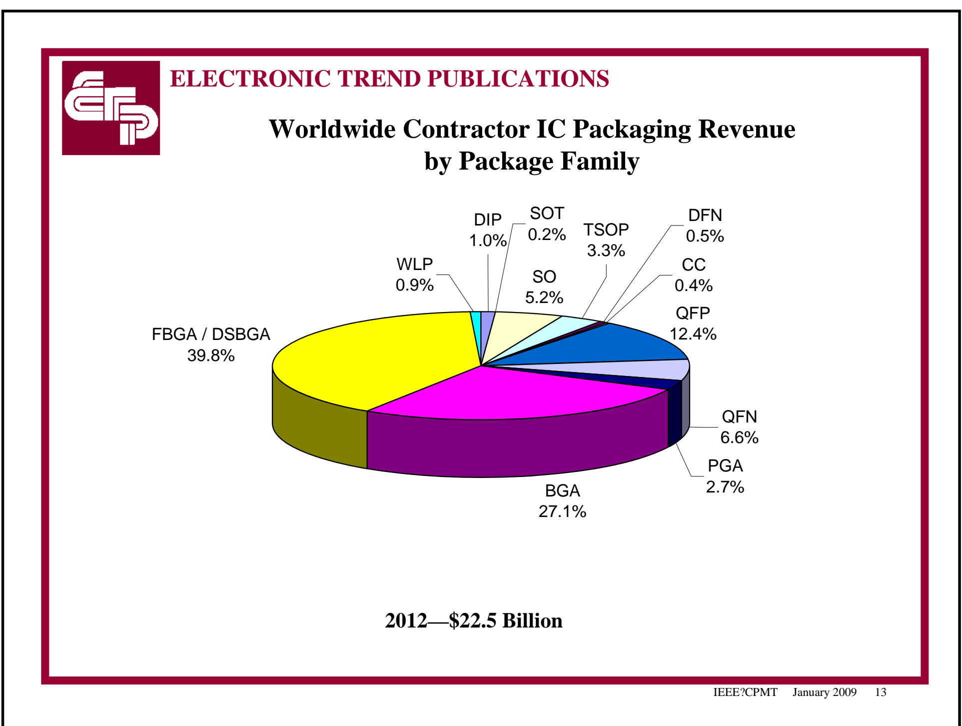

ELECTRONIC TREND PUBLICATIONS
Worldwide Contractor IC Packaging Units by Package Family
FBGA / DSBGA 13.2%
BGA 5.3%
WLP 3.5%
DIP 6.8%
SOT 3.2%
PGA 0.2%
SO 28.1%
QFN 13.0%
QFP 11.0%
TSOP 11.9%
CC 1.4%
DFN 2.4%
2007—48.7 Billion Units
IEEE?CPMT January 2009 10


ELECTRONIC TREND PUBLICATIONS
Worldwide Contractor IC Packaging Units by Package Family
WLP 3.9%
DIP 4.2%
SOT 2.3%
SO 22.0%
FBGA / DSBGA 19.6%
BGA 6.6%
PGA 0.2%
QFN 18.2%
QFP 10.0%
TSOP 8.9%
DFN 3.6%
CC 0.7%
2012—84.1 Billion Units
IEEE?CPMT January 2009 11


ELECTRONIC TREND PUBLICATIONS
Worldwide Contractor IC Packaging Revenue by Package Family
TSOP 5.4%
DIP 1.8%
SOT 0.3%
DFN 0.4%
WLP 1.6%
SO 7.0%
CC 0.8%
FBGA / DSBGA 30.1%
QFP 15.8%
QFN 4.9%
PGA 5.9%
BGA 25.9%
2007—$12.1 Billion
IEEE?CPMT January 2009 12



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Developments in IC Packaging

1. The number of stacked packages is increasing; there is a great interest in 3D or through silicon vias (TSV)

2. Increased integration – such as combining an SOC within a SiP, and embedding an active die within the substrate

3. WLPs continue to grow; creating WLPs which are of a standardized size while taking advantage of wafer level processing is the new twist in this technology

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What are Multicomponent Packages?

Stacked Packages

Multiple die stacked within a package (die stack), or multiple packages stacked on top of each other (package stack), or a combination of the two.

SiP (System in Package)

One or more ICs, can be combined with passives, into a functional block, typically in a JEDEC footprint. Fewer I/O and higher price per I/O when compared with stacked packages

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Fab and Fabless Companies with SiPs and Stacked Packages

- Advanced Micro Devices
- Akita Elpida Memory, Inc.
- BeSang, Inc.
- Casio Computer Co., Ltd.
- Elpida Memory, Inc.
- Endicott Interconnect Technologies, Inc.
- Fairchild Semiconductor
- Freescale Semiconductor, Inc.
- Hitachi, Ltd.
- Hynix Semiconductor
- IBM
- IBM Japan, Ltd.
- Infineon Technologies
- Intel Corporation
- Matsushita Electric Industrial Co., Ltd.
- Micron Semiconductor Asia Pte., Ltd.
- Micron Technology, Inc.
- National Semiconductor
- NEC Electronics Corporation
- Nokia
- Nokia Japan Co., Ltd.
- Oki Electric Industry
- Panasonic Electronic Devices Corporation
- Panasonic Factory Solutions
- Philips Electronics
- Renesas Technology Corporation
- Samsung Electronics Co., Ltd.
- Sanyo Electric Co., Ltd.
- Sharp Corporation
- Skyworks Solutions, Inc.
- Spansion /FASL
- STMicroelectronics
- Tezzaron Semiconductor Corporation
- Toshiba Corporation
- Triquint Semiconductor, Inc.

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Contract Companies offering SiPs and Stacked Packages

- 3-D Plus
- Advanced Interconnect Technologies, Inc. (AIT)
- Amkor Technology, Inc.
- ASAT, Limited
- ASE Group
- Bridge Semiconductor Corporation
- Carsem
- ChipMOS Technologies, Inc.
- CORWIL
- EEMS Italia SpA
- Engent, Inc.
- Epson Electronics America, Inc./Seiko Epson
- Flextronics
- FlipChip International, LLC
- Fujitsu Microelectronics America, Inc.
- Hana Microelectronics, Inc.
- I2A
- Inapac Technology, Inc.
- Irvine Sensors, Microelectronics Product Division
- Kingpak Technology, Inc.
- Kingston Technology Company
- Mitsui High-tec, Inc.
- Orient Semiconductor Electronics (OSE)
- Payton Technology Corporation
- Shinko Electric Industries Co., Ltd.
- Siliconware Precision Industries Co., Ltd. (SPIL)
- SimpleTech
- SMART Modular Technologies, Inc.
- STATS ChipPAC, Ltd.
- Sysflex, Inc.
- Unisem Group
- UTAC
- Valtronic SA
- Vate Technology Co., Ltd.
- VLSIP Technologies, Inc.
- ZyCube Co., Ltd.

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IP Companies with SiP or Stacked Package Designs

- Association of Super Advanced Electronics Technologies (ASET)
- CEA-Grenoble—leti
- Center for Power Electronics Systems (CPES)
- Cubic Wafer
- EOL
- Entorian Technologies Inc.
- ERSO
- Feng Chia University
- Fraunhofer Institute for Reliability & Microintegration IZM
- Georgia Institute of Technology / Packaging Research Center
- Hong Kong University of Science and Technology
- Hongik University
- IMEC's Advanced Packaging and Interconnect Center (APIC)
- Industrial Technology Research Institute (ITRI)
- Institute of Microelectronics (IME)
- KAIST
- Kyushu Institute of Technology
- Los Alamos National Laboratory, Air Force Research Laboratory, General Electric
- Rensselaer Polytechnic Institute
- RTI International
- State University of New York at Binghamton
- Tessera Technologies, Inc.
- Tohoku University
- Tsukuba Research Center
- University of Arkansas
- University of Southampton
- Vertical Circuits
- Ziptronix

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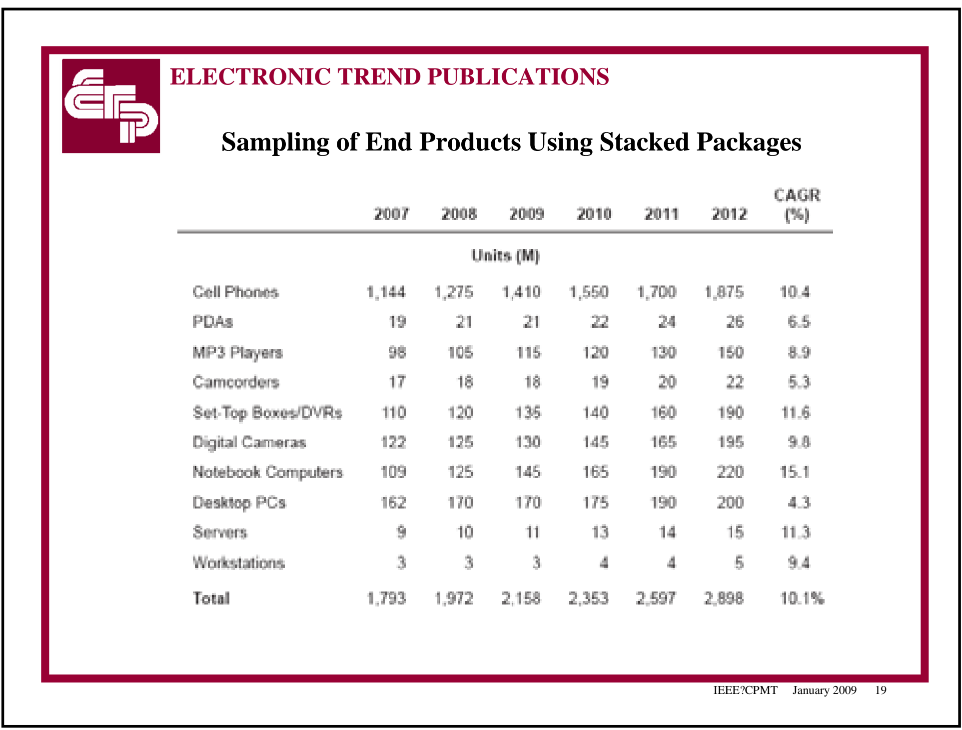

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Sampling of End Products Using Stacked Packages

	2007	2008	2009	2010	2011	2012	CAGR (%)
				Units (M)			
Cell Phones	1,144	1,275	1,410	1,550	1,700	1,875	10.4
PDAs	19	21	21	22	24	26	6.5
MP3 Players	98	105	115	120	130	150	8.9
Camcorders	17	18	18	19	20	22	5.3
Set-Top Boxes/DVRs	110	120	135	140	160	190	11.6
Digital Cameras	122	125	130	145	165	195	9.8
Notebook Computers	109	125	145	165	190	220	15.1
Desktop PCs	162	170	170	175	190	200	4.3
Servers	9	10	11	13	14	15	11.3
Workstations	3	3	3	4	4	5	9.4
Total	1,793	1,972	2,158	2,353	2,597	2,898	10.1%

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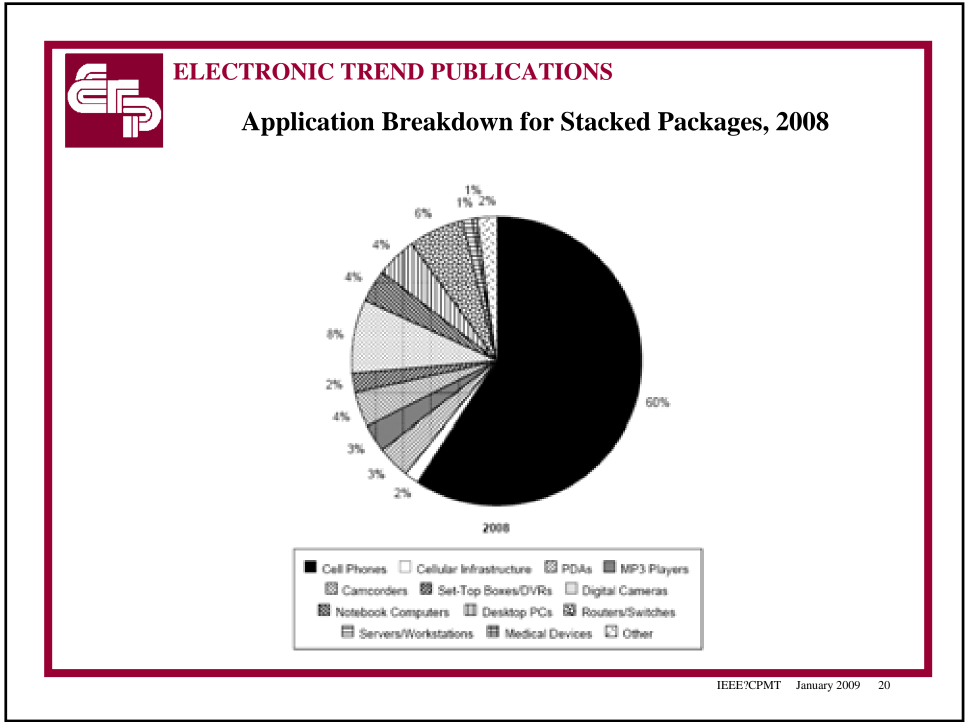

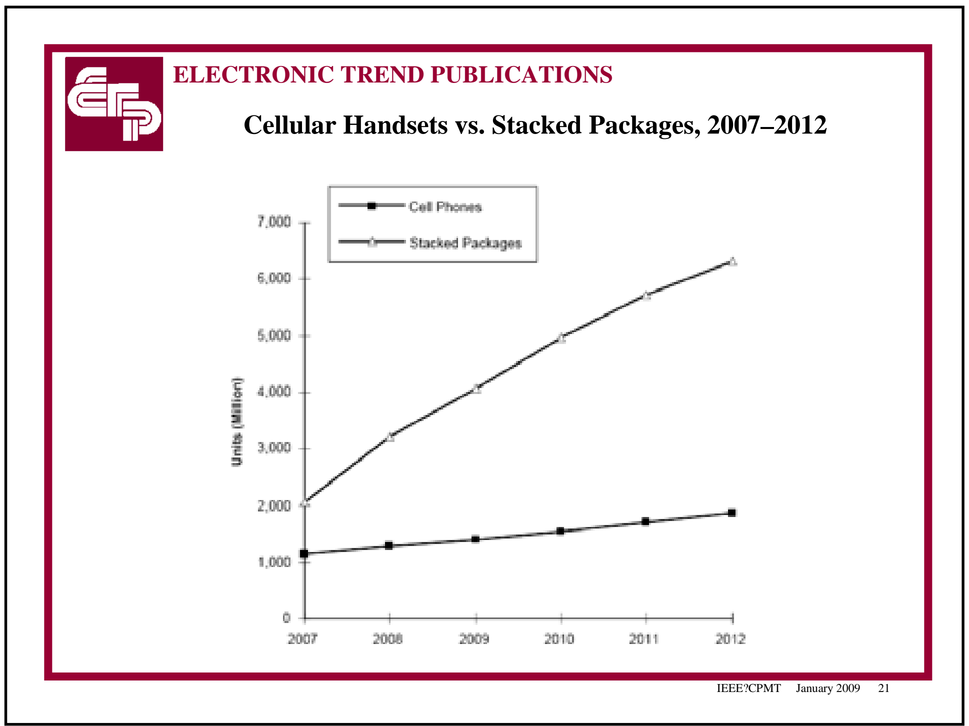

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Styles of Stacked Packages

- **Die Stack —FBGAs**
- **PoP or Package on Package (package stack)**
- **PiP or Package in Package**
- **Stacked TSOPs, or devices stacked within a TSOP, or a combination of the two**
- **Stacked QFNs, or devices stacked within a QFN, or a combination of the two**
- **Stacked MCMs**
- **Folded Stack**
- **Stacked WLPs**

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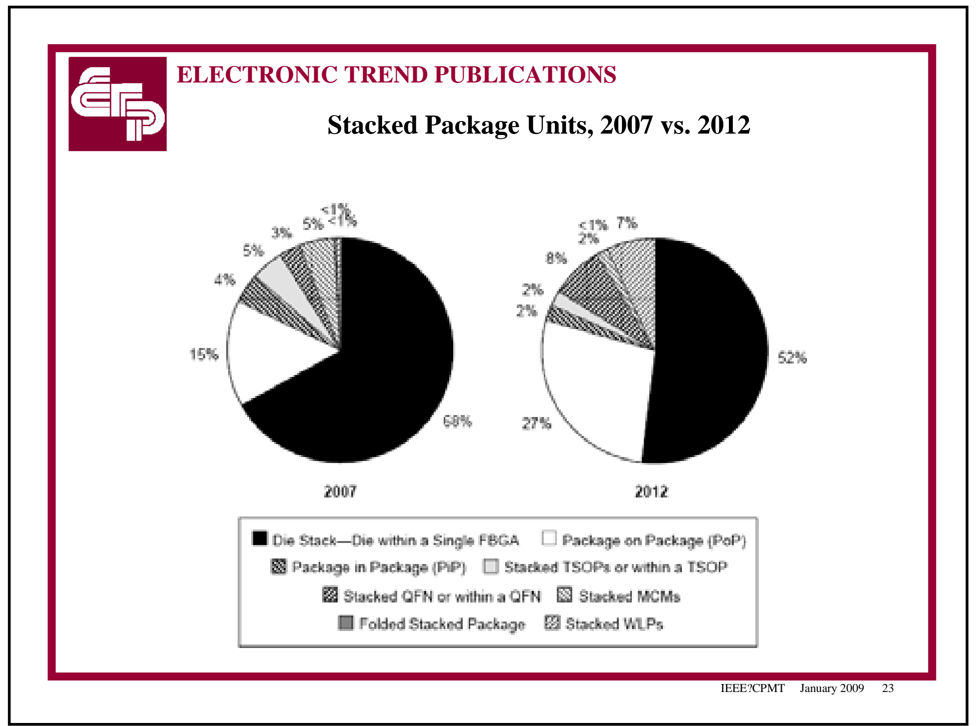
ELECTRONIC TREND PUBLICATIONS
Stacked Package Units, 2007 vs. 2012
68%
15%
4%
5%
3%
5%
<1%
<1%
2007
52%
27%
2%
2%
8%
2%
<1%
7%
2012
Die Stack—Die within a Single FBGA
Package on Package (PoP)
Package in Package (PiP)
Stacked TSOPs or within a TSOP
Stacked QFN or within a QFN
Stacked MCMs
Folded Stacked Package
Stacked WLPs
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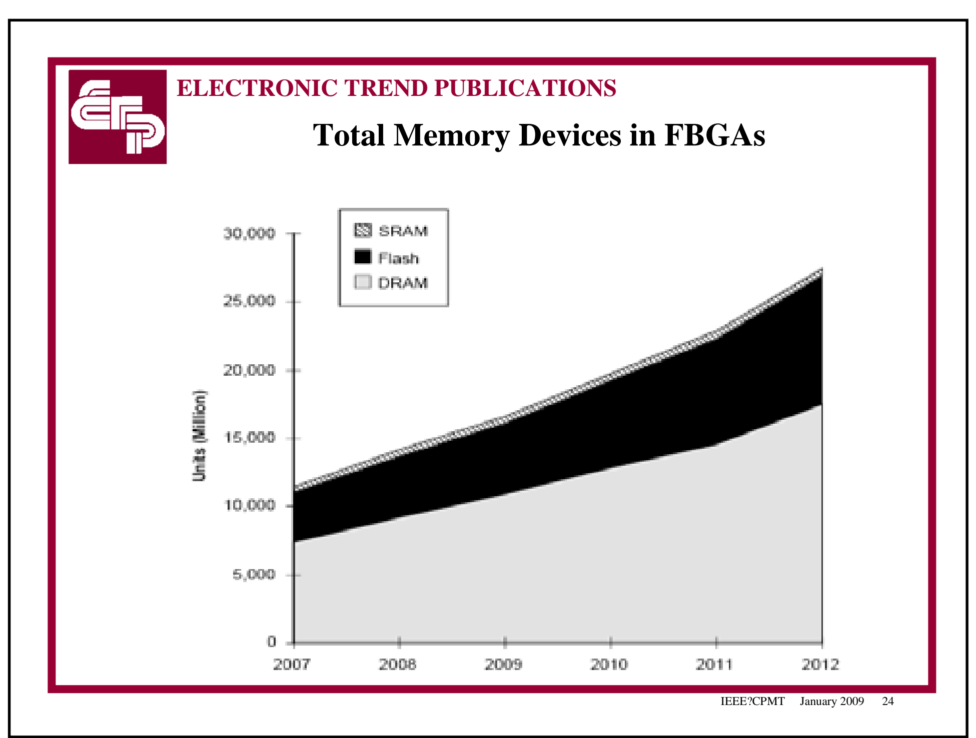
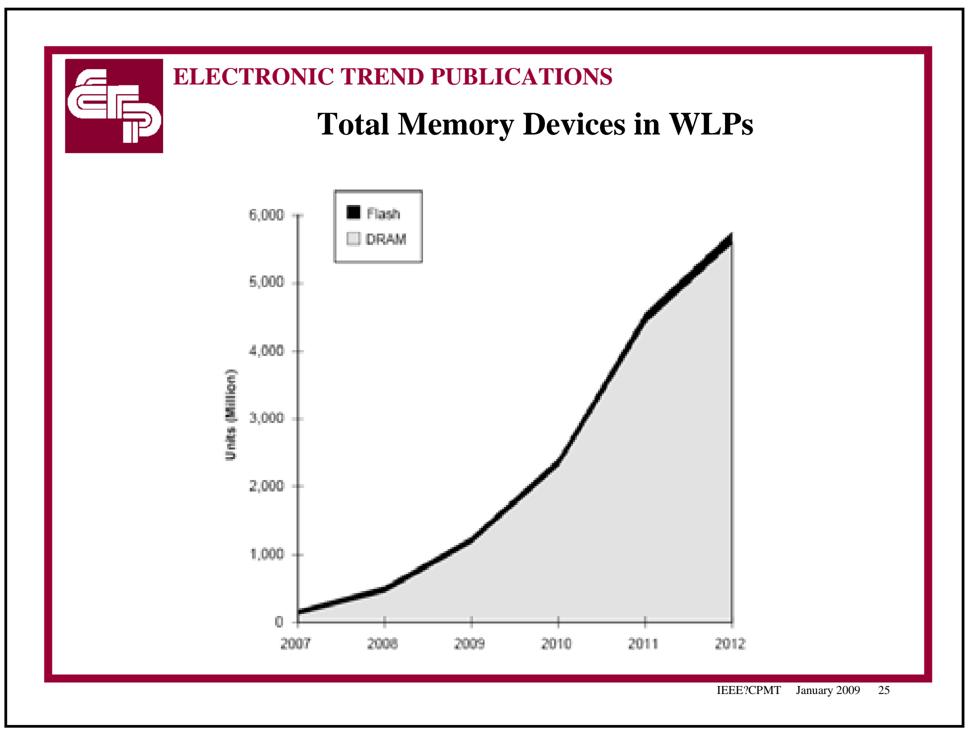

ELECTRONIC TREND PUBLICATIONS
Total Memory Devices in FBGAs
SRAM
Flash
DRAM
Units (Million)
30,000
25,000
20,000
15,000
10,000
5,000
0
2007
2008
2009
2010
2011
2012
IEEE?CPMT January 2009 24



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3-D Integration / Through Silicon Vias

Through silicon vias (TSVs) route the electric signal through all the die in the stack – an alternate method of interconnection in relation to wire bonding or flip chip.

The wafer is thinned, and through vias protrude through the wafer which are filled with copper or other electrically conductive material.

If via last technology, vias are filled in plating baths, slowly and carefully so as not to have voids in the vias.

Redistribution layers can be added between the devices so as to mix and match technologies.

Devices are stacked and vias are connected to other die on a different vertical plane.

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3-D Integration / Through Silicon Vias

Via First:

Vias through the silicon can be added as part of the front end process

- **Finer via diameters**
- **Improved aspect ratios**
- **Eliminate a timely and costly process later to create the TSVs**
- **If some wafers created differently from the rest, this not the most efficient from a manufacturing perspective**

Via Last:

Vias can be added as part of the back-end process, after the wafer is created, either through the top or bottom of the wafer.

- **Thicker via diameters**
- **Larger aspect ratios**
- **Additional wafer processing**
- **Costly, time consuming, yield issues**

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TSV Market

TSVs began being used in CMOS image sensors in the spring of 2008.

ICs stacked with TSVs will be the next market, and include and combine the following:

- Memory
- RF
- Logic
- Analog
- Logic plus baseband
- Mixed signal
- Processor plus cache memory
- Interface (transceivers)

DRAM stacks with TSVs will occur before NOR flash memory is stacked this way, and processor plus memory possibly may be available as early as the 2011/ 2012 time frame.

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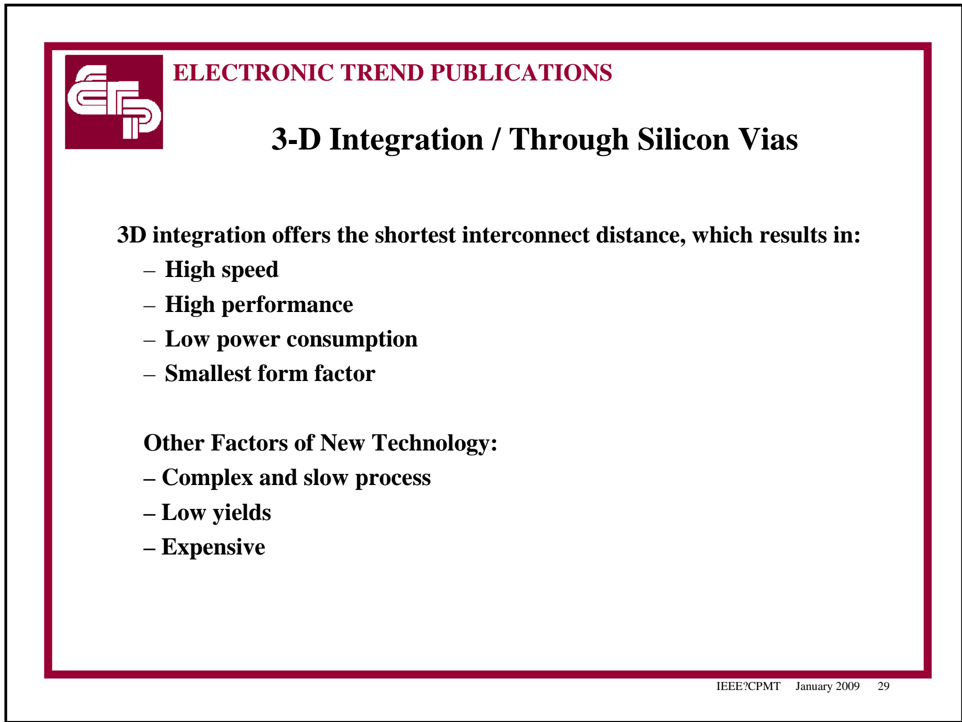
ELECTRONIC TREND PUBLICATIONS
3-D Integration / Through Silicon Vias
3D integration offers the shortest interconnect distance, which results in:
– High speed
– High performance
– Low power consumption
– Smallest form factor
Other Factors of New Technology:
– Complex and slow process
– Low yields
– Expensive
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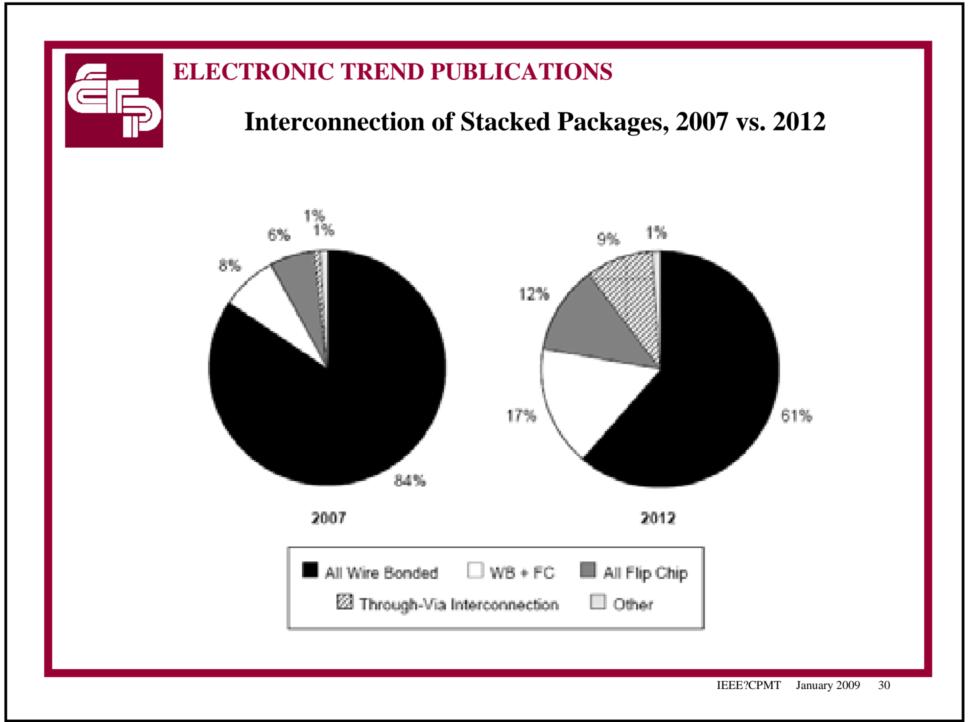
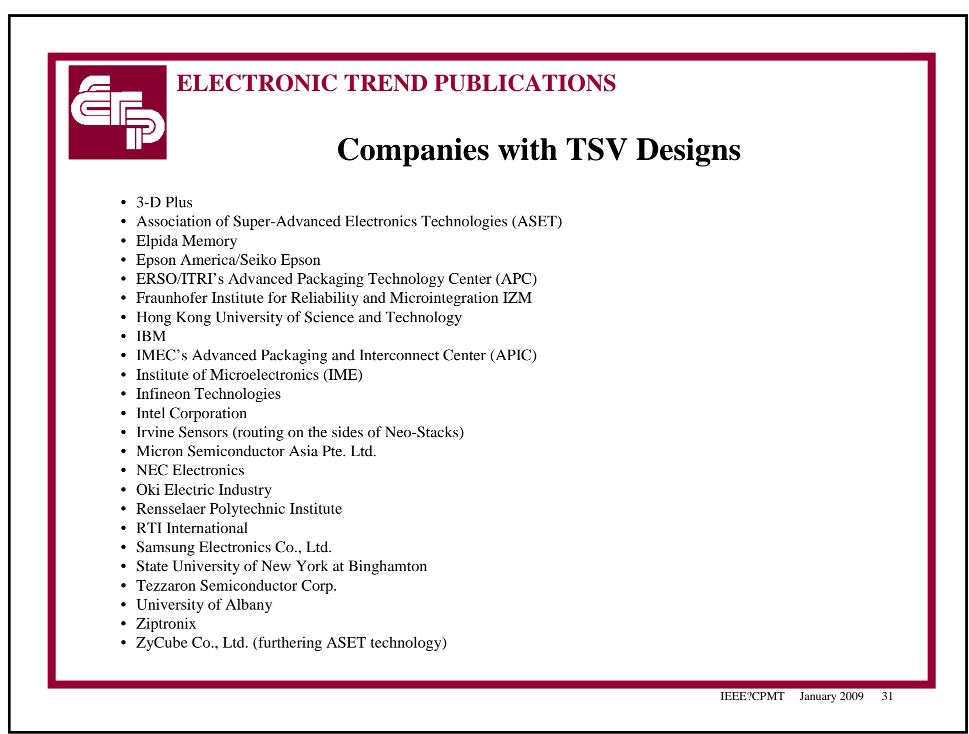

ELECTRONIC TREND PUBLICATIONS
Interconnection of Stacked Packages, 2007 vs. 2012
1%
6%
1%
8%
84%
2007
9%
1%
12%
17%
61%
2012
All Wire Bonded
WB + FC
All Flip Chip
Through-Via Interconnection
Other
IEEE?CPMT January 2009 30


ELECTRONIC TREND PUBLICATIONS
Companies with TSV Designs
• 3-D Plus
• Association of Super-Advanced Electronics Technologies (ASET)
• Elpida Memory
• Epson America/Seiko Epson
• ERSO/ITRI's Advanced Packaging Technology Center (APC)
• Fraunhofer Institute for Reliability and Microintegration IZM
• Hong Kong University of Science and Technology
• IBM
• IMEC's Advanced Packaging and Interconnect Center (APIC)
• Institute of Microelectronics (IME)
• Infineon Technologies
• Intel Corporation
• Irvine Sensors (routing on the sides of Neo-Stacks)
• Micron Semiconductor Asia Pte. Ltd.
• NEC Electronics
• Oki Electric Industry
• Rensselaer Polytechnic Institute
• RTI International
• Samsung Electronics Co., Ltd.
• State University of New York at Binghamton
• Tezzaron Semiconductor Corp.
• University of Albany
• Ziptronix
• ZyCube Co., Ltd. (furthering ASET technology)
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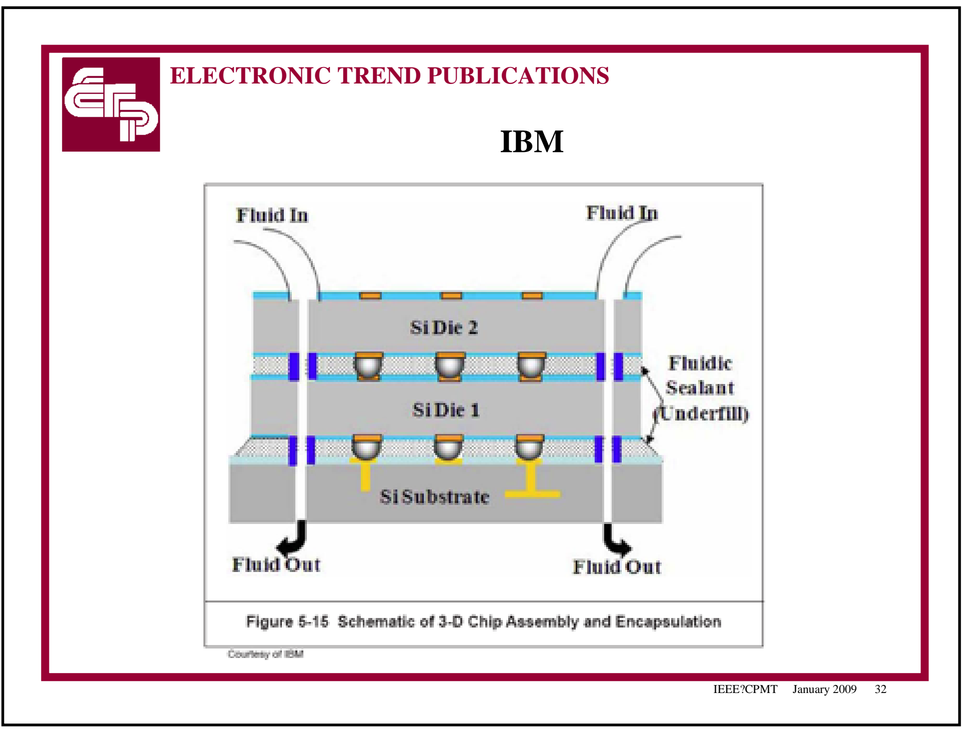
ELECTRONIC TREND PUBLICATIONS
IBM
Fluid In
Fluid In
Si Die 2
Si Die 1
Si Substrate
Fluidic
Sealant
(Underfill)
Fluid Out
Fluid Out
Figure 5-15 Schematic of 3-D Chip Assembly and Encapsulation
Courtesy of IBM
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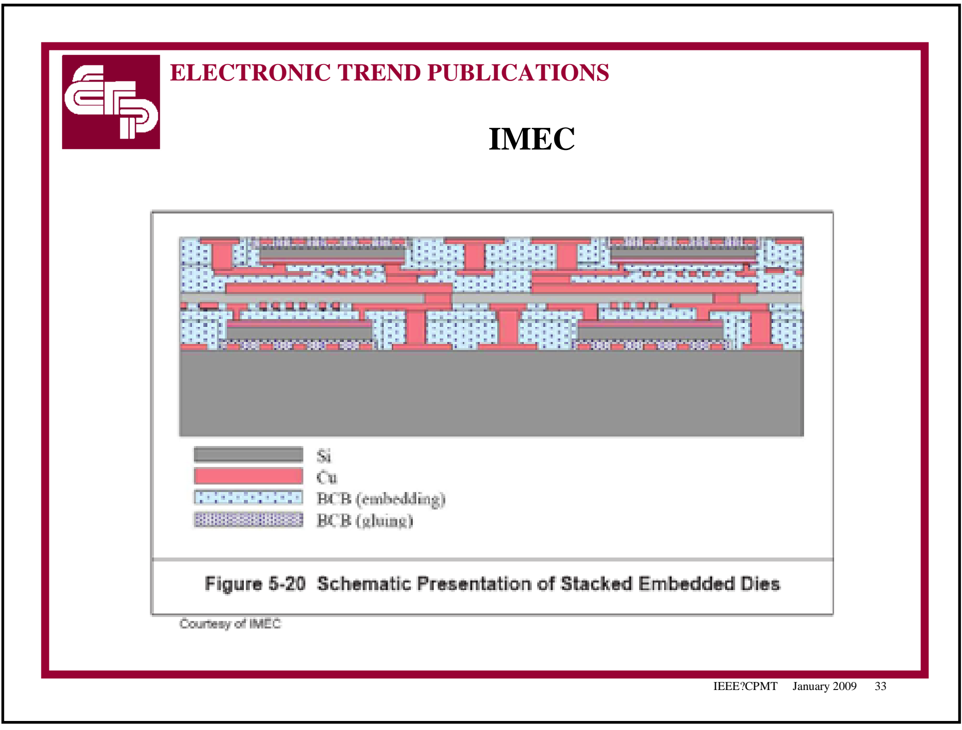
ELECTRONIC TREND PUBLICATIONS
IMEC
Si
Cu
BCB (embedding)
BCB (gluing)
Figure 5-20 Schematic Presentation of Stacked Embedded Dies
Courtesy of IMEC
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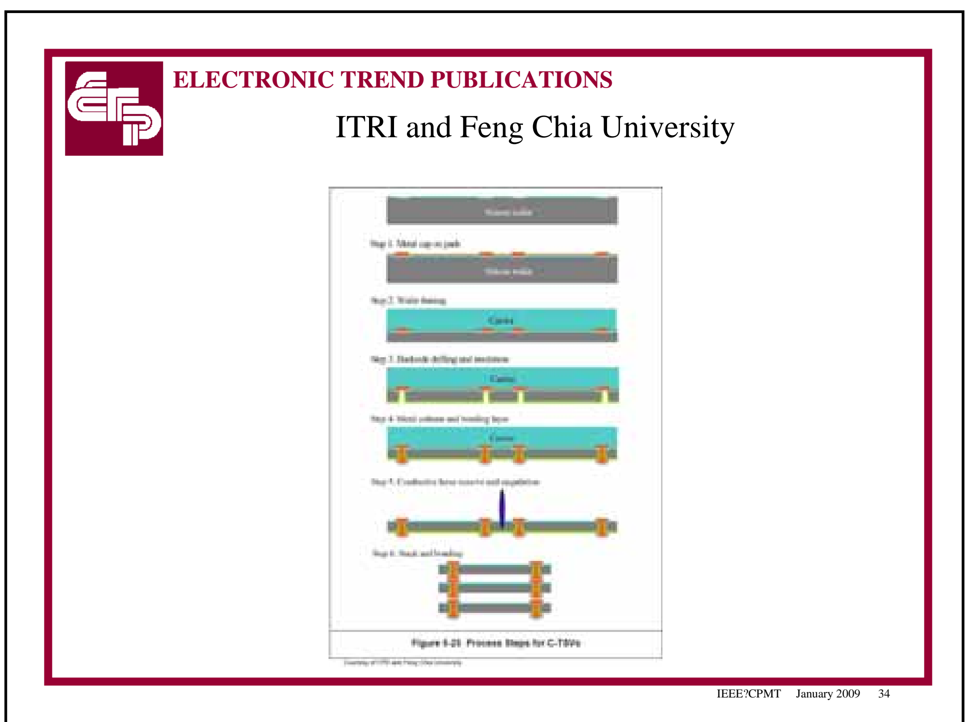
ELECTRONIC TREND PUBLICATIONS
ITRI and Feng Chia University
Figure 5-21 Process Steps for C-TSVs
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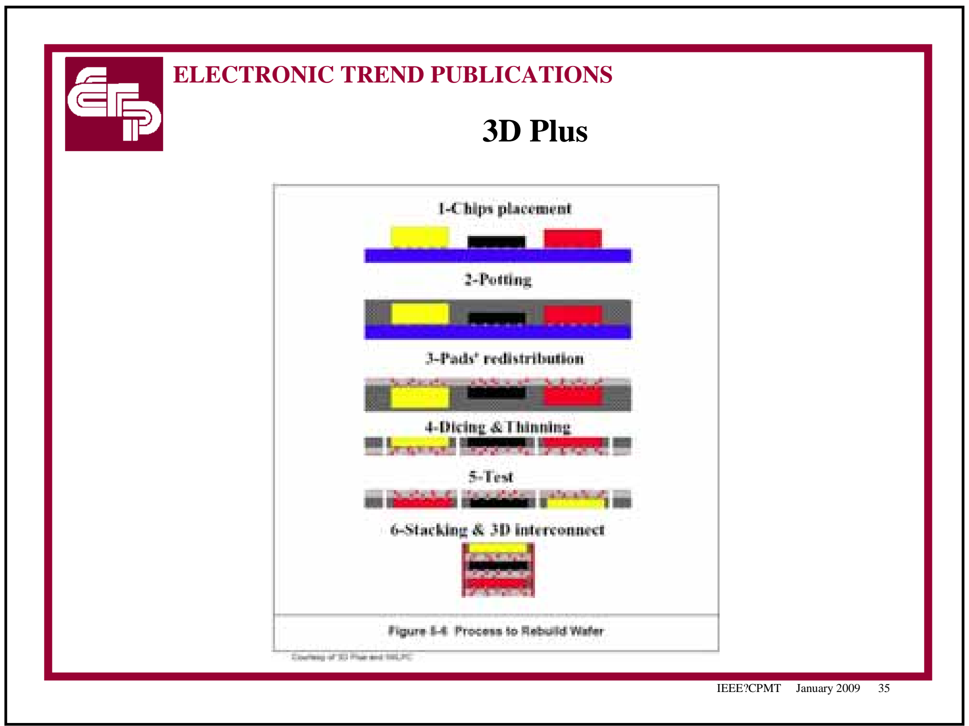
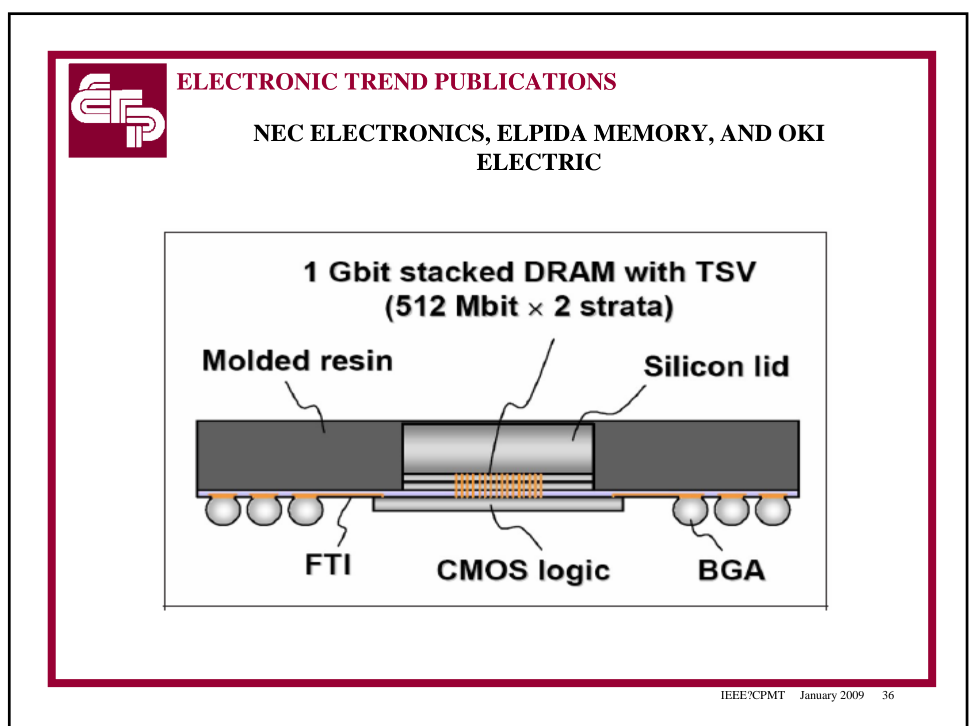
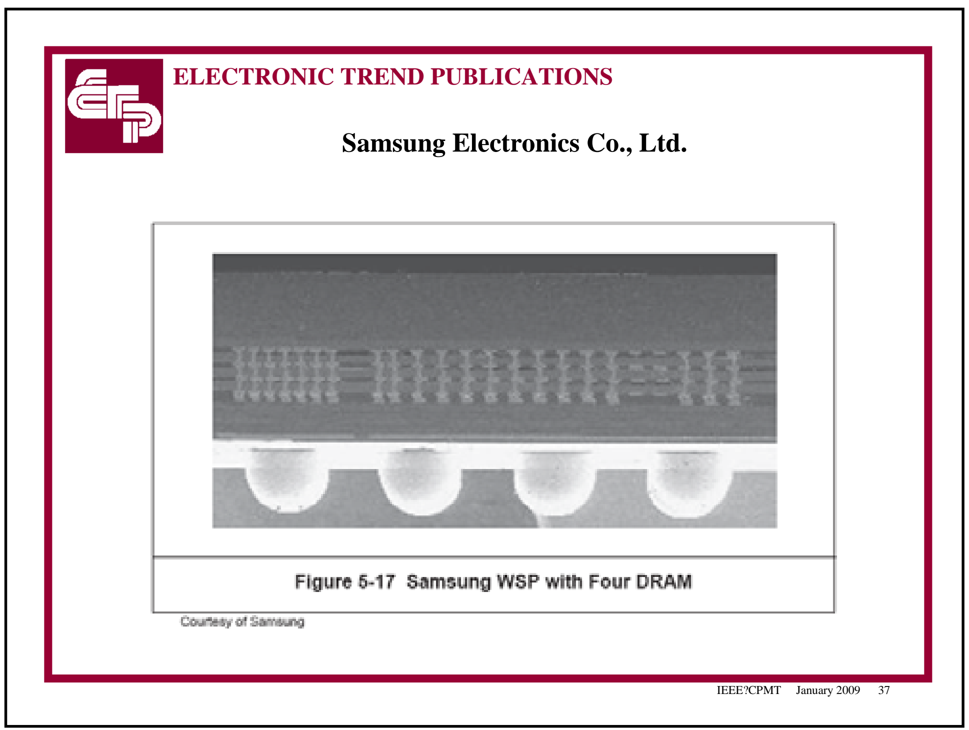
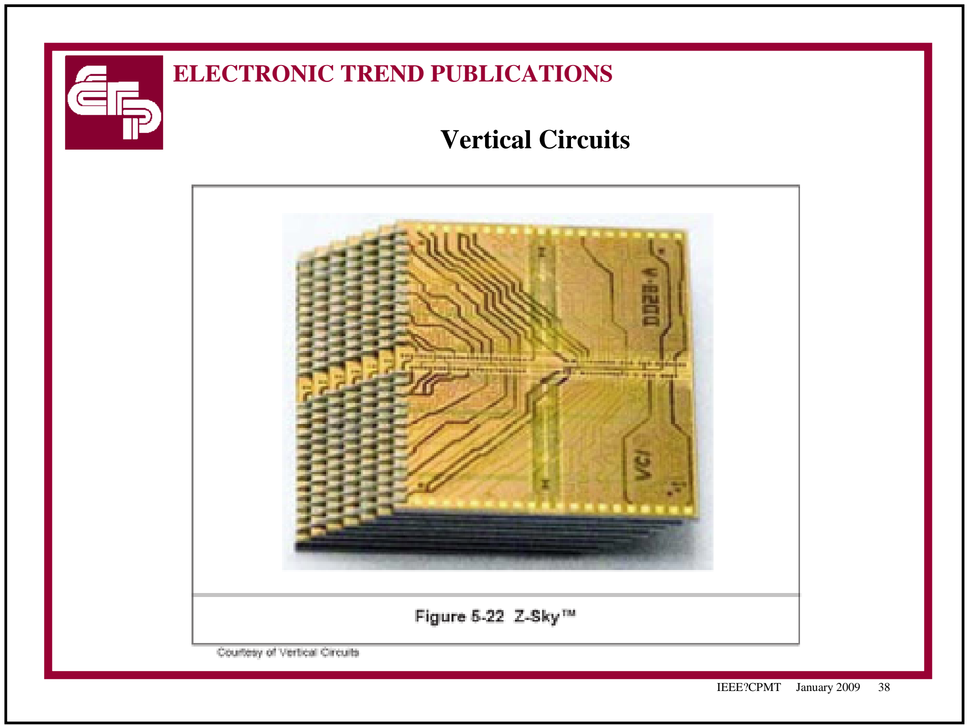

ELECTRONIC TREND PUBLICATIONS
3D Plus
1-Chips placement
2-Potting
3-Pads' redistribution
4-Dicing & Thinning
5-Test
6-Stacking & 3D interconnect
Figure 5-6 Process to Rebuild Wafer
IEEE?CPMT January 2009 35


ELECTRONIC TREND PUBLICATIONS
NEC ELECTRONICS, ELPIDA MEMORY, AND OKI ELECTRIC
1 Gbit stacked DRAM with TSV
(512 Mbit × 2 strata)
Molded resin
Silicon lid
FTI
CMOS logic
BGA
IEEE?CPMT January 2009 36


ELECTRONIC TREND PUBLICATIONS
Samsung Electronics Co., Ltd.
Figure 5-17 Samsung WSP with Four DRAM
Courtesy of Samsung
IEEE?CPMT January 2009 37


ELECTRONIC TREND PUBLICATIONS
Vertical Circuits
Figure 5-22 Z-Sky™
Courtesy of Vertical Circuits
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ELECTRONIC TREND PUBLICATIONS

Conclusions

- A high level of innovation is the key to furthering the advancement of the IC world. This will bring about more desirable and variable end products, from portable electronics for the consumer to medical devices that will save and/or improve lives.

- Advanced IC packaging technologies are key essentials in bringing forth size reduction and performance, which will ultimately lower costs, and allow for a host of new product launches.

- Technological inspirations and innovations should help fuel demand for electronic products, which could result in the technology sector leading the way out of this recession.

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