Non-Contact Wafer Testing and High Performance, Low Power I/O Chip-to-chip Communications

Outline

• High Level Company Overview
• Background
• Test Access Issues and WiTAP™ Solution
• Interconnect Issues and Ultral/O™ Solution
• Summary
The Company

Scanimetrics provides solutions to bottlenecks imposed by traditional semiconductor I/O circuits

Our solutions address:

- Test access during fabrication and packaging of integrated circuits
- Speed and power consumption of integrated circuits

"(Scanimetrics) technology is seminal in nature and the impact will be profound." - Denny Sabo, former CEO, Arithmos
Current Wafer Probing Problems

• Contact Probes
  • Pitch, tip size, restricted pad size

• Pad Damage
  • Maximum allowable damaged area

• ESD Structures

How: Non-contact Test Access

I/O Issues – Pad Pitch and ESD

<table>
<thead>
<tr>
<th>I/O Pad Min. Dimension (μm)</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
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<tr>
<td>Wirebond</td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Bump</td>
<td>75</td>
<td>75</td>
<td>60</td>
<td>60</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
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</table>

• Bond / probe pads are not shrinking with circuit dimensions according to Moore’s Law
• Probes: Pitches not shrinking, tip sizes not changing
• Pad Damage: Maximum allowable damaged area is decreasing
• ESD structures affect signal speed and power consumption
Packaging is Critical

Packaging is now a limiting factor; But is an enabler for more than Moore

• Packaging has become the limiting element in system cost and performance
• The assembly and packaging role is expanding to include system level integration functions
• As traditional Moore’s Law scaling becomes more difficult innovation in assembly and packaging can take up the slack

I/O Issues – Testability of New Technologies

• Redistributed Chip Packaging (RCP)
  - Die connections are redistributed and brought to the outside as part of the package build
  - No pads needed on the die, so how do you test?

From: B. Keser
Freescale Semiconductor
2007 Freescale Technology Forum
SiP Challenges

• Assembly yields low
  – Yield is product of die yields
  – Testability during assembly is non-existent
  – Probing SiP modules difficult due to
    – Mechanical issues
    – Varying component heights
    – Good die lost during substrate build-up process

• Design kits for SiP not available from Vendors

• Vendor availability for start-up volumes
  – Lack of low-volume manufacturing capacity

I/O Issues - Data rate roadmap

• 10 Gbps I/O available
• Power >8 mW/Gbps
• Tbps data rates
• Communications
• Data storage
• Image processing

A good measure (Figure of Merit) is Speed times Distance per unit of Power
The Technology

- Inductive chip-scale communications
- Micro Tx/Rx on chip
- One Tx/Rx per I/O
- High speed
- Low power
- Pitch scales to <20um

The Products

- UltraI/O™
  - Semiconductor I/O circuit IP
  - FASTER data rates
  - LOWER power consumption
  - SMALLER size

- WiTAP™ product family
  - Semiconductor test access IP and probe card
  - Advanced package testing
  - Wafer probing
WiTAP™, Non-Contact Probing Solution

Scanimetrics patented technology – WiTAP™

- Wireless Test Access Port (WiTAP™)
- A chip with Scanimetrics’ wireless transceivers designed to be integrated into SiP/MCM
- Uses Scanimetrics’ UltraI/O™ wireless transceiver
- UltraI/O™ and measurement circuits integrated into chip or package
  - Can source and measure digital, analog and RF signals
- Interfaces can be tested at full functional speed
  - Test during build, before packaging; access ‘hidden’ test points
  - Can be used with stacked chips
- Possibility of high parallelism testing at wafer level
- Allow access to hidden test nodes
- Allow testing of JTAG devices during assembly process
WiTAP™ Features

Probe Chip Mount
Standard Probe Card PCB
Power Connections Probes
Wafer to be Tested
Wafer test

Probe Chip Mount
Standard Probe Card PCB
Power Connections Probes
SIP Substrate
SIP test

WiTAP™ Features

Matching Antenna Pattern on Wireless Probe Card

Single DUT Die with Standard I/O Cells Replaced with Wireless I/O Cells
WiTAP™ SiP Testing Solution

- Complex SiP designs presently are not cost-effective
  - Overall yield is product of individual die yields and assembly yield
  - Mechanical issues and contact probing restrictions prevent testing during assembly process

- Solution: Scanimetrics' Wireless Test Access Port (WiTAP™)
  - Enables design of complex SiP devices with high manufacturing yields
  - Lessens known good die (KGD) requirements of individual die
  - Allows testing of the SiP like a wafer during the assembly process
    - On a prober, with a probe card
  - WiTAP™ enables cost-effective SiP assembly and manufacturing

WiTAP™ SiP Testing Solution

Can be implemented as an independent chip populated on the SiP substrate or as an IP block embedded in other chips

Test substrate

Low-yield and inexpensive die placed first

High value die placed last only on modules with no prior defects
WiTAP™ SiP Testing Solution

Features Benefits
Monitor quality of SiP process in real-time

• Detect problems earlier in the process
• Early detection yield excursions
• Reduce number of dies wasted
• Reduce assembly cost up to 30% or more
## WiTAP™ SiP Testing Solution

<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
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</thead>
<tbody>
<tr>
<td>Non-contact signal probing at high speeds</td>
<td>• Less probing debris</td>
</tr>
<tr>
<td></td>
<td>• Less damage to circuits and pads</td>
</tr>
<tr>
<td></td>
<td>• Less damage to probe cards</td>
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<tr>
<td></td>
<td>• More robust process</td>
</tr>
<tr>
<td></td>
<td>• Full speed testing at wafer level</td>
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</table>

### WiTAP™ Probe

![Single WiTAP™ chip](image)

www.cpmt.org/scv
WiTAP™ SiP DUT

WiTAP™ on SiP module for customer application

Wafer Probe Application

- Interfaces can be tested at full functional speed at the wafer level (SerDes, DDR2, DDR3)
- Supports internal test points with no ESD protection requirements
- Possibility of high parallelism testing at wafer level
Wafer Probe Solution

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<tr>
<td></td>
<td>• Less damage to probe cards</td>
</tr>
<tr>
<td></td>
<td>• Less I/O pads and routing area</td>
</tr>
<tr>
<td></td>
<td>• More robust process</td>
</tr>
</tbody>
</table>

WiTAP™ Product

Alignment Tolerance

• Wide alignment tolerance
• 120 µm antennas
• Envelope of $<10^{-13}$ error rate
WiTAP™ in 45 nm Technology

45 nm 100Mbps Eye Diagram

WiTAP™ Product Summary

- WiTAP™ SiP product qualified for production by top 10 semiconductor firm Q308 in 130 nm
- Non-contact test circuits migrated to 45 nm and demonstrated in Q208
  - Faster and lower power
UltraI/O™, High Performance Low Power Chip-to-chip interconnect

March 13, 2009

UltraI/O™ - Background

"The growing number of full-featured, media-rich mobile applications is creating an increased demand for more memory. Serial Port Memory Technology will be the right solution to support the requirements for low pin count, low power and high bandwidth that will be required for these new applications."

JB Kim, senior vice president of technical marketing, Hynix, member of SPMT group
I/O Issues - Data rate roadmap

Chip power density greater than a ‘Formula One’ engine
>1.5 kW/cu.in … and increasing!
  • Current technology is out of Gas!!!!
  • I/O performance measured by speed, power, distance, density (size)
  • I/O complexity is increasing
  • Speed is available at expense of power
  • I/O is not scaling with technology nodes
  • Chips are pad and power limited
  • Power at Gigabit rates needs to fall
  • Testability issues

The Options – Wired or Wireless

• Wireline I/O (Rambus)
  • Requires complex on-chip clocking with related jitter sensitivity issues (clocking overhead power of 3.6 mW for 6.25 Gbps link)
  • Requires complex equalization circuitry with related jitter sensitivity issues (8mW for 6.25 Gb/s link)
  • Problems with ESD protection structures loading Rx inputs
  • Requires complex pre-emphasis circuitry with related jitter sensitivity issues (4.9 mW for 6.25 Gbps link)
  • Problems with ESD protection structures and PCB parasitics loading Tx outputs
The Options – Wired or Wireless

• Optical
  • Does not have many of the limitations present in electrical signals. However, to enter the optical domain electrical signals have to be converted using optical transceivers
    • These circuits dissipate almost as much power as transceivers that drive PCBs and short backplanes
  • Only useful alternative is to have signal processed and transmitted entirely in optical domain. However, there are many performance problems with silicon photonics
    • Even if performance problems are solved it is doubtful that fully optical links will be economical over short distances
    • Silicon having an indirect bandgap provides no easy path to the integration of optics especially with regard to photon generation

Other approaches to I/O connectivity

Why NOT other types of interconnections?

• Capacitive requires very close chip spacing => not practical
• Inductive extends range => but not far enough still not practical
• Research stage coupling solutions (Sun/ST/Kuroda) offers Tbps rates => but only up to 100 μm distance
• Traditional I/O, Flex I/O, SerDes => require large power and area
Capacitively-coupled Interconnect

- Limited bandwidth on low frequency side (requires high coupling capacitance)
- Receive equalization helps that burns more power
- On-chip coupling capacitor requires very close spacing between capacitor plates

Capacitive Coupling I/O

- Proximity chip to chip communications
  - Non-contact, very high speed chip-to-chip communications programs in development for I/O
- No probe/bond pads required, so what is the testing solution?
Inductive Coupling I/O

External wire

Low power
Data rates are 2.5Gbps now
Major target is 10 Gbps

- High Speed
- Signal Integrity
- Small Size
- Less ESD

- Uses the fact that transformer has inductance to overcome input capacitance.

Scanimetrics Inductive Coupling Solution – UltraI/O™

- **High speed:** >20 Gbps per channel -> 1 Tbps chip-to-chip
- **Low power:** < 1 mW per Gbps
- **Small circuit size:** < 250 um² at 45 nm
- **Scalable**
Scanimetries Inductive Coupling Solution – Ultral/O™

- Less ESD protection is required since no DC connection
- Power, speed, distance and size much better than capacitive coupling and wireline solutions
- 3D packaging compatible
- Scanimetries wireless test solution: WiTAP™ (Wireless Test Access Port) can be used to verify Ultral/O™ connections

Scanimetries Inductive Coupling Solution – Ultral/O™

Ultra I/O™ enables interconnection of die on SiP device
- A large single die replaced with a SiP consisting of many smaller die
- Smaller die can be interconnected using Ultra I/O™ at data rates equivalent to those on a single die with low power consumption
- Very cost-effective (more than 5X) for FPGA applications
### UltraI/O™ features and benefits

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Higher Bandwidth</strong></td>
<td>New Applications</td>
</tr>
<tr>
<td>Higher performance designs</td>
<td>Smaller Chips</td>
</tr>
<tr>
<td>Fewer I/Os</td>
<td>Less pin counts</td>
</tr>
<tr>
<td></td>
<td>Less expensive packages</td>
</tr>
<tr>
<td><strong>Lower power consumption</strong></td>
<td>Cheaper packages</td>
</tr>
<tr>
<td>Simpler package</td>
<td>Simpler system level designs</td>
</tr>
<tr>
<td>Less Heat</td>
<td></td>
</tr>
<tr>
<td><strong>Smaller Size</strong></td>
<td>Lower cost</td>
</tr>
<tr>
<td>Less area</td>
<td>Future Proof</td>
</tr>
<tr>
<td>Scalable</td>
<td></td>
</tr>
<tr>
<td><strong>Simpler Signaling schemes</strong></td>
<td>Faster cycle time</td>
</tr>
<tr>
<td>Easier circuit design</td>
<td></td>
</tr>
<tr>
<td>Simpler board/package designs</td>
<td>Lower cost system design</td>
</tr>
</tbody>
</table>

*Gen 2 chip*  

Eye diagram of PRBS at 475MBits/s
UltraI/O™ results at 130 nm

4 Gbit/s

Input

Tx

Rx

On the road to 10G

- Third generation inductor design
- Receive selectivity
- Automatic Impedance Control
- Simple equalization
UltraI/O™ Applications

Applications of UltraI/O™ includes but not limited to:
- Multiprocessor systems
- High performance multi device Network processing
- High performance Graphics
- High speed I/O bridging
- Multi-FPGA designs
- Raw camera imaging
- Cellular modem
- Compressed video

Comparisons of UltraI/O™ to LPDDR2

<table>
<thead>
<tr>
<th></th>
<th>LPDDR2 Specifications</th>
<th>Implementation Using UltraI/O™</th>
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</thead>
<tbody>
<tr>
<td>BOM cost</td>
<td>2 or more RAM</td>
<td>1 RAM</td>
</tr>
<tr>
<td>Signal pins</td>
<td>53 @ 800 Mbytes/sec</td>
<td>2 @ 800 Mbytes/sec</td>
</tr>
<tr>
<td></td>
<td>69 @ 3.2 Gbytes/sec</td>
<td>4 @ 3.3 Gbytes/sec</td>
</tr>
<tr>
<td>I/O power</td>
<td>60 mW @ 800 Mbytes/sec</td>
<td>7.2 mW @ 800 Mbytes/sec</td>
</tr>
<tr>
<td></td>
<td>220 mW @ 3.2 Gbytes/sec</td>
<td>30 mW @ 3.3 Gbytes/sec</td>
</tr>
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</table>

• Higher UltraI/O™ bandwidth can be achieved by adding more signal channels
Comparisons of UltraI/O™ to PCI Express

<table>
<thead>
<tr>
<th>PCI Express Gen 3 Specifications</th>
<th>Implementation Using UltraI/O™</th>
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</thead>
<tbody>
<tr>
<td>Signal pins</td>
<td></td>
</tr>
<tr>
<td>2 @ 800 Mbytes/sec</td>
<td>2 @ 800 Mbytes/sec</td>
</tr>
<tr>
<td>8 @ 3.2 Gbytes/sec</td>
<td>4 @ 3.3 Gbytes/sec</td>
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<tr>
<td>I/O power</td>
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<tr>
<td>120 mW @ 800 Mbytes/sec</td>
<td>7.2 mW @ 800 Mbytes/sec</td>
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<tr>
<td>480 mW @ 3.2 Gbytes/sec</td>
<td>30 mW @ 3.3 Gbytes/sec</td>
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Comparisons of UltraI/O™ to MIPI UniPro™

<table>
<thead>
<tr>
<th>MIPI UniPro Specifications</th>
<th>Implementation Using UltraI/O™</th>
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<tbody>
<tr>
<td>Signal pins</td>
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<tr>
<td>16 @ 800 Mbytes/sec</td>
<td>2 @ 800 Mbytes/sec</td>
</tr>
<tr>
<td>64 @ 3.2 Gbytes/sec</td>
<td>4 @ 3.3 Gbytes/sec</td>
</tr>
<tr>
<td>I/O power</td>
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<tr>
<td>28 mW @ 800 Mbytes/sec</td>
<td>7.2 mW @ 800 Mbytes/sec</td>
</tr>
<tr>
<td>112 mW @ 3.2 Gbytes/sec</td>
<td>30 mW @ 3.3 Gbytes/sec</td>
</tr>
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</table>
Overview

1. Testing DUT A
2. Testing DUT B
3. Testing SIP
4. Normal Operation

UltraI/O™ Summary

- Current memory interface technology cannot meet growing demand of mobile handheld industry and other markets such as portable media player and digital cameras
- UltraI/O™ offers faster, lower power and smaller area solutions than other approaches such as capacitive and inductive interconnects
- UltraI/O™ has superior performance than current interface standards (LPDDR2, PCI Express, MIPI Unipro®)
- UltraI/O™ is an excellent candidate for the next chip-to-chip and memory interface standards
"The growing number of full-featured, media-rich mobile applications is creating an increased demand for more memory.

Serial Port Memory Technology will be the right solution to support the requirements for low pin count, low power and high bandwidth that will be required for these new applications."

JB Kim, senior vice president of technical marketing, Hynix, member of SPMT group

Ultrapower™ fills this technology gap.