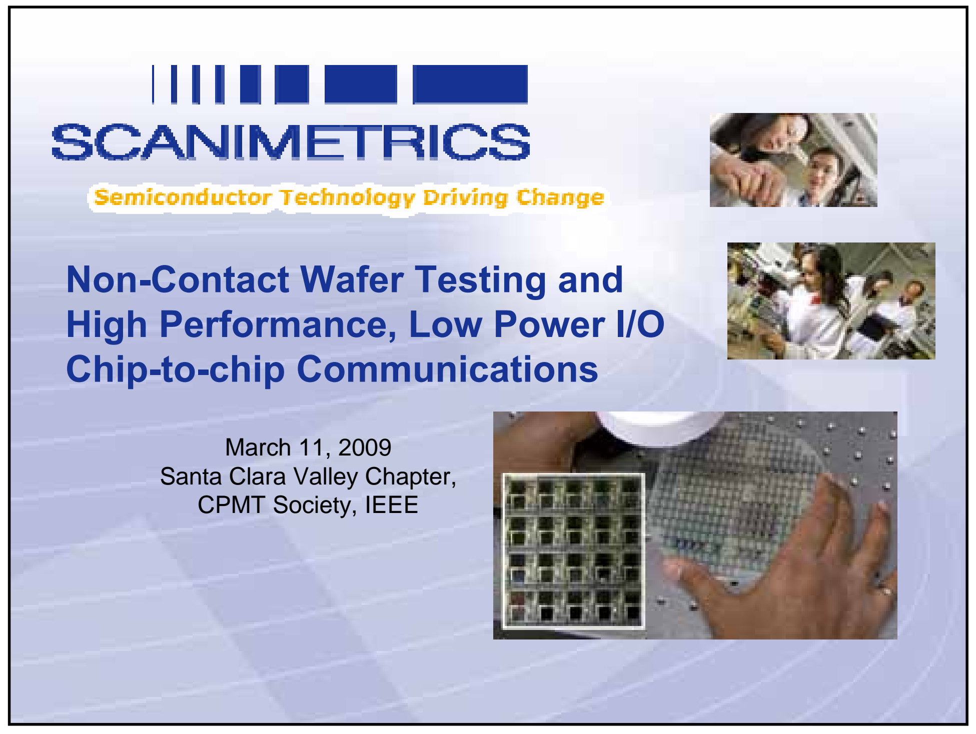
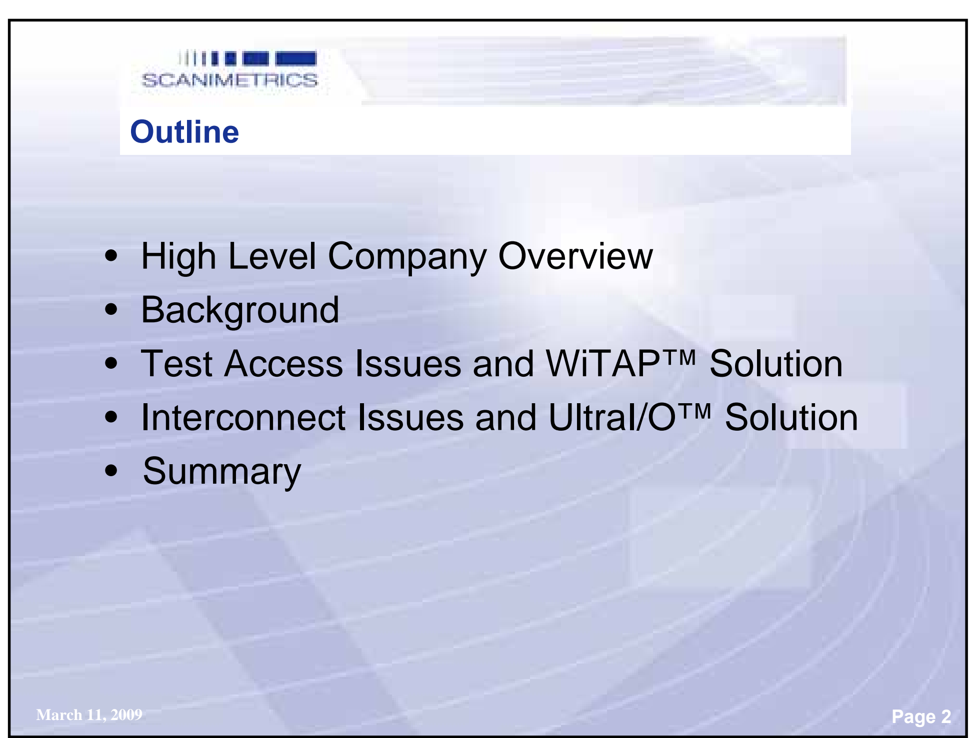
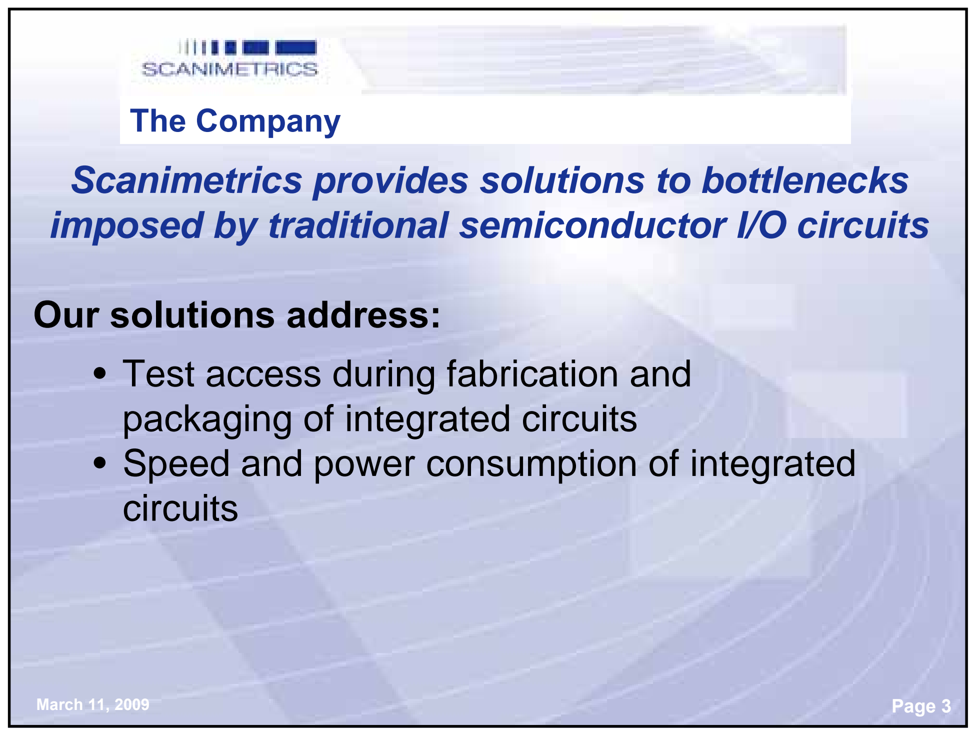
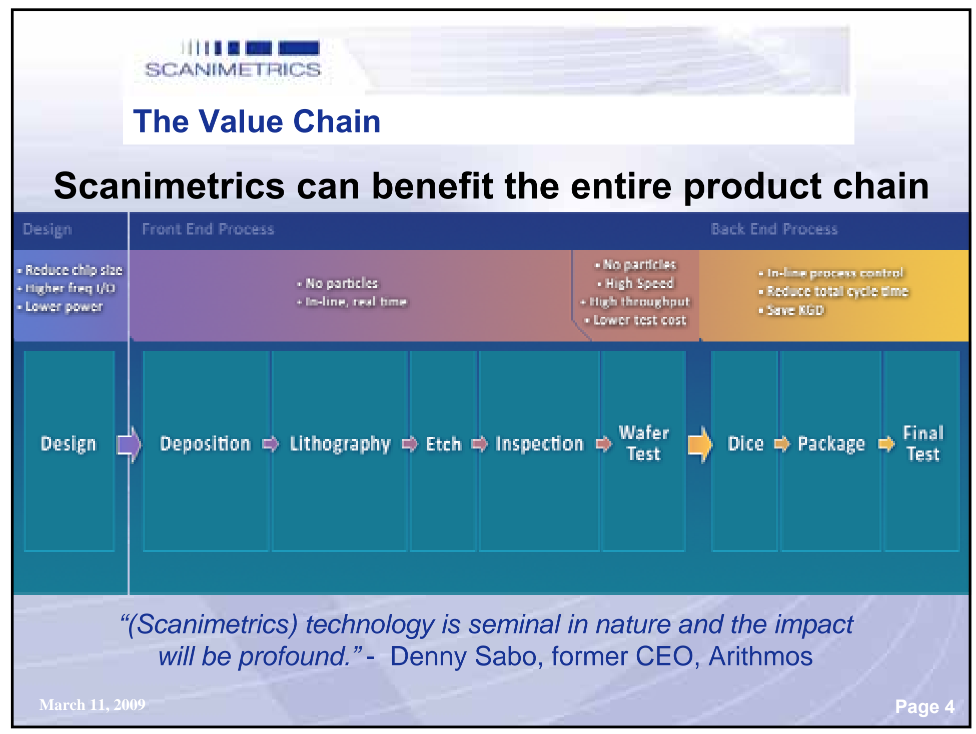
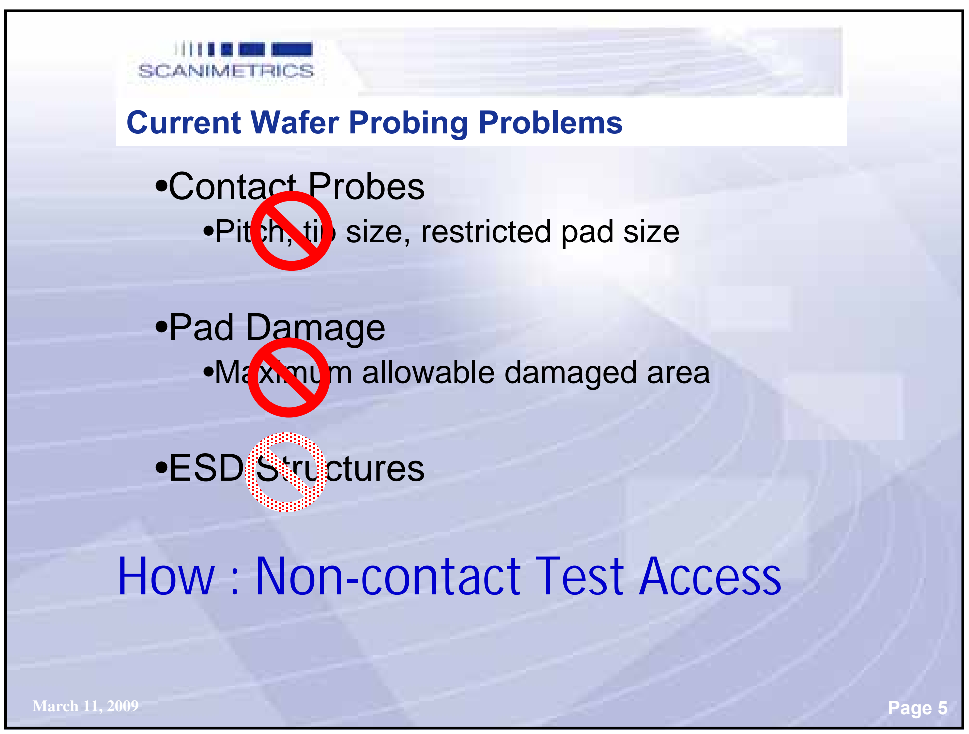
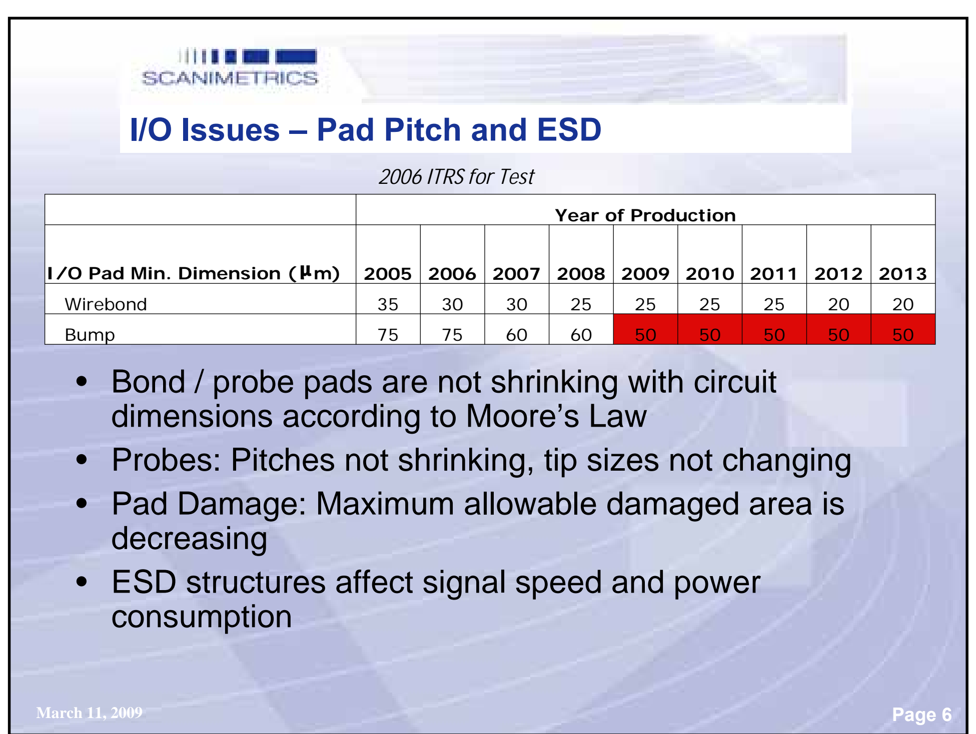

SCANIMETRICS
Semiconductor Technology Driving Change
Non-Contact Wafer Testing and High Performance, Low Power I/O Chip-to-chip Communications
March 11, 2009
Santa Clara Valley Chapter, CPMT Society, IEEE


SCANIMETRICS
Outline
• High Level Company Overview
• Background
• Test Access Issues and WiTAP™ Solution
• Interconnect Issues and UltraI/O™ Solution
• Summary
March 11, 2009
Page 2


SCANIMETRICS
The Company
Scanimetrics provides solutions to bottlenecks imposed by traditional semiconductor I/O circuits
Our solutions address:
• Test access during fabrication and packaging of integrated circuits
• Speed and power consumption of integrated circuits
March 11, 2009
Page 3

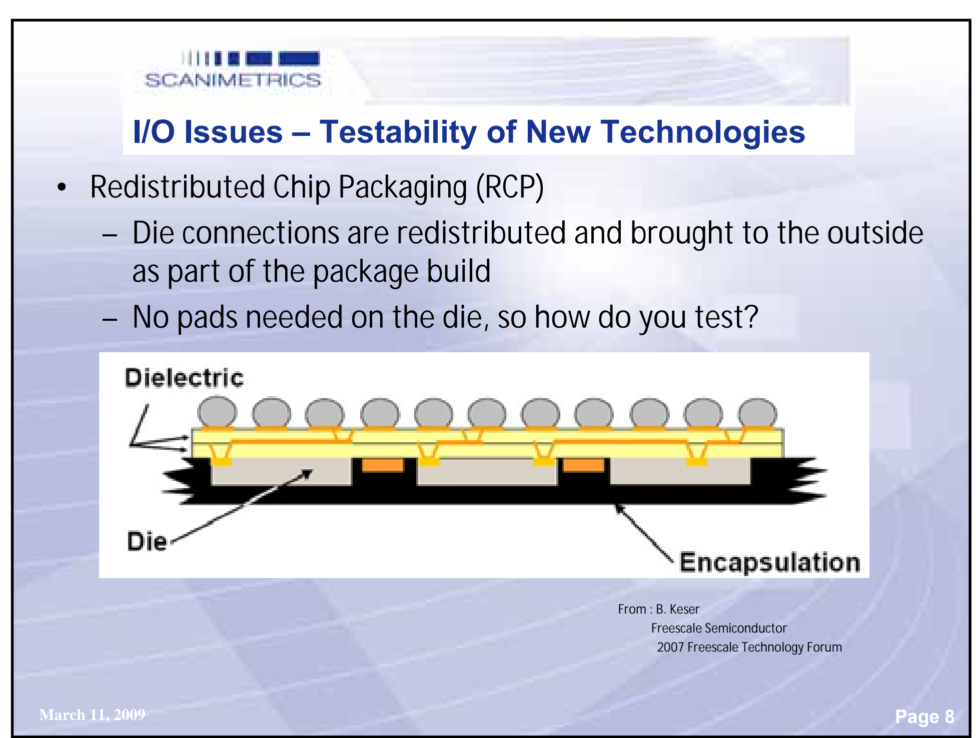

SCANIMETRICS
The Value Chain
Scanimetrics can benefit the entire product chain
Design
Front End Process
Back End Process
• Reduce chip size
• Higher freq I/O
• Lower power
• No particles
• In-line, real time
• No particles
• High Speed
• High throughput
• Lower test cost
• In-line process control
• Reduce total cycle time
• Save KGD
Design
Deposition
Lithography
Etch
Inspection
Wafer Test
Dice
Package
Final Test
"(Scanimetrics) technology is seminal in nature and the impact will be profound." - Denny Sabo, former CEO, Arithmos
March 11, 2009
Page 4



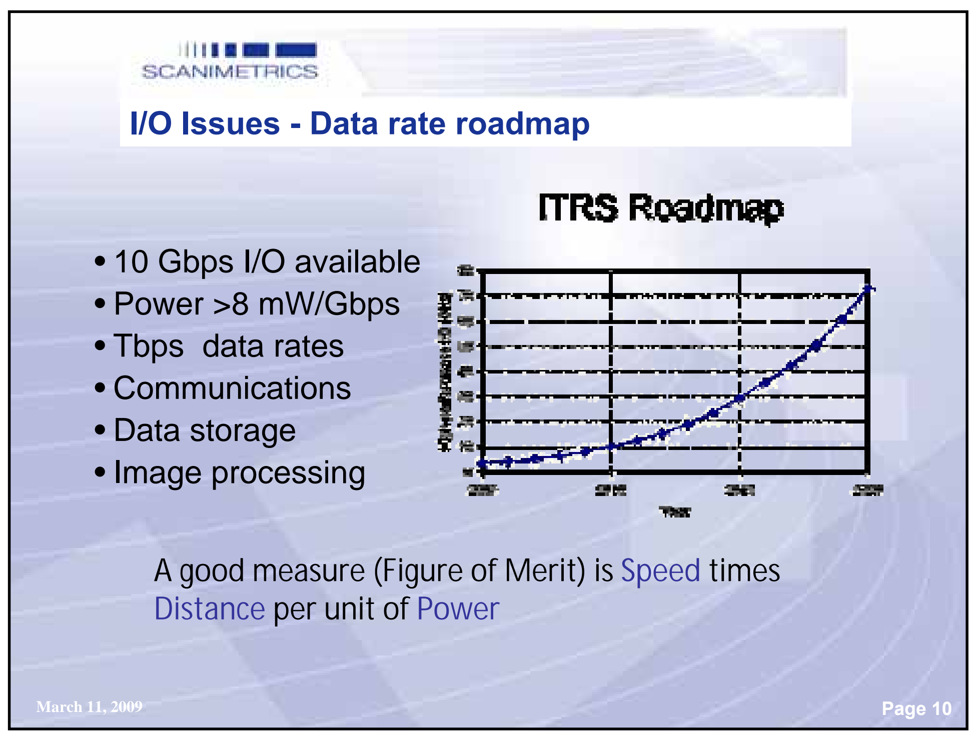


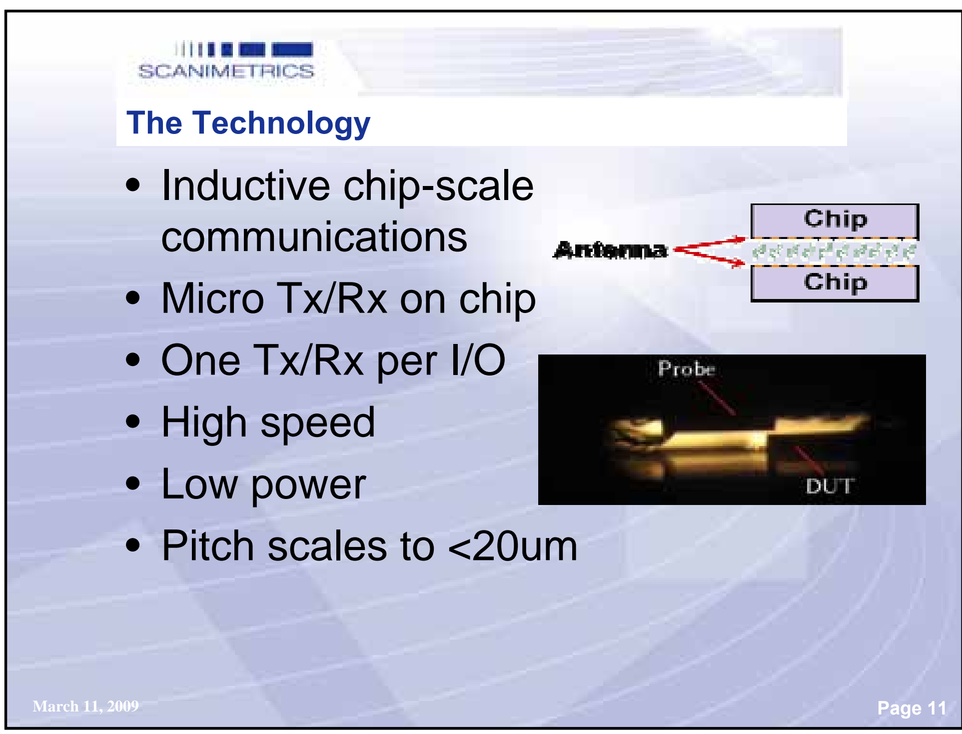
	Year of Production								
I/O Pad Min. Dimension (µm)	2005	2006	2007	2008	2009	2010	2011	2012	2013
Wirebond	35	30	30	25	25	25	25	20	20
Bump	75	75	60	60	50	50	50	50	50

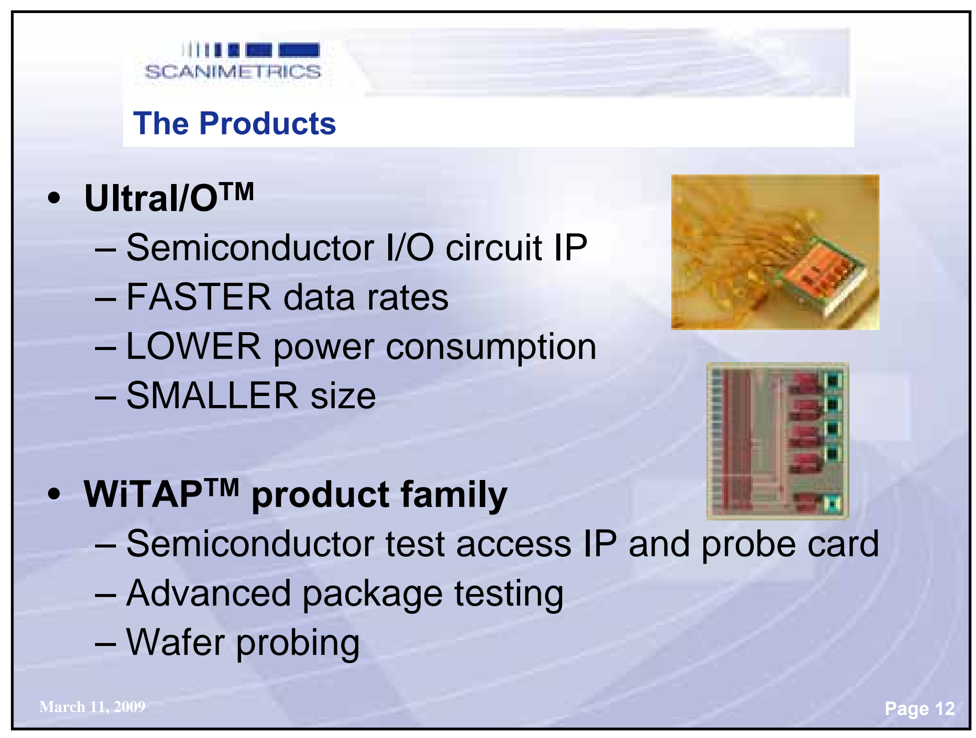
SCANIMETRICS
Packaging is Critical
Packaging is now a limiting factor;
But is an enabler for more than Moore
•Packaging has become the limiting element in system cost and performance
•The assembly and packaging role is expanding to include system level integration functions
•As traditional Moore's Law scaling becomes more difficult innovation in assembly and packaging can take up the slack
March 11, 2009
Page 7

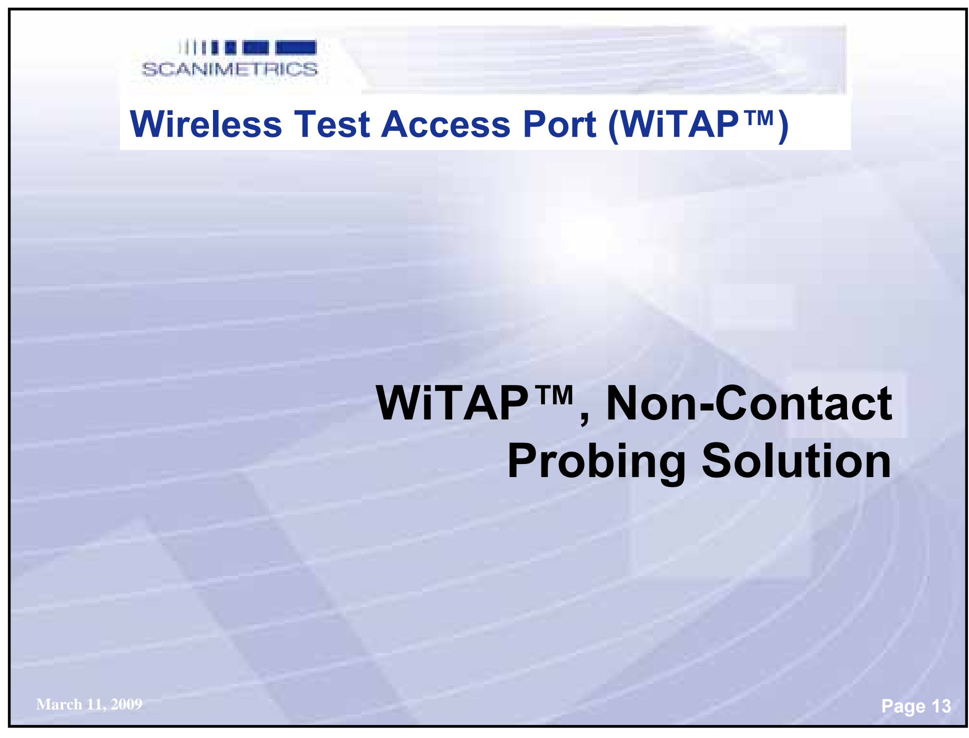

SCANIMETRICS
I/O Issues – Testability of New Technologies
• Redistributed Chip Packaging (RCP)
– Die connections are redistributed and brought to the outside as part of the package build
– No pads needed on the die, so how do you test?
Dielectric
Die
Encapsulation
From : B. Keser
Freescale Semiconductor
2007 Freescale Technology Forum
March 11, 2009
Page 8

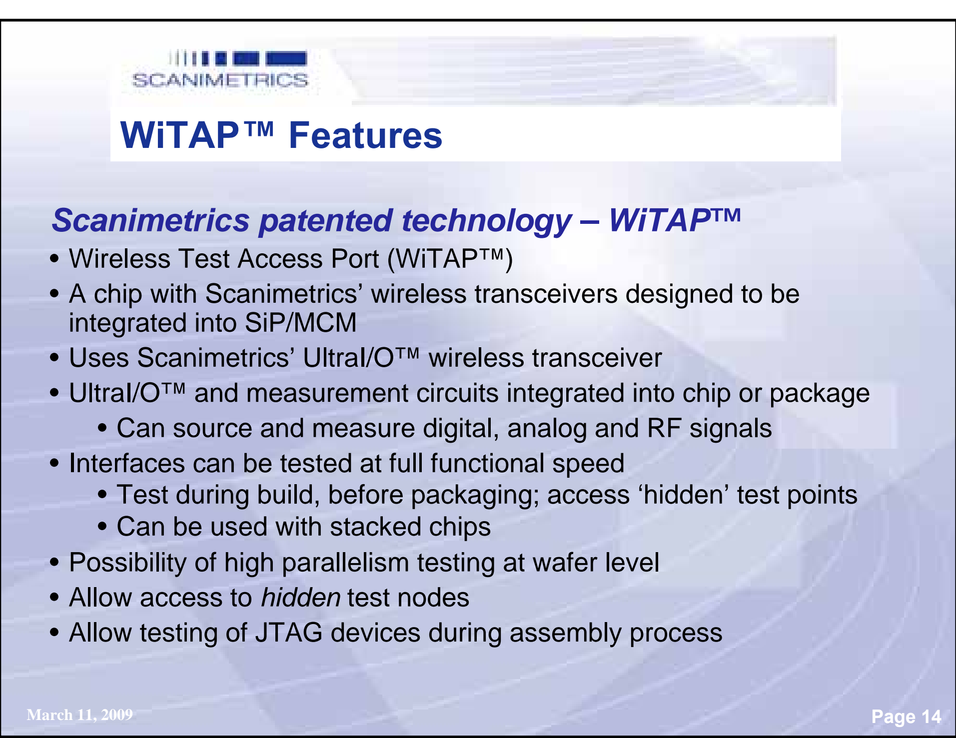
SCANIMETRICS
SiP Challenges
• Assembly yields low
– Yield is product of die yields
– Testability during assembly is non-existent
– Probing SiP modules difficult due to
– Mechanical issues
– Varying component heights
– Good die lost during substrate build-up process
• Design kits for SiP not available from Vendors
• Vendor availability for start-up volumes
– Lack of low-volume manufacturing capacity
March 11, 2009
Page 9

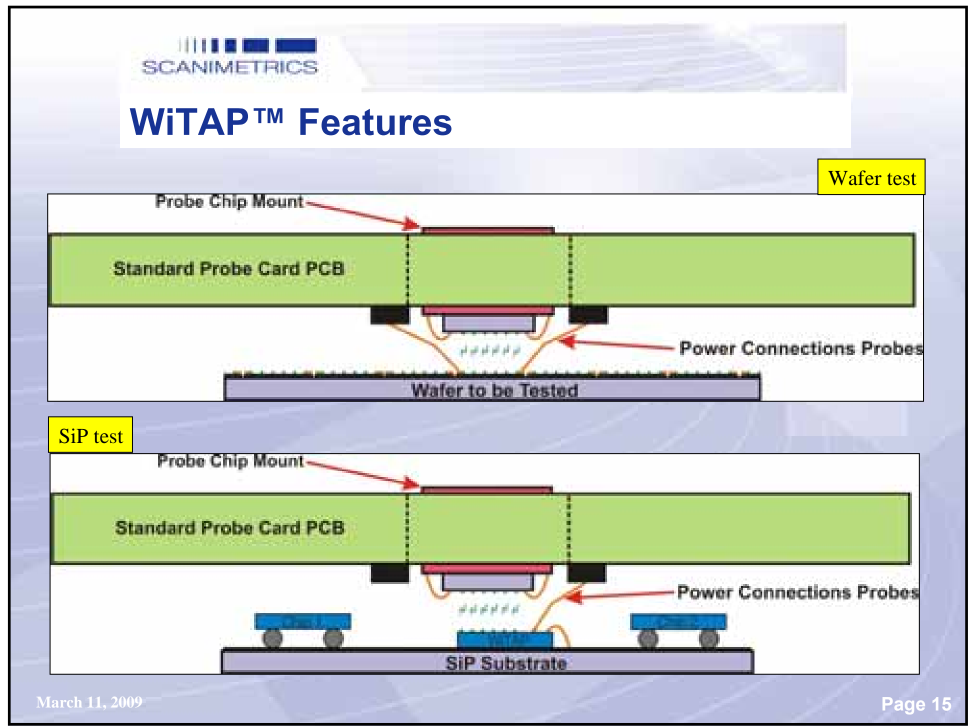

SCANIMETRICS
I/O Issues - Data rate roadmap
ITRS Roadmap
• 10 Gbps I/O available
• Power >8 mW/Gbps
• Tbps data rates
• Communications
• Data storage
• Image processing
A good measure (Figure of Merit) is Speed times Distance per unit of Power
March 11, 2009
Page 10

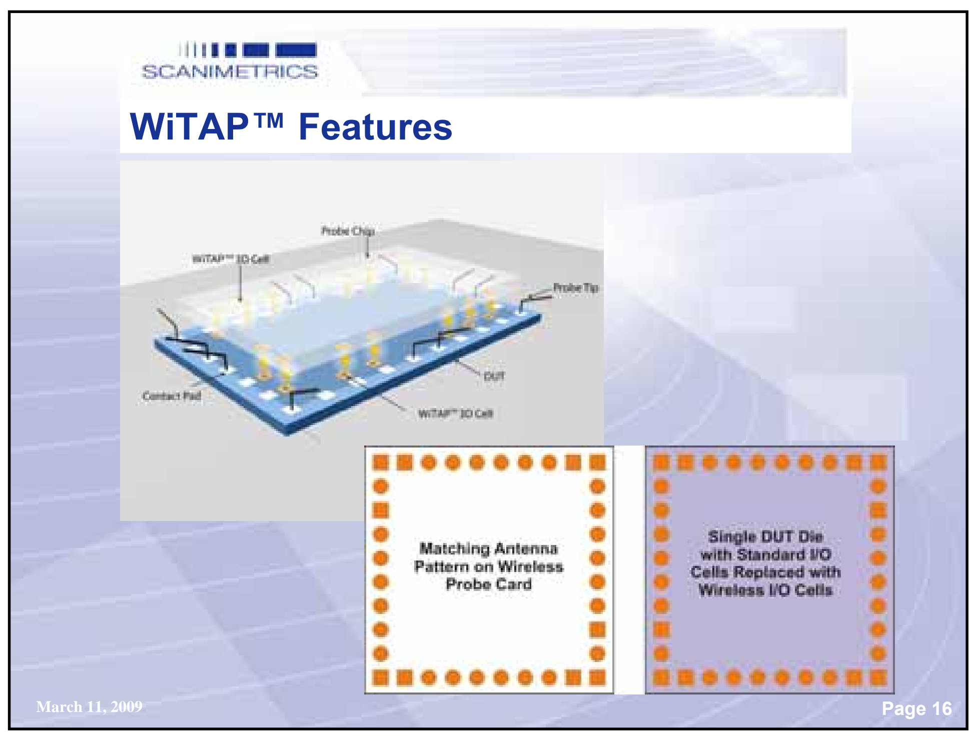

SCANIMETRICS
The Technology
• Inductive chip-scale communications
• Micro Tx/Rx on chip
• One Tx/Rx per I/O
• High speed
• Low power
• Pitch scales to <20um
Antenna
Chip
Chip
Probe
DUT
March 11, 2009
Page 11

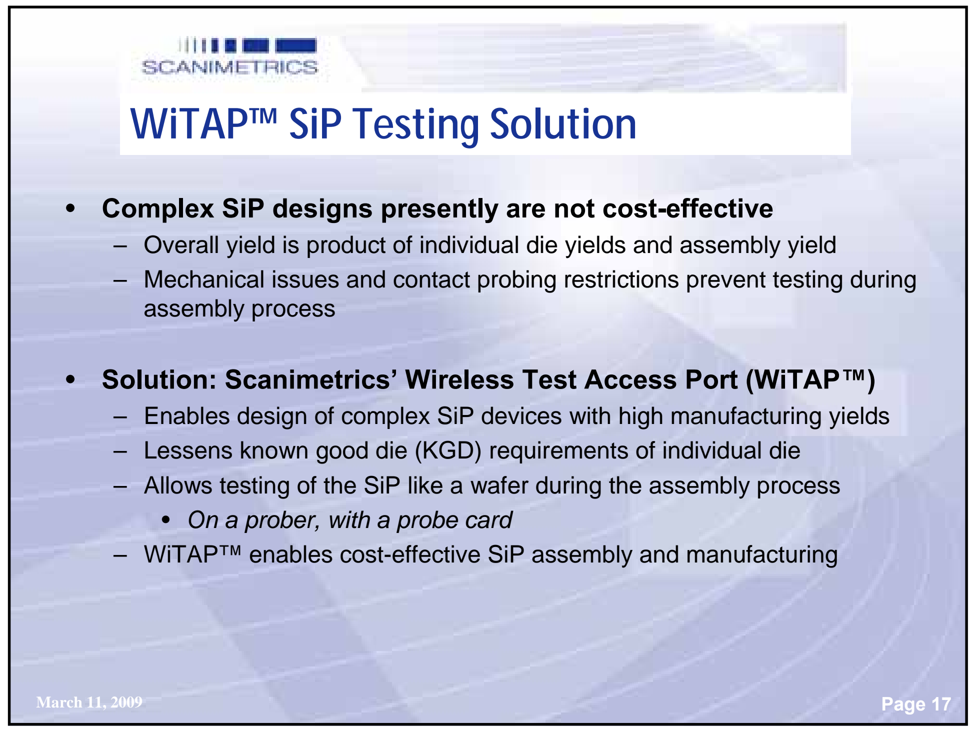

SCANIMETRICS
The Products
• Ultral/O™
– Semiconductor I/O circuit IP
– FASTER data rates
– LOWER power consumption
– SMALLER size
• WiTAP™ product family
– Semiconductor test access IP and probe card
– Advanced package testing
– Wafer probing
March 11, 2009
Page 12


SCANIMETRICS
Wireless Test Access Port (WiTAP™)
WiTAP™, Non-Contact Probing Solution
March 11, 2009
Page 13


SCANIMETRICS
WiTAP™ Features
Scanimetrics patented technology – WiTAP™
• Wireless Test Access Port (WiTAP™)
• A chip with Scanimetrics' wireless transceivers designed to be integrated into SiP/MCM
• Uses Scanimetrics' UltraI/O™ wireless transceiver
• UltraI/O™ and measurement circuits integrated into chip or package
• Can source and measure digital, analog and RF signals
• Interfaces can be tested at full functional speed
• Test during build, before packaging; access 'hidden' test points
• Can be used with stacked chips
• Possibility of high parallelism testing at wafer level
• Allow access to hidden test nodes
• Allow testing of JTAG devices during assembly process
March 11, 2009
Page 14


SCANIMETRICS
WiTAP™ Features
Wafer test
Probe Chip Mount
Standard Probe Card PCB
Power Connections Probes
Wafer to be Tested
SiP test
Probe Chip Mount
Standard Probe Card PCB
Power Connections Probes
SiP Substrate
March 11, 2009
Page 15


SCANIMETRICS
WiTAP™ Features
Probe Chip
WiTAP™ IO Cell
Probe Tip
DUT
Contact Pad
WiTAP™ IO Cell
Matching Antenna Pattern on Wireless Probe Card
Single DUT Die with Standard I/O Cells Replaced with Wireless I/O Cells
March 11, 2009
Page 16


SCANIMETRICS
WiTAP™ SiP Testing Solution
• Complex SiP designs presently are not cost-effective
– Overall yield is product of individual die yields and assembly yield
– Mechanical issues and contact probing restrictions prevent testing during assembly process
• Solution: Scanimetrics' Wireless Test Access Port (WiTAP™)
– Enables design of complex SiP devices with high manufacturing yields
– Lessens known good die (KGD) requirements of individual die
– Allows testing of the SiP like a wafer during the assembly process
• On a prober, with a probe card
– WiTAP™ enables cost-effective SiP assembly and manufacturing
March 11, 2009
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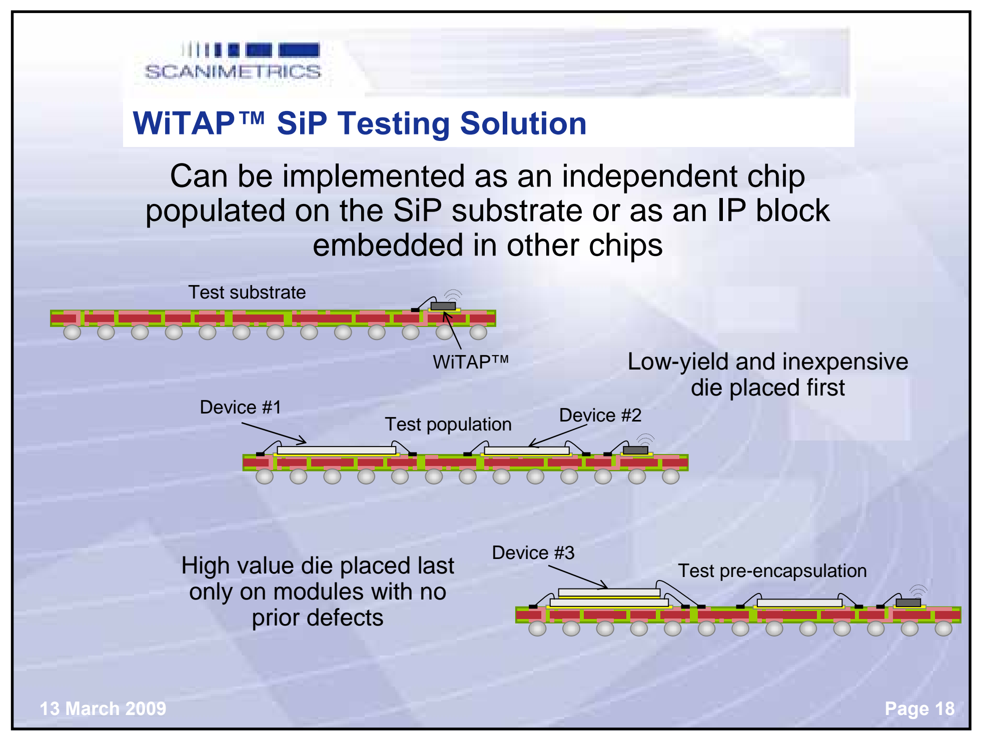
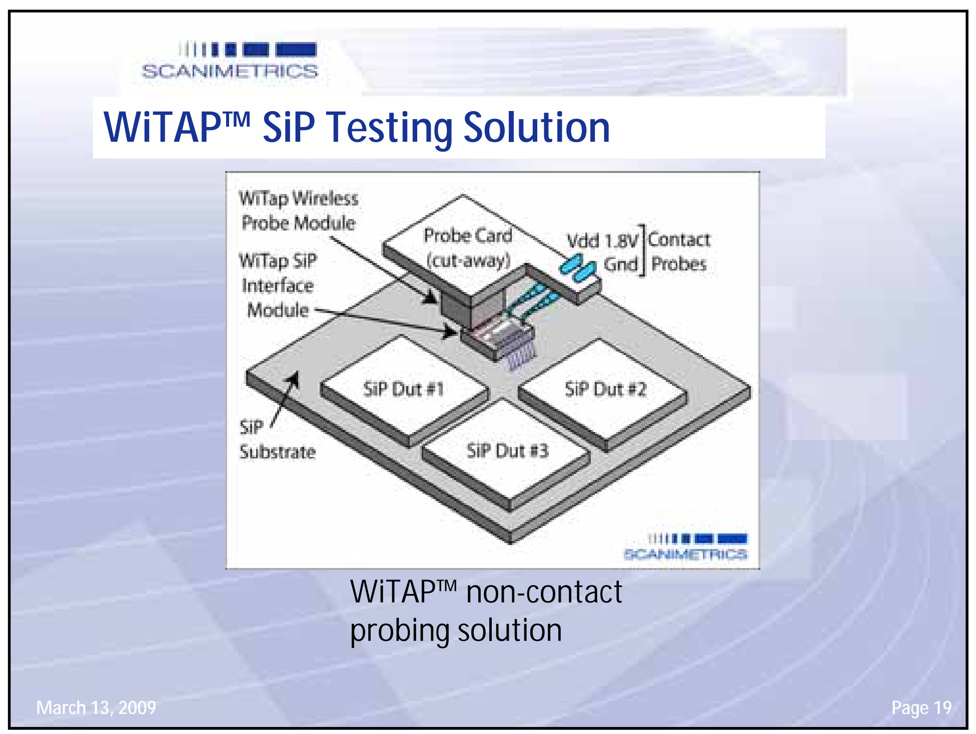
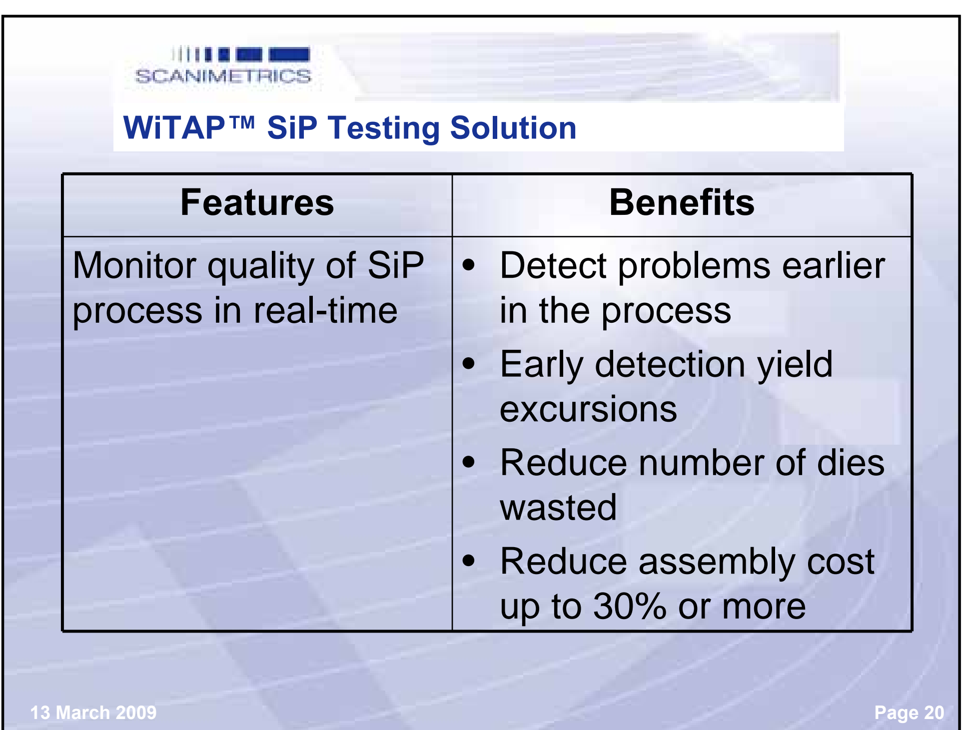

SCANIMETRICS
WiTAP™ SiP Testing Solution
Can be implemented as an independent chip populated on the SiP substrate or as an IP block embedded in other chips
Test substrate
WiTAP™
Low-yield and inexpensive die placed first
Device #1
Test population
Device #2
High value die placed last only on modules with no prior defects
Device #3
Test pre-encapsulation
13 March 2009
Page 18





Features	Benefits
Monitor quality of SiP process in real-time	• Detect problems earlier in the process • Early detection yield excursions • Reduce number of dies wasted • Reduce assembly cost up to 30% or more

SCANIMETRICS

WiTAP™ SiP Testing Solution

Features	Benefits
Non-contact signal probing at high speeds	• Less probing debris • Less damage to circuits and pads • Less damage to probe cards • More robust process • Full speed testing at wafer level

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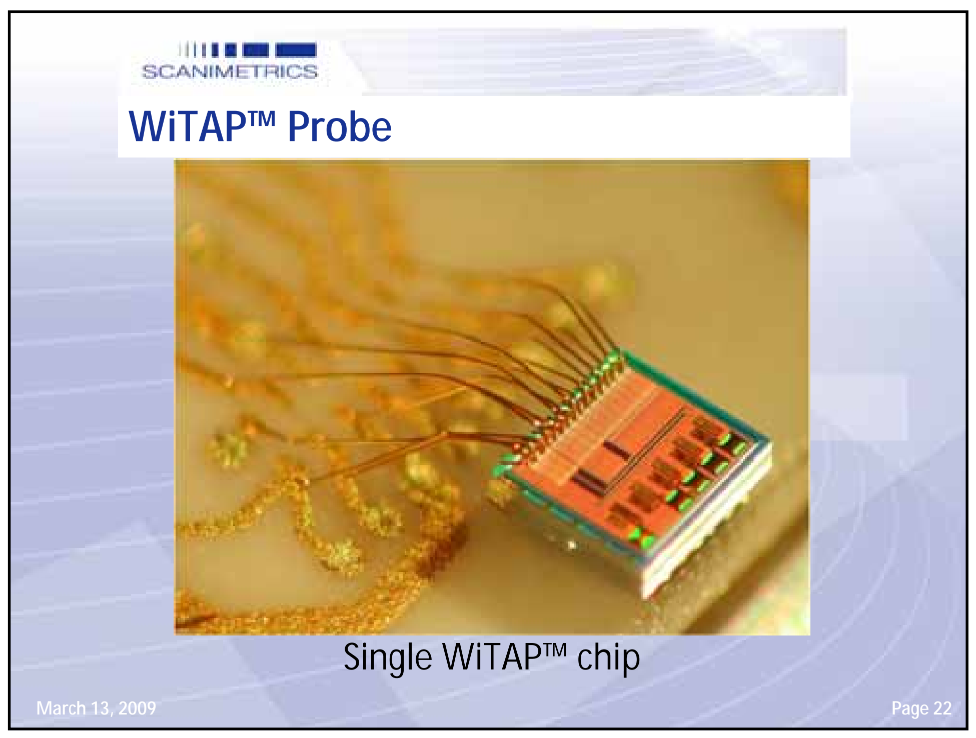
SCANIMETRICS

WiTAP™ Probe



Single WiTAP™ chip

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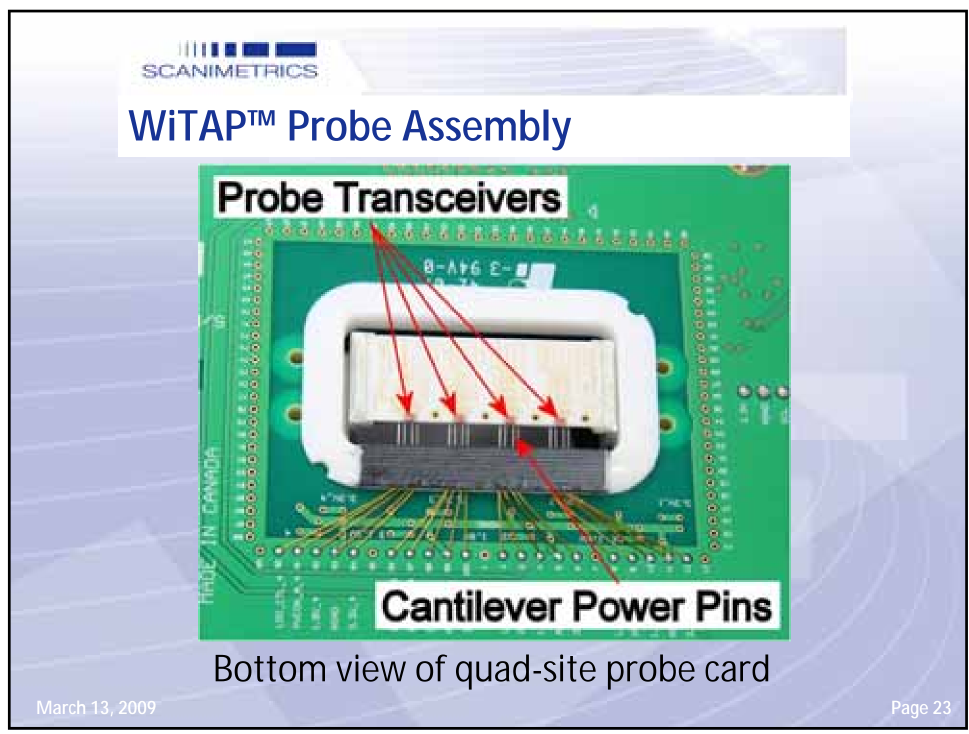
SCANIMETRICS
WiTAP™ Probe Assembly
Probe Transceivers
Cantilever Power Pins
Bottom view of quad-site probe card
March 13, 2009
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SCANIMETRICS
WiTAP™ Probe Card
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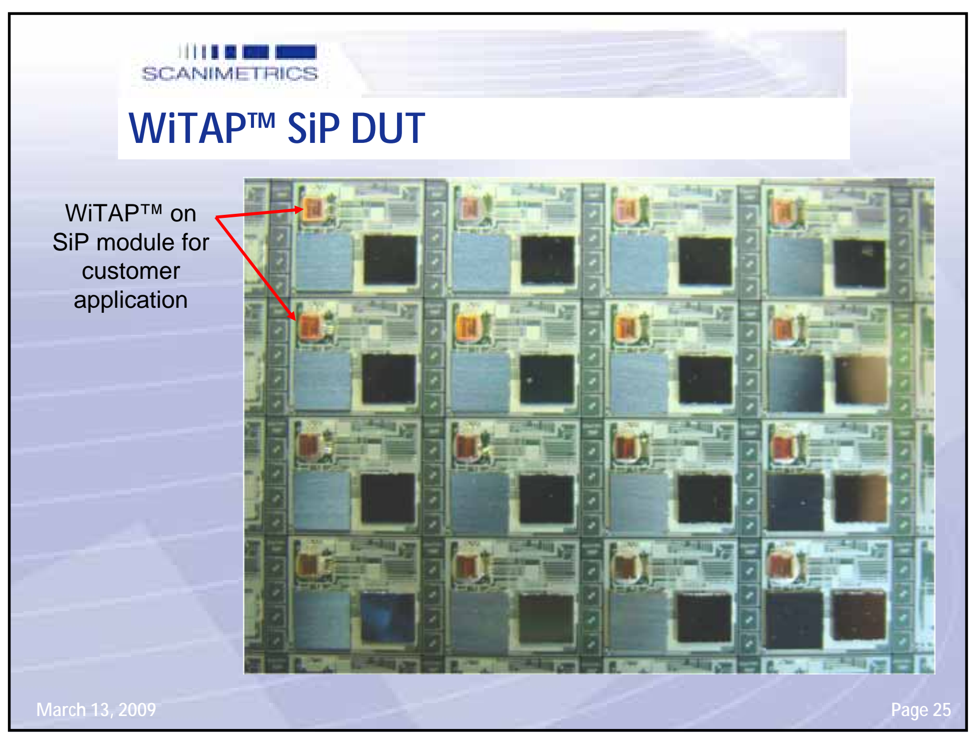
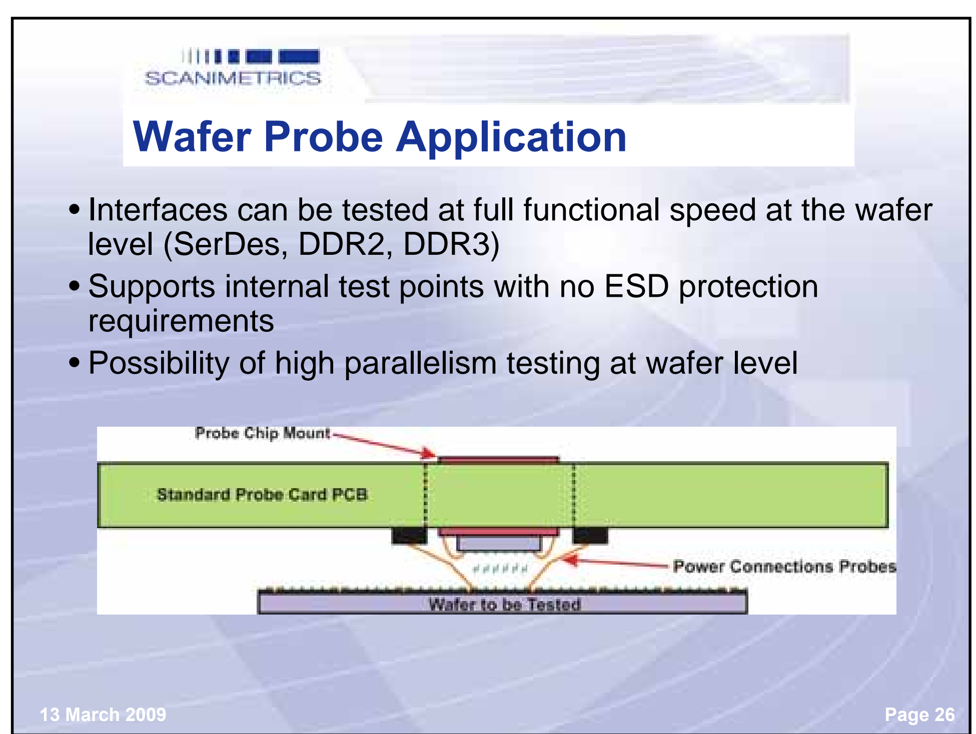
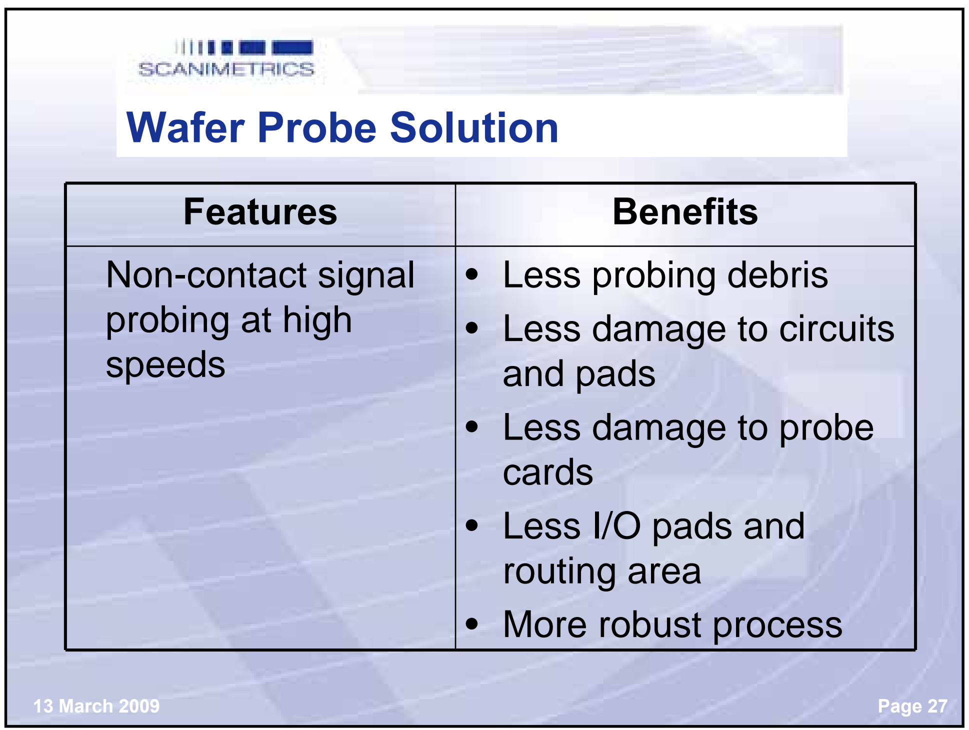

SCANIMETRICS
WiTAP™ SiP DUT
WiTAP™ on SiP module for customer application
March 13, 2009
Page 25


SCANIMETRICS
Wafer Probe Application
• Interfaces can be tested at full functional speed at the wafer level (SerDes, DDR2, DDR3)
• Supports internal test points with no ESD protection requirements
• Possibility of high parallelism testing at wafer level
Probe Chip Mount
Standard Probe Card PCB
Power Connections Probes
Wafer to be Tested
13 March 2009
Page 26


SCANIMETRICS
Wafer Probe Solution
Features
Benefits
Non-contact signal probing at high speeds
• Less probing debris
• Less damage to circuits and pads
• Less damage to probe cards
• Less I/O pads and routing area
• More robust process
13 March 2009
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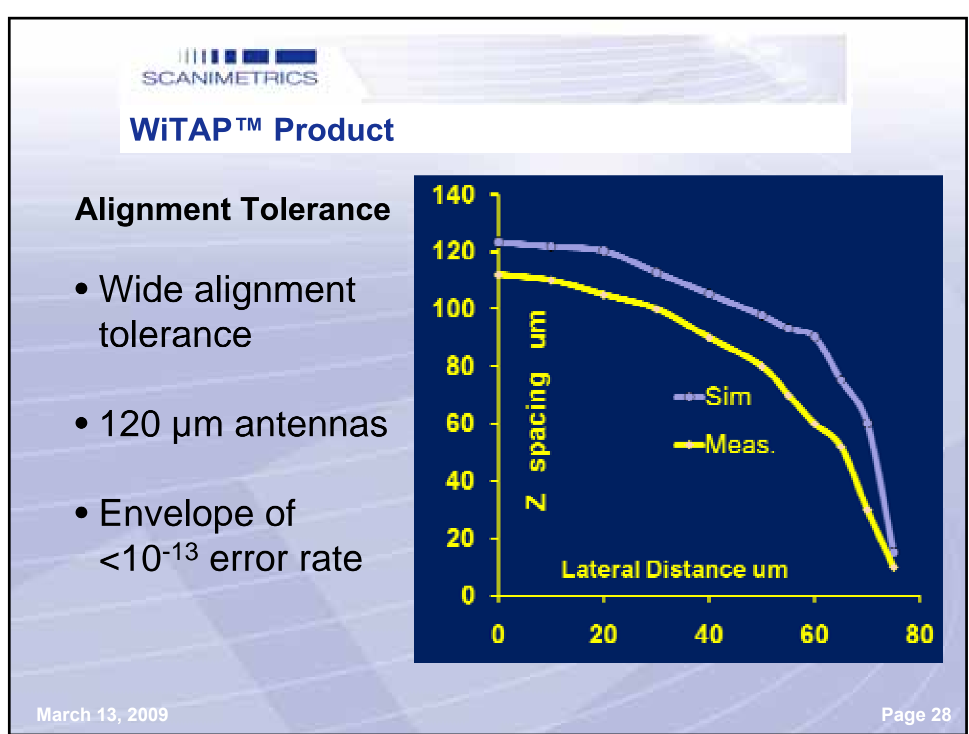
SCANIMETRICS
WiTAP™ Product
Alignment Tolerance
• Wide alignment tolerance
• 120 µm antennas
• Envelope of <10-13 error rate
Z spacing um
Lateral Distance um
Sim
Meas.
0
20
40
60
80
100
120
140
March 13, 2009
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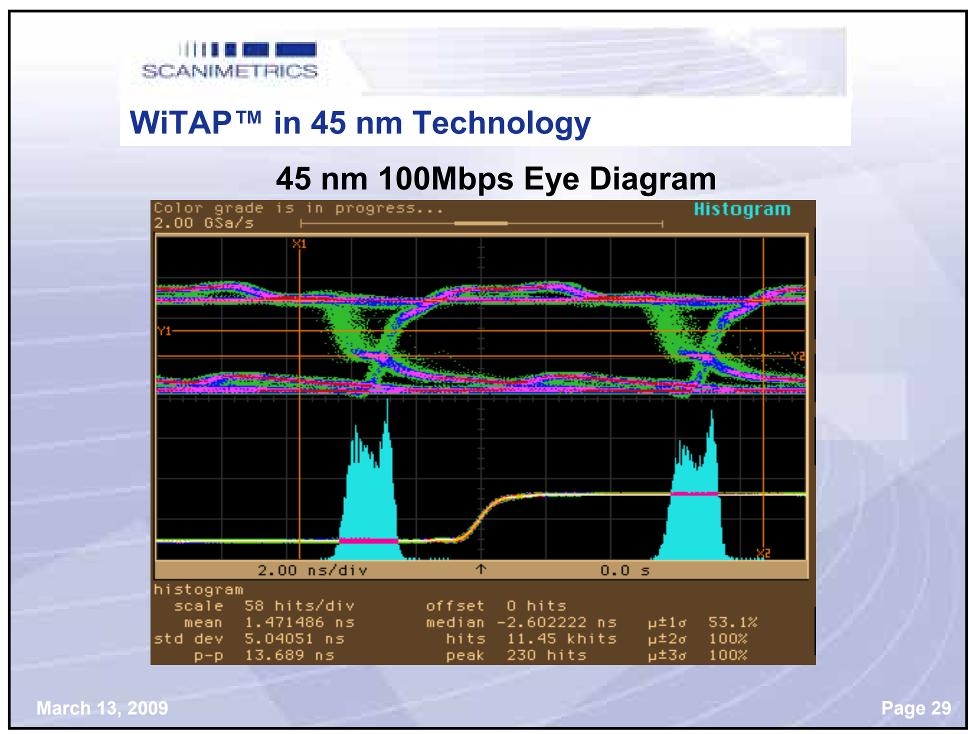
SCANIMETRICS
WiTAP™ in 45 nm Technology
45 nm 100Mbps Eye Diagram
Color grade is in progress...
2.00 GSa/s
Histogram
2.00 ns/div
0.0 s
histogram
scale 58 hits/div
mean 1.471486 ns
std dev 5.04051 ns
p-p 13.689 ns
offset 0 hits
median -2.602222 ns
hits 11.45 khits
peak 230 hits
μ±1σ 53.1%
μ±2σ 100%
μ±3σ 100%
March 13, 2009
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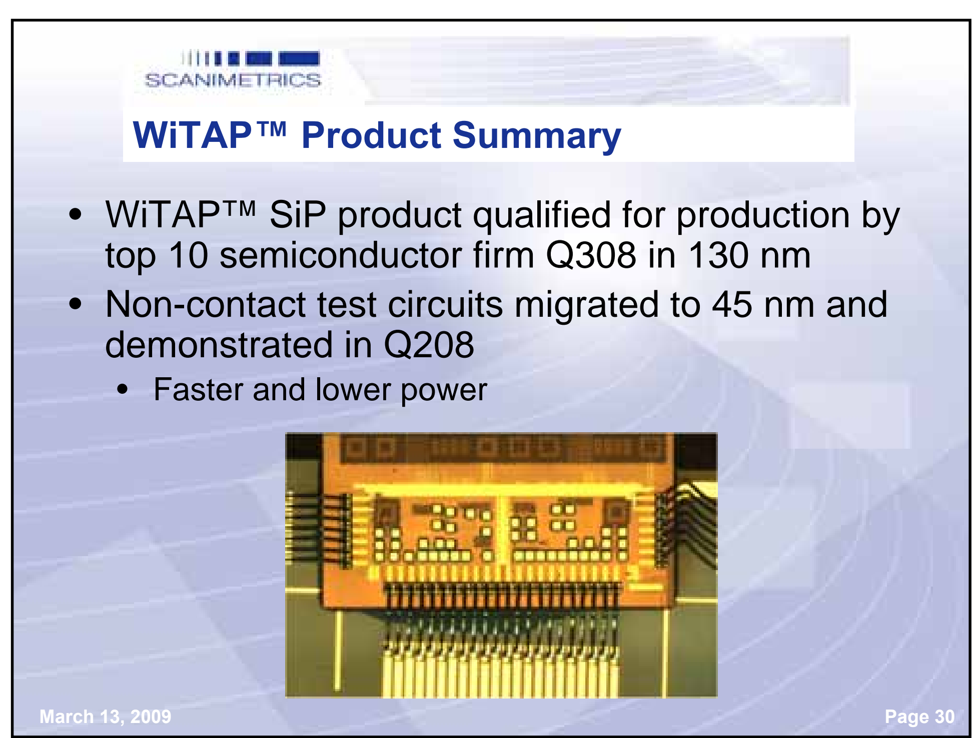
SCANIMETRICS
WiTAP™ Product Summary
• WiTAP™ SiP product qualified for production by top 10 semiconductor firm Q308 in 130 nm
• Non-contact test circuits migrated to 45 nm and demonstrated in Q208
• Faster and lower power
March 13, 2009
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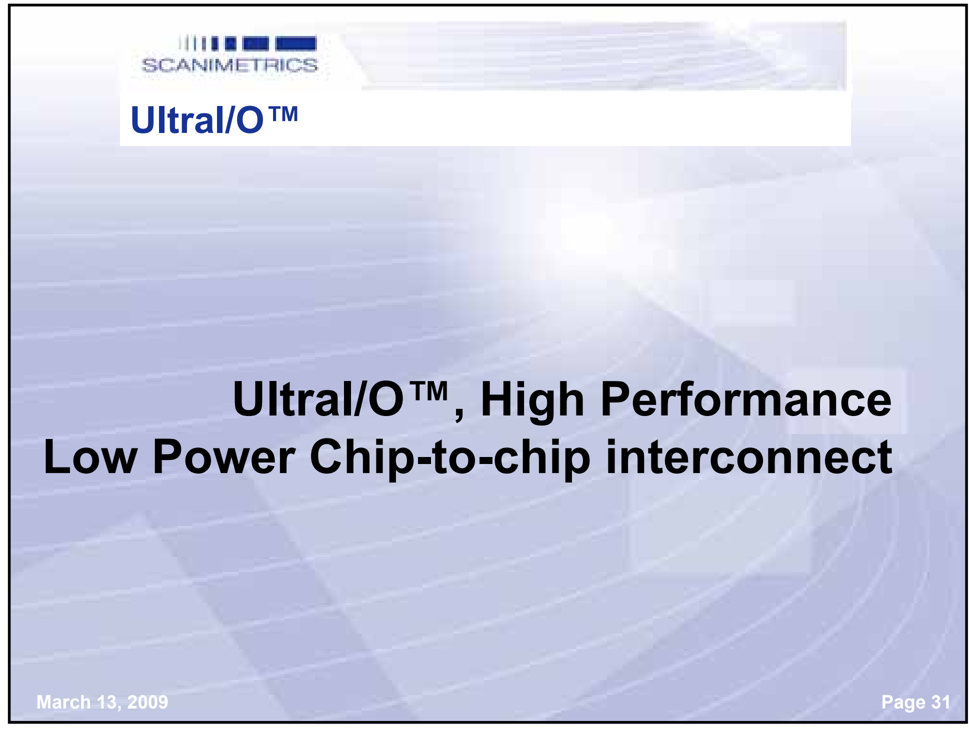
SCANIMETRICS
UltraI/O™
UltraI/O™, High Performance
Low Power Chip-to-chip interconnect
March 13, 2009
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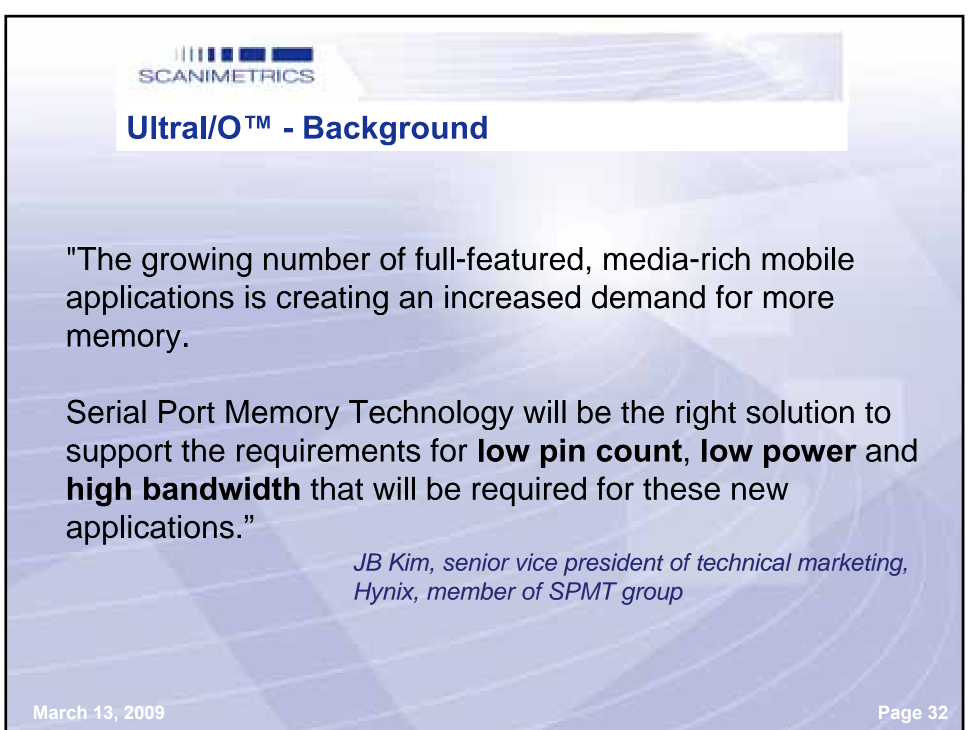
SCANIMETRICS
UltraI/O™ - Background
"The growing number of full-featured, media-rich mobile applications is creating an increased demand for more memory.
Serial Port Memory Technology will be the right solution to support the requirements for low pin count, low power and high bandwidth that will be required for these new applications."
JB Kim, senior vice president of technical marketing, Hynix, member of SPMT group
March 13, 2009
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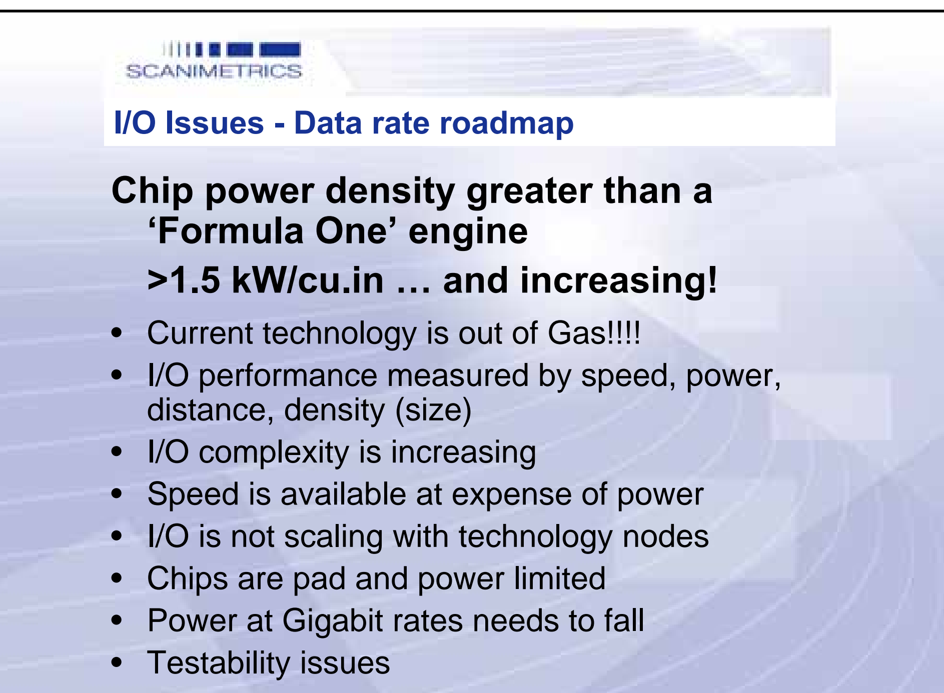
SCANIMETRICS
I/O Issues - Data rate roadmap
Chip power density greater than a 'Formula One' engine
>1.5 kW/cu.in … and increasing!
• Current technology is out of Gas!!!!
• I/O performance measured by speed, power, distance, density (size)
• I/O complexity is increasing
• Speed is available at expense of power
• I/O is not scaling with technology nodes
• Chips are pad and power limited
• Power at Gigabit rates needs to fall
• Testability issues
March 13, 2009
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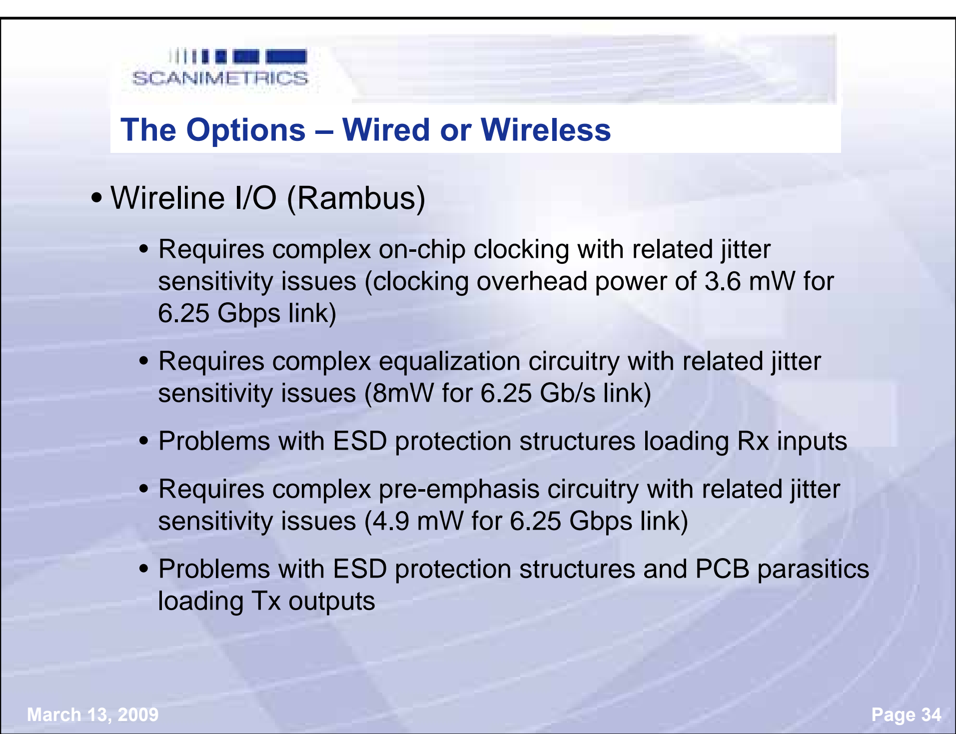
SCANIMETRICS
The Options – Wired or Wireless
• Wireline I/O (Rambus)
• Requires complex on-chip clocking with related jitter sensitivity issues (clocking overhead power of 3.6 mW for 6.25 Gbps link)
• Requires complex equalization circuitry with related jitter sensitivity issues (8mW for 6.25 Gb/s link)
• Problems with ESD protection structures loading Rx inputs
• Requires complex pre-emphasis circuitry with related jitter sensitivity issues (4.9 mW for 6.25 Gbps link)
• Problems with ESD protection structures and PCB parasitics loading Tx outputs
March 13, 2009
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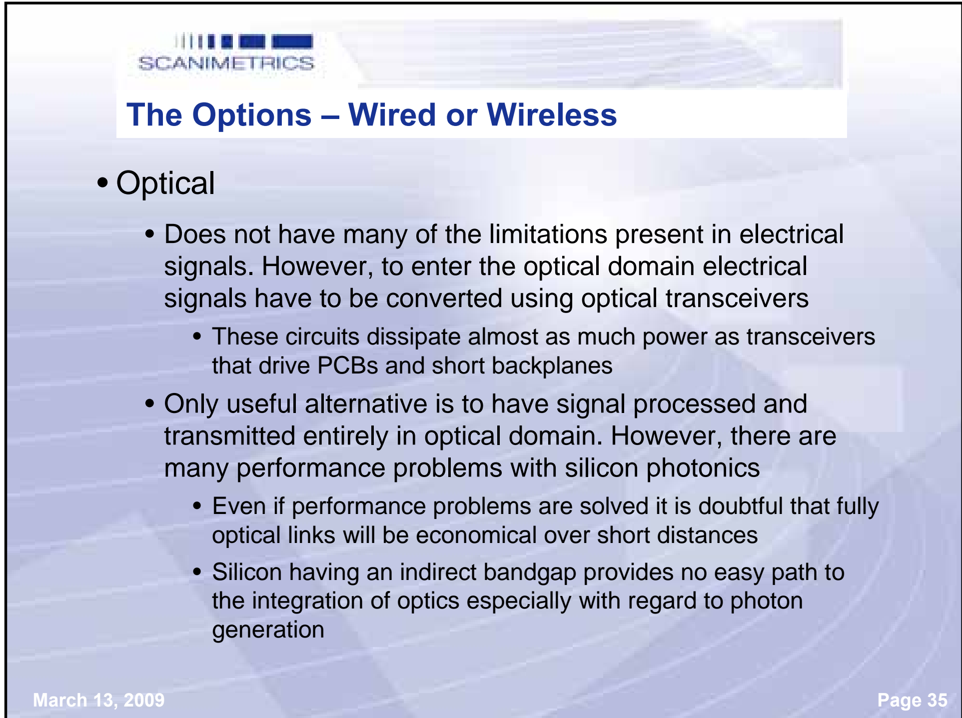
SCANIMETRICS
The Options – Wired or Wireless
• Optical
• Does not have many of the limitations present in electrical signals. However, to enter the optical domain electrical signals have to be converted using optical transceivers
• These circuits dissipate almost as much power as transceivers that drive PCBs and short backplanes
• Only useful alternative is to have signal processed and transmitted entirely in optical domain. However, there are many performance problems with silicon photonics
• Even if performance problems are solved it is doubtful that fully optical links will be economical over short distances
• Silicon having an indirect bandgap provides no easy path to the integration of optics especially with regard to photon generation
March 13, 2009
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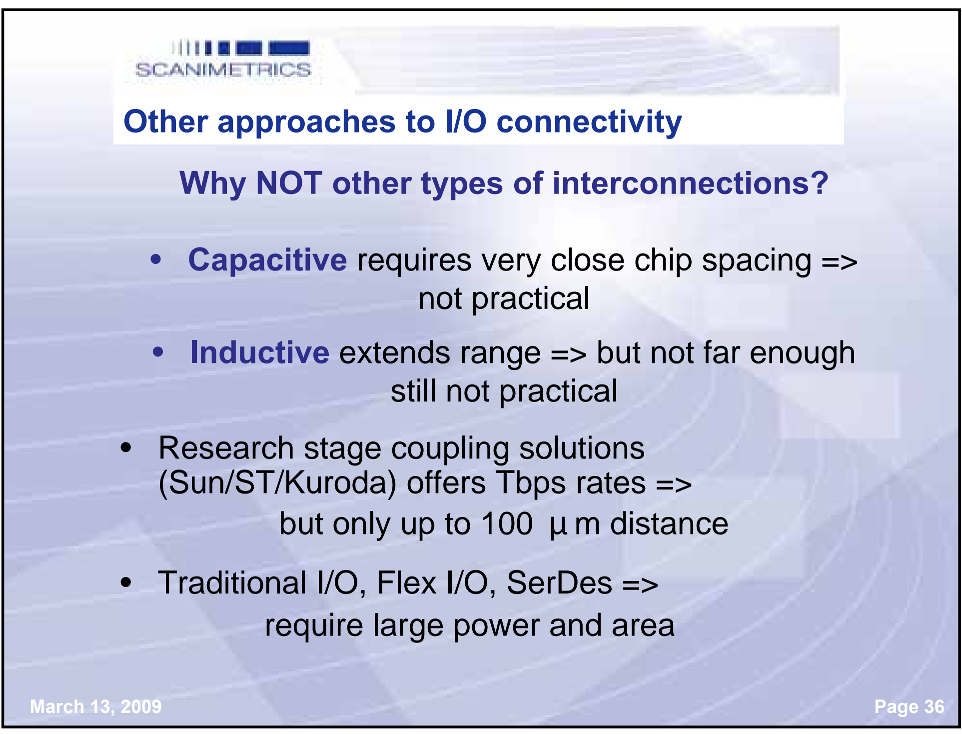
SCANIMETRICS
Other approaches to I/O connectivity
Why NOT other types of interconnections?
• Capacitive requires very close chip spacing => not practical
• Inductive extends range => but not far enough still not practical
• Research stage coupling solutions (Sun/ST/Kuroda) offers Tbps rates => but only up to 100 µm distance
• Traditional I/O, Flex I/O, SerDes => require large power and area
March 13, 2009
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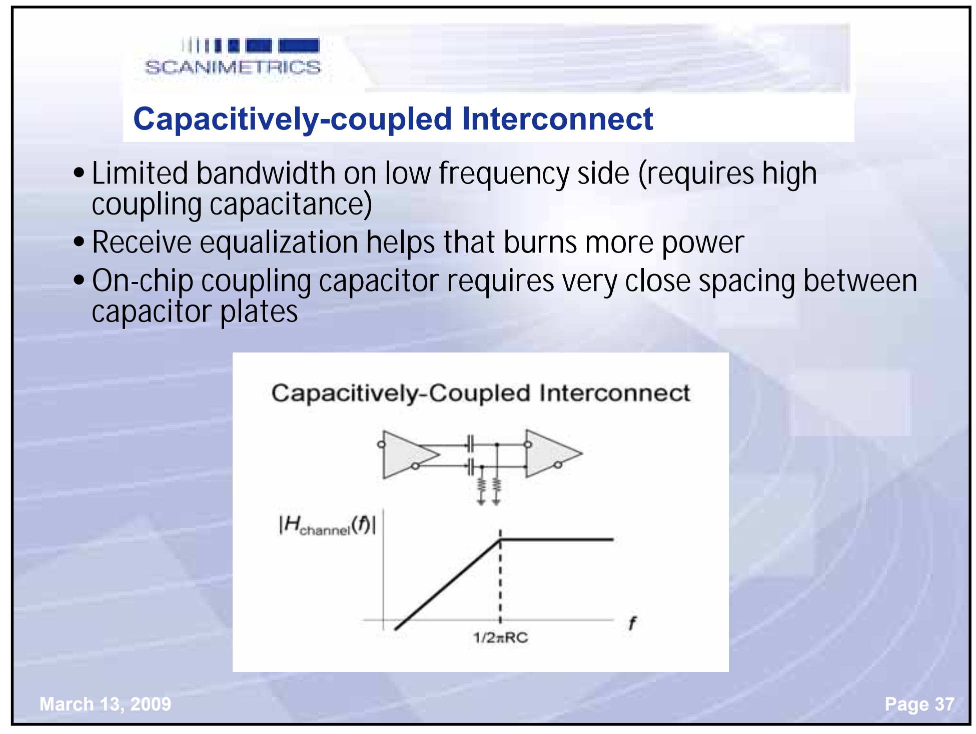
SCANIMETRICS
Capacitively-coupled Interconnect
• Limited bandwidth on low frequency side (requires high coupling capacitance)
• Receive equalization helps that burns more power
• On-chip coupling capacitor requires very close spacing between capacitor plates
Capacitively-Coupled Interconnect
|Hchannel(f)|
f
1/2πRC
March 13, 2009
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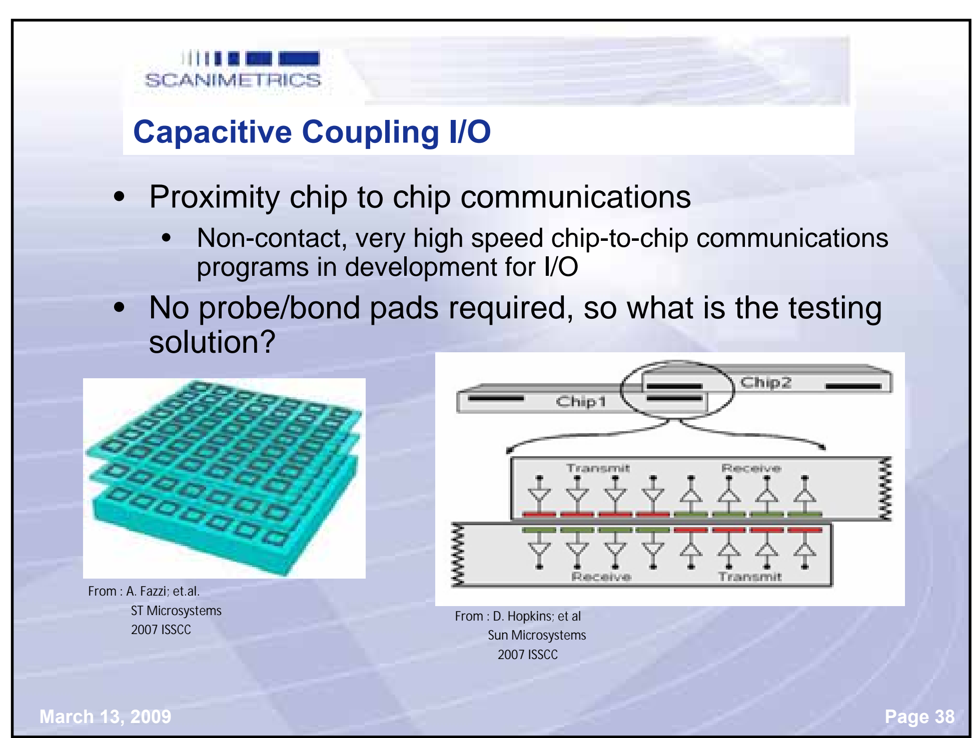
SCANIMETRICS
Capacitive Coupling I/O
• Proximity chip to chip communications
• Non-contact, very high speed chip-to-chip communications programs in development for I/O
• No probe/bond pads required, so what is the testing solution?
Chip1
Chip2
Transmit
Receive
Receive
Transmit
From : A. Fazzi; et.al.
ST Microsystems
2007 ISSCC
From : D. Hopkins; et al
Sun Microsystems
2007 ISSCC
March 13, 2009
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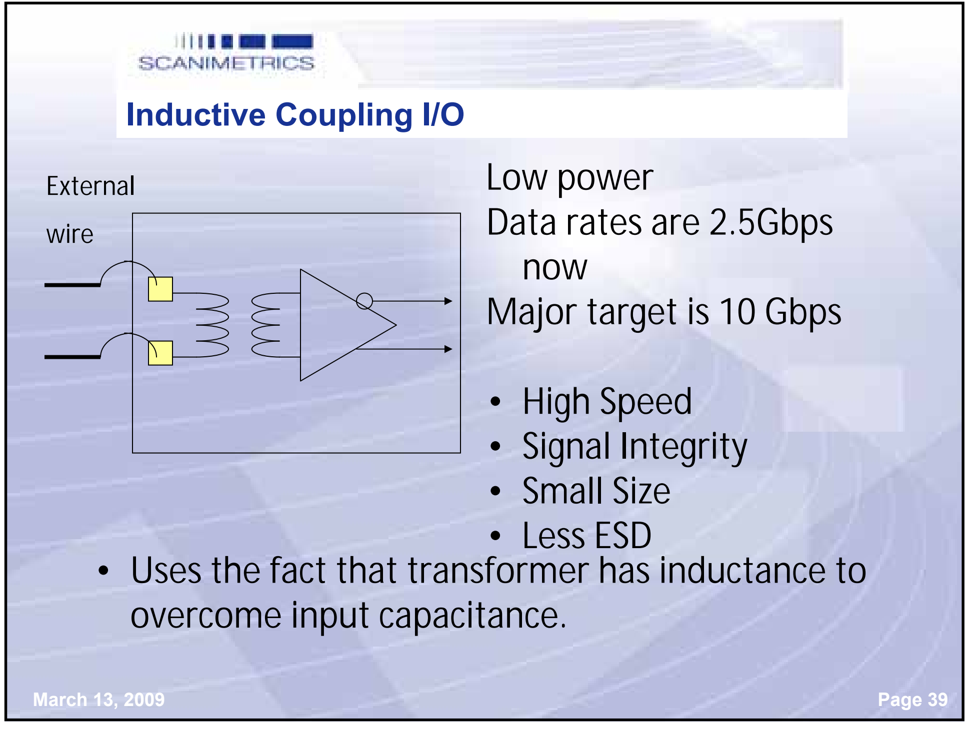
SCANIMETRICS
Inductive Coupling I/O
External
wire
Low power
Data rates are 2.5Gbps now
Major target is 10 Gbps
• High Speed
• Signal Integrity
• Small Size
• Less ESD
• Uses the fact that transformer has inductance to overcome input capacitance.
March 13, 2009
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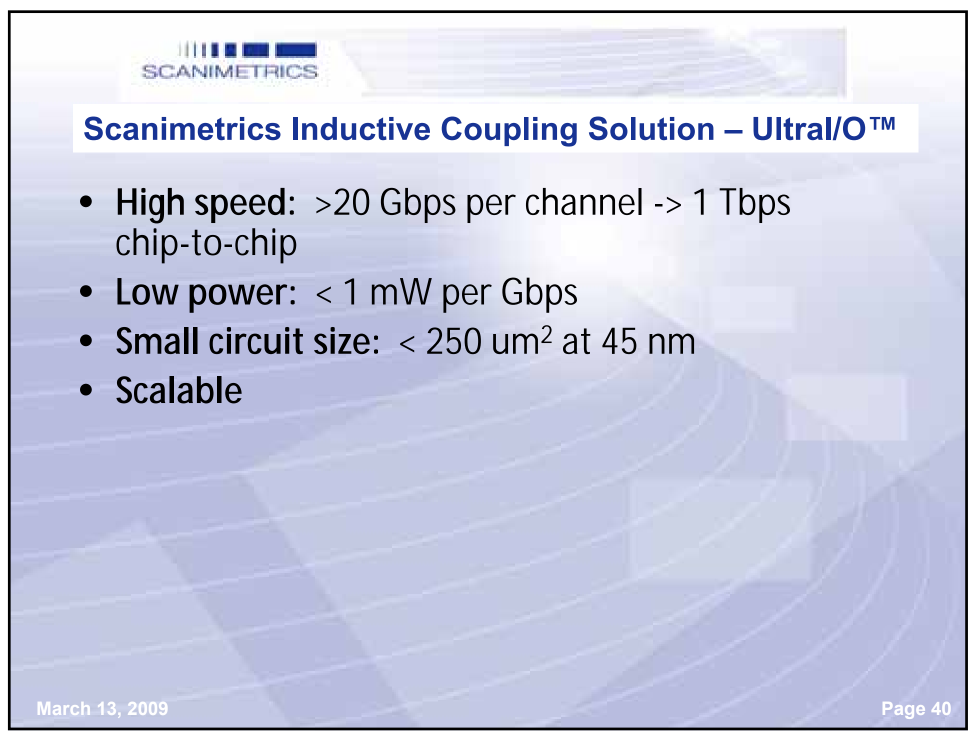
SCANIMETRICS
Scanimetrics Inductive Coupling Solution – UltraI/O™
• High speed: >20 Gbps per channel -> 1 Tbps chip-to-chip
• Low power: < 1 mW per Gbps
• Small circuit size: < 250 um² at 45 nm
• Scalable
March 13, 2009
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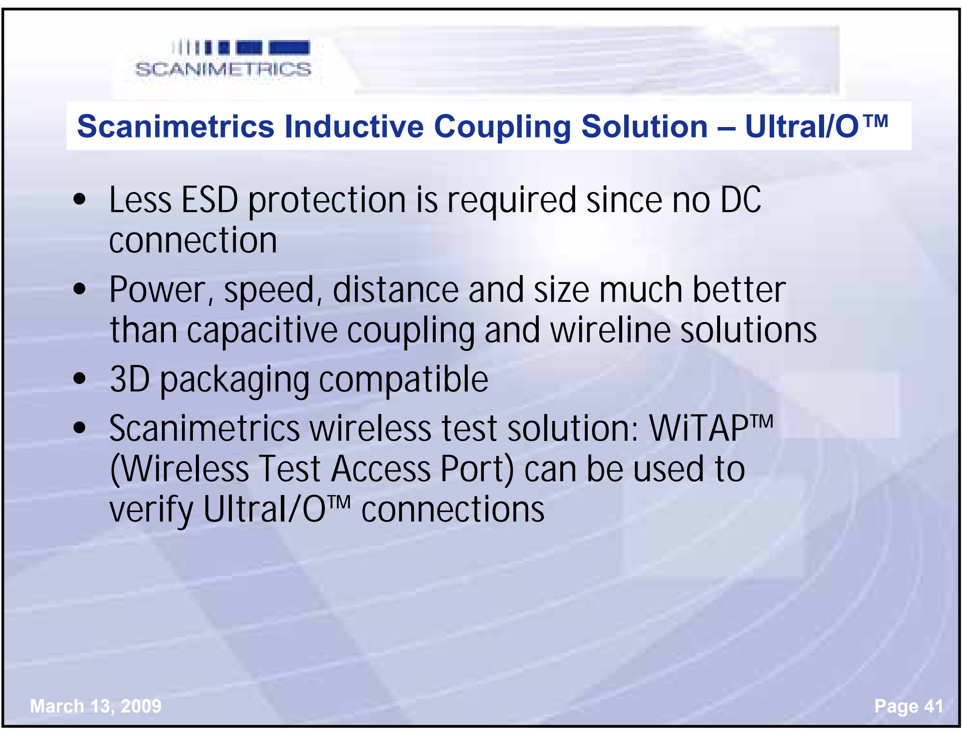
SCANIMETRICS
Scanimetrics Inductive Coupling Solution – UltraI/O™
• Less ESD protection is required since no DC connection
• Power, speed, distance and size much better than capacitive coupling and wireline solutions
• 3D packaging compatible
• Scanimetrics wireless test solution: WiTAP™ (Wireless Test Access Port) can be used to verify UltraI/O™ connections
March 13, 2009
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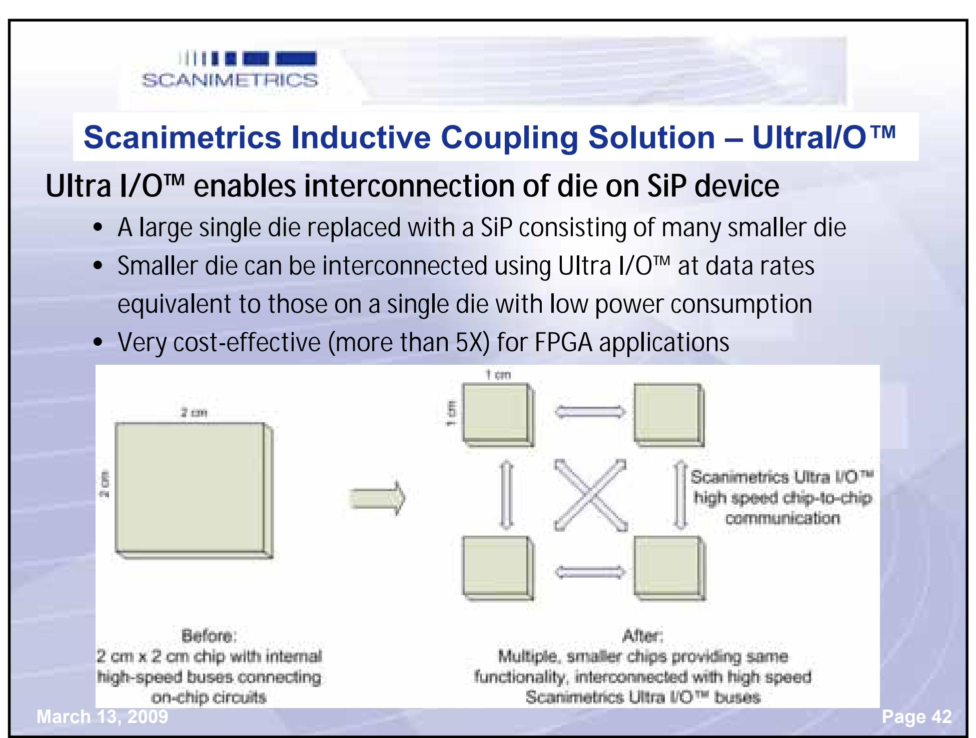
SCANIMETRICS
Scanimetrics Inductive Coupling Solution – UltraI/O™
Ultra I/O™ enables interconnection of die on SiP device
• A large single die replaced with a SiP consisting of many smaller die
• Smaller die can be interconnected using Ultra I/O™ at data rates equivalent to those on a single die with low power consumption
• Very cost-effective (more than 5X) for FPGA applications
2 cm
2 cm
1 cm
1 cm
Scanimetrics Ultra I/O™ high speed chip-to-chip communication
Before:
2 cm x 2 cm chip with internal high-speed buses connecting on-chip circuits
After:
Multiple, smaller chips providing same functionality, interconnected with high speed Scanimetrics Ultra I/O™ buses
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SCANIMETRICS
UltraI/O™ features and benefits
Feature
Benefit
Higher Bandwidth
Higher performance designs
Fewer I/Os
New Applications
Smaller Chips
Less pin counts
Less expensive packages
Lower power consumption
Simpler package
Less Heat
Cheaper packages
Simpler system level designs
Smaller Size
Less area
Scalable
Lower cost
Future Proof
Simpler Signaling schemes
Easier circuit design
Simpler board/package designs
Faster cycle time
Lower cost system design
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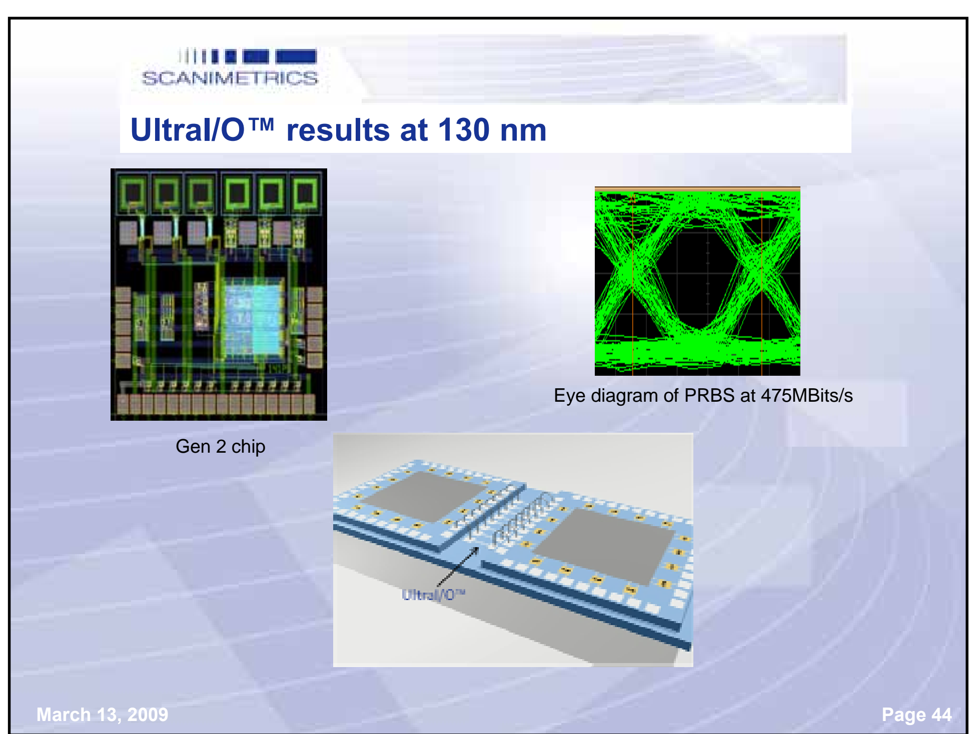
SCANIMETRICS
UltraI/O™ results at 130 nm
Gen 2 chip
Eye diagram of PRBS at 475MBits/s
UltraI/O™
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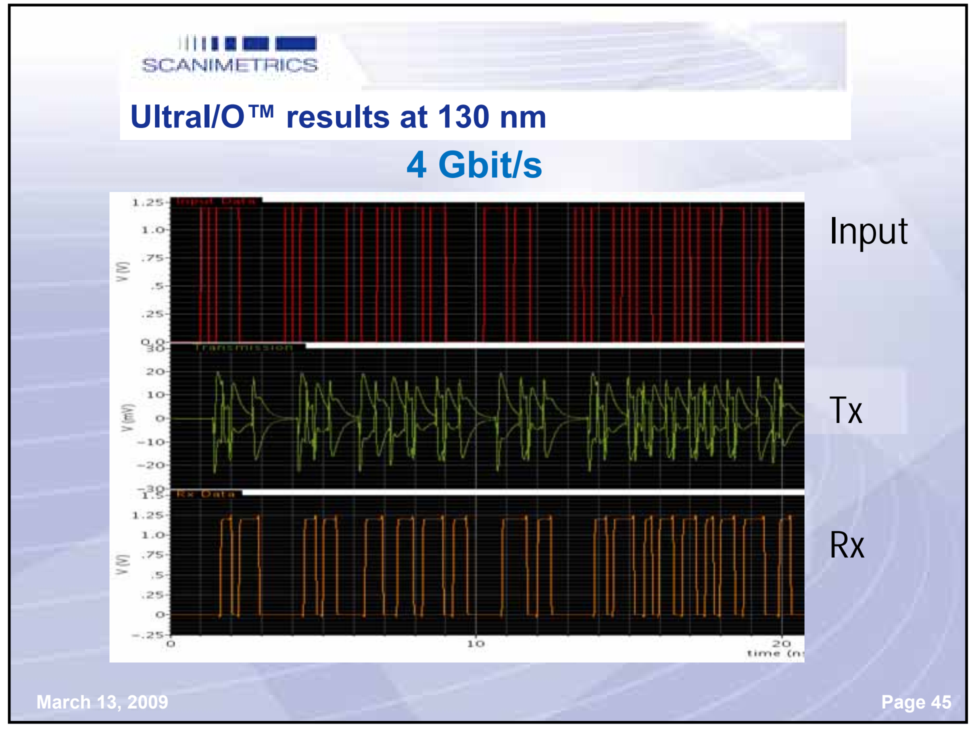
SCANIMETRICS
UltraI/O™ results at 130 nm
4 Gbit/s
Input
Tx
Rx
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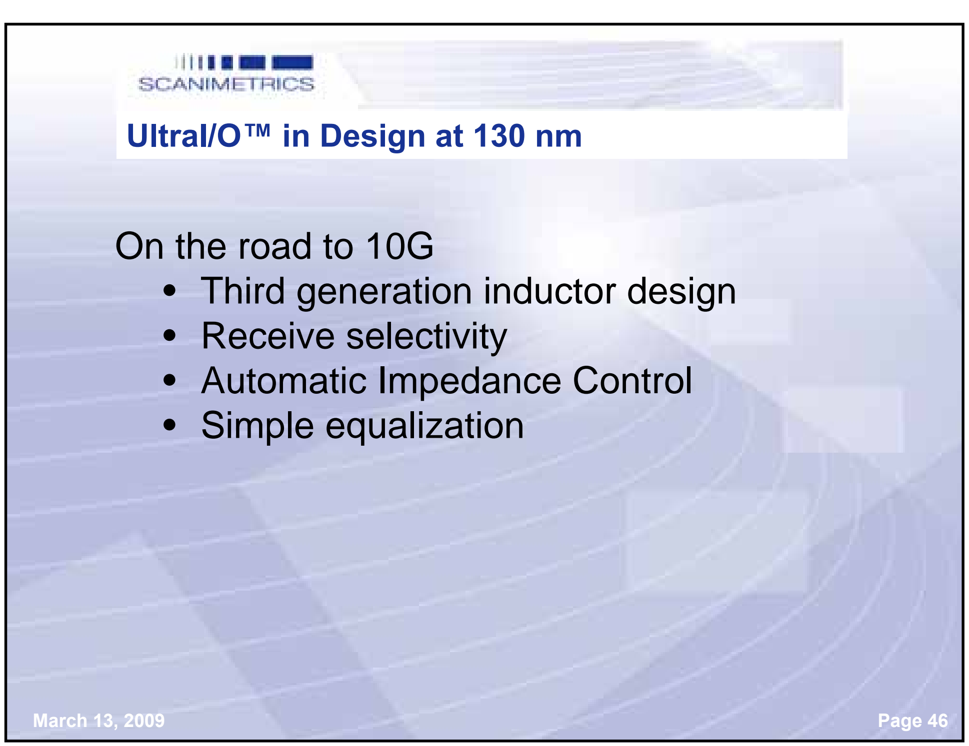
SCANIMETRICS
UltraI/O™ in Design at 130 nm
On the road to 10G
• Third generation inductor design
• Receive selectivity
• Automatic Impedance Control
• Simple equalization
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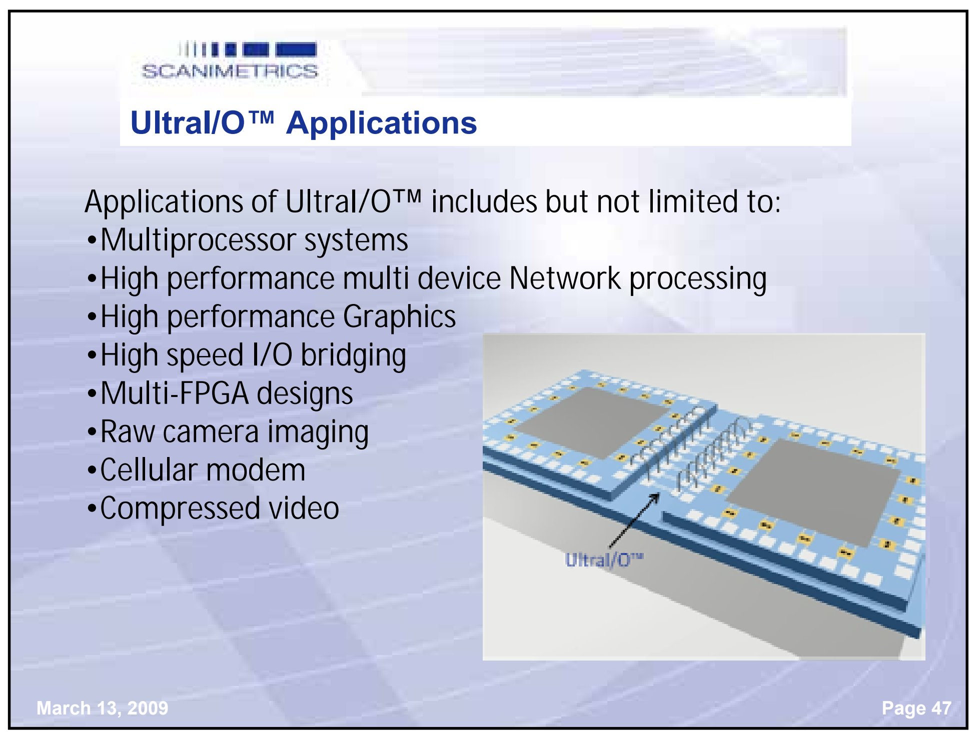
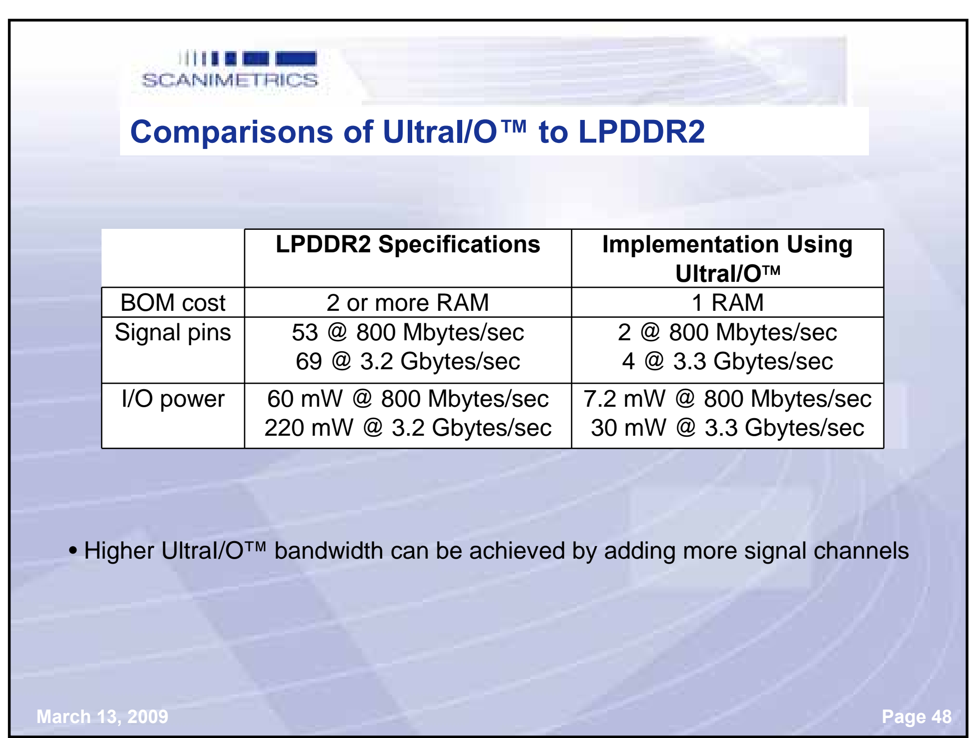
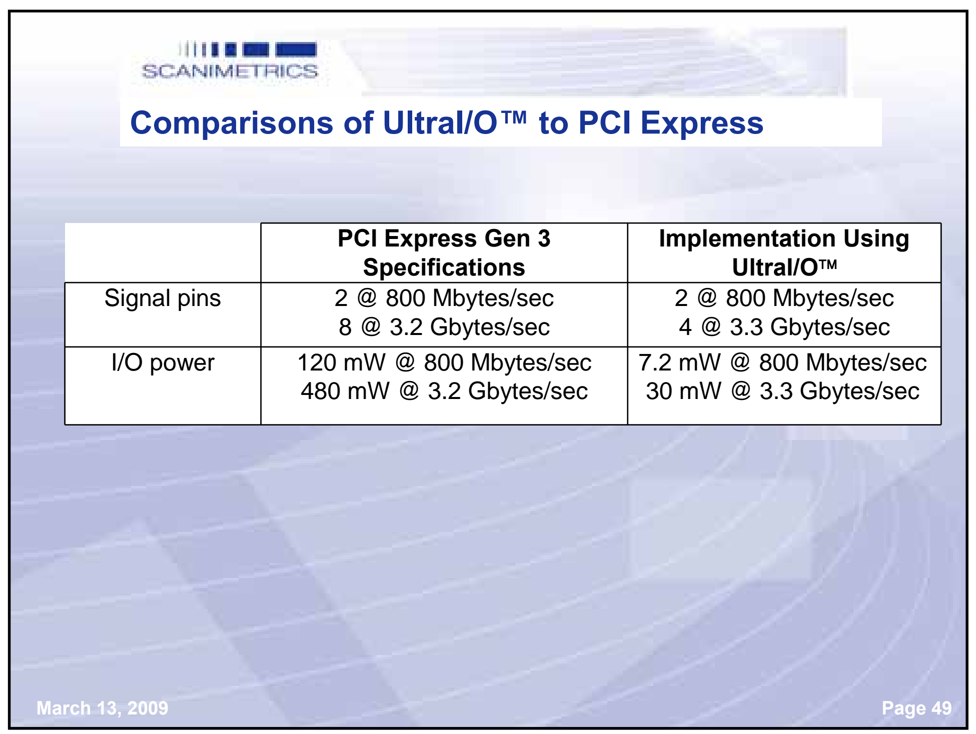




	LPDDR2 Specifications	Implementation Using UltraI/O™
BOM cost	2 or more RAM	1 RAM
Signal pins	53 @ 800 Mbytes/sec 69 @ 3.2 Gbytes/sec	2 @ 800 Mbytes/sec 4 @ 3.3 Gbytes/sec
I/O power	60 mW @ 800 Mbytes/sec 220 mW @ 3.2 Gbytes/sec	7.2 mW @ 800 Mbytes/sec 30 mW @ 3.3 Gbytes/sec


SCANIMETRICS
Comparisons of UltraI/O™ to PCI Express
	PCI Express Gen 3 Specifications	Implementation Using UltraI/O™
Signal pins	2 @ 800 Mbytes/sec 8 @ 3.2 Gbytes/sec	2 @ 800 Mbytes/sec 4 @ 3.3 Gbytes/sec
I/O power	120 mW @ 800 Mbytes/sec 480 mW @ 3.2 Gbytes/sec	7.2 mW @ 800 Mbytes/sec 30 mW @ 3.3 Gbytes/sec
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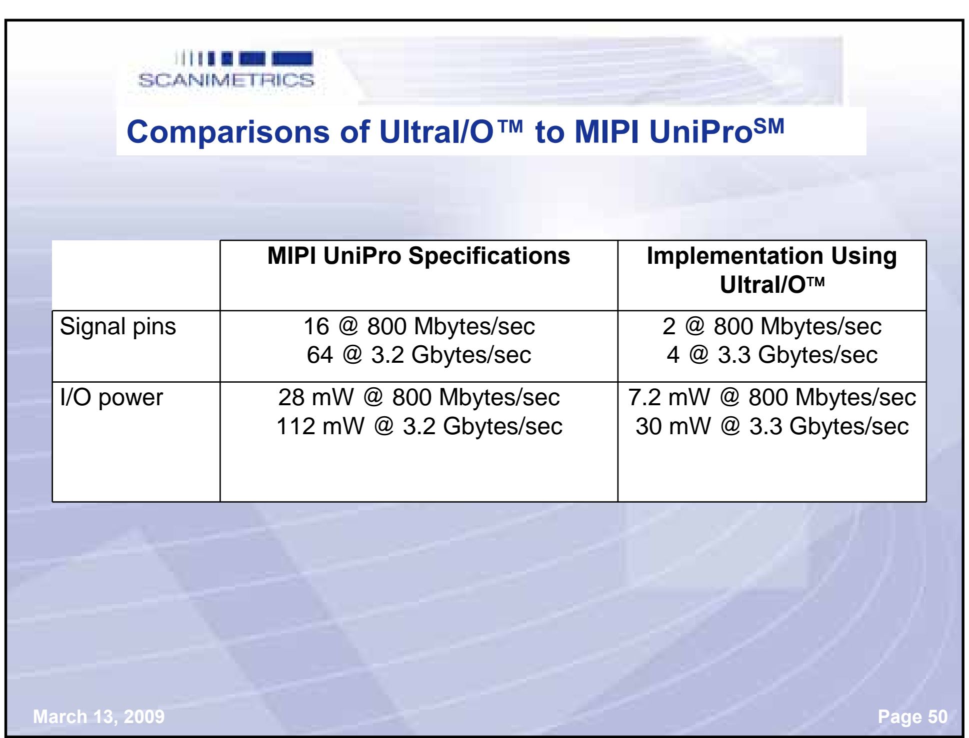
SCANIMETRICS
Comparisons of UltraI/O™ to MIPI UniPro℠
	MIPI UniPro Specifications	Implementation Using UltraI/O™
Signal pins	16 @ 800 Mbytes/sec 64 @ 3.2 Gbytes/sec	2 @ 800 Mbytes/sec 4 @ 3.3 Gbytes/sec
I/O power	28 mW @ 800 Mbytes/sec 112 mW @ 3.2 Gbytes/sec	7.2 mW @ 800 Mbytes/sec 30 mW @ 3.3 Gbytes/sec
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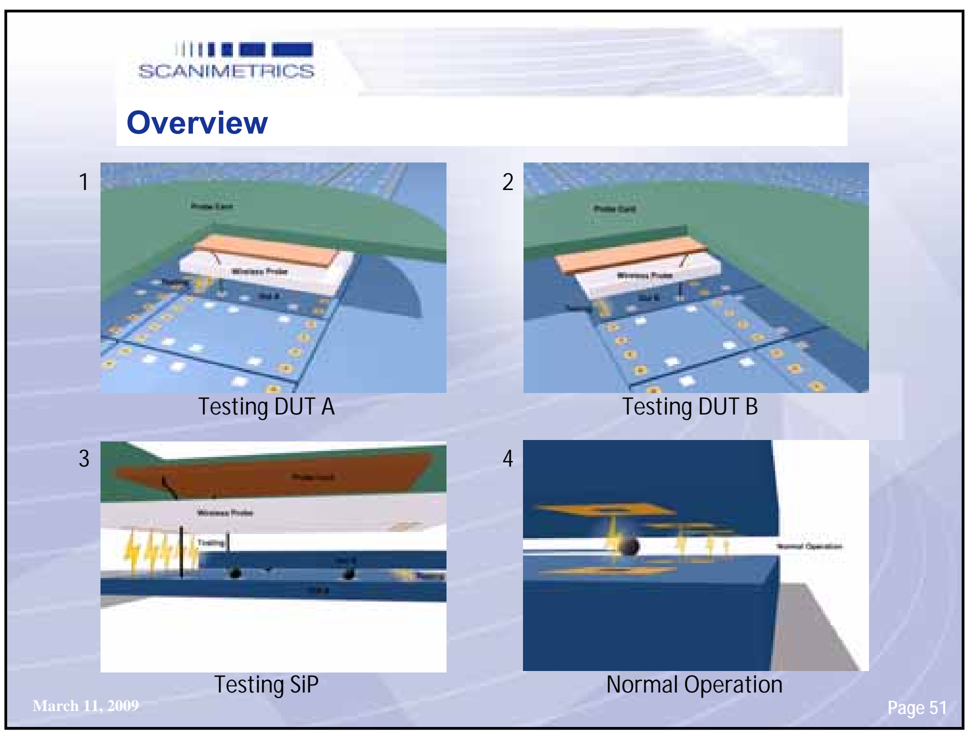

SCANIMETRICS

UltraI/O™ Summary

- Current memory interface technology cannot meet growing demand of mobile handheld industry and other markets such as portable media player and digital cameras
- UltraI/O™ offers faster, lower power and smaller area solutions than other approaches such as capacitive and inductive interconnects
- UltraI/O™ has superior performance than current interface standards (LPDDR2, PCI Express, MIPI Unipro℠)
- UltraI/O™ is an excellent candidate for the next chip-to-chip and memory interface standards

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SCANIMETRICS
UltraI/O™ - Summary
"The growing number of full-featured, media-rich mobile applications is creating an increased demand for more memory.
Serial Port Memory Technology will be the right solution to support the requirements for low pin count, low power and high bandwidth that will be required for these new applications."
JB Kim, senior vice president of technical marketing, Hynix, member of SPMT group
UltraI/O™ fills this technology gap.
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