Through Silicon Vias (TSV): Design and Reliability

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May, 2009

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- Introduction to TSV foundry
- TSV design issues
- TSV foundry and customers
- TSV foundry product lines
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Introduction to ALLVIA, Inc.

- ALLVIA provides Thru-Silicon Via Foundry Services for the semiconductor, RF and MEMS industries
- ALLVIA offers:
  - TSV prototyping and volume production
  - 3D integrated products
- ALLVIA was formed in 2004 to address prototyping and volume production

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Steps for FlipChip commercialization

Wait 30-40 years till performance demand strikes

- Performance - prototyping facilities
- Reliability - qualification data
- Manufacturability – high or low volume data
- Cost – high volume
- Supply Chain – the total investment

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Steps for TSVs commercialization

In 2000, there was not enough interest

In 2008, not enough data to design products

- Performance - issues with prototyping facilities
- Reliability - issues with qualification data
- Manufacturability – issues with high or low volume data
- Cost – issues with cost models (5um vs 200um)
- Supply Chain – issues with new steps and technologies

ALLVIA addressing all these issues since 2004

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How ALLVIA works with Customers

Product customers

ALLVIA designs and manufactures TSVs

Foundries
IC, MEMS, Internal

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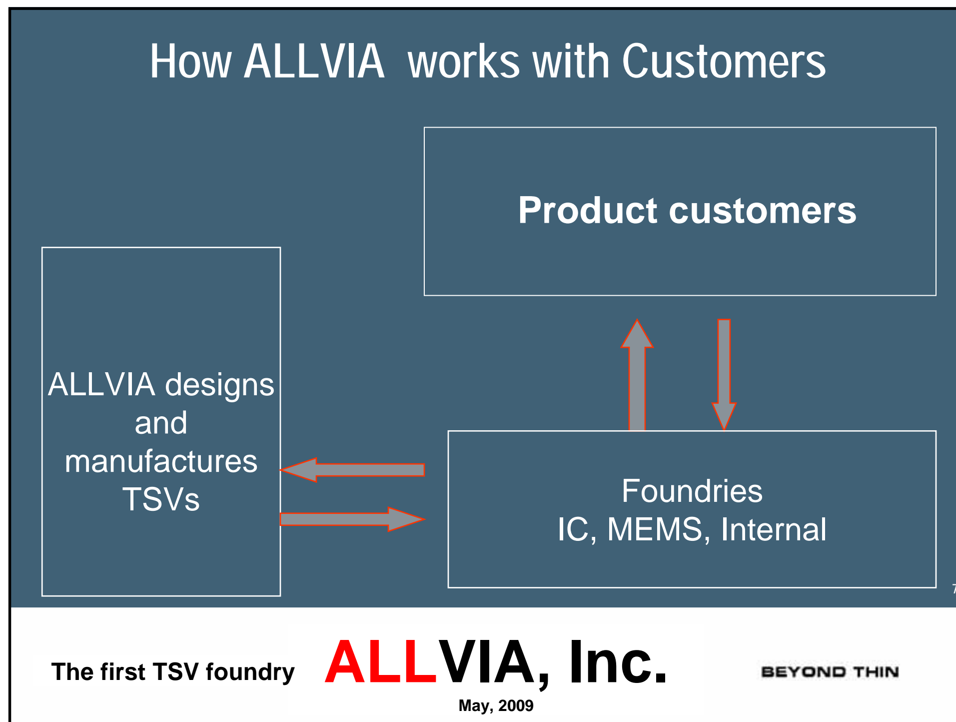
How ALLVIA works with Customers
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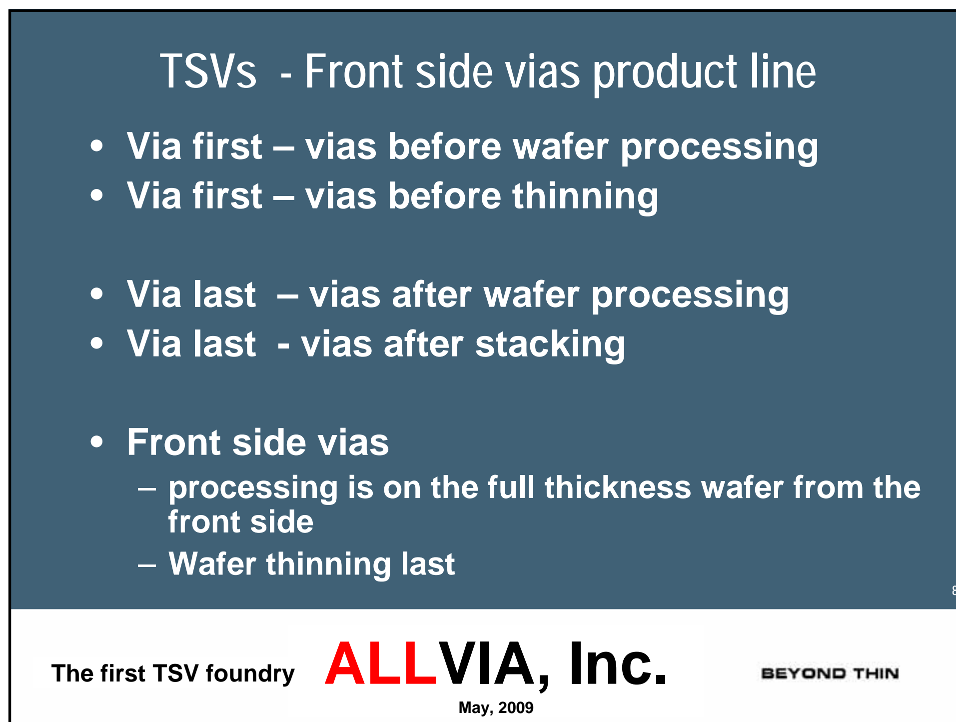
TSVs - Front side vias product line
• Via first – vias before wafer processing
• Via first – vias before thinning
• Via last – vias after wafer processing
• Via last - vias after stacking
• Front side vias
– processing is on the full thickness wafer from the front side
– Wafer thinning last
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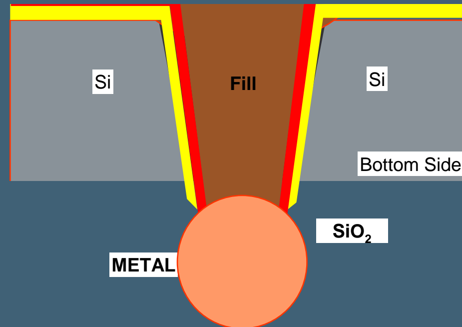
Thru-Silicon blind front side vias

Up to 5: 1 ratio via Top to Bottom Interconnects

1. Form holes, usually in bond pad area
2. Oxidize hole (CVD)
3. Metalize hole
4. Plate hole, usually Cu
5. CMP front side
6. ADP etch backside to expose via
7. Solder transfer



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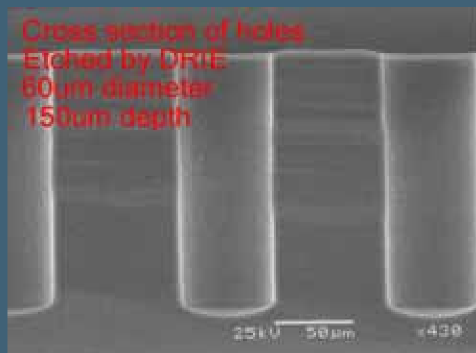
Deep Etching Via, Oxidation, (150um, 60um)



Characterized:

Thickness of oxide layer

Thickness of barrier layer

Thickness of seed layer

Failure mode:
Oxide cracks
De-lamination
Copper diffusion

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Copper via filling (200um, 60um)

Characterized:

Amount copper
On
The front side

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Front side Chemical Mechanical Polishing

Characterized:

CMP dishing

Voids

Ex. Via first

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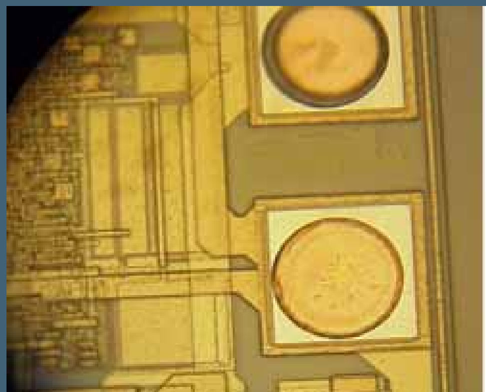
Front side IC device with the vias after CMP



Characterized:

Copper Via interface with

Al pads

Ex. Via last or Via first

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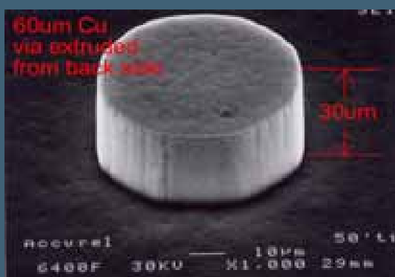
Grind & ADP opening (150um, 60um, 30um)



Backside picture

Etch removes silicon but not metal

Characterized:

Height of copper post

And oxide layer

No via voids

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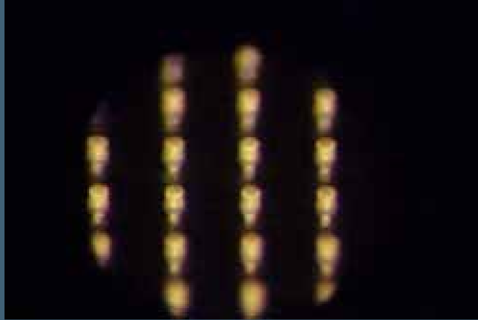
Cu post on the back side (300um, 60um, 50um)



Characterized:

Copper post uniformity

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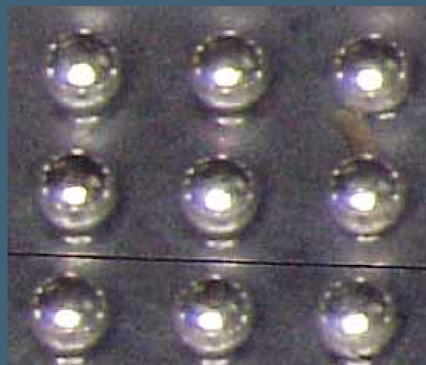
Copper post soldering (200, 60, 90, 120)



Characterized:

Size of solder balls

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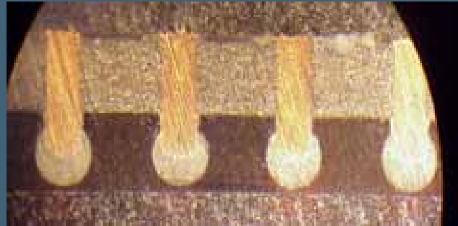
Copper post soldering (300, 60, 80, 100)



Characterized:

Solder adhesion to copper posts

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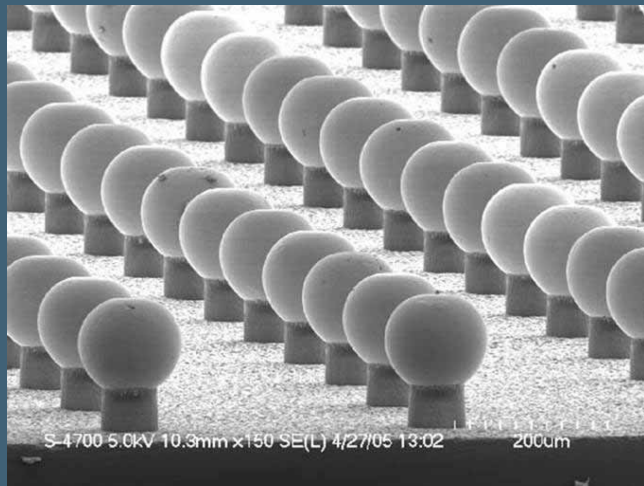
Copper post soldering (200, 60, 90, 100)



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TSV - Back side vias product line

- **Via last – vias build after wafer processing**
- **Via processing is on the thin wafer**
- **Wafer thinning first**
- **Might require temporary bonding/debonding**

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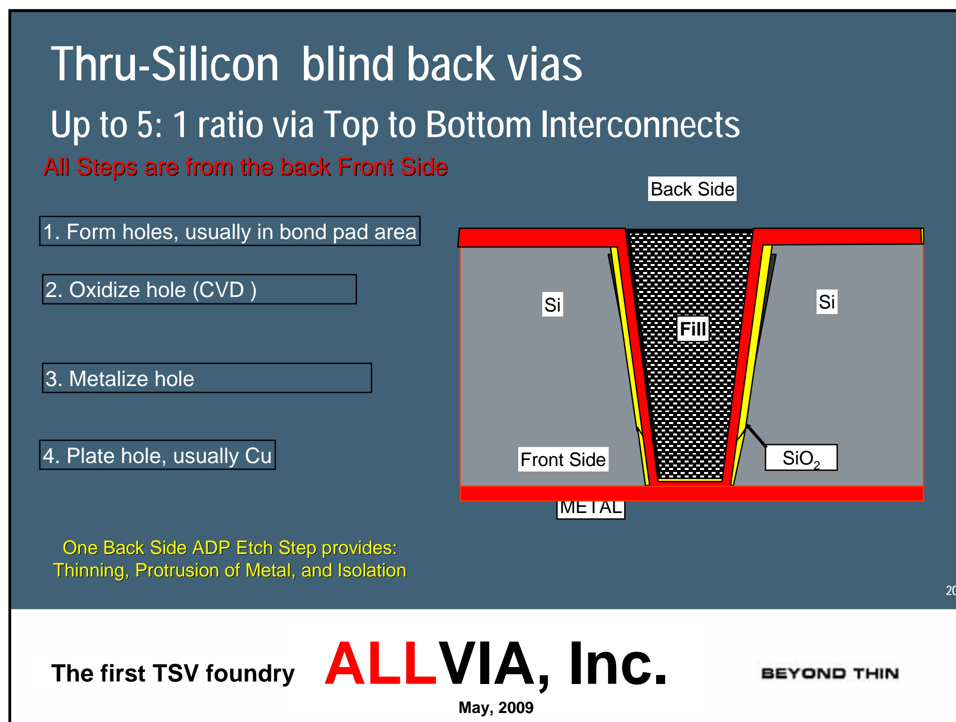
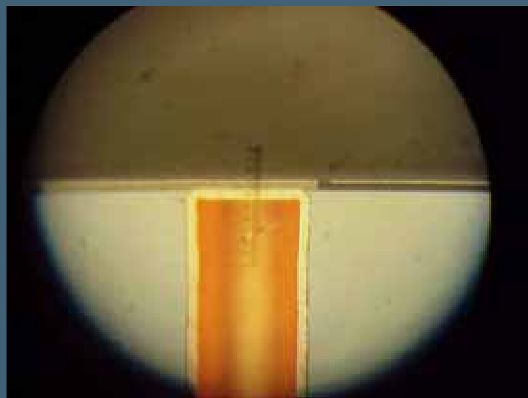


Backside Silicon etch, oxide, seed



Characterized:

Thickness of oxide layer

Thickness of barrier layer

Thickness of seed layer

Failure Mode:
Oxide cracks
De-lamination
Copper diffusion

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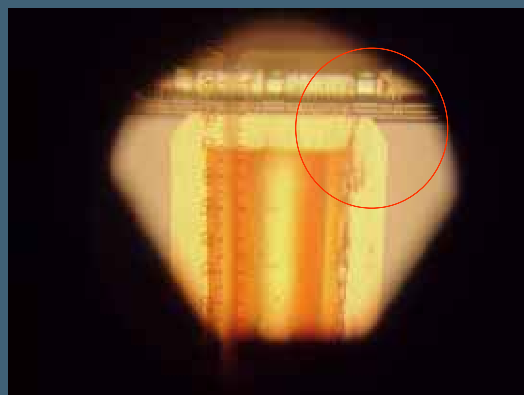
Copper interconnection to IC



Characterized:

Oxide opening

Copper adhesion to other materials

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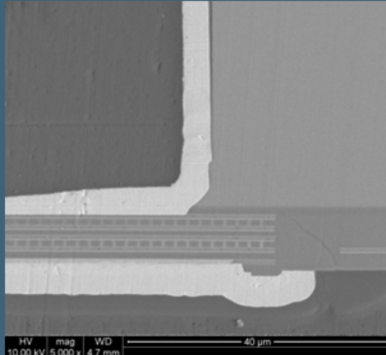
Copper interconnection to IC



Characterized:

Resistance properties between Front side and Back side

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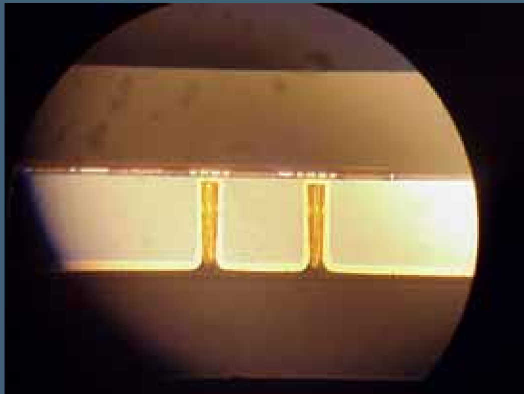
Complete 3D interconnect



Characterized:

Thickness of copper inside and outside vias

Conformal plating

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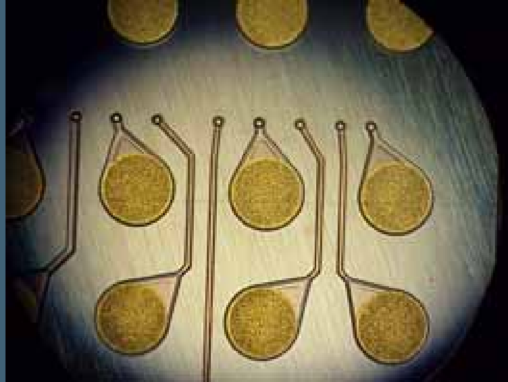
Back side via rerouting



Characterized:

Thickness of copper lines
And spaces and
their electrical properties

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Products with TSVs

Semiconductors

- 3D stacked Integrated Circuits
- Thru-Silicon CSP ICs processed in wafer form

Passive Interposers and System In a Package

Sensors and Opto-electronic devices

MEMS hermetic and non-hermetic applications

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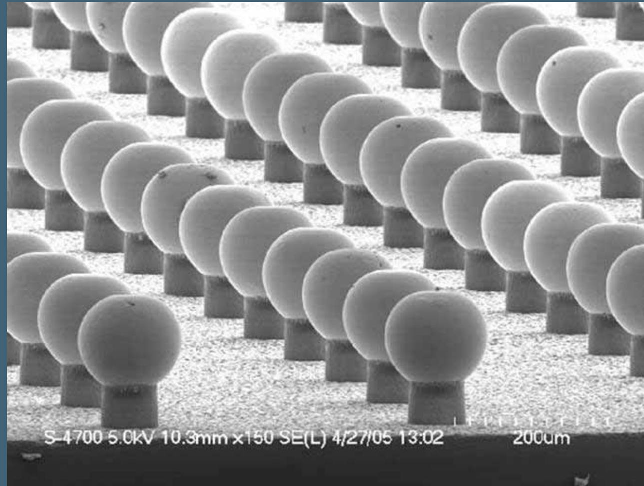
Copper post soldering (200, 60, 90, 100)



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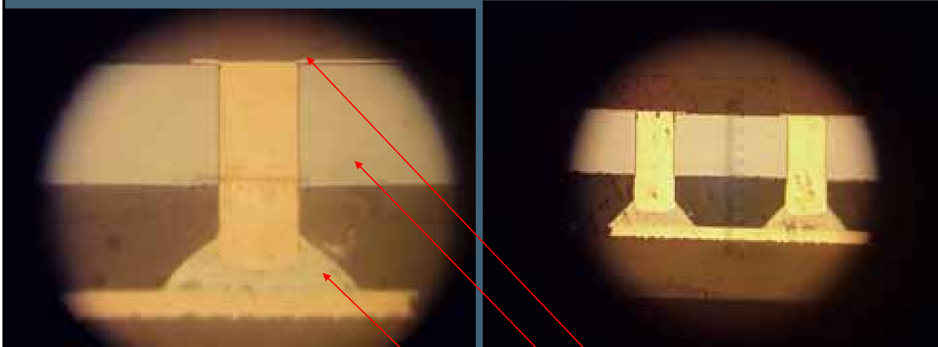
Si-on-BT stacking with under-fill



Front side metal
Silicon
Solder

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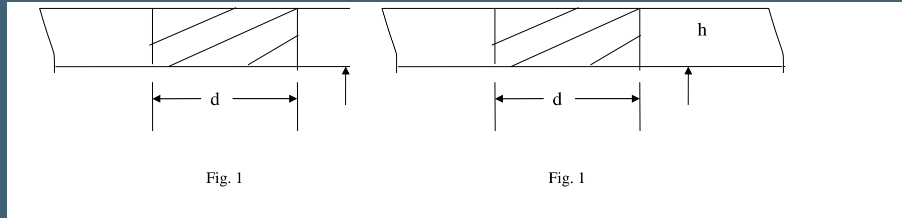
TSV Pitch Design for Reliability



Based on the case studies and Mathematical models
TSV pitch should be

greater than 2.5 diameters

Failure mode Silicon cracks with Temp cycling

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Conclusion

ALLVIA offers:

– Deep Silicon and Oxide Etching Cu filling
– Cu CMP Cu/Pi rerouting
– Soldering Wafer Thinning
– 3D Applications 3D Stacking

- ALLVIA early design involvement is required for successful design of TSVs
- ALLVIA considers TSV pitch greater than 2.5 diameters reliable

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