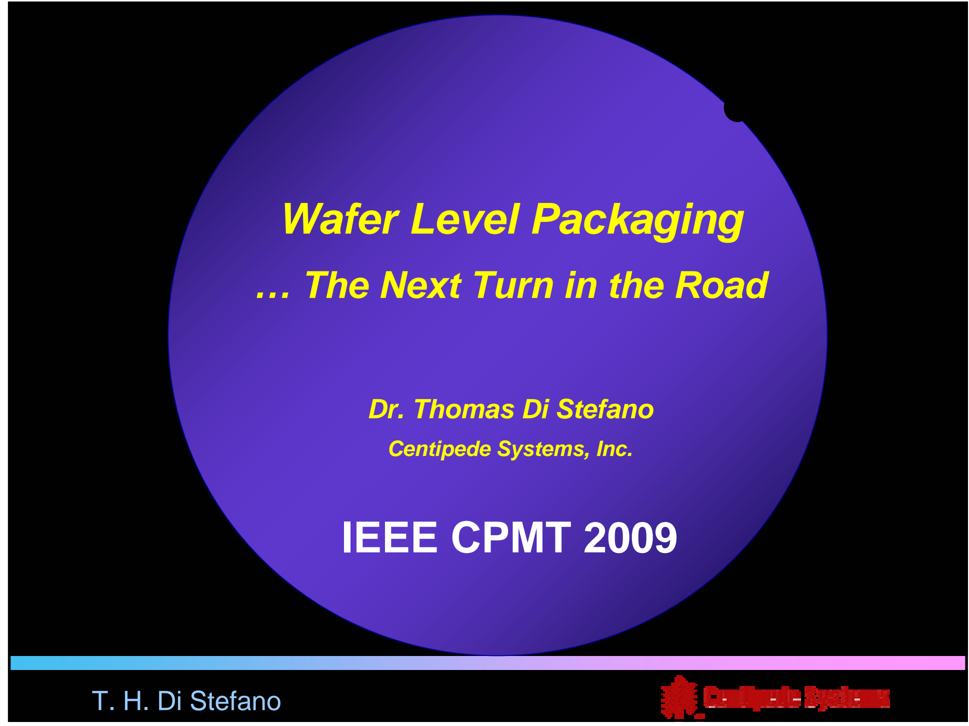

Could back end packaging and test provide productivity improvements like the Moore's Law gains enjoyed by Semiconductor FABs?

- Wafer Level Processing
- Lights Out Automation
- Standard Handling Protocols
- Intelligent Burn-in and Test

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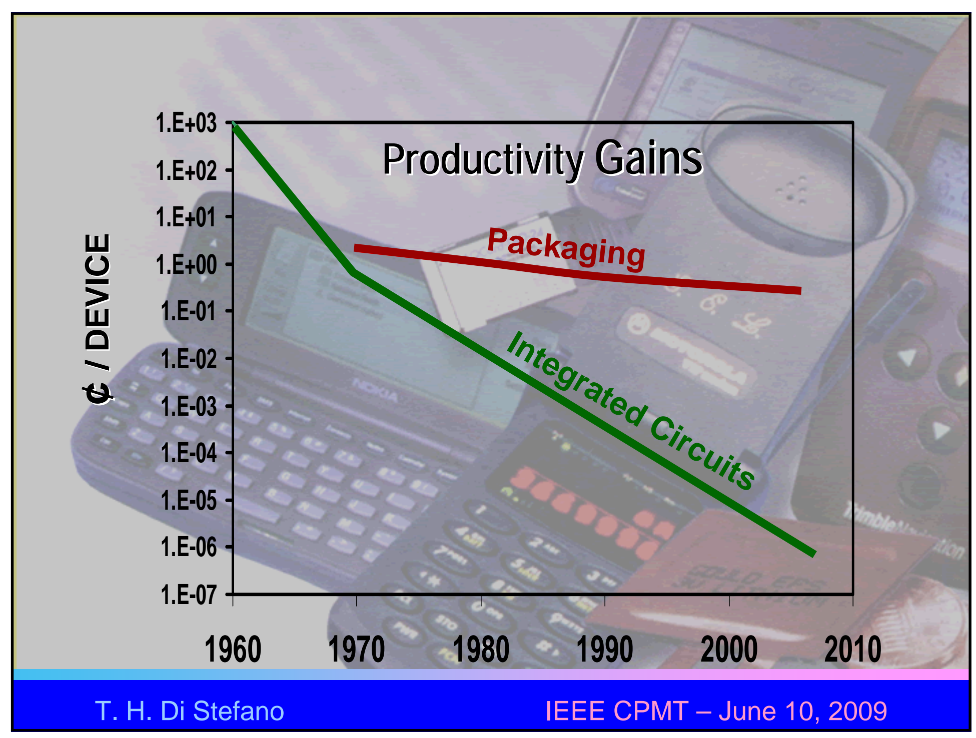

Semiconductor Productivity Gains

Parallel Processing – More Devices per Wafer
- Increasing level of integration
- Shrinking device dimensions

Device Improvements
- Increases in Clock speed
- Fewer devices per Cell

Automation
- Lights out FAB
- Focus on process/tool improvement

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Single Wafer FOUP *

- Standard Interface for Full Automation of FAB Front End
- Enables Lights-Out Semiconductor Automation+

* **Front Opening Unified Pod**
+ **Allen Ibara, CEO PhiAm**

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Lights Out Automation *

Cycle Time
- 50% improvement in two years

Tool Utilization
- 10-30% improvement in two years
- Re-use of (standard) tools is essential

Process Learning
- Focus on tool and process instead of moving WIP
- WIP is moved automatically

* **From Tom Franz, VP and GM FAB/Sort Manufacturing, Intel Corp. VLSI Research July 25, 2007**

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Packaging/Test Productivity

Relatively Static Cost Structure

- Packaging cost per chip slowly decreasing
- Test costs increase with complexity
- Test and burn-in fixtures
- Lack of standardization
- Mixture of handling and logistics protocols

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Lights Out Automation

Key Enabling Factors for the Back End

- Wafer Level Packaging Facilitates Automation (FOUP)
- Standard Chip Transport (Tray)
- Test in Tray (TNT)
- Intelligent Burn in (TDBI)

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Tessera WAVE
IEEE CMPT 1999
WLP 1999
• Driven by Size/Performance
• Solder Attach to PCB
• Single Chip Applications
• Cost Parity
WLP 2009
• Driven by Cost
• Through Silicon Via Option
• SiP and Stacking Applications
• Integrated Processing
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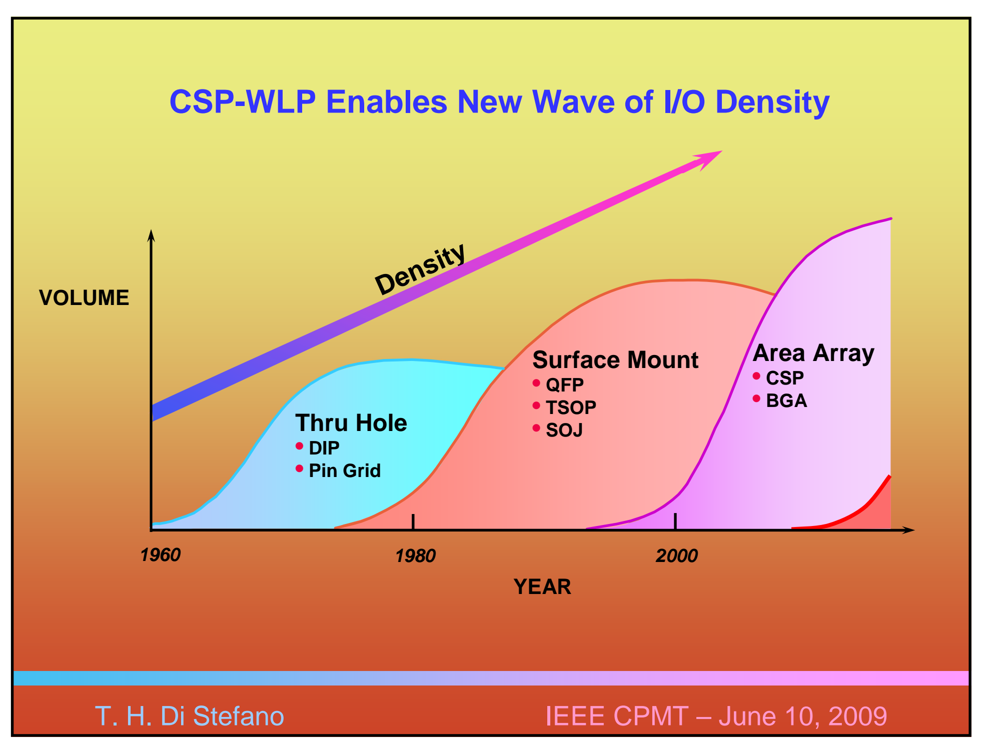
CSP-WLP Enables New Wave of I/O Density
Density
VOLUME
Thru Hole
• DIP
• Pin Grid
Surface Mount
• QFP
• TSOP
• SOJ
Area Array
• CSP
• BGA
1960
1980
2000
YEAR
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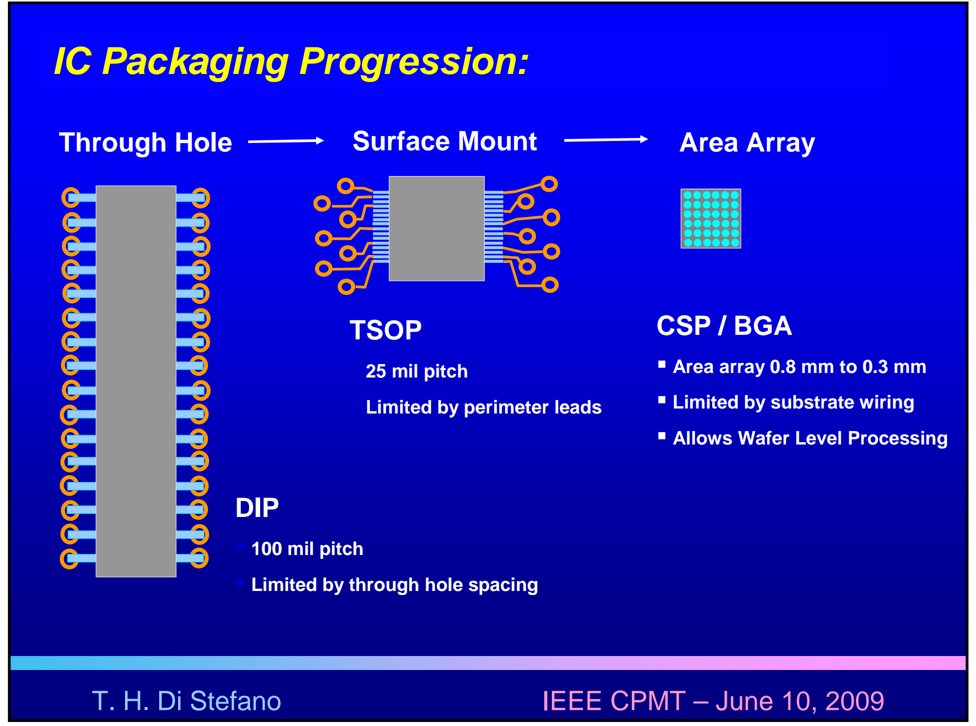

WLP Enjoys Exceptional Growth

TechSearch Projects 14% Growth (CAGR) for 2007 - 2014

- Diverse set of applications & technologies
- Growth concentrated in packages < 50 pins
- Driven by performance, form-factor (…AND COST!)

Growth in Wafer Level Packaging of MEMS Devices

- Camera chips
- Pressure sensors
- Crystal Oscillators, …

Emerging Applications in Through Silicon Via (TSV)

- Stacked memory

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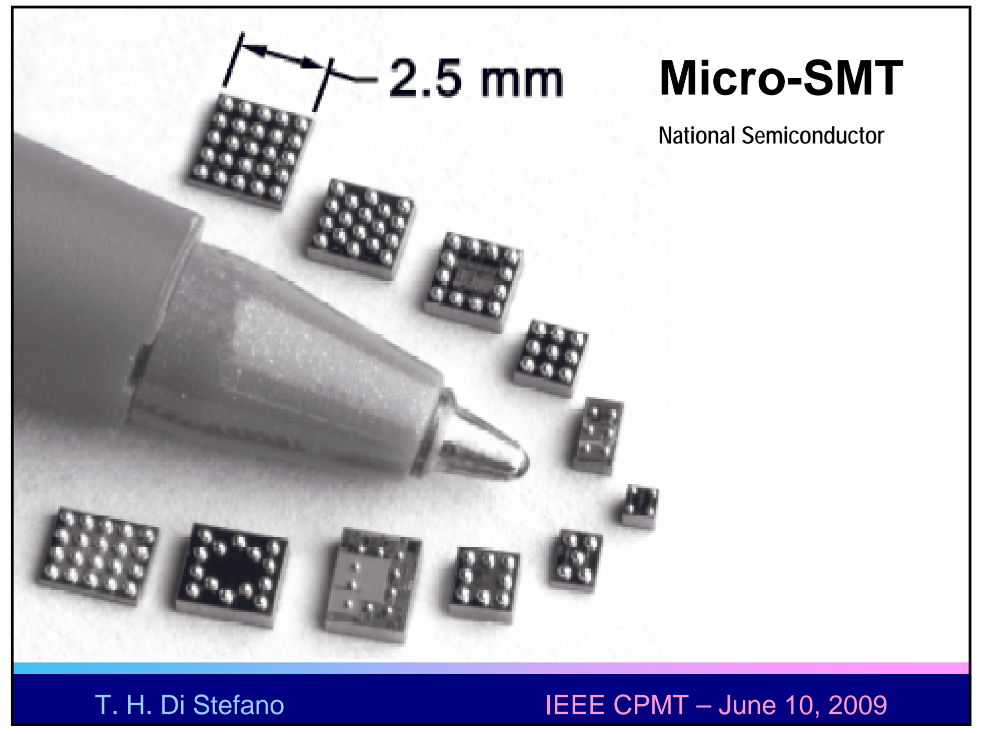

WLCSP Market*

- Strategic and rapidly growing WLCSP business
- > 1. 3 Billion WLCSP's shipped since 2005
- >95% of WLCSP's shipped include RDL and lead free solder bumps
- Multiple customers in production, wide range of new designs in qualification
  - 0.5mm pitch dominant
  - 0.4mm pitch emerging
  - 0.3mm pitch in development
- First 300mm WLCSP qual achieved in T5 as of October 1, 2006
- Global wafer level process manufacturing footprint
  - 7 countries and 15 sites

* From Lee Smith, Amkor

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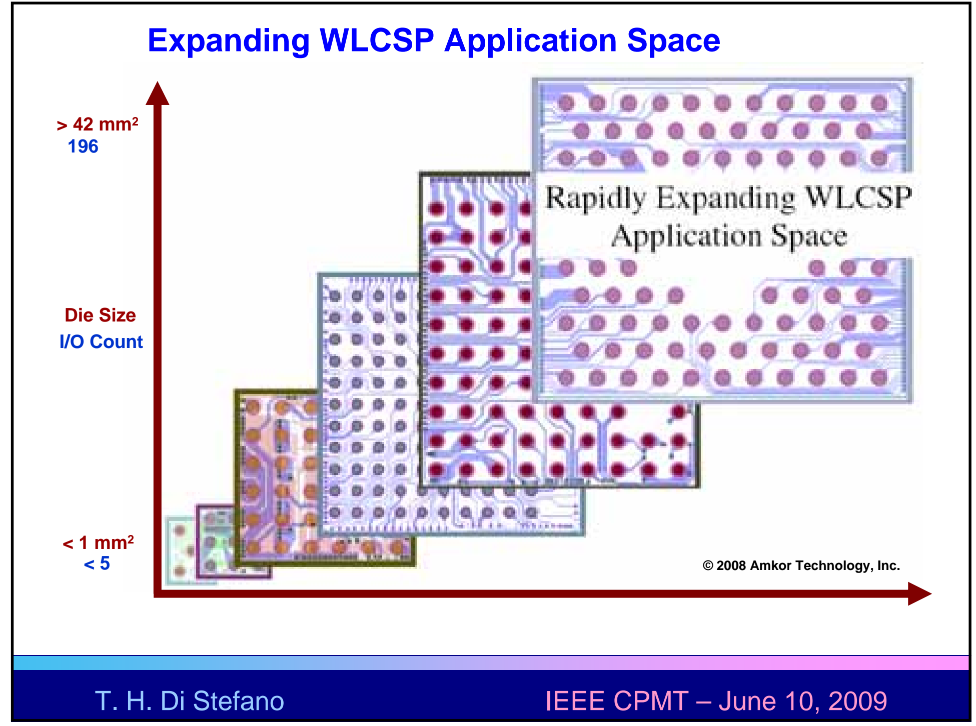
Expanding WLCSP Application Space
> 42 mm²
196
Die Size
I/O Count
< 1 mm²
< 5
Rapidly Expanding WLCSP
Application Space
© 2008 Amkor Technology, Inc.
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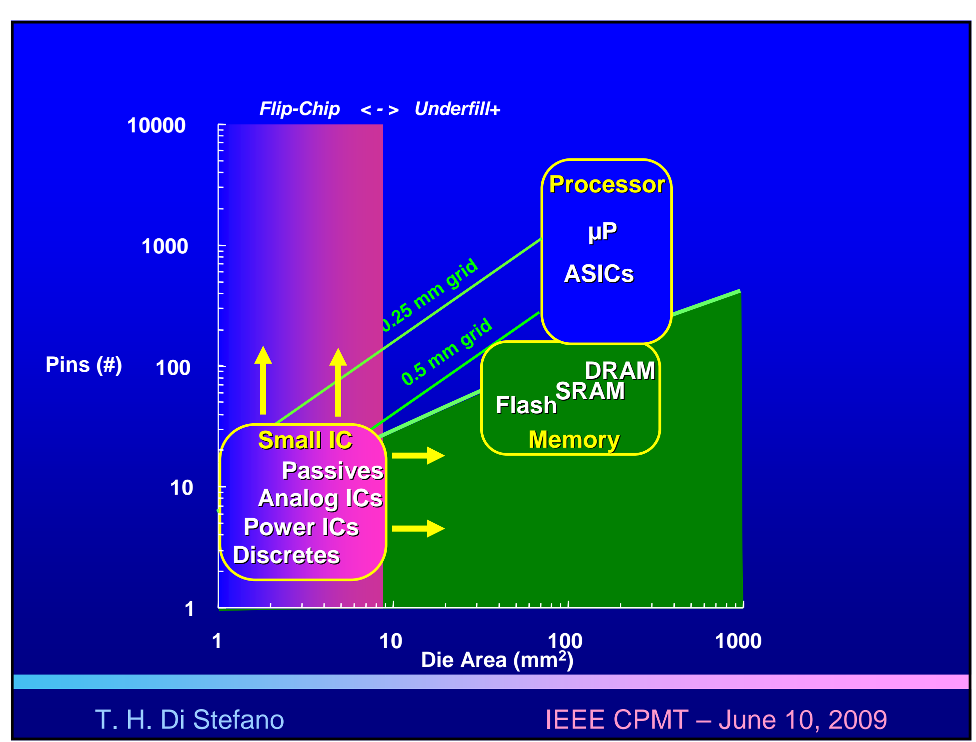
Flip-Chip < - > Underfill+
10000
1000
100
10
1
Pins (#)
Processor
µP
ASICs
0.25 mm grid
0.5 mm grid
DRAM
SRAM
Flash
Memory
Small IC
Passives
Analog ICs
Power ICs
Discretes
1
10
100
1000
Die Area (mm²)
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Wafer Level Packaging

Utilizes Processing to achieve lower costs

- Wafer Processing
- Wafer Handling and Automation
- Industry Standards

WLP is not a specific packaging technology

- Small bumped die
- MEMS
- Through silicon via
- Stacked Chips
- …

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WLP has not gone Mainstream (i.e. DRAM)

- Reliable Solder Attach Technology
- Cost Effective Wafer Burn-in and Test
- Cost!

Recent developments could change the game

- SiP relaxes thermal mismatch problem
- TSV allows stacked chips
- Intelligent burn-in and test
- Automation Standards

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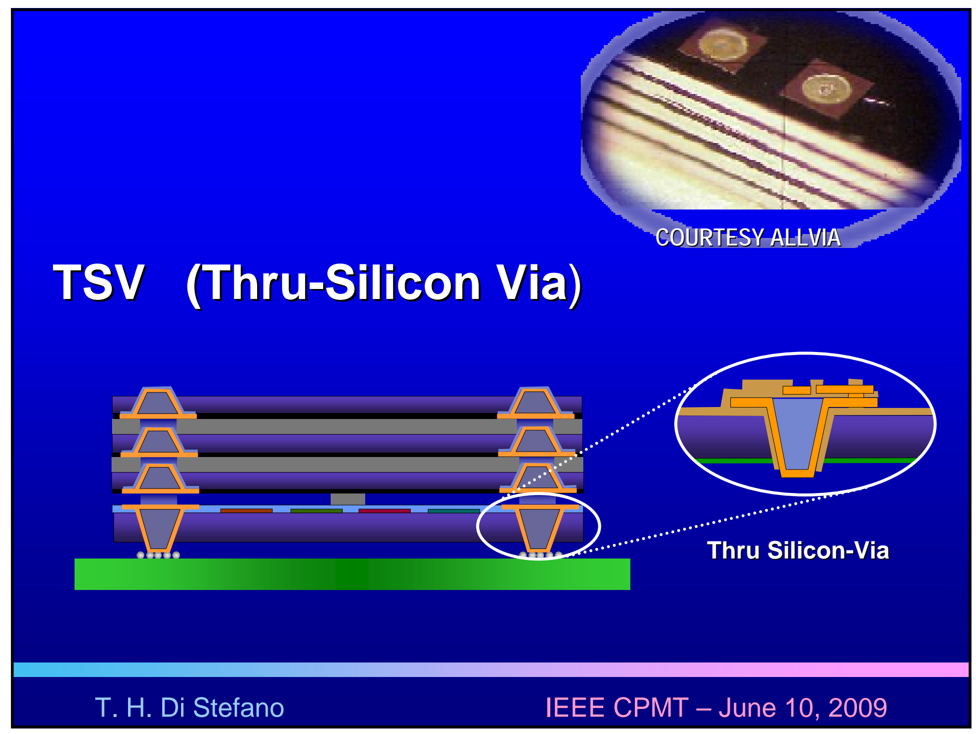

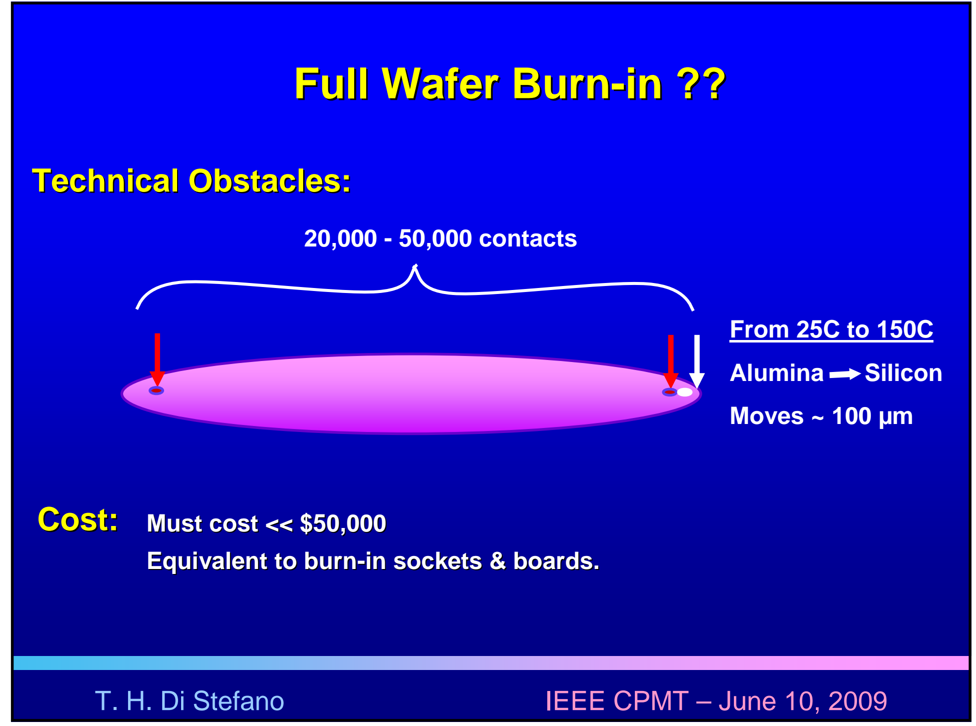
Full Wafer Burn-in ??
Technical Obstacles:
20,000 - 50,000 contacts
From 25C to 150C
Alumina → Silicon
Moves ~ 100 µm
Cost:
Must cost << $50,000
Equivalent to burn-in sockets & boards.
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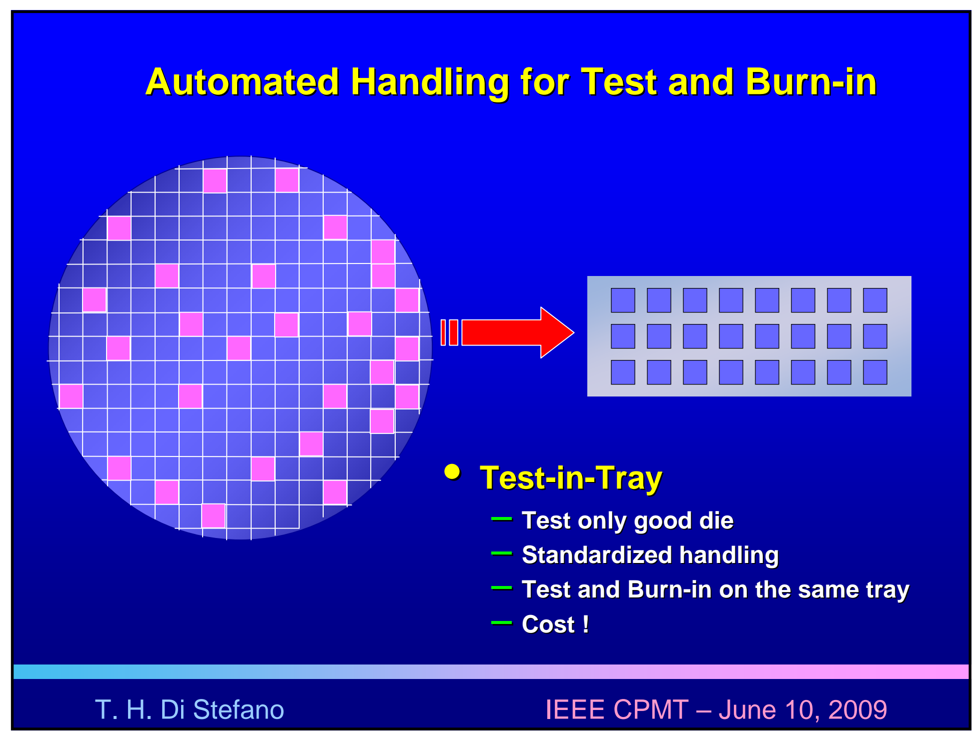
Automated Handling for Test and Burn-in
Test-in-Tray
Test only good die
Standardized handling
Test and Burn-in on the same tray
Cost !
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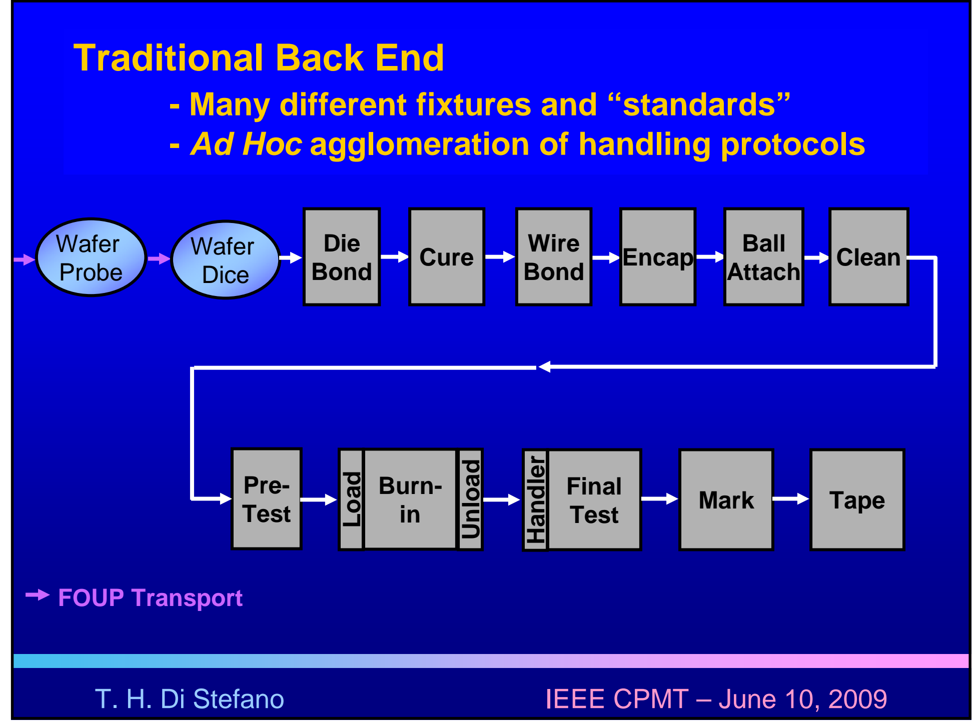
Traditional Back End
- Many different fixtures and "standards"
- Ad Hoc agglomeration of handling protocols
Wafer Probe
Wafer Dice
Die Bond
Cure
Wire Bond
Encap
Ball Attach
Clean
Pre-Test
Load
Burn-in
Unload
Handler
Final Test
Mark
Tape
FOUP Transport
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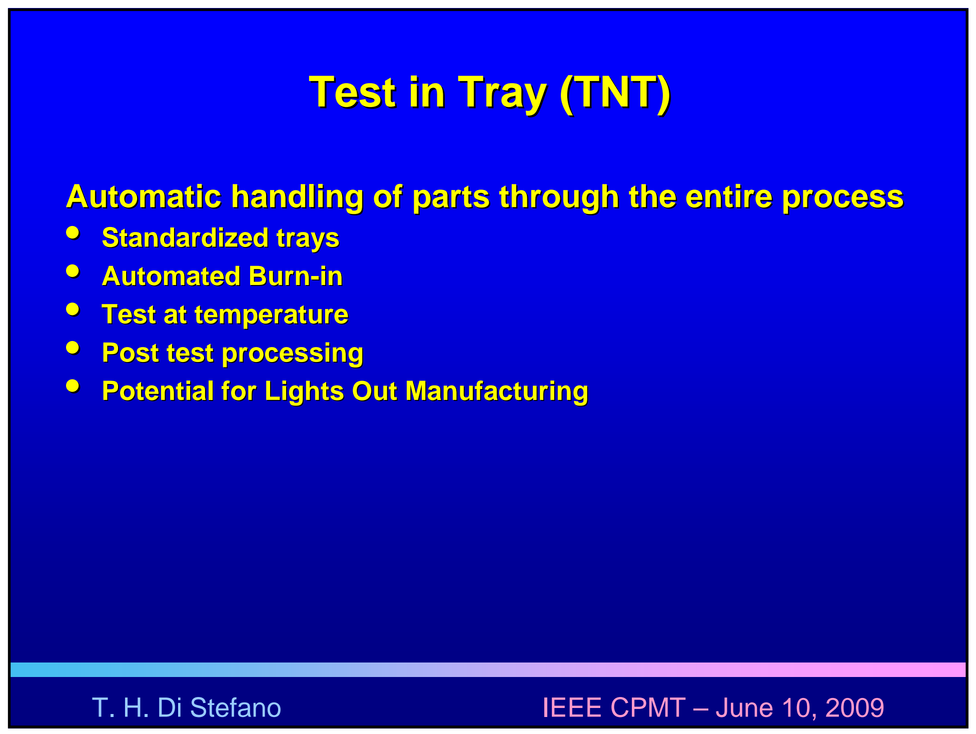
Test in Tray (TNT)
Automatic handling of parts through the entire process
Standardized trays
Automated Burn-in
Test at temperature
Post test processing
Potential for Lights Out Manufacturing
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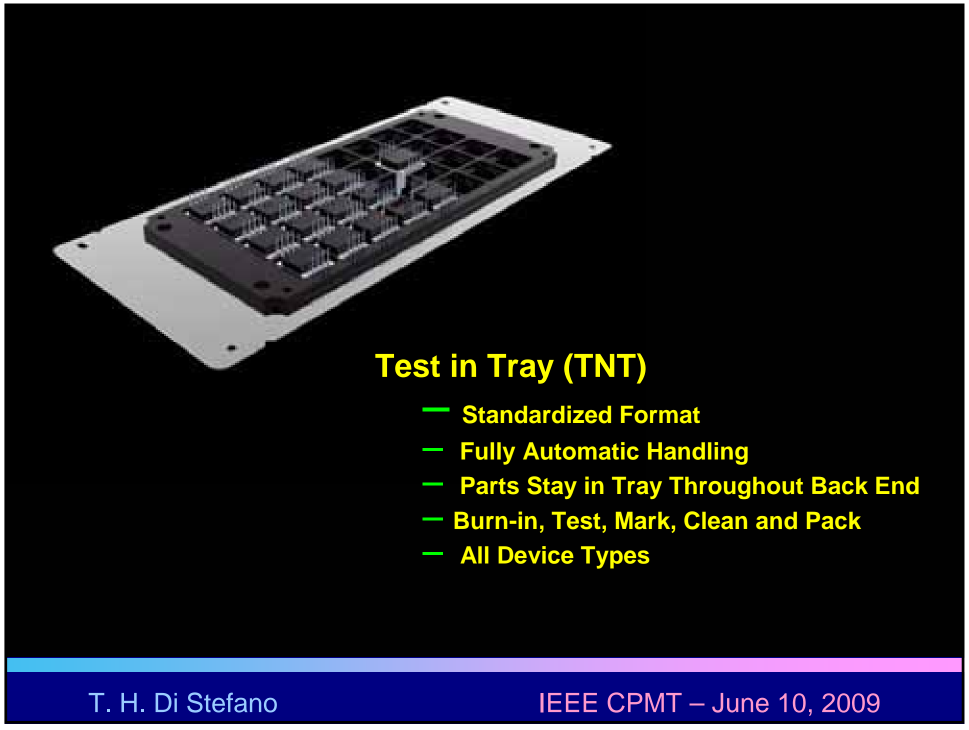
Test in Tray (TNT)
Standardized Format
Fully Automatic Handling
Parts Stay in Tray Throughout Back End
Burn-in, Test, Mark, Clean and Pack
All Device Types
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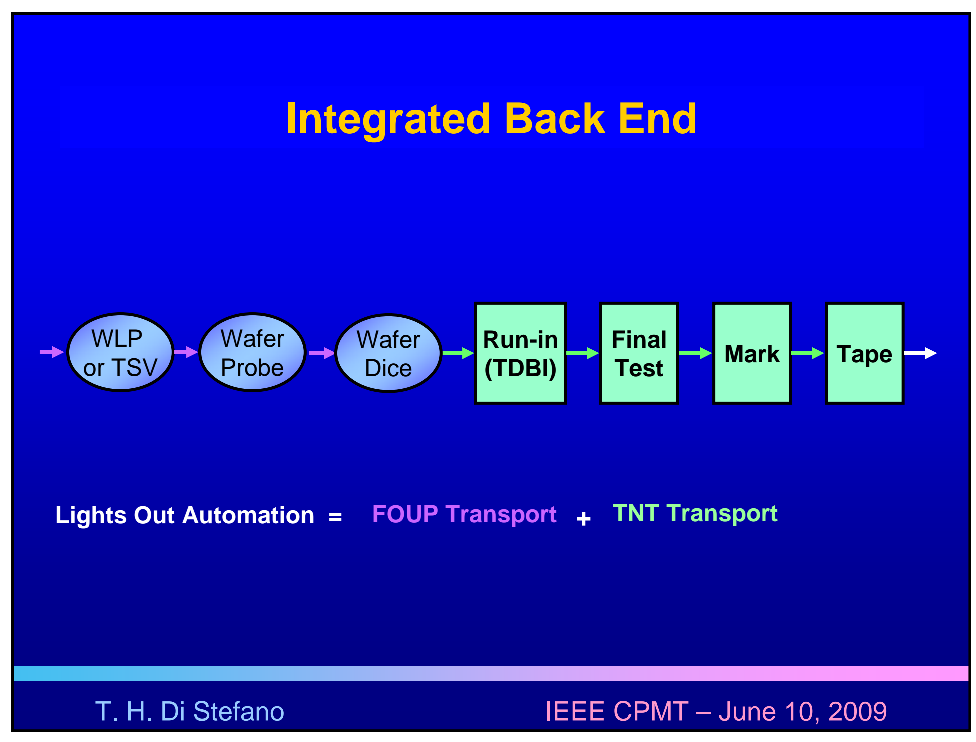
Integrated Back End
WLP or TSV
Wafer Probe
Wafer Dice
Run-in (TDBI)
Final Test
Mark
Tape
Lights Out Automation = FOUP Transport + TNT Transport
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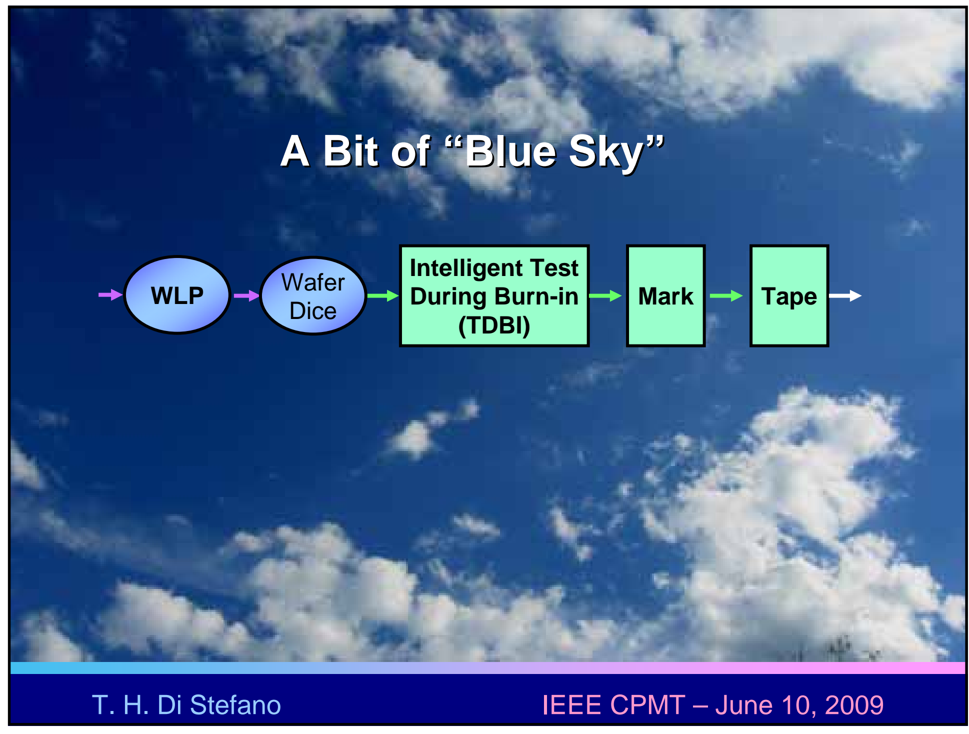
A Bit of "Blue Sky"
WLP
Wafer Dice
Intelligent Test During Burn-in (TDBI)
Mark
Tape
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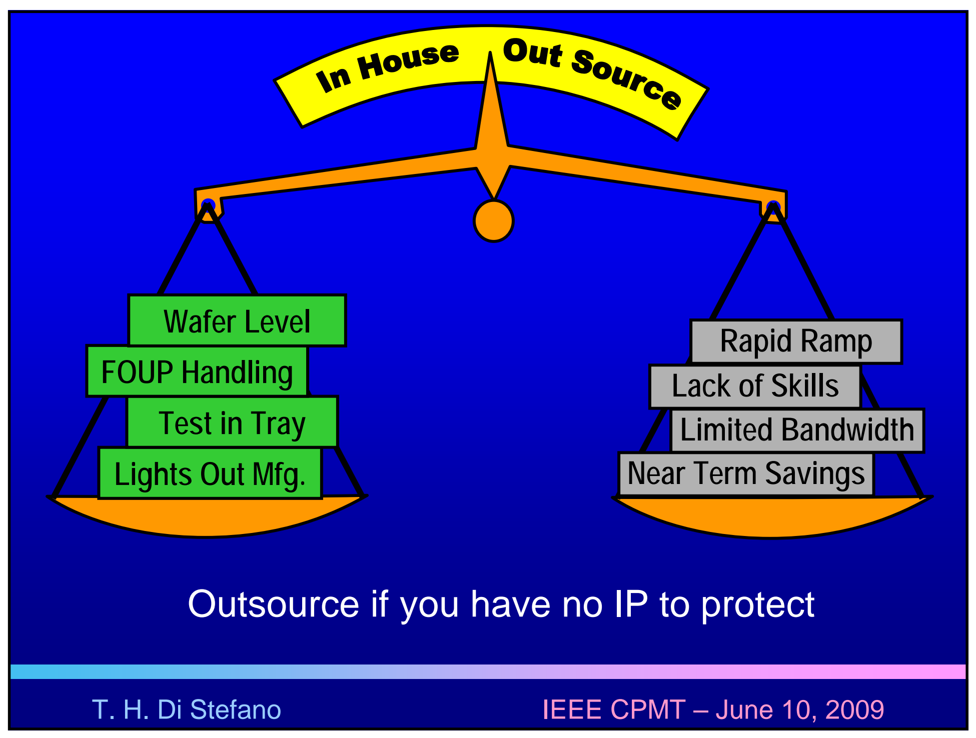
In House
Out Source
Wafer Level
FOUP Handling
Test in Tray
Lights Out Mfg.
Rapid Ramp
Lack of Skills
Limited Bandwidth
Near Term Savings
Outsource if you have no IP to protect
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Wafer Level Packaging

Packaging and Test can Contribute to Productivity

- Wafer Processing of Package Components
- Automation of Wafer Handling (FOUP)
- Test in Tray (TNT)
- Intelligent Burn-in and Test
- Lights out Factory

Future

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