Embedded Passives Methodologies and Opportunities for Implementation

John Savic

Presentation to IEEE
September 24, 2009

"The Bean" in Chicago's Millennium Park
Michigan Ave skyline collapsing into the bean is a good metaphor for the product miniaturization and the driving force for advanced integration technologies

Background Information

- Collaborate with product development teams to enable manufacturing processes for improving the functionality of PWB's and advanced package substrates to meet existing and future product performance requirements.
- Focus on developing and utilizing new Embedded Passives (EP) technologies has been a consequence of pursuing the best possible solution.
- Picking a title…7 choices
  - Get the Pb out - with EP!
  - Enabling Functionality: The Who What and How of EP
  - Embedded Passives - I Don't Get It!
  - Embedded Passives - The (For)Ever-Emerging Technology
  - Embedded Passives Methodologies and Opportunities for Implementation
- Learn from what has been done and evolve

2

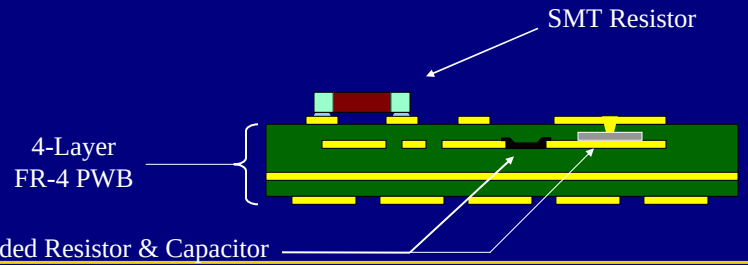
Outline

- Introduction
- Overview of EP technology
- EP in RF applications: Case Study of a Cost and Size Reduction Opportunity
- EP in ASIC applications: Case Study of a Performance Improvement Opportunity
- Conclusions and Key Takeaways
- Future of EP

3

What are Embedded Passives (EP)?

- Replace traditional Surface Mount Components with embedded equivalents
  - Improves electrical performance – Decoupling , lower inductance
  - Reduces part count
  - Reduces solder joints – improves reliability
  - Can reduce net cost in high volume applications
  - Reduces product thickness and overall size
- Compatible with conventional manufacturing processes



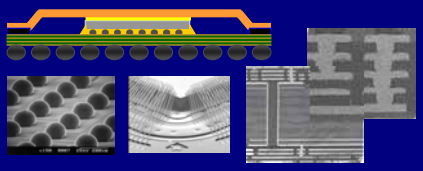
4

EP Overview - Phases of Integration

Lead frame WB and Ceramic substrate

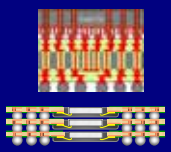
- Double sides boards
- 4/4mil L/S 20mil PTH
- Alumina substrate

Organic FCBGA and WB



- Large body size WB and organic FcBGA components
- Multiple layer build-up (6-2-6)
- Stacked microvias, 18/18μm LS

Embedded Actives, PoP, TSV



- Embedded Si
- PoP designs
- TSV for increased functionality.

Embedded Passives Span all Phases

- Buried Capacitance in organic Laminate systems
- Printable materials for resistors and capacitors
- Embeddable bulk components

5

EP Overview - Types of EP

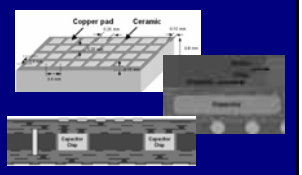
Laminate/Foil Systems

- Parallel plate caps in HDI
- Print and etch L's
- Low inductance/impedance shared capacitance layers
- Capacitors in LTCC substrates
- Foil based and plated resistive materials
- Compatible with ceramic substrates, organic PWB's, MCM's SiP applications - interposers

Printable Materials

- Screen printed Polymer Thick Film (PTF) resistors
- Ceramic Filled Photoimageable (CFP) dielectric for organic PWB
- Screen printed ceramic filled paste with printed top electrode.
- Used as RLC networks, termination resistors, decoupling capacitors.
- Demonstrated in SiP, MCM's Audio components, Memory modules, VCO's, PA matching

SMT's & Bulk Materials



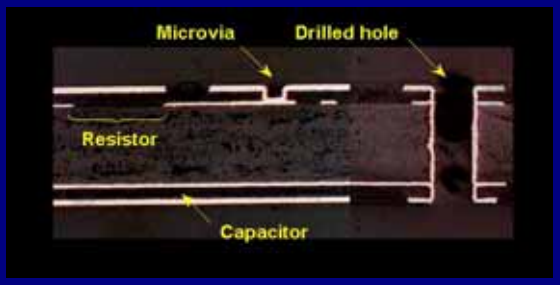
- Embedded Bulk Capacitance (EBC)
- Individual embedded SMT's
- Used in decoupling application to reduce power noise
- Demonstrated for core power noise decoupling in ASIC application.

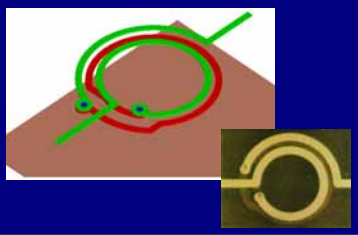
6

EP Overview – Laminate/Foil Systems

Inherent EP Opportunities – Low Hanging Fruit

- Leverages HDI dielectric properties & design rules
- Capacitance density of HDI dielectric 0.8pF/mm2
- Single and multi-layer spiral inductors with embedded value up to 12nH
- Should always be considered if space is available

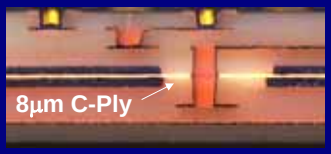


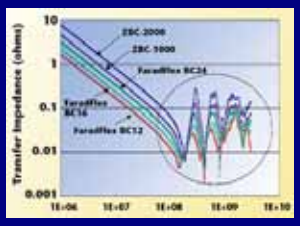


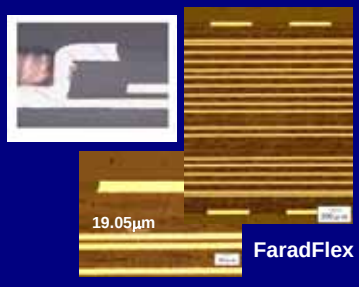
7

EP Overview – Laminate/Foil Systems (Capacitors)

- Thin laminate systems for buried/shared capacitance
- Examples include: 3M C-Ply®, Oak-Mitsui FaradFlex®, and Sanmina ZBC®
- High frequency by-pass decoupling
- Low power loop inductance
- Shielding
- Thickness range from 8–50μm depending on type
- Demonstrated in PWB's and ASIC package interposers





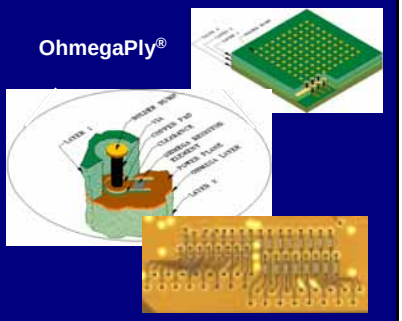


8

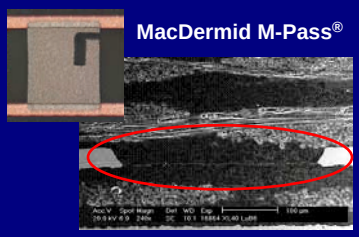
EP Overview - Laminate/Foil Systems (Resistors)

- Embedded resistance via preformed foil such as OhmegaPly
  - Available in various sheet resistivity
  - Compatible with conventional PWB manufacturing processes
- Embedded Resistance via Plated Resistor technology
  - 100Ω/☐ sheet resistivity
- Trimmable for high tolerance.
- Termination resistors in FCBGA applications, MCM's, Interposers and PWB's.
- Can be combined with embedded C's and L's for circuit tuning.

OhmegaPly®



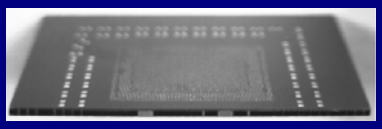
MacDermid M-Pass®

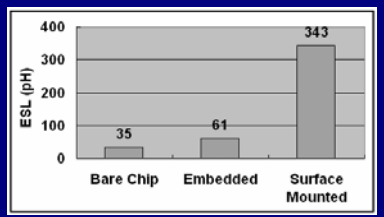


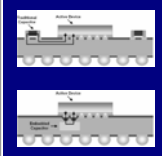
9

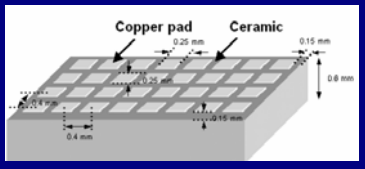
EP Overview - Embedded Bulk Capacitance (EBC)

- SMT's and capacitor arrays
  - Discrete cap solutions
  - Localized placement
- Highest level of embeddable capacitance
- Best for power integrity – highest levels of decoupling
- Lowest package inductance solution - >60% performance







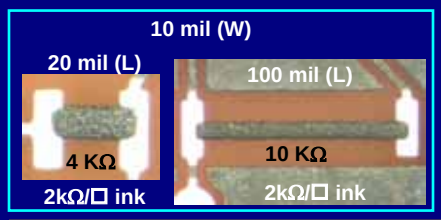


Images courtesy of PPT

10

EP Overview – Printed Materials (PTF Resistors)

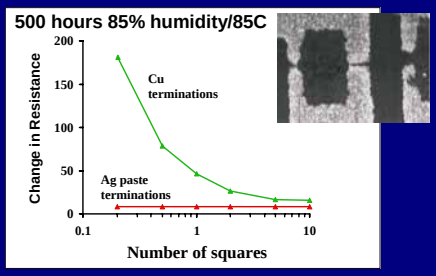
- EP Polymer Thick Film (PTF) Resistors
  - Wide array of resistive inks available
  - Embeddable from 5Ω-1MΩ
  - 15% tolerance as printed – trimmable to 5%
  - Compatible with HDI and conventional PWB processes
  - Demonstrated cost and size reduction in RF application

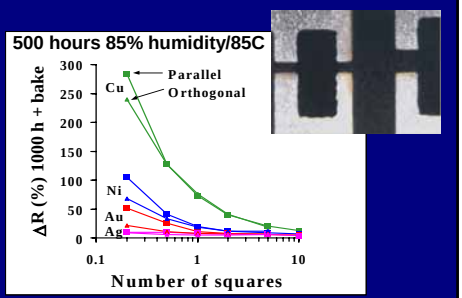


- PTF Resistor Trimming
  - Active laser trimming

EP Overview – Printed Materials (PTF Innovations)

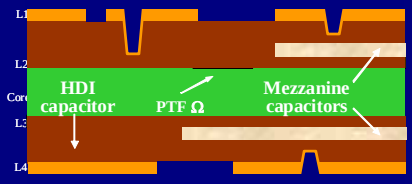
- PTF History
  - Printing PTF directly onto Cu terminations
    - resulted in poor stability during 85% humidity/85C
  - Printing PTF onto Ag paste terminations
    - excellent stability
    - poor uniformity and precision
    - more costly
- Novel PTF process:
  - Replacing Ag paste with immersion Ag plating
  - high stability, low cost, greater precision

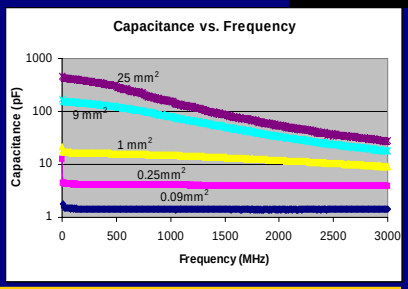




EP Overview - Printed Materials (Capacitors)

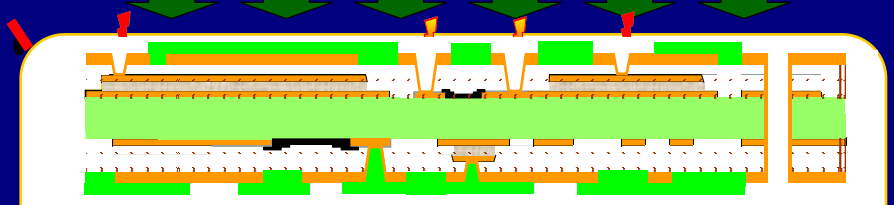
- Ceramic Filled Photo Dielectric (CFP)
- UV-imageable epoxy mixed w/ ceramic powder
- Produces discreet embedded caps or shared capacitance layers
- Buried mezzanine layer → Does NOT occupy surface space
- Utilizes conventional equipment and processes - drop-in compatible into most PWB factories
- Capacitance density 18pF/mm2; tan δ=0.04
- Typical range: 2-450pF with 15% tolerance





13

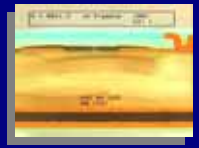
EP Overview - Manufacturing Process Flow



EP PWB complete

Process Steps
1. Start with Cu-clad inner-layer
2. Roller coat CFP
3. Laminate Cu foil
4. P & E top Mez. plate
5. Photo-define CFP
6. Print and etch inner-layer; black oxide
7. Apply stability promoter
8. Screen print PTF resistors

Process Steps continued…
9. Laminate RCC
10. Drill MVH and PTH
11. Electroplate outer-layer
12. Circuitize OL & apply SM



14

EP in RF Applications: Case Studies of Cost and Size Reduction Opportunities for Cell Phone Applications

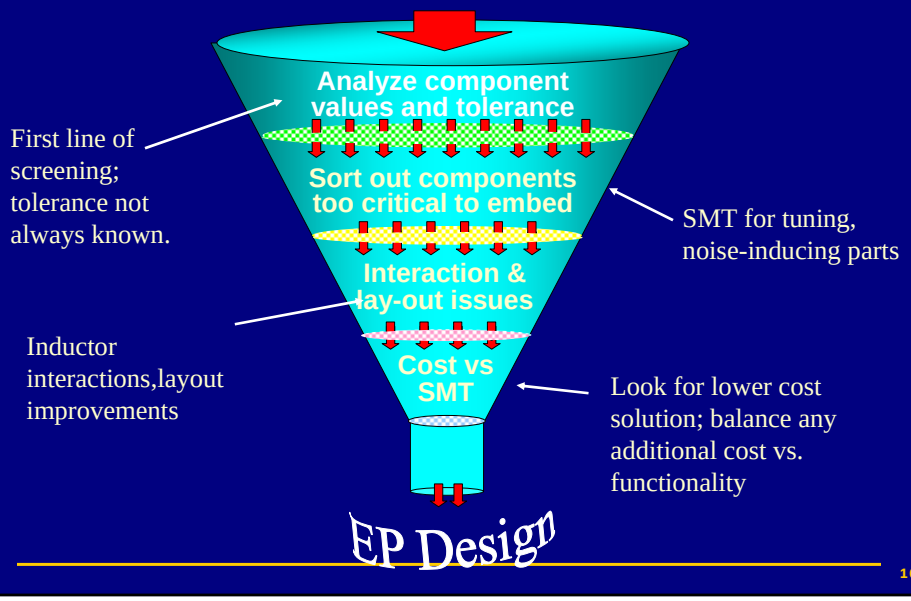
Case A: RxVCO

&

Case B: 800 MHz LO

Case Studies - EP Design Methodology

BOM and Electrical Schematic



16

Case A: Rx-VCO Design Objective

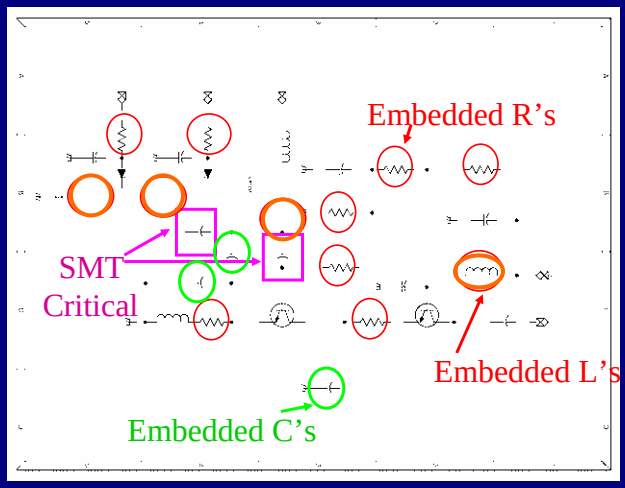
- The goal was to create an EP Rx-VCO to replace the incumbent ceramic VCO.
- Ceramic VCO was experiencing yield problems and was expensive.
- Alternative organic PWB VCO's were unable to meet size and design rule & size requirements.
- Restictions
  - Must match LTCC footprint and pin-out

- Ceramic Rx-VCO
- 7 x 9 mm
- 27 SMT parts

17

Case A: Rx-VCO Schematic Review

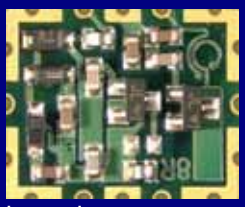
- Schematic review
- Identify Critical Components
- Identify printable resistors
  - 20% tolerance
  - 50 & 1kΩ/□
- Identify EP caps
  - HDI only
  - 10 pF max
- Identify L's
  - T-lines
  - Spiral



18

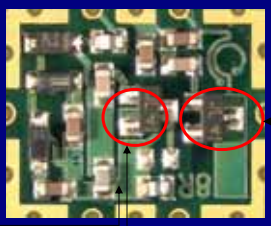
Case A: RxVCO Results and Impact

- **Embedded 8 resistors using 2 inks**
- **Embedded 3 capacitors 1.8 – 2.2 pF using HDI dielectric as capacitance material**
- **Embedded 4 inductors: Two T-Lines and two 2.5 turn spiral inductors (1.5 nH – 10 nH)**
- **Impact: 13 fewer parts than ceramic (10 % savings)**
  - Lower cost substrate (30% less) and assembly (40% less) resulting in >$2 savings/part
  - Equivalent performance and size (could have been smaller)
  - Improved manufacturability and immediate high yield supply
  - Implemented with Ohmega-Ply and PTF resistors



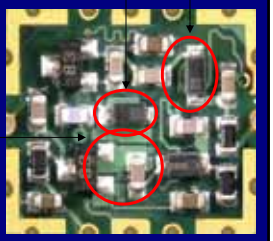
19

Case A: RxVCO Results and Impact



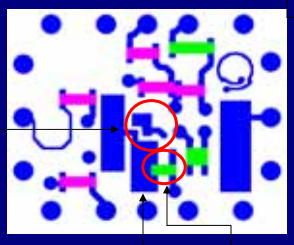
SMT pad on embedded C's plate

Spiral L's + embedded C's underneath SMTs



Effect of mutual capacitance

SMT pad as part of embedded C's plate/parallel C's using microvia



Ground plane utilized for embedded C's connected to ground

PTF R's terminated on embedded C's plate

20

Case B: 800 MHz LO Design Objective

- Modularize a Motherboard functionality
- Enable module reuse across products
- Must be lower cost than incumbent and offer improved yields over a non-EP based (full SMT) modular solution

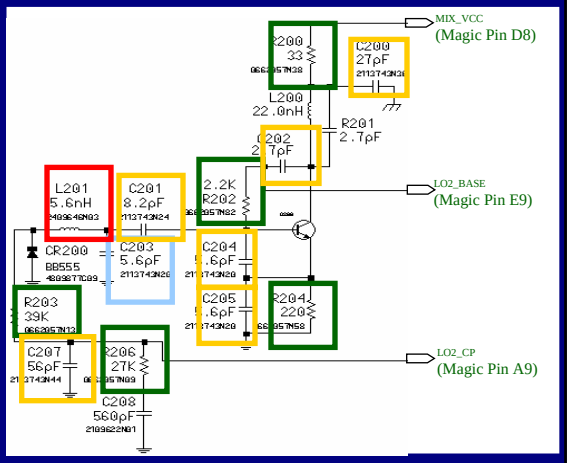
Incumbent Technology	HDI EP Technology
• Discrete solution on motherboard	• 1+2+1 HDI with CFP capacitors
• Area on motherboard 48 mm²	• Module area = 24.3 mm²
• 18 placed parts	• 5 placed parts
• Implementation cost: $ 0.38	• Implementation cost: $ 0.28
• DM $ 0.20	
• Conversion $ 0.18	• Area reduction = 49.4 %
	• Cost Reduction = 27.3 %
	• Part count reduction = 13
	• Pick & place directly onto motherboard

21

Case Study: 800 MHz LO Schematic Review

- Identify Critical Parts
- Identify printable resistors (20% tol)
  - 50Ω & 50kΩ inks
- Identify Caps for GEN2 embedding
- Identify inductors for embedding

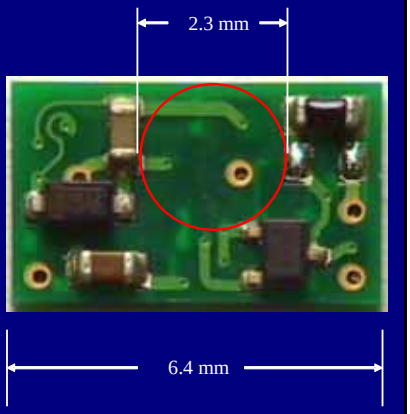
- Schematic Review

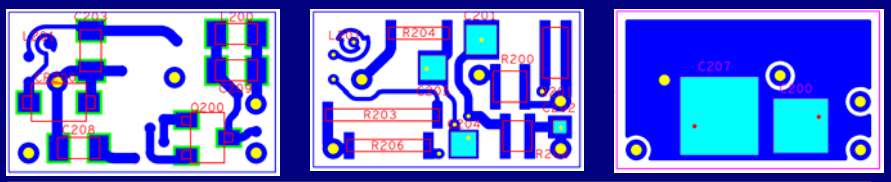


22

Case Study: 800 MHz LO Results and Impact

- LGA module
- 6 EP resistors, 6 EP capacitors, 5 SMT
- Discreet embedded CFP capacitors on top side of module.
- Capacitors to ground on backside
- Module size 6.4mm X 3.8mm
- Economies of scale - Greater than 3000 pieces produced per production panel
- Facilitated assembly by increasing open surface area for pick and place.
- Shipped in over 12M phones





23

Cell Phone Implementation and Impact

1999/2000

Rx/Tx VCOs

2001

GCAP Audio

800 MHz LO

2002

Tx VCO Bluetooth

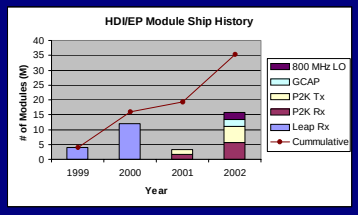
2003

GSM SOM

2004-06

EP Resistors

EP Resistors + Capacitors



- Technology shipped in over 80 million cell phones
- Realized many millions of dollars in cost savings

24

EP in an ASIC Application: Case Study of a Performance Improvement Opportunity

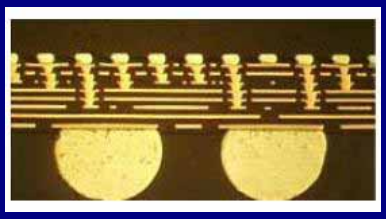
ASIC Case Study - Advanced ASIC Packaging

- Next generation (90nm and below) ASIC's have significantly higher Power & Signal Integrity challenges
  - Decrease in core power and higher levels of IC integration increases resultant IR drop in the power rails eroding power integrity and circuit timing margins.
  - Implementation of various power saving techniques like clock gating, module power down and sleep mode, will result in steeper steps in power delivery requirements
  - Noise and crosstalk will increase due to density & isolation limitations
- To overcome the challenges, next generation package substrates require revolutionary change in capability
  - Decreased pkg inductance – more direct connections/shorter paths
  - Enable increased incidence of localized (appropriately placed) decoupling
  - Increase circuit density along with methods for improved isolation

26

ASIC Case Study – Advanced ASIC Packaging

- **Coreless substrates** utilizing fully stacked μvia's.
- **BGA-side Capacitance** - SMT capacitors interspersed between BGA balls
- **Embedded Bulk Capacitance (EBC)** & alternative materials
- Interposer solution w/ **buried/shared capacitance**



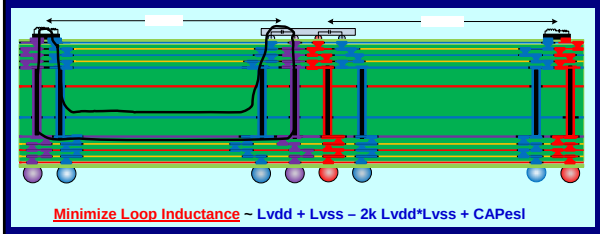
8-layer coreless w/ stacked μ-via

0402 SMT's assembled under BGA

27

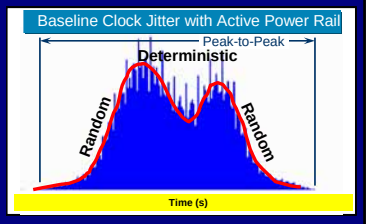
ASIC Case Study – Design Objective

- A high volume ASIC was selected as the baseline performance comparison
  - 40 x 40 mm; 4-4-4 conventional construction
  - Known PI and clock jitter issues
  - All test hardware & software available



Minimize Loop Inductance ~ Lvdd + Lvss – 2k Lvdd*Lvss + CAPesl

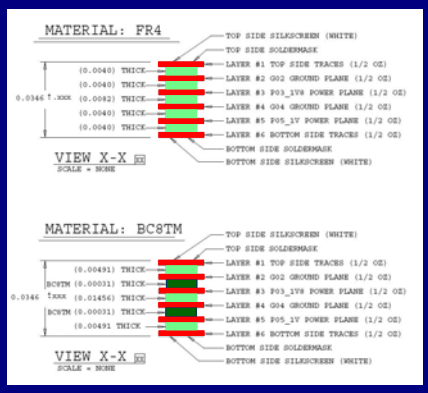
STATS (Baseline)	
Stackup Type	4-4-4
Power Core/IO	~8/2 Watts
Die Size/Bumps	13.2mm/2545
Pkg Size/Pins	40mm/1520
PKG Decap TOP	17 VDD, 7 VDDIO
PKG Decap Type	SMT-0306, ESL=300pH, ESC=.22uF



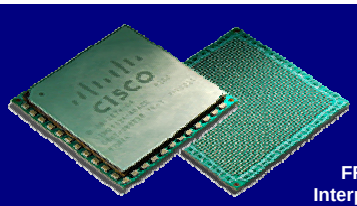
- Minimized changes to circuit routing to enable better comparison
- Restricted to the same foot-print and pin-out in order to enable test.
- Model and simulate advanced package options and correlate simulation results with system level electrical measurement
- Eliminate known PI and SI issues

28

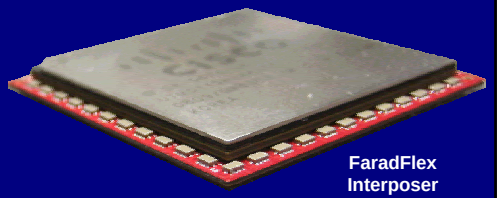
ASIC Case Study - Interposer w/ Buried Capacitance



- 6 layer interposer
  - FR4 with IDC caps
  - Faradflex BC8TM buried/shared capacitance layers and IDC caps
- Objective was to generate independent power planes isolated from MB
- IDC caps mounted on periphery of interposer
- Maintained same footprint



FR4 Interposer

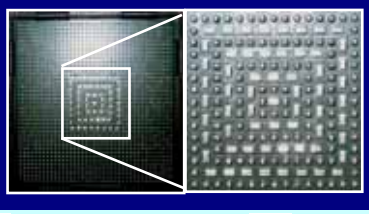


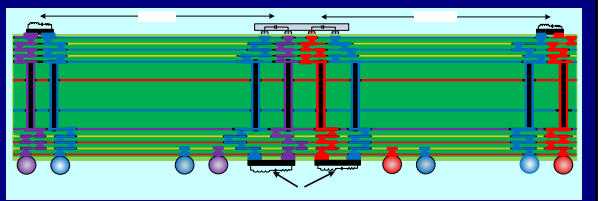
FaradFlex Interposer

29

ASIC Case Study - BGA Side Capacitors

- Maintained the same 4-4-4 construction and overall foot-print
- Most layers were undisturbed to maintain timing
- Replaced top side capacitors with 61 bottom side 0204 SMT capacitors
- Adopted a concentric pattern under the die only
- 97 BGA PWR/GND balls removed with no ill effects
- Fabricated and assembled together w/ supply chain partners





30

ASIC Case Study - BGA Side Capacitor Conversion

	Original Package	BGA Side Capacitor	Difference (%)	Number of Capacitors
GND	**339**	**288**	**51 (15%)**	**---**
VDD (1.0V)	**126**	**104**	**22 (17.5%)**	**31**
VDDO18 (1.8V)	**98**	**74**	**24 (24.5%)**	**27**
VDDO25 (2.5V)	**6**	**6**	**0 (0%)**	**3**
Total	569	472	97 (17%)	61

Capacitor Choice dictated by the following factors:

- **Low ESL** value was the key factor – 83 pH.
- **Size**: Needed to fit in a row where the BGA balls were depopulated and the height needed to be less than the package standoff height – 0204-2T t=0.35 mm. max.
- **Capacitance Value**: With the above constraints the maximum capacitance value available today is 0.47uF

31

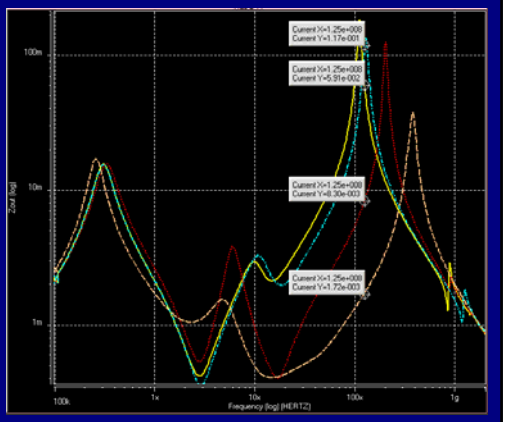
ASIC Case Study – Embedded Bulk Capacitance

- **Currently it is Confidential Design information and cannot be shared**
- **Conventional PCB materials layer stack-up**
- **"Next best thing" to capacitance on the die**
- **Available commercially in low volume**

32

ASIC Case Study – Simulation of 1V AC

- EBC predicts lowest impedance at higher frequency
- BGA-side capacitor design second best
- Mounting L is negligible for EBC and ~4x lower for BGA side when compared to caps mounted on the top layer (~40pH/cap on the bottom vs. ~160pH/cap on the top).
- Coreless shows minimal improvement for 1.0 volt plane because minimal change to relevant layers



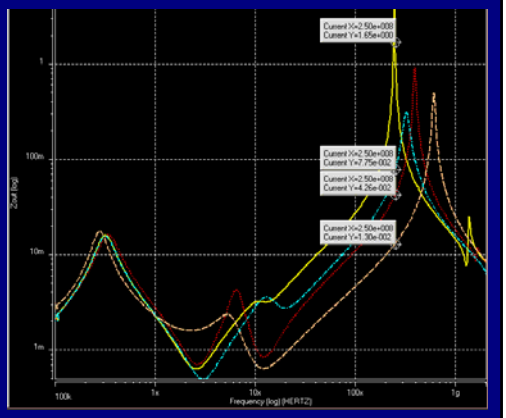
1.0V Zout measured at die side with die

Red: BGA-side cap
Cyan: Coreless
Orange: EBC
Yellow: Baseline

33

ASIC Case Study – Simulation of 1.8V AC

- EBC and BGA-side designs continue to offer best performance at higher frequency
- Coreless design is able to deliver better results as the 1.8V plane is moved to the top layer with the plane L as low as 4pH vs. 15pH in the original 4-4-4 package.
- Coreless design rules facilitated a simple layer swap to realize performance improvement

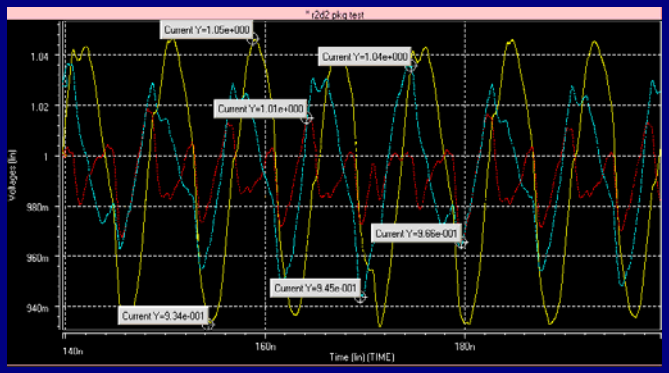


1.8V Zout measured at die side with die

Red: BGA-side cap
Cyan: Coreless
Orange: EBC
Yellow: Baseline

34

ASIC Case Study – 1.8V AC Transient Analysis

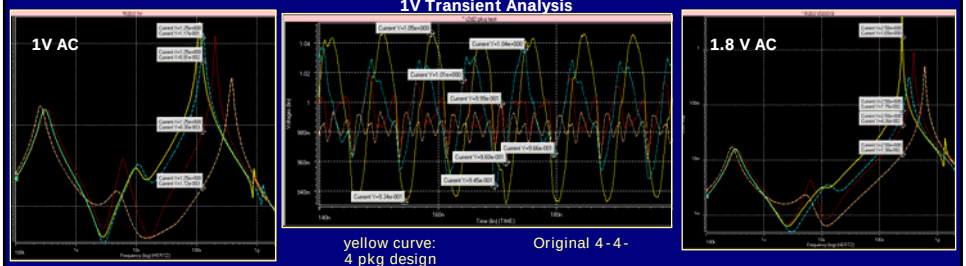


Red: BGA-side cap Cyan: Coreless Orange: EBC Yellow: Baseline

1 volt Transient Analysis	Min Voltage (V)	Max Voltage (V)	Peak-peak Voltage (V)	% Improve
Original 4-4-4 design	0.904	1.05	0.116	-
Bottom-side cap design	0.966	1.02	0.054	53%
Integrated Bulk Cap	0.960	0.99	0.030	74%
Coreless design	0.915	1.04	0.095	18%

35

ASIC Case Study - Simulation Results Summary



yellow curve: Original 4-4-4 pkg design
red curve: Bottom-side capacitor design
orange curve: EBC
cyan curve: Coreless design

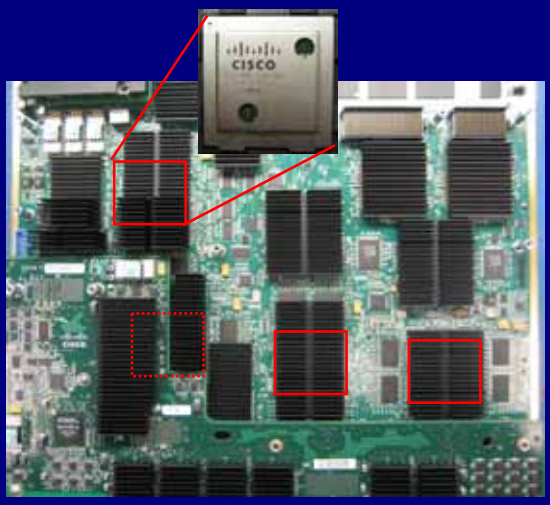
- **Simulation shows significant reduction in impedance and core power noise (~74%) with advanced substrate designs: EBC**
- **Simulation did not anticipate improvement for interposer solutions**

1 volt Transient Analysis	Min Voltage (V)	Max Voltage (V)	Peak-peak Voltage (V)	% Improve
Original 4-4-4 design	0.904	1.05	0.116	-
Bottom-side cap design	0.966	1.02	0.054	53%
Integrated Bulk Cap	0.960	0.99	0.030	74%
Coreless design	0.915	1.04	0.095	18%

36

ASIC Case Study - Electrical Test Set-up

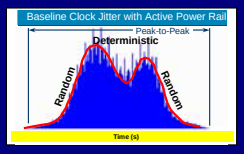
- ASIC's with advanced substrates were placed onto a functional Motherboard for system level test
- 12Gbps traffic generated with IXIA packet generator
- Measurements were made on bottom side of motherboard and at special test points through opening in lid.

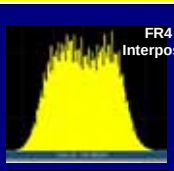


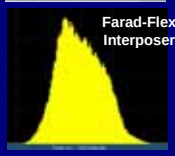
37

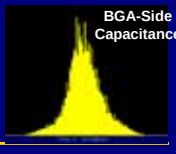
ASIC Case Study – Measured Performance Results

- **Excellent correlation with simulation results**
- **EBC show greatest improvement in power noise and clock jitter (54%)**
- **FaradFlex interposer and BGA-side caps show similar improvement (~20%)**
- **Deterministic jitter leading to bimodal clock is eliminated with BGA-side capacitance and FaradFlex interposer solutions**
  - **Much more stable clock as a result of lower power noise**









		Performance			
		Power Noise (normailized)	% Improvement (Noise)	Clock Jitter (normalized)	% Improvement (Jitter)
1.0 Volt Plane	Baseline	1	N/A	1.00	N/A
	Interposer-FR4	0.82	18%	0.87	13%
	Interposer-Flex	0.64	36%	0.76	24%
	BGA-side	0.69	32%	0.79	21%
	Int. Bulk Cap	TBD	TBD	0.46	**54%**
	Coreless	TBD	TBD	TBD	TBD

38

Conclusion and Key Takeaways

- EP can provide value for PWB, organic and ceramic packages, MCM's and SiP by enabling cost and size reduction, and performance improvement
- EP technology and materials are available in many formats and multiple commercial vendors to accommodate various application needs
- Value of printed resistor and capacitor technology has been demonstrated in over 100M cell phone and memory module applications
- Laminate based buried capacitance materials have been used for years in server boards and other large format PCB's – now being demonstrated for ASIC and advanced packaging applications
- Buried bulk capacitance is "next best thing" to on-die decoupling offering lowest inductance and highest performance .

39

Future of EP – Where to Next?

- **My favorite title applies: "Embedded Passives - The (For)Ever-Emerging Technology" …unless**
  - More design, lay-out and modeling tools are needed to facilitate EP use.
  - Engineering familiarity with the value-ads needs to grow
- **Broad-based use in MCM's, SiP and advanced packaging applications will struggle until familiarity and comfort level is achieved**
- **As Si nodes and PI/SI margins continue to shrink, advanced packages need to bridge performance gaps**
  - Trade-off assessment between on-die capacitance and "next best thing" . EP and other advanced packaging options become a necessity
  - Space limitation on MB's will require size reduction
  - Cost reduction via improved yield, part count reduction and reliability becomes a driving force
- **2 more titles with which to conclude…**
  - Embedded Passives - Just Shove Them Where The Sun Don't Shine
  - **Embedded Passives - Just Do It! :)**

40