Embedded Passives Methodologies and Opportunities for Implementation

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“The Bean” in Chicago’s Millennium Park
Michigan Ave skyline collapsing into the bean is a good metaphor for the product miniaturization and the driving force for advanced integration technologies

Background Information

• Collaborate with product development teams to enable manufacturing processes for improving the functionality of PWB’s and advanced package substrates to meet existing and future product performance requirements.
• Focus on developing and utilizing new Embedded Passives (EP) technologies has been a consequence of pursuing the best possible solution.
• Picking a title...7 choices
  – Get the Pb out - with EP!
  – Embedded Passives - I Don't Get It!
  – Embedded Passives - The (For)Ever-Emerging Technology
  – Embedded Passives Methodologies and Opportunities for Implementation
• Learn from what has been done and evolve
Outline

• Introduction
• Overview of EP technology
• EP in RF applications: Case Study of a Cost and Size Reduction Opportunity
• EP in ASIC applications: Case Study of a Performance Improvement Opportunity
• Conclusions and Key Takeaways
• Future of EP

What are Embedded Passives (EP)?

• Replace traditional Surface Mount Components with embedded equivalents
  – Improves electrical performance – Decoupling, lower inductance
  – Reduces part count
  – Reduces solder joints – improves reliability
  – Can reduce net cost in high volume applications
  – Reduces product thickness and overall size

• Compatible with conventional manufacturing processes

4-Layer FR-4 PWB
Embedded Resistor & Capacitor
SMT Resistor
EP Overview - Phases of Integration

- Lead frame WB and Ceramic substrate
  - Double sides boards
  - 4/4mil L/S 20mil PTH
  - Alumina substrate

- Organic FCBGA and WB
  - Large body size WB and organic FcBGA components
  - Multiple layer build-up (6-2-6)
  - Stacked microvias, 18/18µm LS

- Embedded Actives, PoP, TSV
  - Embedded Si
  - PoP designs
  - TSV for increased functionality.

Embedded Passives Span all Phases

- Buried Capacitance in organic Laminate systems
- Printable materials for resistors and capacitors
- Embeddable bulk components

EP Overview - Types of EP

Laminate/Foil Systems
- Parallel plate caps in HDI
- Print and etch L’s
- Low inductance/impedance shared capacitance layers
- Capacitors in LTCC substrates
- Foil based and plated resistive materials
- Compatible with ceramic substrates, organic PWB’s, MCM’s SiP applications - interposers

Printable Materials
- Screen printed Polymer Thick Film (PTF) resistors
- Ceramic Filled Photoimageable (CFP) dielectric for organic PWB
- Screen printed ceramic filled paste with printed top electrode.
- Used as RLC networks, termination resistors, decoupling capacitors.
- Demonstrated in SIP, MCM’s Audio components, Memory modules, VCO’s, PA matching

SMT’s & Bulk Materials
- Embedded Bulk Capacitance (EBC)
- Individual embedded SMT’s
- Used in decoupling application to reduce power noise
- Demonstrated for core power noise decoupling in ASIC application.
EP Overview – Laminate/Foil Systems

Inherent EP Opportunities – Low Hanging Fruit

- Leverages HDI dielectric properties & design rules
- Capacitance density of HDI dielectric 0.8pF/mm²
- Single and multi-layer spiral inductors with embedded value up to 12nH
- Should always be considered if space is available

EP Overview – Laminate/Foil Systems (Capacitors)

- Thin laminate systems for buried/shared capacitance
- Examples include: 3M C-Ply®, Oak-Mitsui FaradFlex®, and Sanmina ZBC®
- High frequency by-pass decoupling
- Low power loop inductance
- Shielding
- Thickness range from 8–50µm depending on type
- Demonstrated in PWB’s and ASIC package interposers
**EP Overview - Laminate/Foil Systems (Resistors)**

- Embedded resistance via preformed foil such as OhmegaPly
  - Available in various sheet resistivity
  - Compatible with conventional PWB manufacturing processes
- Embedded Resistance via Plated Resistor technology
  - $100\,\Omega$/\(\square\) sheet resistivity
- Trimmable for high tolerance.
- Termination resistors in FCBGA applications, MCM’s, Interposers and PWB’s.
- Can be combined with embedded C’s and L’s for circuit tuning.

**EP Overview - Embedded Bulk Capacitance (EBC)**

- SMT’s and capacitor arrays
  - Discrete cap solutions
  - Localized placement
- Highest level of embeddable capacitance
- Best for power integrity – highest levels of decoupling
- Lowest package inductance solution - >60% performance

Images courtesy of PPT
EP Overview – Printed Materials (PTF Resistors)

- **EP Polymer Thick Film (PTF) Resistors**
  - Wide array of resistive inks available
  - Embeddable from $5\Omega$-1M$\Omega$
  - 15% tolerance as printed – trimmable to 5%
  - Compatible with HDI and conventional PWB processes
  - Demonstrated cost and size reduction in RF application

![Image of PTF Resistors](image)

- **PTF Resistor Trimming**
  - Active laser trimming

EP Overview – Printed Materials (PTF Innovations)

- **PTF History**
  - Printing PTF directly onto Cu terminations
    - resulted in poor stability during 85% humidity/85C
  - Printing PTF onto Ag paste terminations
    - excellent stability
    - poor uniformity and precision
    - more costly

- **Novel PTF process:**
  - Replacing Ag paste with immersion Ag plating
  - high stability, low cost, greater precision

![Image of PTF Innovations](image)
EP Overview - Printed Materials (Capacitors)

- Ceramic Filled Photo Dielectric (CFP)
- UV-imageable epoxy mixed w/ ceramic powder
- Produces discreet embedded caps or shared capacitance layers
- Buried mezzanine layer → Does NOT occupy surface space
- Utilizes conventional equipment and processes - drop-in compatible into most PWB factories
- Capacitance density 18pF/mm²; tan δ=0.04
- Typical range: 2-450pF with 15% tolerance

EP Overview - Manufacturing Process Flow

<table>
<thead>
<tr>
<th>Process Steps</th>
<th>Process Steps continued...</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. Roller coat CFP</td>
<td>10. Drill MVH and PTH</td>
</tr>
<tr>
<td>3. Laminate Cu foil</td>
<td>11. Electroplate outer-layer</td>
</tr>
<tr>
<td>4. P &amp; E top Mez. plate</td>
<td>12. Circuitize OL &amp; apply SM</td>
</tr>
<tr>
<td>5. Photo-define CFP</td>
<td>6. Print and etch inner-layer; black oxide</td>
</tr>
<tr>
<td>7. Apply stability promoter</td>
<td>7. Screen print PTF resistors</td>
</tr>
<tr>
<td>8. Screen print PTF resistors</td>
<td>8. Laminate RCC</td>
</tr>
</tbody>
</table>

EP PWB complete
EP in RF Applications: Case Studies of Cost and Size Reduction Opportunities for Cell Phone Applications

Case A: RxVCO

&

Case B: 800 MHz LO

Case Studies - EP Design Methodology

BOM and Electrical Schematic

First line of screening; tolerance not always known.

Inductor interactions, layout improvements

Analyze component values and tolerance

Sort out components too critical to embed

Interaction & lay-out issues

Cost vs SMT

SMT for tuning, noise-inducing parts

Look for lower cost solution; balance any additional cost vs. functionality
Case A: Rx-VCO Design Objective

- The goal was to create an EP Rx-VCO to replace the incumbent ceramic VCO.
- Ceramic VCO was experiencing yield problems and was expensive.
- Alternative organic PWB VCO's were unable to meet size and design rule & size requirements.
- Restictions
  - Must match LTCC footprint and pin-out

- Ceramic Rx-VCO
  - 7 x 9 mm
  - 27 SMT parts

Case A: Rx-VCO Schematic Review

- Schematic review
- Identify Critical Components
- Identify printable resistors
  - 20% tolerance
  - 50 & 1kΩ
- Identify EP caps
  - HDI only
  - 10 pF max
- Identify L’s
  - T-lines
  - Spiral

Embedded R’s
Embedded L’s
Embedded C’s
**Case A: RxVCO Results and Impact**

- **Embedded 8 resistors** using 2 inks
- **Embedded 3 capacitors** 1.8 – 2.2 pF using HDI dielectric as capacitance material
- **Embedded 4 inductors:** Two T-Lines and two 2.5 turn spiral inductors (1.5 nH – 10 nH)
- **Impact:** 13 fewer parts than ceramic (10 % savings)
  - Lower cost substrate (30% less) and assembly (40% less) resulting in >$2 savings/part
  - Equivalent performance and size (could have been smaller)
  - Improved manufacturability and immediate high yield supply
  - Implemented with Ohmega-Ply and PTF resistors

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**Case A: RxVCO Results and Impact**

- SMT pad on embedded C’s plate
- Ground plane utilized for embedded C’s connected to ground
- PTF R’s terminated on embedded C’s plate
- Spiral L’s + embedded C’s underneath SMTs
- Effect of mutual capacitance
- SMT pad as part of embedded C’s plate/parallel C’s using microvia
Case B: 800 MHz LO Design Objective

- Modularize a Motherboard functionality
- Enable module reuse across products
- Must be lower cost than incumbent and offer improved yields over a non-EP based (full SMT) modular solution

<table>
<thead>
<tr>
<th>Incumbent Technology</th>
<th>HDI EP Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Discrete solution on motherboard</td>
<td>1+2+1 HDI with CFP capacitors</td>
</tr>
<tr>
<td>Area on motherboard 48 mm²</td>
<td>Module area = 24.3 mm²</td>
</tr>
<tr>
<td>18 placed parts</td>
<td>5 placed parts</td>
</tr>
<tr>
<td>Implementation cost: $ 0.38</td>
<td>Implementation cost: $ 0.28</td>
</tr>
<tr>
<td>• DM $ 0.20</td>
<td>• Area reduction = 49.4 %</td>
</tr>
<tr>
<td>• Conversion $ 0.18</td>
<td>• Cost Reduction = 27.3 %</td>
</tr>
<tr>
<td></td>
<td>• Part count reduction = 13</td>
</tr>
<tr>
<td></td>
<td>• Pick &amp; place directly onto motherboard</td>
</tr>
</tbody>
</table>

Case Study: 800 MHz LO Schematic Review

- Schematic Review

  - Identify Critical Parts
  - Identify printable resistors (20% tol)
    - 50Ω & 50kΩ inks
  - Identify Caps for GEN2 embedding
  - Identify inductors for embedding
Case Study: 800 MHz LO Results and Impact

- LGA module
- 6 EP resistors, 6 EP capacitors, 5 SMT
- Discreet embedded CFP capacitors on top side of module.
- Capacitors to ground on backside
- Module size 6.4mm X 3.8mm
- Economies of scale - Greater than 3000 pieces produced per production panel
- Facilitated assembly by increasing open surface area for pick and place.
- Shipped in over 12M phones

Cell Phone Implementation and Impact

- Technology shipped in over 80 million cell phones
- Realized many millions of dollars in cost savings
EP in an ASIC Application: Case Study of a Performance Improvement Opportunity

ASIC Case Study - Advanced ASIC Packaging

• Next generation (90nm and below) ASIC’s have significantly higher Power & Signal Integrity challenges
  • Decrease in core power and higher levels of IC integration increases resultant IR drop in the power rails eroding power integrity and circuit timing margins.
  • Implementation of various power saving techniques like clock gating, module power down and sleep mode, will result in steeper steps in power delivery requirements
  • Noise and crosstalk will increase due to density & isolation limitations
• To overcome the challenges, next generation package substrates require revolutionary change in capability
  • Decreased pkg inductance – more direct connections/shorter paths
  • Enable increased incidence of localized (appropriately placed) decoupling
  • Increase circuit density along with methods for improved isolation
ASIC Case Study – Advanced ASIC Packaging

- Coreless substrates utilizing fully stacked \( \mu \text{via’s} \).
- BGA-side Capacitance - SMT capacitors interspersed between BGA balls
- Embedded Bulk Capacitance (EBC) & alternative materials
- Interposer solution w/ buried/shared capacitance

ASIC Case Study – Design Objective

- A high volume ASIC was selected as the baseline performance comparison
  - 40 x 40 mm; 4-4-4 conventional construction
  - Known PI and clock jitter issues
  - All test hardware & software available

<table>
<thead>
<tr>
<th>STATS (Baseline)</th>
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<tbody>
<tr>
<td>Stackup Type</td>
</tr>
<tr>
<td>Power Core/ID</td>
</tr>
<tr>
<td>Die Size/Bumps</td>
</tr>
<tr>
<td>Pkg Size/Pins</td>
</tr>
<tr>
<td>PKG Decap TOP</td>
</tr>
<tr>
<td>PKG Decap Type</td>
</tr>
</tbody>
</table>

- Minimized changes to circuit routing to enable better comparison
- Restricted to the same foot-print and pin-out in order to enable test.
- Model and simulate advanced package options and correlate simulation results with system level electrical measurement
- Eliminate known PI and SI issues
ASIC Case Study - Interposer w/ Buried Capacitance

- 6 layer interposer
  - FR4 with IDC caps
  - Faradflex BC8TM buried/shared capacitance layers and IDC caps
- Objective was to generate independent power planes isolated from MB
- IDC caps mounted on periphery of interposer
- Maintained same footprint

ASIC Case Study - BGA Side Capacitors

- Maintained the same 4-4-4 construction and overall foot-print
- Most layers were undisturbed to maintain timing
- Replaced top side capacitors with 61 bottom side 0204 SMT capacitors
- Adopted a concentric pattern under the die only
- 97 BGA PWR/GND balls removed with no ill effects
- Fabricated and assembled together w/ supply chain partners
Capacitor Choice dictated by the following factors:

- **Low ESL** value was the key factor – 83 pH.
- **Size**: Needed to fit in a row where the BGA balls were depopulated and the height needed to be less than the package standoff height – 0204-2T t=0.35 mm. max.
- **Capacitance Value**: With the above constraints the maximum capacitance value available today is 0.47uF.

### ASIC Case Study - BGA Side Capacitor Conversion

<table>
<thead>
<tr>
<th></th>
<th>Original Package</th>
<th>BGA Side Capacitor</th>
<th>Difference (%)</th>
<th>Number of Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>339</td>
<td>288</td>
<td>31 (15%)</td>
<td>---</td>
</tr>
<tr>
<td>VDD (1.0V)</td>
<td>126</td>
<td>104</td>
<td>22 (17.5%)</td>
<td>31</td>
</tr>
<tr>
<td>VDDO18 (1.8V)</td>
<td>98</td>
<td>74</td>
<td>24 (24.5%)</td>
<td>27</td>
</tr>
<tr>
<td>VDDO25 (2.5V)</td>
<td>6</td>
<td>6</td>
<td>0 (0%)</td>
<td>3</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>569</strong></td>
<td><strong>472</strong></td>
<td>97 (17%)</td>
<td><strong>61</strong></td>
</tr>
</tbody>
</table>

### ASIC Case Study – Embedded Bulk Capacitance

- Currently it is Confidential Design information and cannot be shared.
- Conventional PCB materials layer stack-up.
- “Next best thing” to capacitance on the die.
- Available commercially in low volume.
ASIC Case Study – Simulation of 1V AC

- EBC predicts lowest impedance at higher frequency
- BGA-side capacitor design second best
- Mounting L is negligible for EBC and ~4x lower for BGA side when compared to caps mounted on the top layer (~40pH/cap on the bottom vs. ~160pH/cap on the top).
- Coreless shows minimal improvement for 1.0 volt plane because minimal change to relevant layers

1.0V Zout measured at die side with die
- Red: BGA-side cap
- Cyan: Coreless
- Orange: EBC
- Yellow: Baseline

ASIC Case Study – Simulation of 1.8V AC

- EBC and BGA-side designs continue to offer best performance at higher frequency
- Coreless design is able to deliver better results as the 1.8V plane is moved to the top layer with the plane L as low as 4pH vs. 15pH in the original 4-4-4 package.
- Coreless design rules facilitated a simple layer swap to realize performance improvement

1.8V Zout measured at die side with die
- Red: BGA-side cap
- Cyan: Coreless
- Orange: EBC
- Yellow: Baseline
### ASIC Case Study – 1.8V AC Transient Analysis

#### Simulation Results Summary

- Simulation shows significant reduction in impedance and core power noise (~74%) with advanced substrate designs: EBC
- Simulation did not anticipate improvement for interposer solutions

<table>
<thead>
<tr>
<th>1 volt Transient Analysis</th>
<th>Min Voltage (V)</th>
<th>Max Voltage (V)</th>
<th>Peak-peak Voltage (V)</th>
<th>% Improve</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original 4-4-4 design</td>
<td>0.854</td>
<td>1.05</td>
<td>0.116</td>
<td>-</td>
</tr>
<tr>
<td>Bottom side cap design</td>
<td>0.866</td>
<td>1.02</td>
<td>0.054</td>
<td>52%</td>
</tr>
<tr>
<td>Integrated Bulk Cap</td>
<td>0.863</td>
<td>1.01</td>
<td>0.054</td>
<td>52%</td>
</tr>
<tr>
<td>Coreless design</td>
<td>0.875</td>
<td>1.04</td>
<td>0.055</td>
<td>10%</td>
</tr>
</tbody>
</table>
ASIC Case Study - Electrical Test Set-up

- ASIC’s with advanced substrates were placed onto a functional Motherboard for system level test
- 12Gbps traffic generated with IXIA packet generator
- Measurements were made on bottom side of motherboard and at special test points through opening in lid.

ASIC Case Study – Measured Performance Results

- Excellent correlation with simulation results
- EBC show greatest improvement in power noise and clock jitter (54%)
- FaradFlex interposer and BGA-side caps show similar improvement (~20%)
- Deterministic jitter leading to bimodal clock is eliminated with BGA-side capacitance and FaradFlex interposer solutions
  - Much more stable clock as a result of lower power noise

<table>
<thead>
<tr>
<th>1.0 Volt Plane</th>
<th>Performance</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Power Noise (normalized)</td>
<td>% Improvement (Noise)</td>
</tr>
<tr>
<td>Baseline</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>Interposer-FR4</td>
<td>0.82</td>
<td>18%</td>
</tr>
<tr>
<td>Interposer-Flex</td>
<td>0.64</td>
<td>36%</td>
</tr>
<tr>
<td>BGA-side</td>
<td>0.69</td>
<td>32%</td>
</tr>
<tr>
<td>Int. Bulk Cap</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Coreless</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>
Conclusion and Key Takeaways

- EP can provide value for PWB, organic and ceramic packages, MCM’s and SiP by enabling cost and size reduction, and performance improvement
- EP technology and materials are available in many formats and multiple commercial vendors to accommodate various application needs
- Value of printed resistor and capacitor technology has been demonstrated in over 100M cell phone and memory module applications
- Laminate based buried capacitance materials have been used for years in server boards and other large format PCB’s – now being demonstrated for ASIC and advanced packaging applications
- Buried bulk capacitance is “next best thing” to on-die decoupling offering lowest inductance and highest performance.

Future of EP – Where to Next?

- My favorite title applies: “Embedded Passives - The (For)Ever-Emerging Technology” …unless
  - More design, lay-out and modeling tools are needed to facilitate EP use.
  - Engineering familiarity with the value-ads needs to grow
- Broad-based use in MCM’s, SiP and advanced packaging applications will struggle until familiarity and comfort level is achieved
- As Si nodes and PI/SI margins continue to shrink, advanced packages need to bridge performance gaps
  - Trade-off assessment between on-die capacitance and “next best thing”. EP and other advanced packaging options become a necessity
  - Space limitation on MB’s will require size reduction
  - Cost reduction via improved yield, part count reduction and reliability becomes a driving force
- 2 more titles with which to conclude…
  - Embedded Passives - Just Shove Them Where The Sun Don’t Shine
  - Embedded Passives - Just Do It! :)