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High-Reliability Through Silicon Via (TSV) Solutions for Image Sensor Packaging

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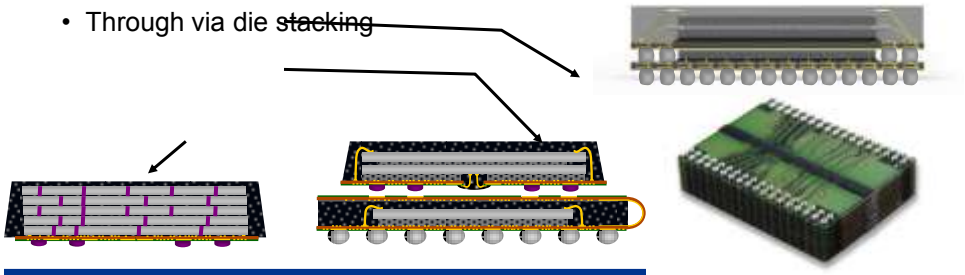
TESSERA
13 January 2010

Outline

- Why a Through Silicon Via (TSV) ?
- Adoption and Barriers
- CMOS image sensors and TSV
- Conclusion

Third direction: Z direction

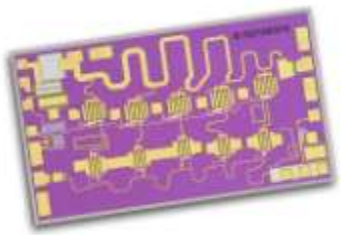
- As many die as possible in z-direction
- 3 solutions:
  - Wire bondable die stacking in single package
  - Package stacking (POP: package on package)
    - Ball-Stack
    - Fold over
  - Through via die ~~stacking~~

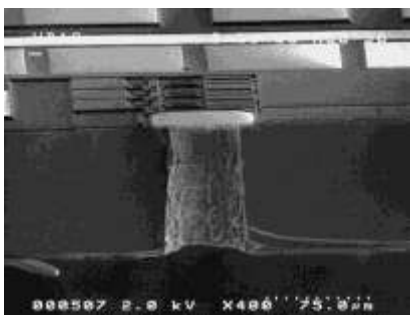


TSV – actually an old technology

Co-planar GaAs RF die always have TSVs!

Via hole grounding technology used in commercial GaAs MMICs since 1976!

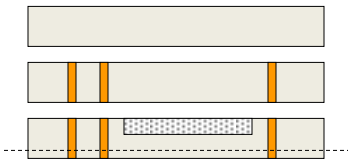




Source: MWT Inc, OPT Inc, STS Inc

TSV Process Routes

Via before CMOS



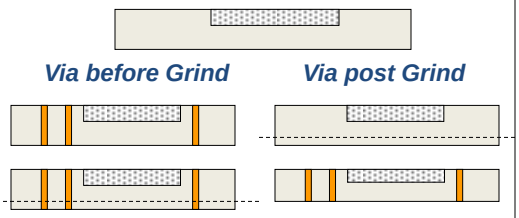
Fabricate vias in blank wafer

Fabricate CMOS circuitry

Grind to thickness

- High risk process first
- Dielectric limited to silicon oxide
- Conductive material limited to poly silicon

Via post CMOS



Via before Grind *Via post Grind*

Fabricate CMOS circuitry

Grind to thickness then fabricate vias OR Fabricate vias then grind to thickness

- Wide choice of materials and processes
- Via first = high aspect ratio vias, additional mask steps
- Via last = low aspect ratio vias, thin wafer handling

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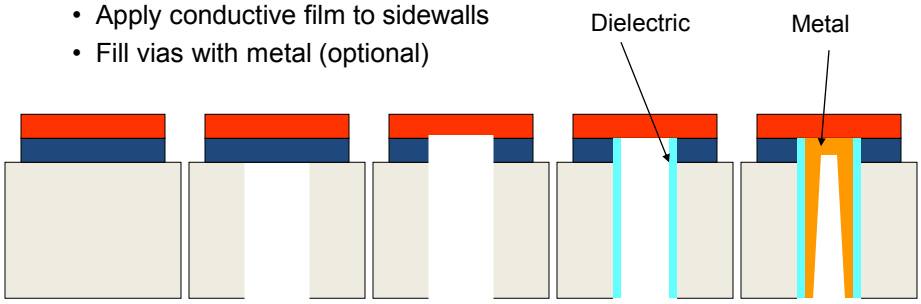
TSV Process Steps

- Etch through thickness of silicon wafer, to oxide stop
- Etch through silicon oxide dielectric underneath bond pad, to metal stop
- Apply dielectric to sidewalls
- Form conductive pipe
  - Apply conductive film to sidewalls
  - Fill vias with metal (optional)



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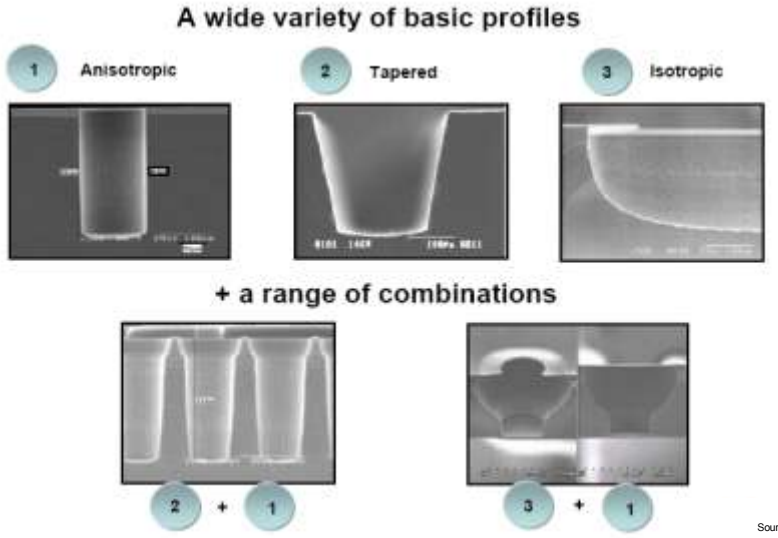
Silicon Through-hole Formation



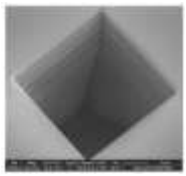
Source: Alcatel

Plasma Etching of Silicon

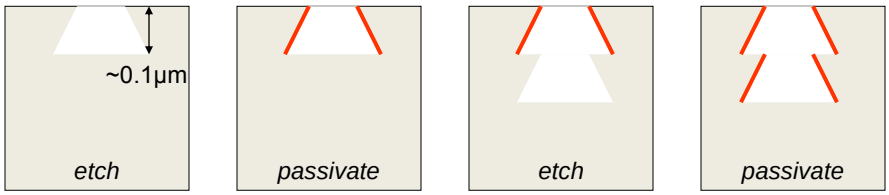
Wet chemistry has insufficient detail for this application

Plasma (dry) etching always used

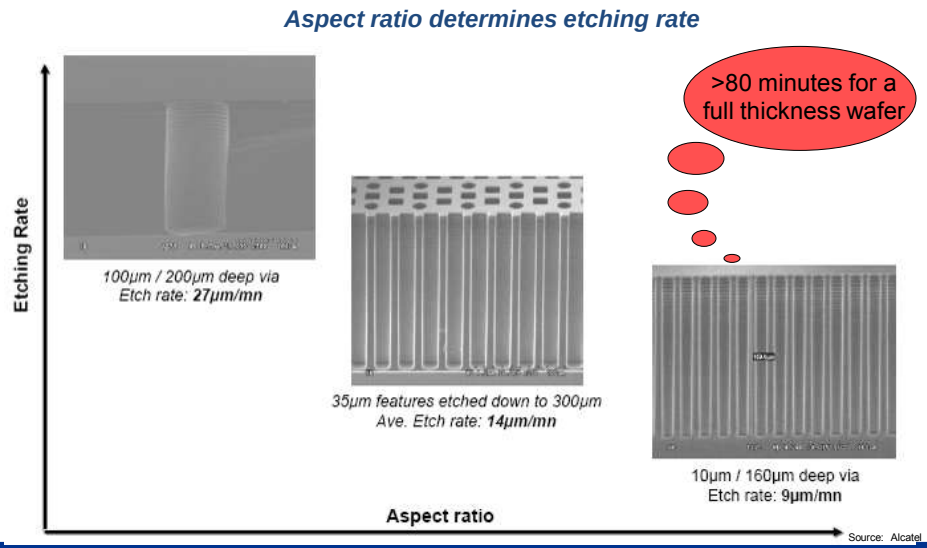
- Tapered etch (SF_6 chemistry)
- Anisotropic etch
  - Bosch process (SF_6 / C_4F_8 alternating chemistry)
  - SF_6 etch with O_2, Cl_2 and HBr sidewall passivation



Source: Alcatel



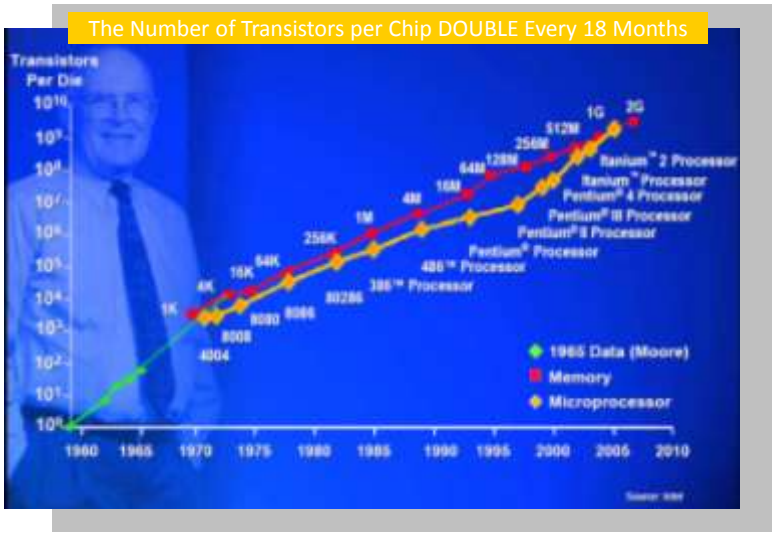
Plasma Etching of Silicon



Why a TSV ?

- When performance fails
- When form factor is needed
- When it simplifies the structure or process

Semiconductor
- Moore's Law…



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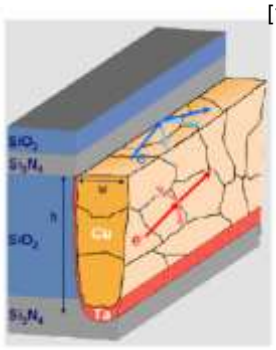
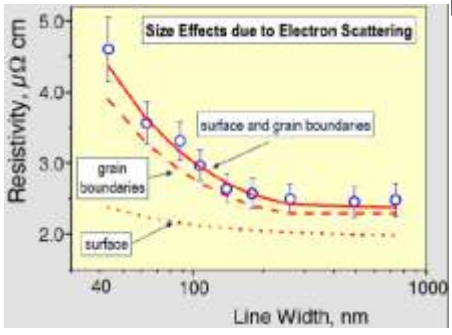
Scaling Conventional Wires

[1]



[1]



More scatterings at wire surfaces and grain boundaries.
Resistivity increases as cross-sectional dimensions scale.
No known technology solution to this problem [2].

[1] W. Steinhögl, et al., *Physical Rev. B*, Vol. 66, 075414 (2002).

[2] Sematech/Novellus Copper Resistivity Workshop, June 2005.

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The Problem with Interconnects

- More than 50% of electronics power is consumed by interconnects

$$\text{Power} \sim C \cdot V^2 \cdot F$$

Capacitance | Voltage | Frequency

- Interconnect length does not scale with transistor nodes
  - Complexity increases to keep chip size constant e.g. memory

RC delay is tending to increase

1mm PCB track ~100 times intrinsic NMOSFET delay

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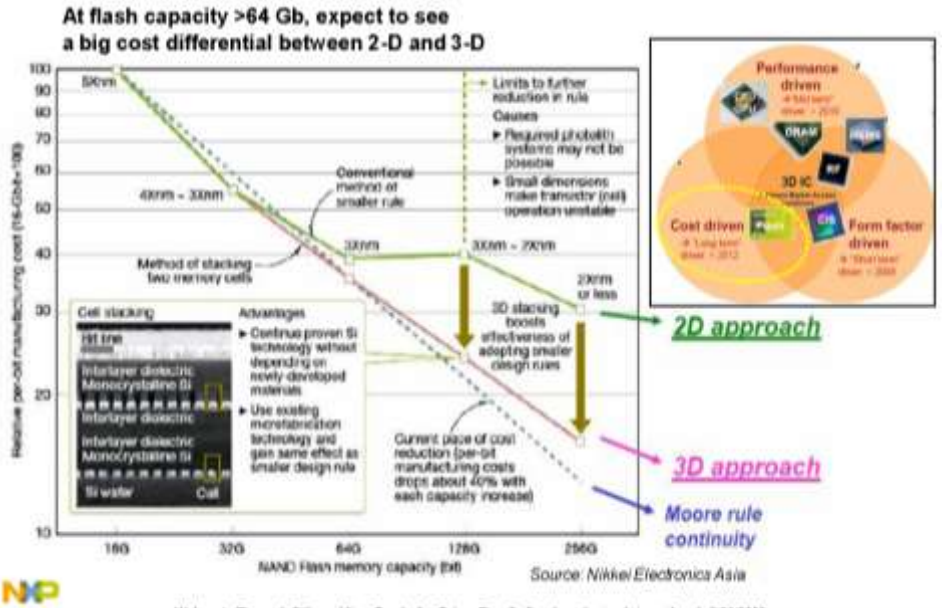
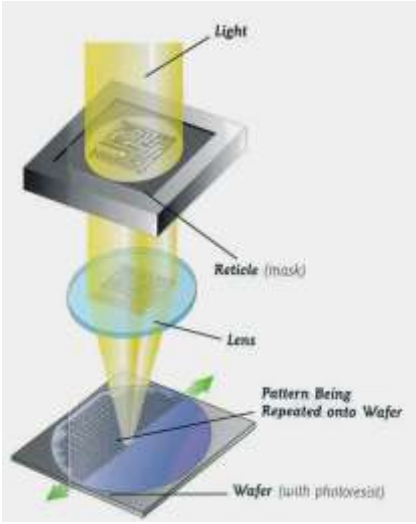
3D Cost Effective way to Scale



Webcast: Through-Silicon Vias: Ready for Prime Time?, Semiconductor International, 3/25/2008

Optical Exposure Systems

"Steppers and Scanners"



$$R = k\frac{\lambda}{NA}$$

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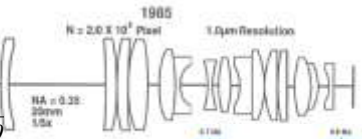
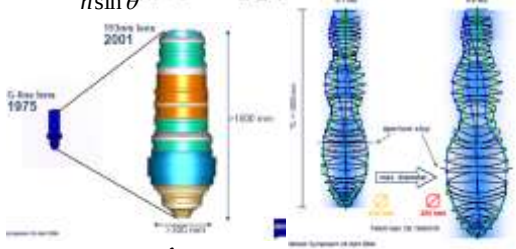
Lithographic Lenses



$$NA = K_1\frac{\lambda}{n\sin\theta}$$



$$NA = K_1\frac{\lambda}{n\sin\theta}$$

Starlith 500 Lens (Zeiss)

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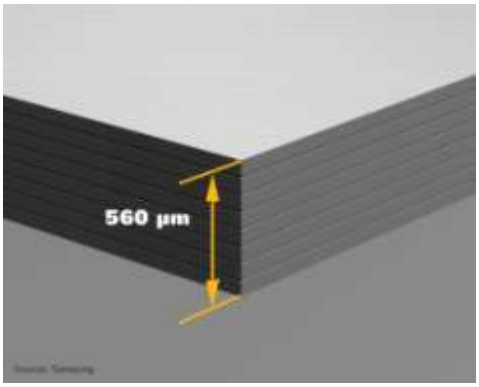
Evolution of Memory

- 5MB IBM hard drive, 1956

Jan 7th PR: SanDisk Announces the 12-Gigabyte microSDHC Card – the World's Largest Capacity Card for Mobile Phones

Through Silicon Vias

Eight Stacked Chips (WSP)



8-die Stack

Example Via Last TSS Memory Application (Samsung ISSCC2009)

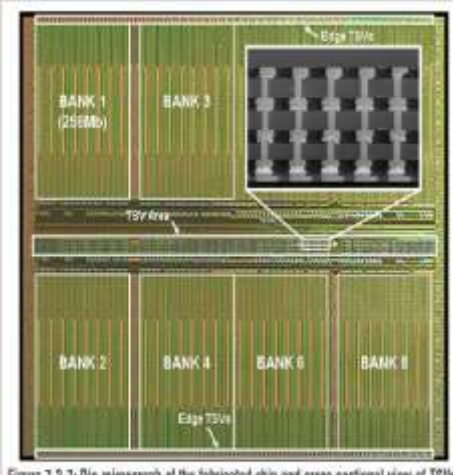
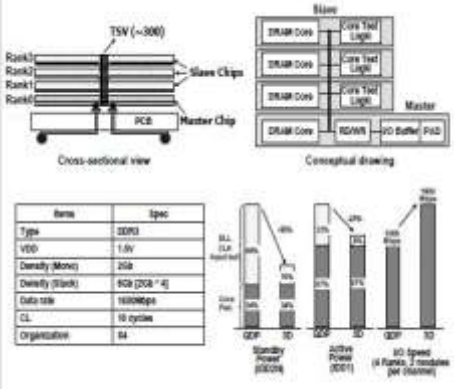


Figure 7.2.7: Die micrograph of the fabricated chip and cross-sectional view of TSVs. The chip size is 10.9×9.8mm².

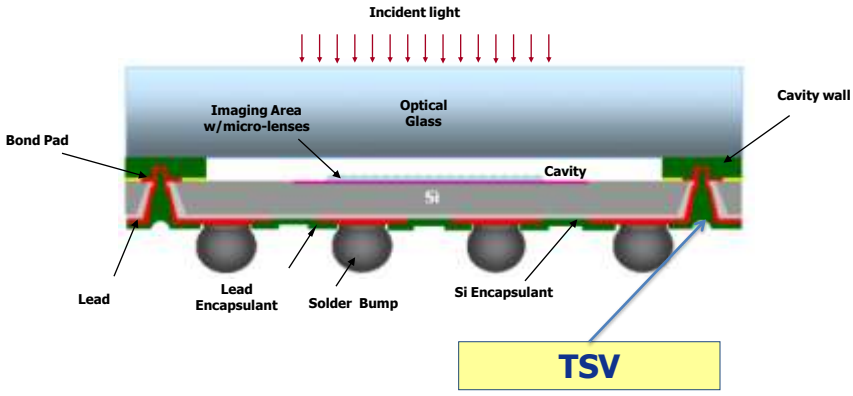
8Gb DDR3 DRAM

- 4 tiers
- 2010 ramp-up.
- Overcomes scaling limit

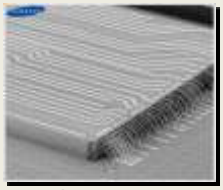


Item	Spec
Type	DDR3
VDD	1.5V
Density (Mono)	2Gb
Density (Stack)	8Gb (2Gb * 4)
Data rate	1600Mbps
CL	10 cycles
Organization	×4

SHELLCASE MVP structure



Latest High Die Stacking Press Releases



Samsung

- 16 die stacked
- 8Gb NAND flash chips, can enable up to a 16 gigabyte (GB) MCP solution
- Wafer-thinning technology to only 30-micrometers (µm) (65% thickness of 10 chips)

November 01, 2006

Akida Elpida

- 20 stacked NAND Flash Chips @1.4mm thickness
- Die Thickness: 30µm

April 23, 2007

Hynix

- 20 stacked NAND Flash Chips @1.4mm thickness
- Die Thickness: 25µm

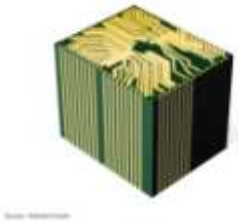
May 06, 2007

High die stacking (beyond 4-6) has substantial manufacturing challenges:

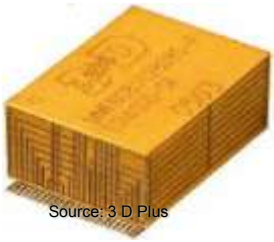
- High cost
- Compound yield
- Complex assembly process
- Questionable reliability performance

Stacking By Edge Connect

16-die Flash Stack



16-die Flash Stack

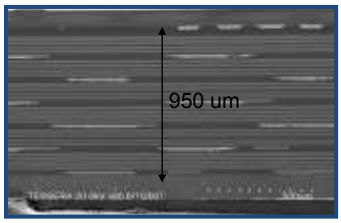


8-die Flash Stack

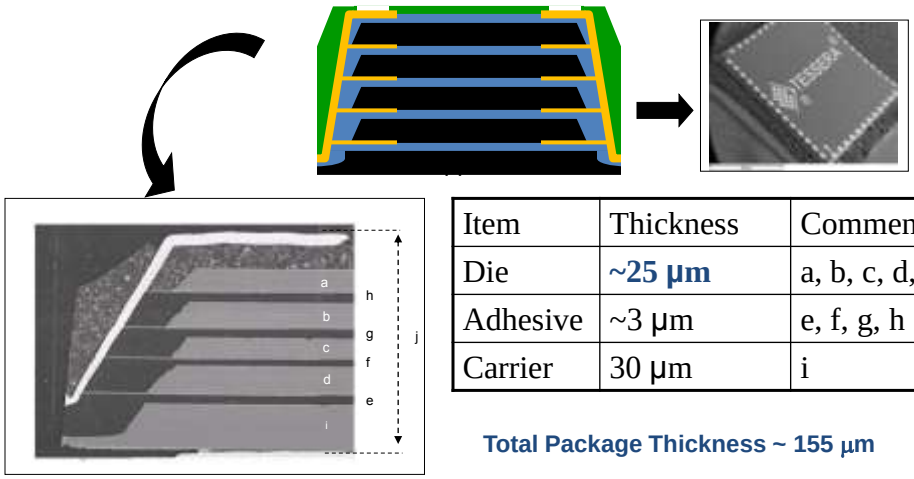
24 WLS Within a Package < 1.0 mm

Micro SD Card Footprint

Cross Sectional SEM



Final Product (Ready For Wire Bond)



Item	Thickness	Comments
Die	**~25 µm**	a, b, c, d, e
Adhesive	~3 µm	e, f, g, h
Carrier	30 µm	i

Total Package Thickness ~ 155 µm

Outline

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The Potential of Imaging

additional 10m units

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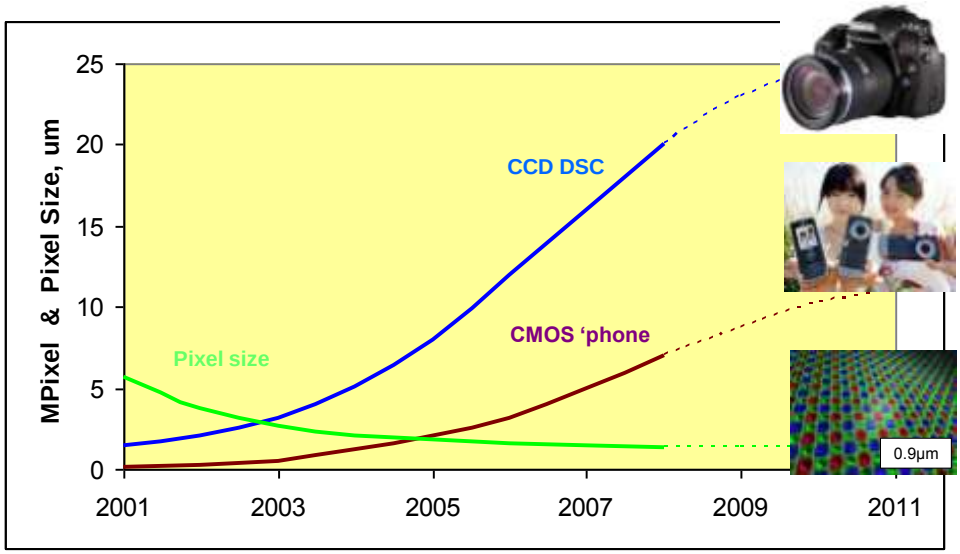
Image Sensor Trends



Source: Techno Systems Research 2008

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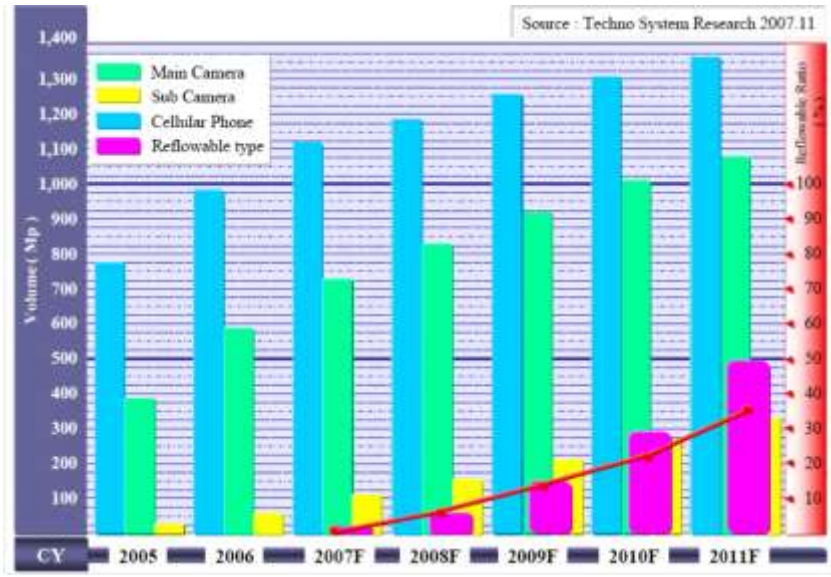
Cell Phone Camera Trend



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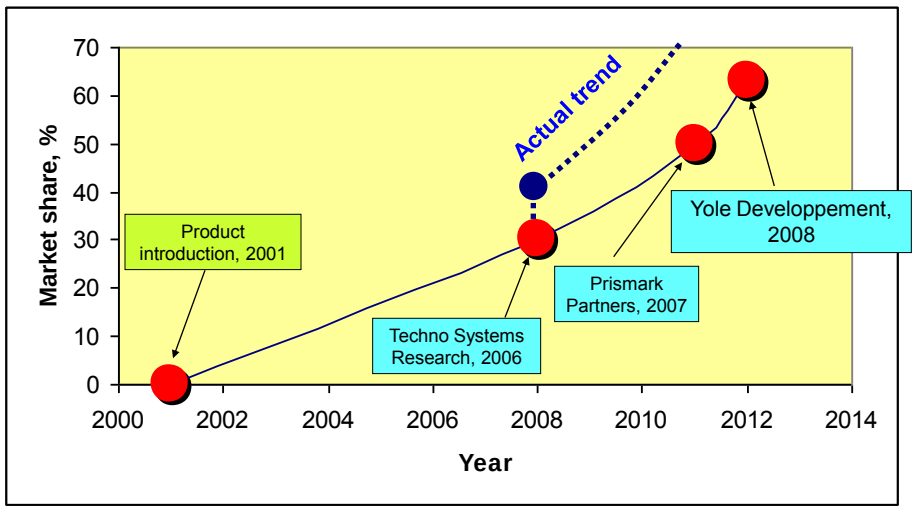
Market Adoption: Imager Wafer-Level Packaging (WLP)



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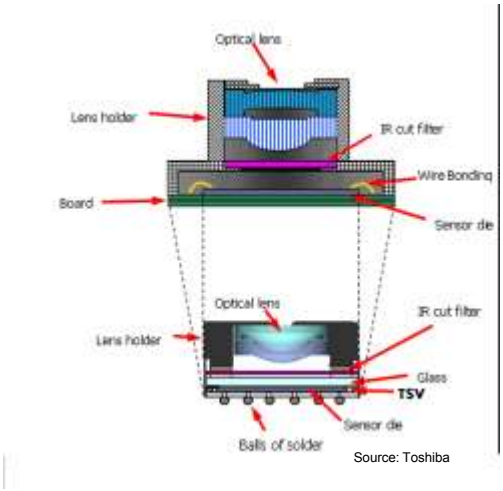
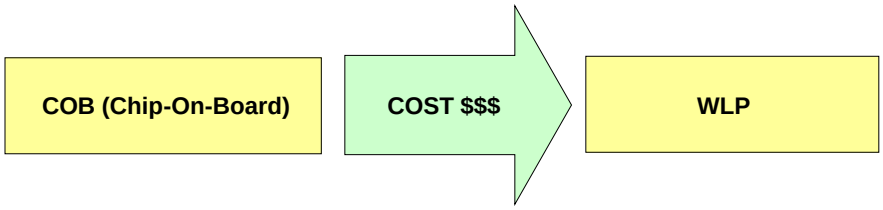
Camera Module Trend



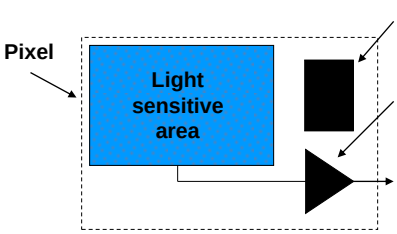
Transition from traditional plastic lenses and barrel to reflowable camera module

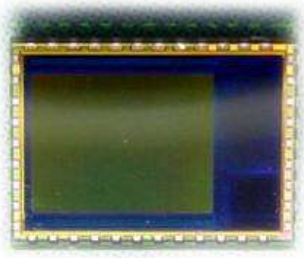
Image Sensor Packaging Trend



- **COB line requires Clean Room infrastructure (camera module assembly yield)**
- **COB requires substrate, connector, flex**
- **Die size shrink (more dice on wafer → WLP cost per die is reduced)**
- **Industry drive for Wafer Level Camera and reflowable camera modules.**

CMOS Sensor



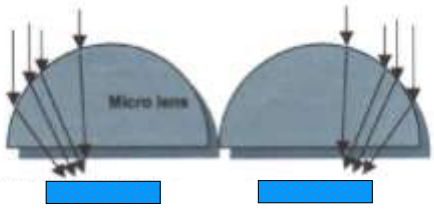


- Multiple sensor configurations
- Lower cost and power
- Integrated electronics
- Variable mode per frame

- Higher noise
- Lower sensitivity (fill factor)

Micro Lenses

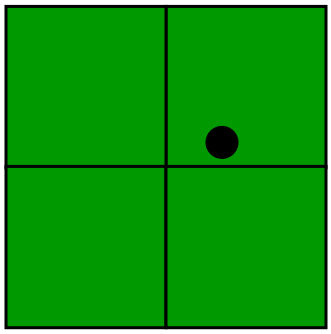
Provide optical compensation for low fill factor of imagers, but…



- Require air space above micro lenses
- Collect particles
- Limit subsequent thermal excursions

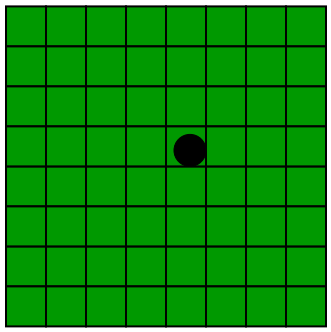
COB Assembly
Smaller pixels - More particle problems

Lower Resolution
Larger Pixels



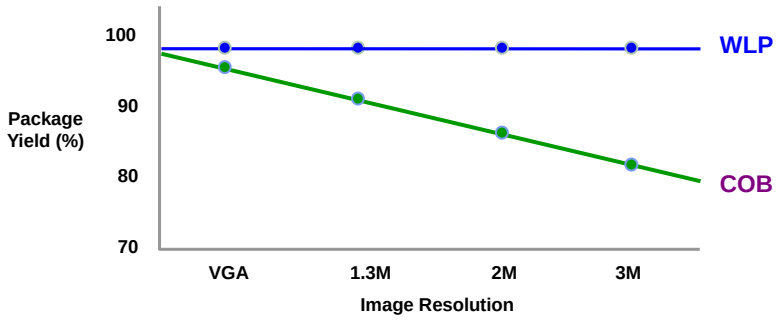
Particle has small effect on pixel

Higher Resolution
Smaller Pixels



Particle has large effect on pixel

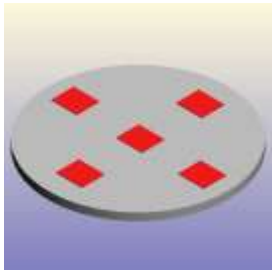
COB vs WLP Module Yield



Particle Contamination During COB Manufacturing Decreases Yield at Higher Resolution

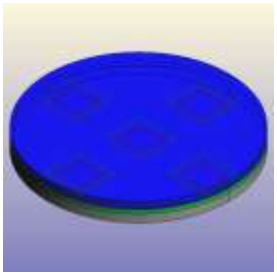
Wafer Level Packaging

WLP “solves” the problem of particle contamination by applying a protective glass cover to the die, while in wafer form, as the FIRST step of the module build process.



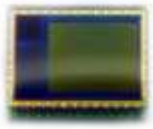
Device wafer

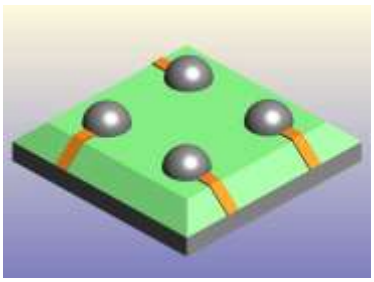
Device wafer plus picture frame seal



Device wafer, picture frame seal and lid wafer

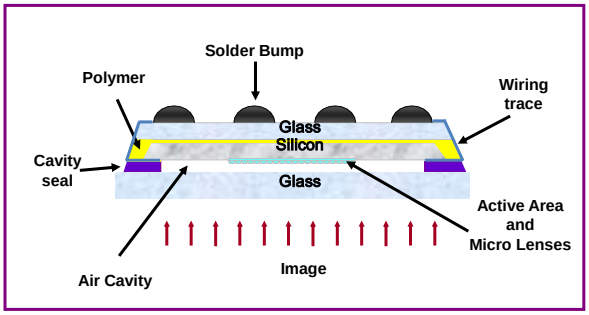
Wafer Level Package: Ball Grid Array interconnect





- Chip size package
- Electrical connection is through embedded leadframe and solder balls
- Entire wafer is encapsulated and then singulated
- Resulting particle-free package can then be built into a module using surface mount assembly techniques

Wafer Level Package: Ball Grid Array interconnect



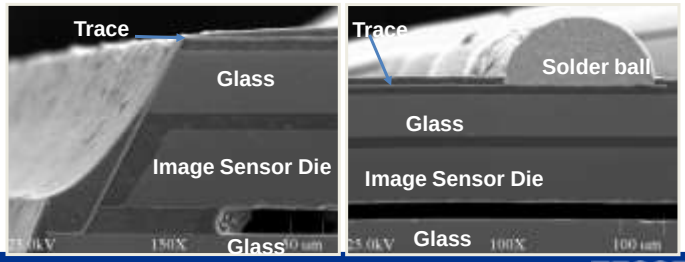


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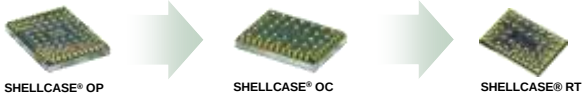
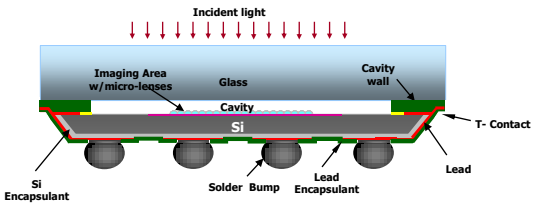
Image Sensor Evolution for WLP

ShellCase WLCSP



2000 2002 2006



In Future: Transition from edge connect to TSV → WLCSP

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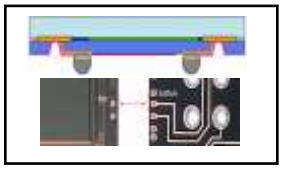
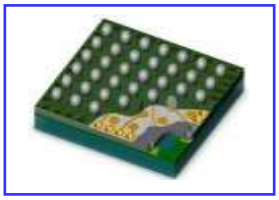
2008: Introduction of TSV type WLCSP



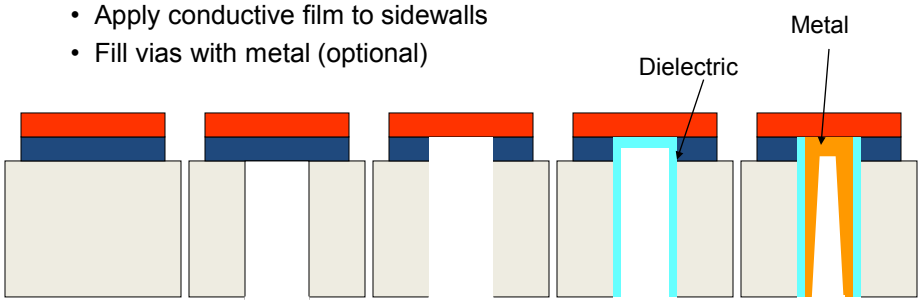
TSV type WLP



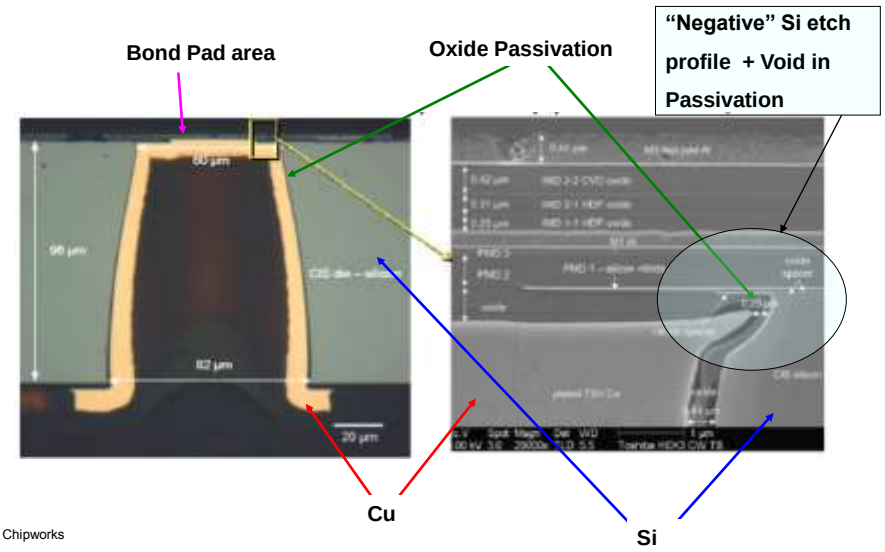
Tessera SHELLCASE® MVP – Through Pad Interconnect

Typical TSV flow

- Etch through thickness of silicon wafer, to oxide stop
- Etch through silicon oxide dielectric underneath bond pad, to metal stop
- Apply dielectric to sidewalls
- Form conductive pipe
  - Apply conductive film to sidewalls
  - Fill vias with metal (optional)

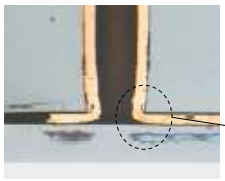


Typical TSV



Source: Chipworks

TSV Thermal Cycling

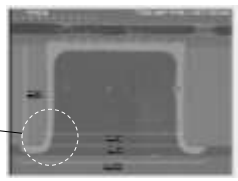


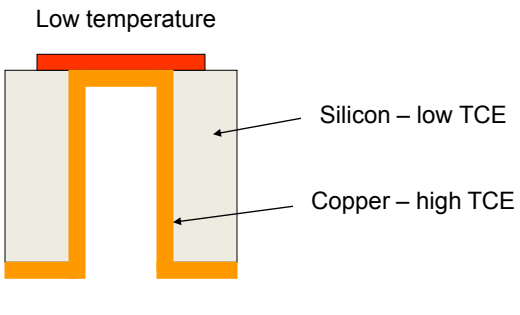
High aspect ratio via

Re-entrant feature

Low aspect ratio via

Sharp angle





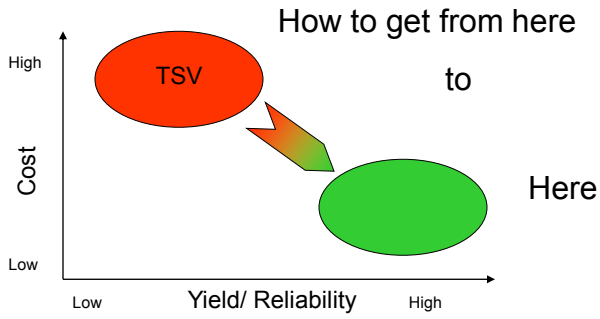
Source: ILETI

Cost and Reliability Barriers

- Semiconductor-based equipment set (expensive)
- Semiconductor-grade materials (expensive)
- Slow throughput (high capital $ / wafer)
- Critical processes all conducted at blind end of high aspect ratio via (low yield)
  - Oxide etching
  - Ohmic contact to back side of bond pad
  - Sidewall passivation and conductive coating
- Sharp changes in section at top and bottom of via (vulnerable to fatigue during thermal cycling)

The Problem with TSV…..

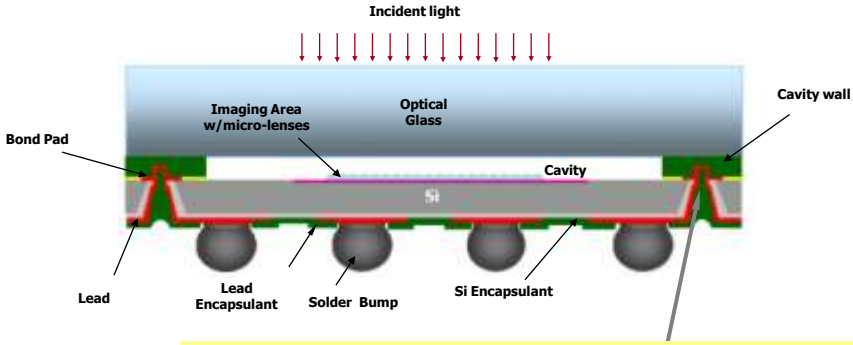
TSVs have never been widely adopted by industry



A New Approach to TSVs

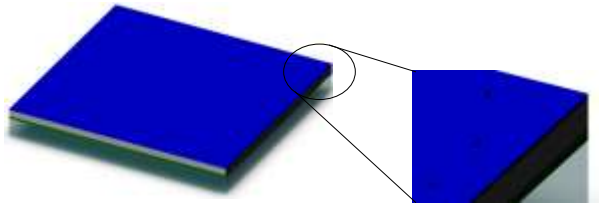
- Low cost Si polymeric passivation
  - Thicker than SiO2 (few microns instead of less than micron).
  - Passivation uniformity
  - No need for very expensive tools (of the shelf coater instead of LPCVD/ PECVD).
- Make TSV structure using PCB tools
  - Laser Drill through Polymer and bond pad
  - High throughput and low cost per drilled Via
  - Of the shelf Laser tool
- Low Cost Lead Metalization
  - No need for Via fill process
- Proven Supply Chain
  - Rely on HVM proven material/ tools

SHELLCASE MVP structure

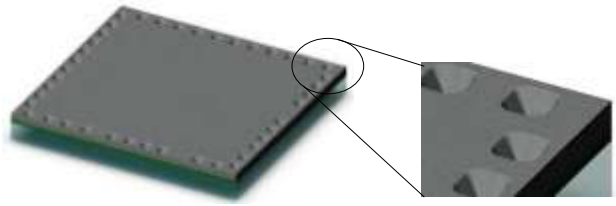


"T- Contact": Through Pad Interconnect

SHELLCASE MVP flow – cont.



Apply PR Via mask



Etch tapered holes through silicon

Source: Tessera

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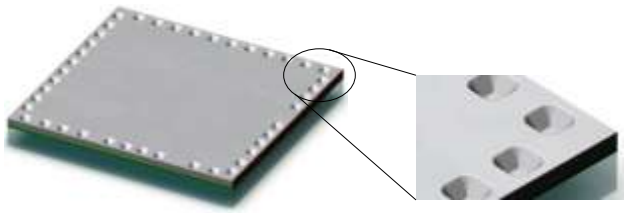
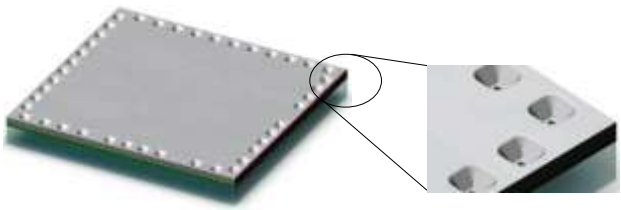
SHELLCASE MVP flow – cont.



Apply polymeric passivation



Laser ablate small via through Si polymeric passivation, oxide and bond pad

Source: Tessera

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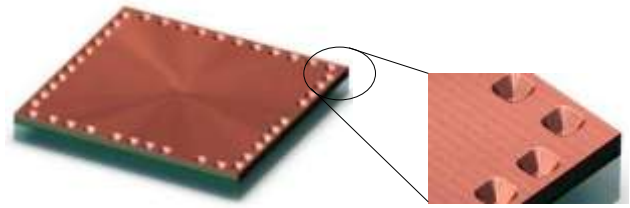
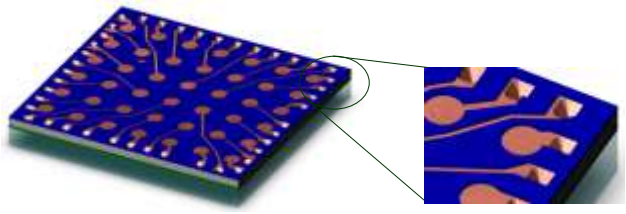
SHELLCASE MVP flow – cont.



Coat with metal



Pattern metal

Source: Tessera

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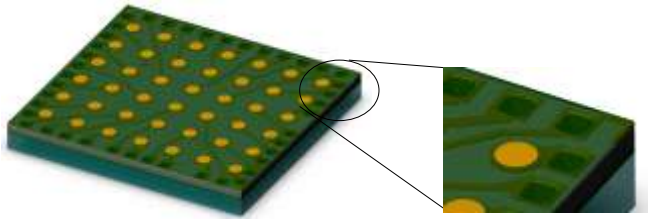
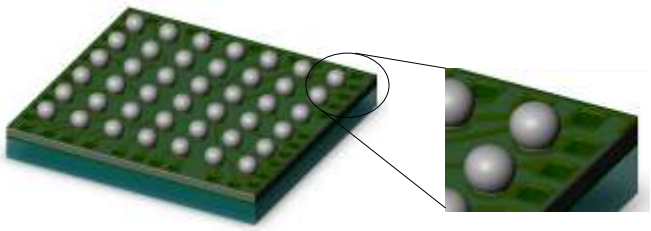
SHELLCASE MVP flow - cont.



Apply and pattern solder mask



Apply solder to form BGA interface

Source: Tessera

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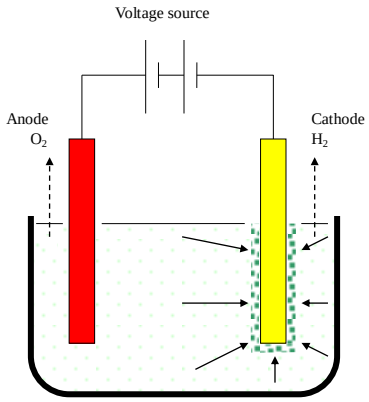
Electrophoretic Paint

Electrophoretic painting is an immersion painting process in which charged paint particles are attracted to an oppositely charged metallic surface. Deposition ceases when the coating forms a dielectric layer.



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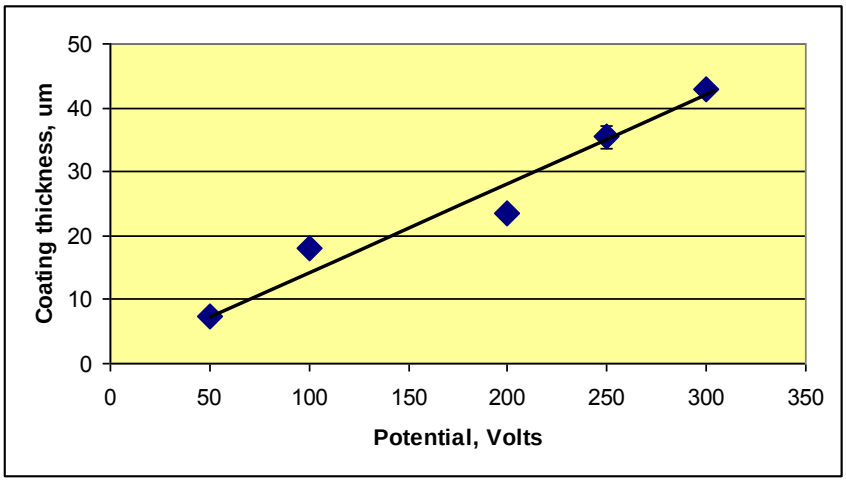
Self-limiting coating thickness Vs applied potential



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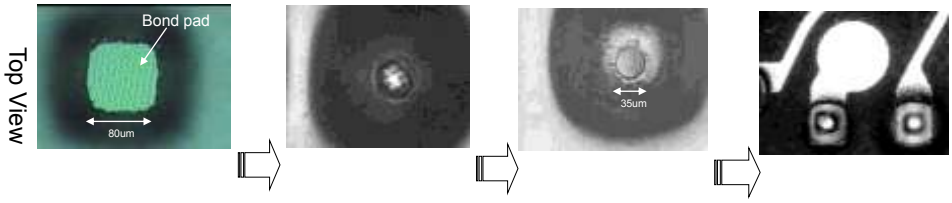
SHELLCASE MVP- process details



Source: Tessera

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SHELLCASE MVP - Reliability Results

Test	Test Conditions	Standard	Duration	Results
Automotive specification				
Moisture soak (pre-conditioning) Level 1 – MSL1	• 125°C / 24hrs • 85°C/85% RH/ 168 hrs • Reflow (peak 265°C) / 3 times	JESD22-A113-D	1 sequence	Pass
Steady state temperature humidity - TH	• 85°C/85% RH	JESD22-A101-B	2000 hrs	Pass
High temperature storage life HTS	• 150°C	JESD22- A103-A	2000 hrs	Pass
Temperature Cycling - TMCL	• -40°/+125° • 32 cycles/ day	JESD22-A104-B	2000 cycles	Pass

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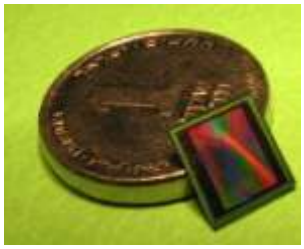
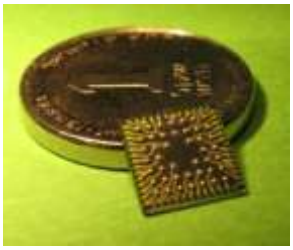
SHELLCASE MVP – Module Level Reliability

Test	Test Conditions	Standard	Duration	Results
Low Temperature Operation	• -20°C	Cell Phone Maker #M/ #N	96 hrs - operational	Pass: Optical and functional
High Temperature Operation	• 80°C	Cell Phone Maker #M/ #N	96 hrs - operational	Pass: Optical and functional
Thermal Shock	• +80°C, 30min • - 20°C, 30min	Cell Phone Maker #M/ #N	35 Cycles	Pass: Optical and functional
High Temperature and Humidity	• 80°/95%RH	Cell Phone Maker #M/ #N	96 hrs - operational	Pass: Optical and functional
Vibration Test	• 20-2000 Hz • 0-8gr • 3 axis, 15 min per plane •Load 100gr	Cell Phone Maker #M/ #N	1 Cycle	Pass: Optical and functional
ESD	• +/- 0.5KV, 1KV, 2KV	Cell Phone Maker #M/ #N	1 Cycle	Pass: Optical and functional

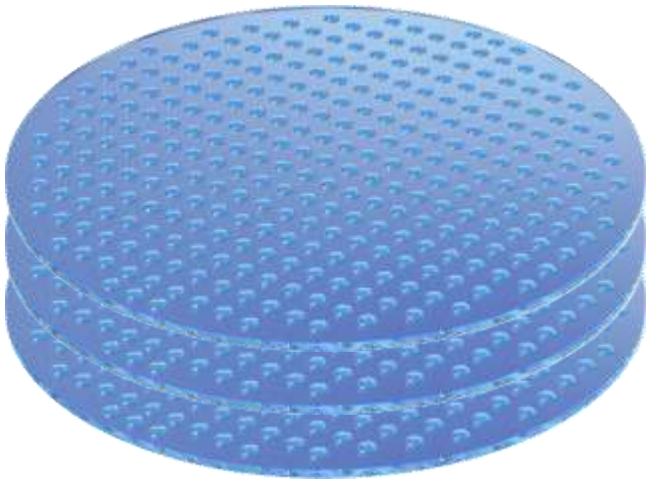
SHELLCASE MVP: WLCP for CMOS Image Sensors

- Low cost, high yield, wafer level package
- Exceptional reliability – meet MSL 1 and exceeds automotive specifications
- Micro Via Pad interconnect – true TSV technology



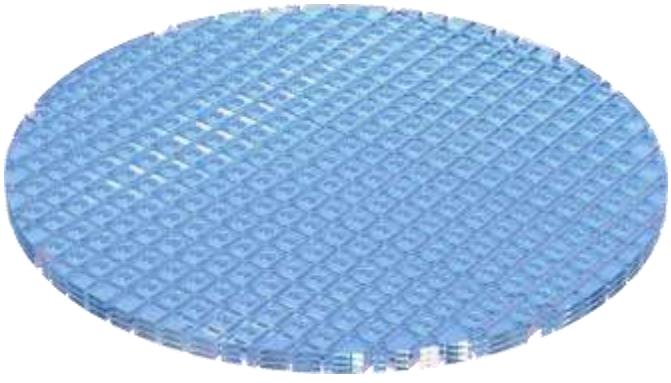


Wafer Level Camera : Process Overview



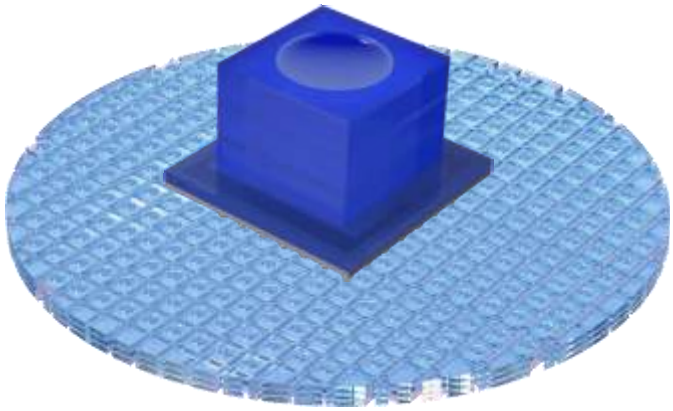
Step B: Wafers aligned and bonded

Wafer Level Camera : Process Overview



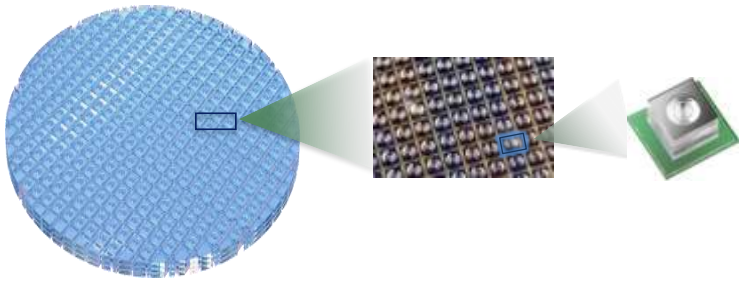
Step C: Wafers singulated into individual optical elements

Wafer Level Camera : Process Overview



Step D: Assembly optical elements on image sensors

OptiML WLC Technology



Revolutionizing the Camera Module

Conventional camera phone

OptiML™ wafer level technology

Conclusions

- Packaging of image sensors at the wafer level
  - Cost-effective solution
  - Eliminates multiple camera module elements
  - Allows reflowable camera module
- Low adoption rate of TSVs
  - High cost
  - Low yield
  - Low reliability
- Leveraging PCB industry materials and tool set greatly decreases the cost of making TSVs
- SHELLCASE MVP is the TSV solution for WLP of Image Sensors
  - Low cost
  - Reliable

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Thank You

bhaba@tessera.com