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# THIN IS IN

## Thinning of IC chips

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Jan 28, 2010  
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### CONTENT

- Industry Demand for thinness
- Method to achieve ultrathin dies
- Mechanical testing of ultrathin die
- Die strength variation source
- Methods to achieve strong ultrathin dies
- Assembly of Ultrathin dies
  - Die Attach Films
  - Interconnection

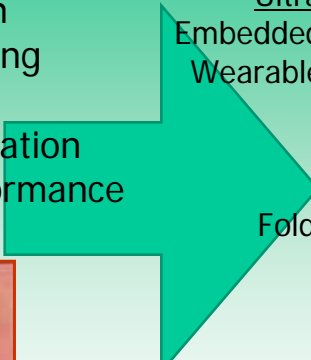


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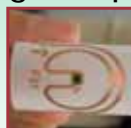

### Reasons to go thin


- Decrease street width
- Stackable 3D packaging
- Smart cards
- Improved Heat dissipation
- Better electrical performance
- Higher speeds




### Ultra Paper thin

- Embedded packaging
- Wearable packaging
  - Appliques
  - Skin patch
- Implantable
- Foldable 3D die
  - cylinders
  - cones
  - origami



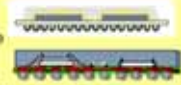
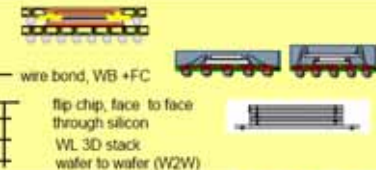
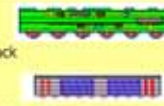



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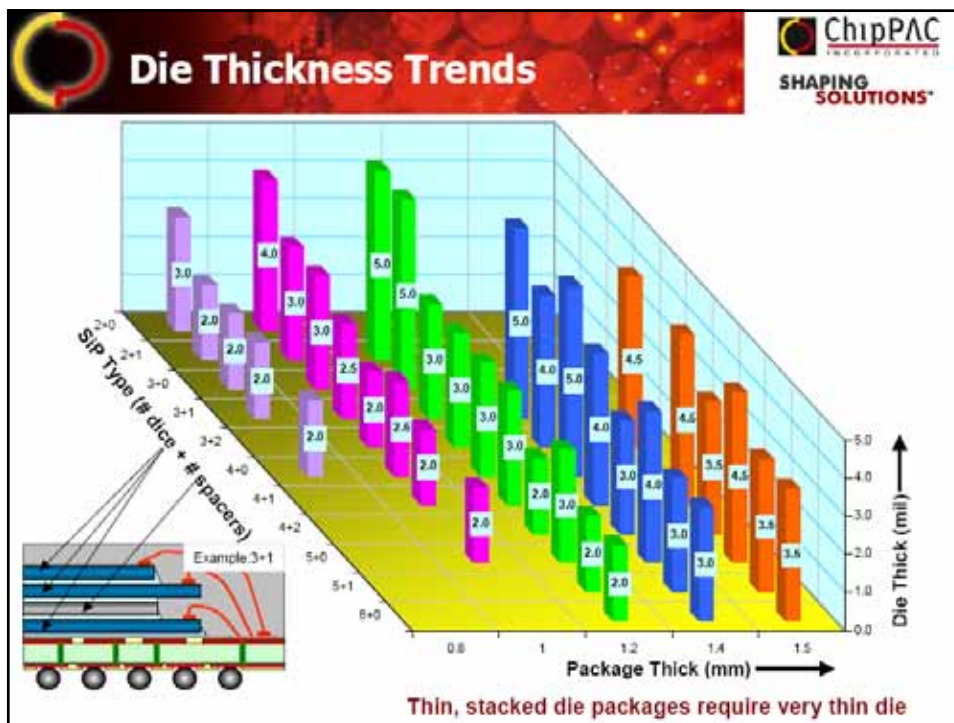
## iNEMI Roadmap

### International Electronic Manufacturing Initiative

Chip / Component Configuration	Technology
<p><b>Side by Side Placement</b></p>	<p>Substrate: organic laminate, ceramic, glass, silicon, leadframe</p> <p>Chip interconnection: wire bond and/or flip chip</p> <p>+ passive components</p> <p style="text-align: right;">└ integrated into the substrate discrete (CSP, SMD)</p> 
<p><b>Stacked Structure</b></p>	<p>PoP PIP</p> <p>stacked die — wire bond, WB + FC</p> <p>chip to chip / wafer</p> <p style="text-align: right;">└ flip chip, face to face through silicon WL 3D stack wafer to wafer (W2W)</p> 
<p><b>Embedded Structure</b></p>	<p>Chip in PCB / polymer — single layer multi-layer 3D stack</p> <p>WL thin chip integration — single layer stacked functional layers</p> 



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Year	Volume Production (um)	Development (um)
2005	~300	~100
2007	~100	~75
2009	~100	~60
2011	~60	~50

Fig.3.2. Bumped wafer with 50umSi thickness

STATSchipPAC  
ECTC 2009  
50um flip chip

Fig. 3.1 Bumped wafer thinning trend

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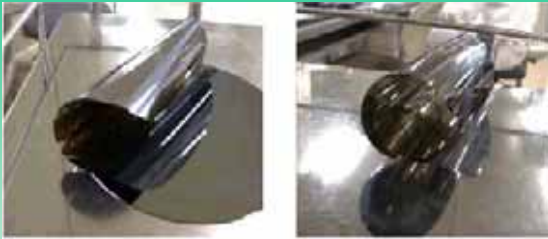
## Conventional Flow for Wafer Thinning (DAG)


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**DAG Results:**  
**LOW YIELD**

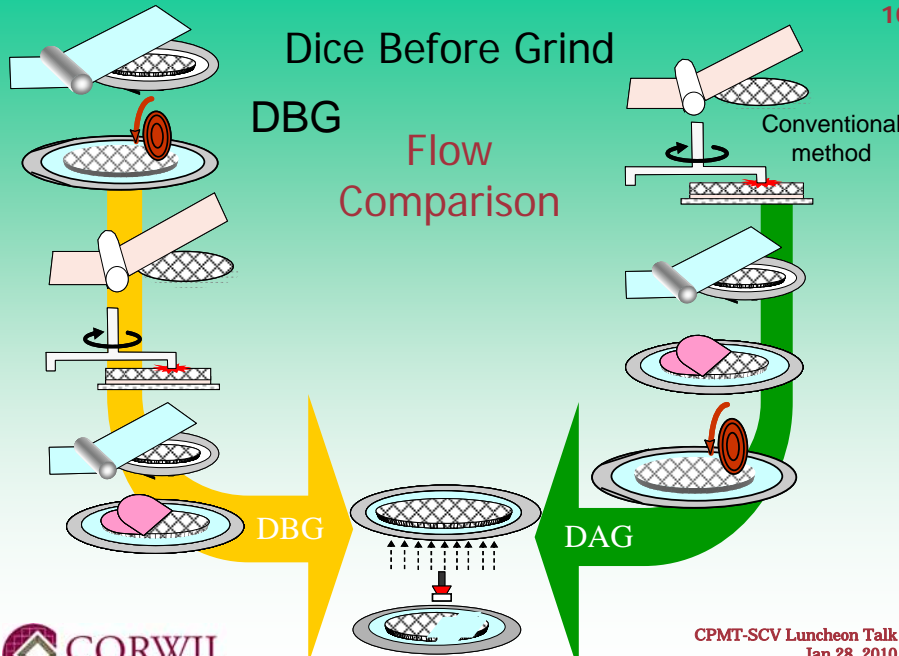
- Warpage & curl
- Non conformal
- Transport challenge
- Storage challenge
- Lamination challenge




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**Dice Before Grind**  
**DBG**      **Flow Comparison**      **Conventional method**




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## Dice Before Grind Method

**Singulation Depth**  
**Rough grind 300 grit**  
**Fine grind >2000**  
**Removed thickness**  
**Final thickness**  
**Front side tape**  
**Trench depth**




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## Results


- No Wafer Warpage & curl
- No Wafer Breakage
- Conformal
- Transportable
- Storable
- Easy to Laminate
- Easier to bond/debond




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32um after DBG with Polygrind wheel



Sidewall Flaws



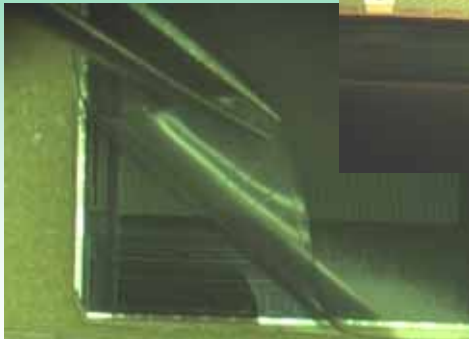
Punctures




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15um silicon die  
attache to package  
by 25um DAF.  
20um gold wire bond







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### Thin die Strength Characterization Techniques

**2 Point Test**

**3 Point Test**

**4 Point Test**

Strength =  $\frac{3F \cdot \text{length}}{2 \cdot \text{width} \cdot \text{thickness}^2}$

Strength =  $\frac{3F \cdot \text{length}}{\text{width} \cdot \text{thickness}^2}$

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### Fracture strength Test Methods

**Point Load test (PLT)**

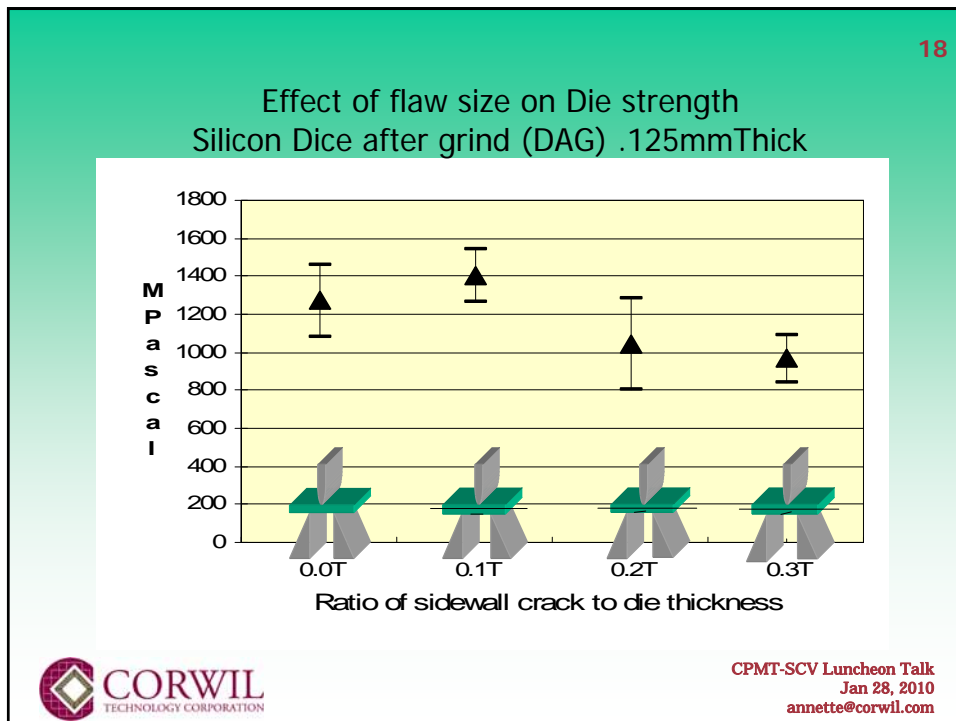
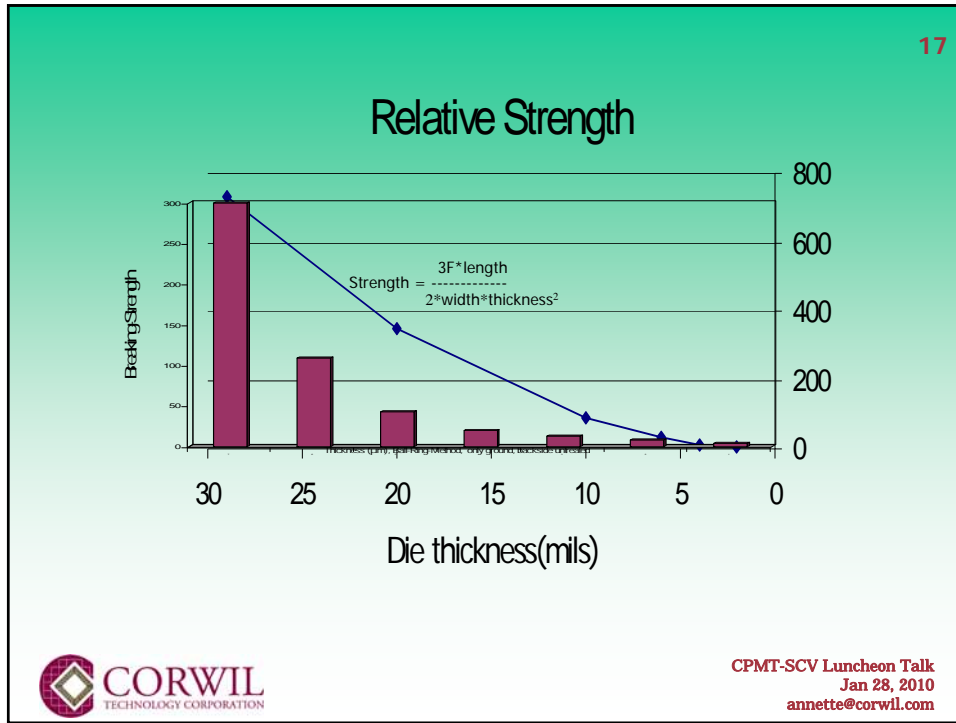
**Plate on Elastic Foundation Test (PEFT)**

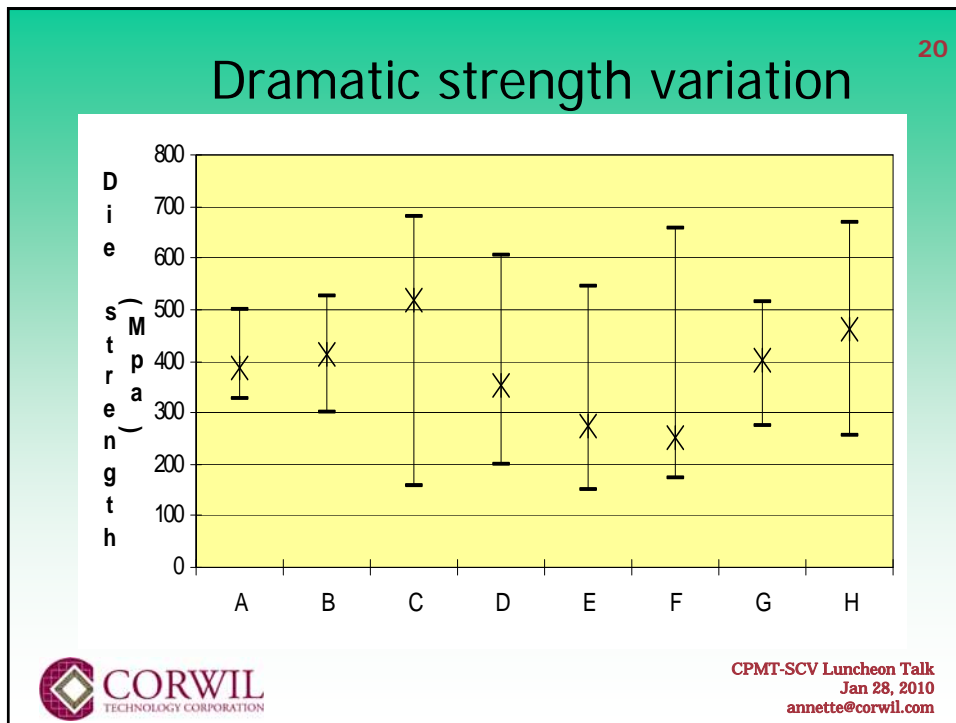
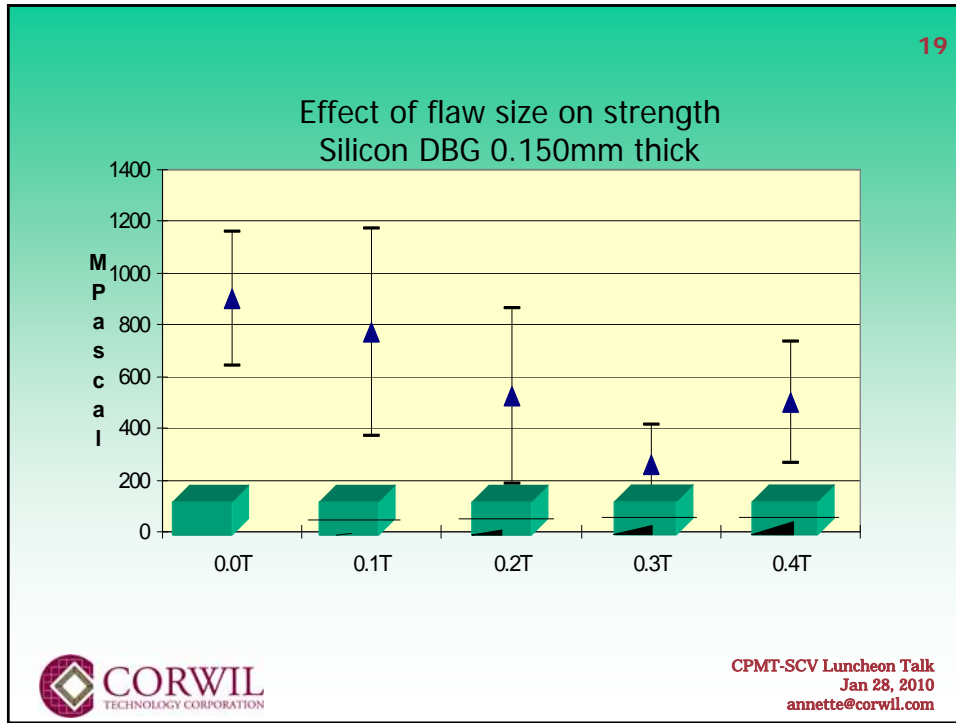
M.Y. Tsai, ASE et al

**Ball & Ring Test**

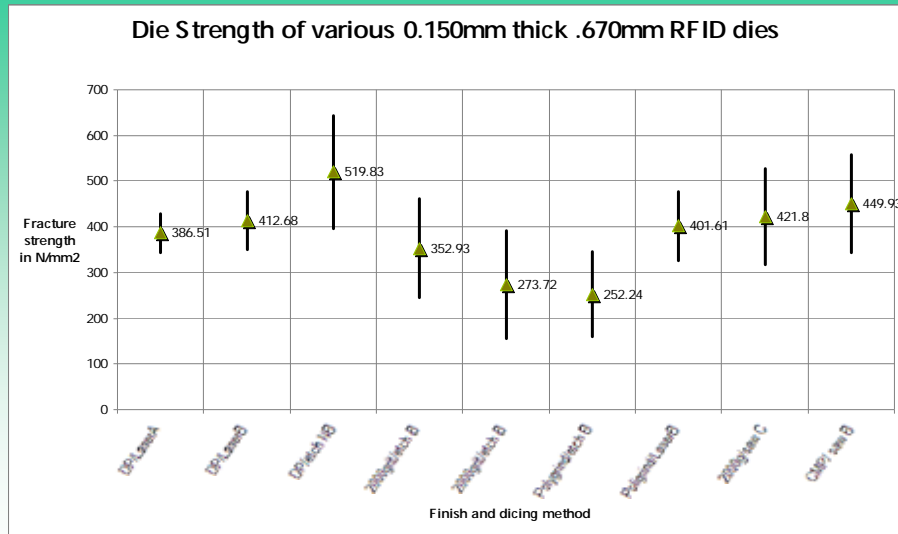
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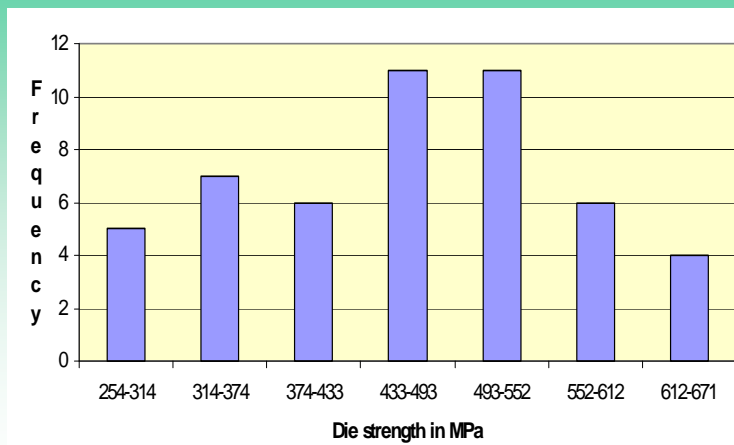
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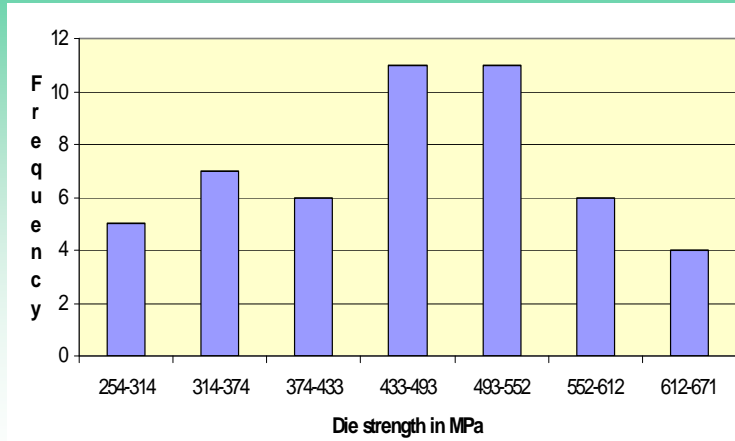
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### Distribution plot -sample size 50 Group H (CMP-blade saw)



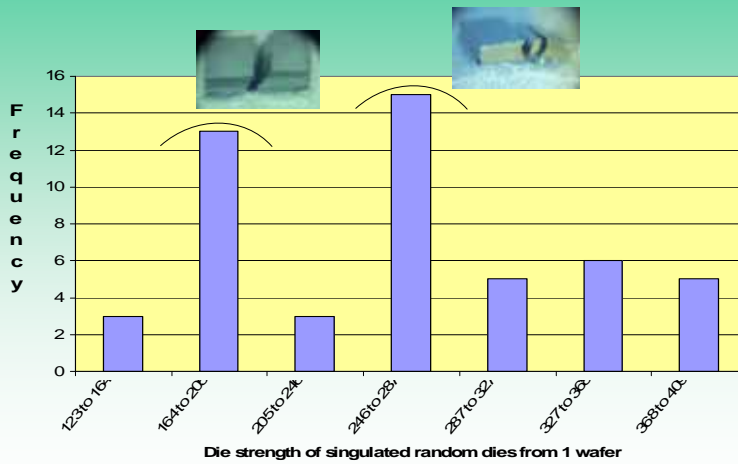
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Distribution plot -sample size 50  
Group H (CMP-blade saw)



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Distribution plot of 2000grit etched group



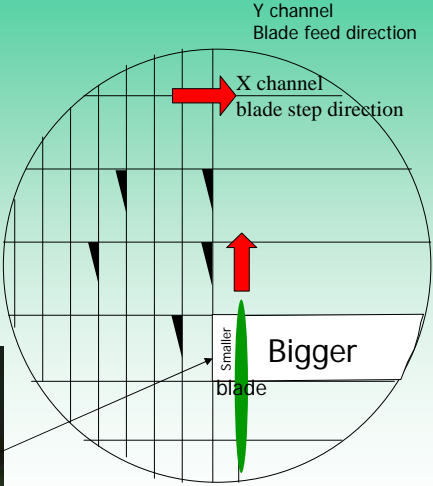
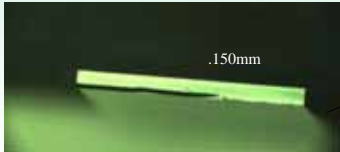
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### Examples of Surface defects

Most common chipout is last side rip of the Smaller piece

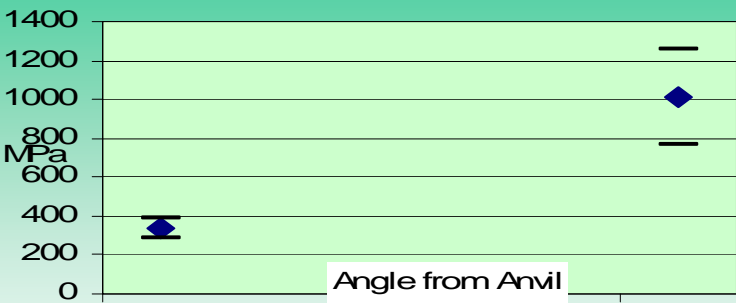
- Snaps off
- Shifts away from blade
- Vibrates more

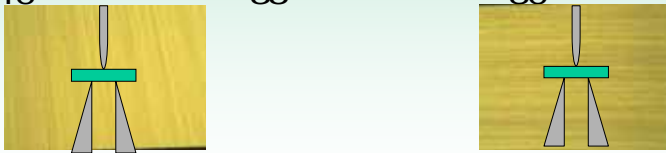
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### Large fracture strength variations within 1 wafer



Angle from Anvil	Fracture Strength (MPa)
-10	~300
35	~750
80	~1000



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## Laser generated roughness

Laser ablation

The diagram illustrates the laser ablation process. A pulsed laser beam is directed at a silicon (Si) substrate. A transparent dielectric foil is positioned above the substrate. The process generates dust and particles, which are captured by a vacuum exhaust system. The resulting sidewall has a rough, porous structure. A scanning electron microscope (SEM) image shows the sidewall with a 20 µm scale bar. A red double-headed arrow indicates the sidewall height, labeled as 0.250mm.

Vakuumentsaug  
Dust, Particles

Pulsed Laser Beam

Si

Transparent Dielectric Foil

20 µm

SIDEWALL 0.250mm

infineon  
Werner Königler

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## Laser scribe and break

The top SEM image shows a laser scribe on a silicon substrate, creating a series of vertical, parallel lines. A red double-headed arrow indicates the height of the scribe, labeled as 0.250mm. The bottom SEM image shows the laser scribe and break process, where the scribe has been broken, resulting in a rough, expanded surface. A red double-headed arrow indicates the height of the broken scribe, labeled as 0.250mm.

SIDEWALL 0.250mm

Laser scribe and break

SIDEWALL 0.250mm

Laser Scribe and expand

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PERSONAL PREFERENCE - VISUAL

REJECT

ACCEPT

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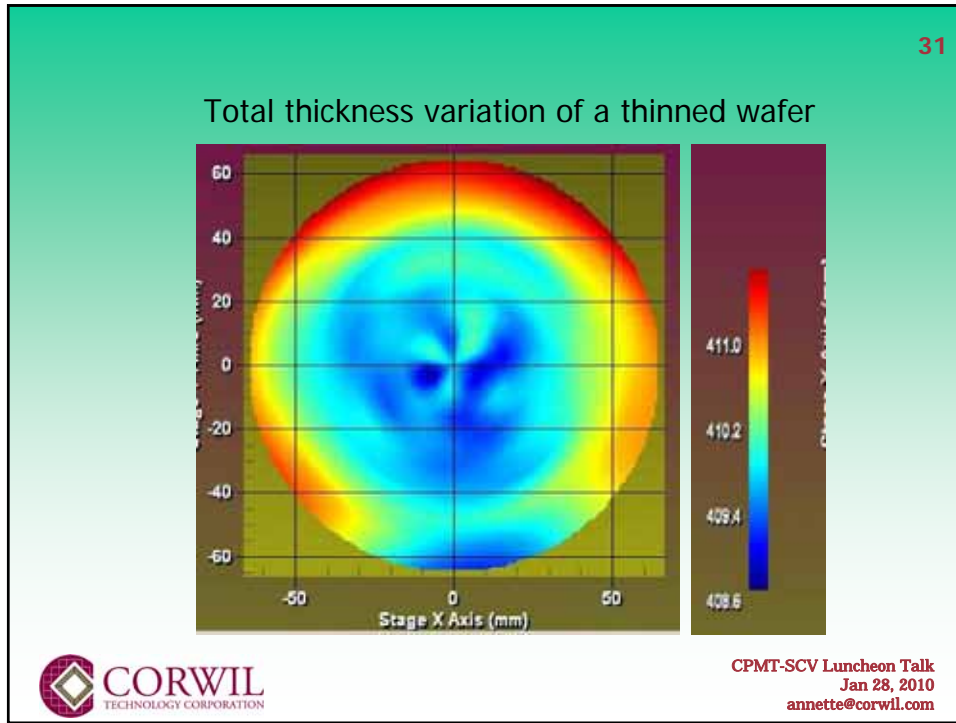
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Examples of Surface Flaws

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TTV HAS MAJOR IMPACT ON ULTRATHIN DIE

Wafer Thinning Target Thickness	8 $\mu\text{m}$ TTV to thickness ratio	TTV effect on 3 pt bend die strength
0.150 mm	5.3% (0.146-0.154mm)	10.6%
0.100 mm	8% (0.096-0.104mm)	16.0%
0.050 mm	16% (0.046-0.054mm)	32.0%

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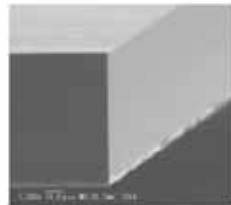
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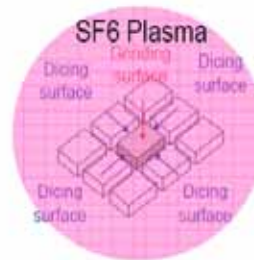
- Side etching on DBG dies  
– Realizes "ideal chip"



DBG chip without Etching



After 20um dry etch



Source: Disco  
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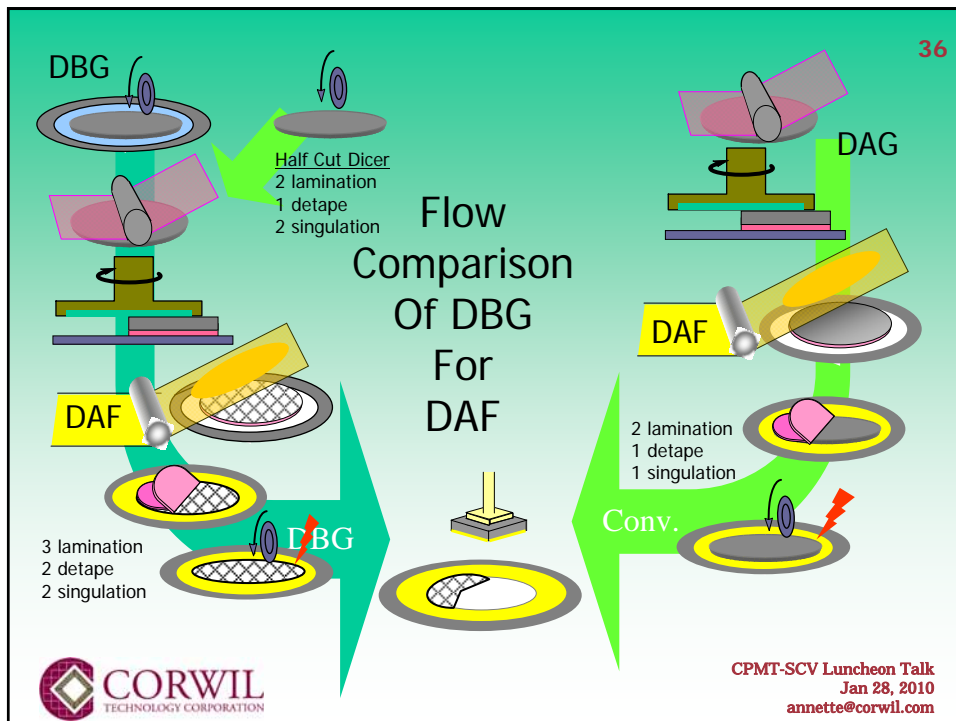
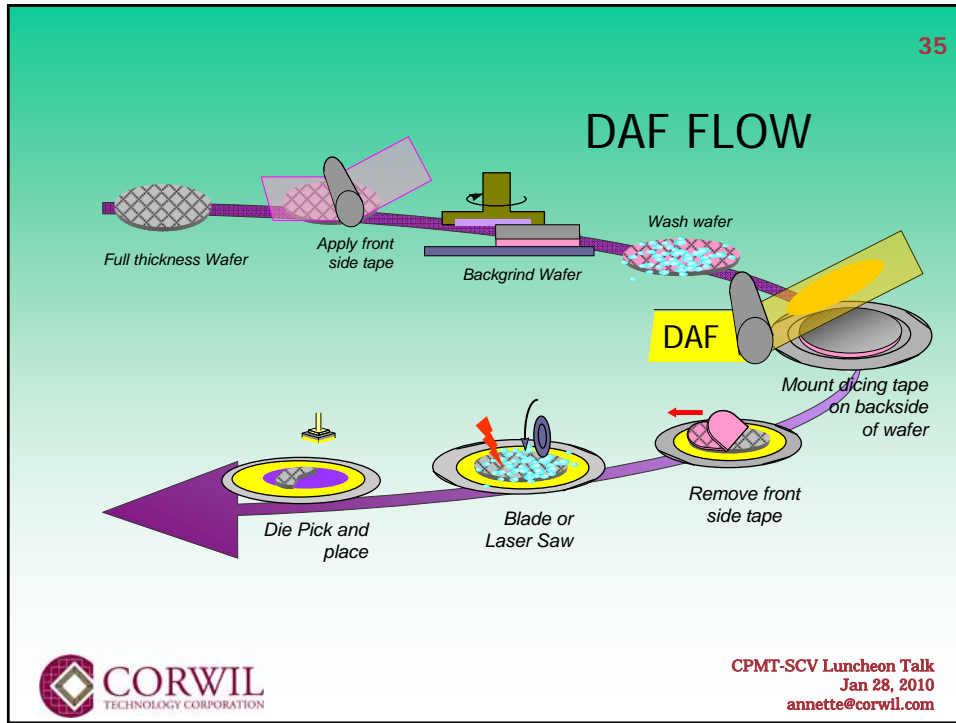


## 5 sided smoothening

	Surface	Side	Back Side	Edge
Conventional				
DBG				
DBG+CMP				
RIE-DBG+CMP				



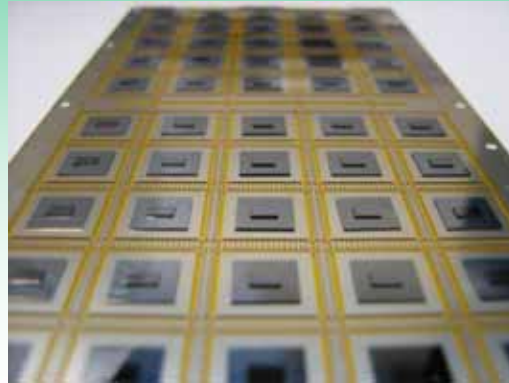
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DAF services are easily integrated into existing line

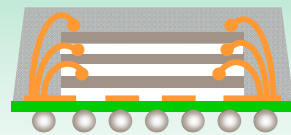
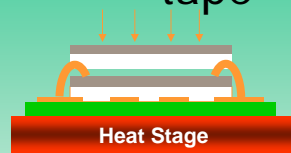
- automated thin wafer grind
- automated DAF mounting
- automated dicing with DAF
- automated die attach with DAF



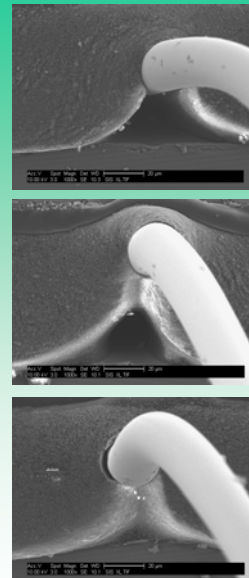
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Film Over Wire (FOM) tape



Adhesive with viscosity so low that it will wrap around gold wire loops when heated to 150°C



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processed. 20um diameter Au wire was used for wire bonding process.

After bonding Au wire on bottom chips onto PCB, 2nd chip and 3rd chip were attached in sequence. Other assembly processes were performed to complete SCSPs. Figure3 shows the cross section of actual 3 die stack CSP and used dies, DAF and FOW (Film Over Wire).

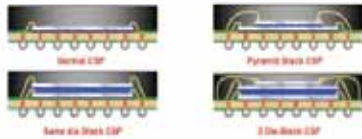


Figure 1 : Schematic structure of each SCSP.

Structure of Pkg	die information			Dicing method		
	width x length x thickness (mm)	bottom	middle	top	Lower substrate	Stable base
Normal CSP	1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25	no	no	no	no	no
Pyramic stack CSP	1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25	no	no	no	no	no
Same die stack CSP	1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25	DAF 20um	POW 40um	no	no	no
3 Die-Stack CSP	1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25 1.0x1.0x0.25	DAF 20um	POW 40um	DAF 25um	no	no

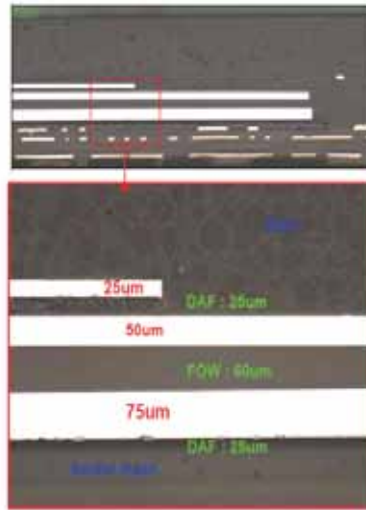


Figure 3 : Cross section view of 3 die SCSP. Amkor



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Half Cut Dicer  
2 lamination  
1 detape  
2 singulation



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## DAF FLOW

Full thickness Wafer  
Apply front side tape  
Backgrind Wafer  
Wash wafer  
DAF  
Mount dicing tape on backside of wafer  
Remove front side tape  
Blade or Laser Saw  
Die Pick and place

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## Reasons to use DAF

1. NO VOIDS
2. NO PINHOLES
3. NO BUBBLES
4. NO DIE TILT
5. UNIFORM BONDLINE
6. NO FUMES
7. HIGH THROUGHPUT

1. Memory DRAM/SRAM
2. High adhesion to all surfaces
3. Pass MSL; Pass Reliability testing
4. Strength improvement for ultrathin die
5. Compact Medical prosthetics
6. For laminating ultrathin dies
7. Vertical Stacking

paste

DAF

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## DAF LIMITATIONS

Suppliers

1. Hitachi-
2. Lintec Adwill (UV)
3. Nitto Denko
4. Nippon Steel
5. Hysol/Ablestik

1. Not quite DBG compatible
2. Not electrically conductive
3. Not thermally conductive
4. Not required for non stack pkg



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## Ultrathin die Interconnect

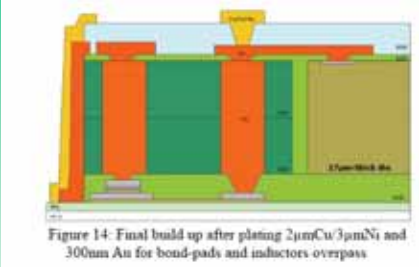


Figure 14: Final build up after plating 2µmCu/3µmNi and 300nm Au for bond-pads and inductors overpass

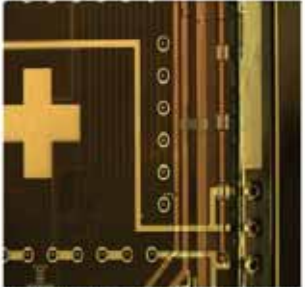


Figure 16: Microscope picture of the final build up after plating 2µmCu/3µmNi and 300nm Au. Pads of the chip are redistributed to the Cu pillars.





Figure 15: FIB illustration of advanced 10µm diameter and 20µm-thick Cu pillars (HARVT) interconnected with MI with a 7.5µm-VIA and M3 with a 30µm VIA.

17µm die IMEC, Belgium  
140µm package thickness



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## Ultrathin bumping is after thinning



Figure 7. Cross-section of 50µm Thick Die Assembly after Underfill

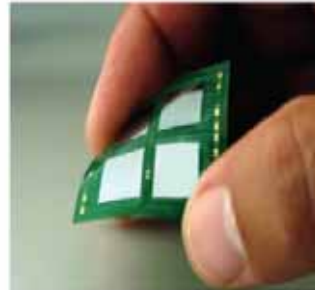


Figure 8. Example of the flexibility of the thinned die on flex

Applied Physics Lab  
Johns Hopkins Univ.  
ECTC 2009



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## Summary of Ultrathin Technology

- Dice Before Grind
- Thickness as low as 10µm available
- High flexibility
- High scatter of die strength
  - After DAG laser or blade saw
  - After DBG
  - Independent of test methods
  - Predictable by 5 side inspection
- Chemical Smoothing of 5 sides
  - Decreases scatter dramatically
- Die attach using DAF
  - 10µm thickness available
- Interconnect
  - Metal patterning
  - Bump (Bump after thinning)



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# THANK YOU!!

Finn Wilhelmsen

Robert Corrao

Dan Miranda

Precision Wafer Thinning and Dicing Group  
CORWIL Technology.

Ron Koepp

IMPINJ



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