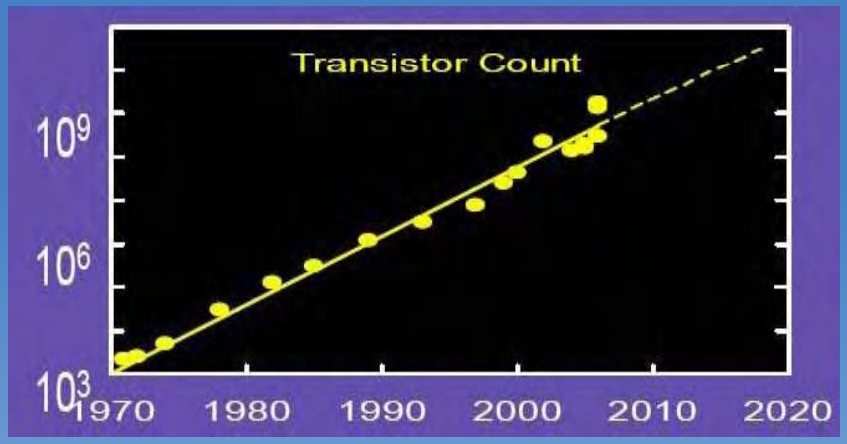
3D IC Integration:

The next generation of electronics

IEEE Santa Clara Valley CPMT Society Chapter
March 10, 2010

Moore's Law 40 Year Trend

1,000,000 times improvement

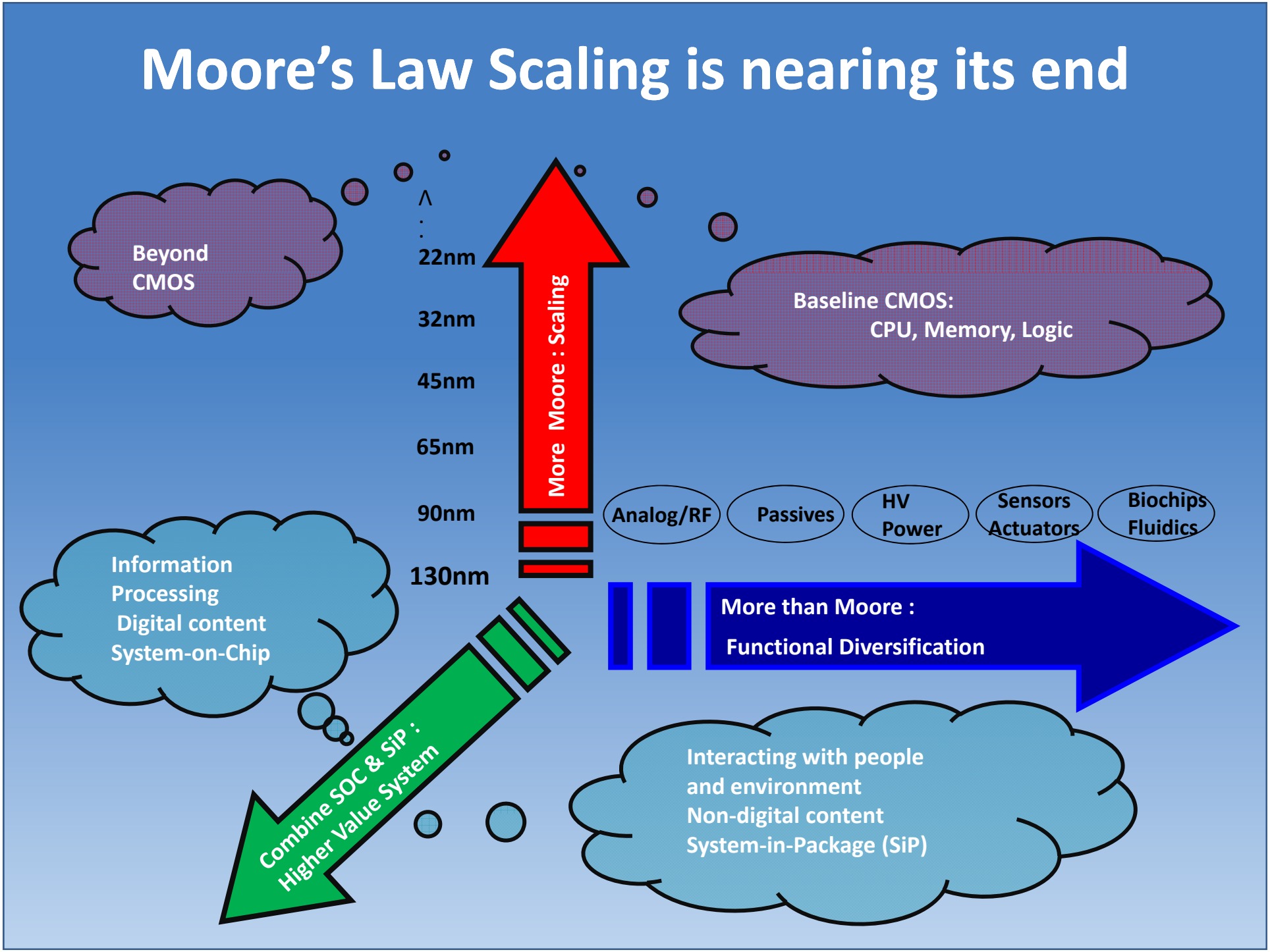


The only activities of mankind that have even come close to this achievement have been enabled by progress in electronics.

Progress was in Predicted Directions

- For 40 years we knew what was coming next and the path to progress understood
  - Increase parallelism to reduce cost
    - Shrink geometries
    - Improve designs for higher density
    - Increase wafer size
  - Focus was on design and fab

Moore's Law Scaling is nearing its end



Where is Industry Going?

Until this decade progress was paced by:

- Advances in manufacturing processes
- Advances in design tools
- New Materials
- Advances in test equipment and methodology

3D integration has been a contributor but not a key enabler

All of this will change as the era of 3D Electronics arrives

The 3rd dimension will be *the* key enabler in maintaining the price elastic growth of the electronics industry

The Consumer dominates the Market and the Market makes the decisions

What does the Consumer want?

1. Lower cost
2. Higher performance
3. Longer battery life
4. Innovative features
5. Connectivity (wireless)
6. Smaller size
7. Lighter weight
8. Less heat generation
9. Short time to market

The Consumer dominates the Market and the Market makes the decisions

What does the Consumer want?

The only path to deliver what the consumer demands is through 3D System Level integration

-----This presents many challenges

8 Less heat generation
9 Short time to market

Functional Diversification and "More than Moore" are driving rapid change in Packaging Technology

Everything is changing:

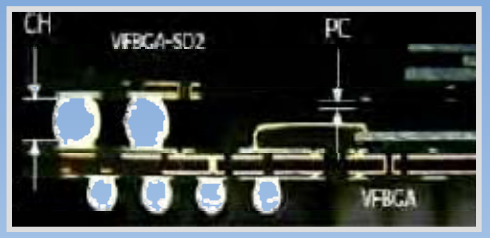
- Architectures
- Materials
- processes
- equipment

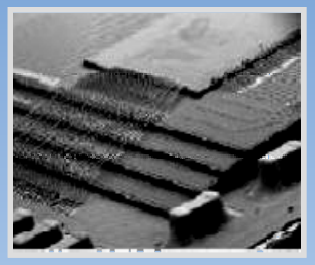
The Fundamental Changes taking place in the industry are both the driver of 3D integration and the result of its successful adoption

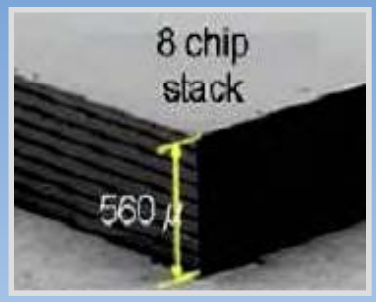
Driving forces for 3D Integration

Near-term:

- *Miniaturization (reduced volume and weight)*
- *Higher performance*
- *Lower power*
- *Mixed-functional integration*
  - Camera modules, Stacked memory, SiP / RF modules, MEMS / Sensors and more







Package on Package (POP) **Stacked Die** **3D IC**

Driving Forces for 3D Integration

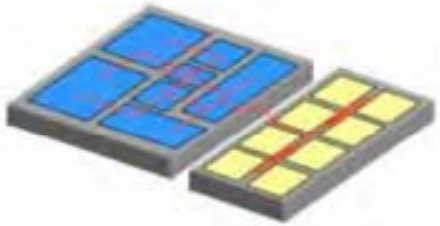
Long-term:

- *Continued improvement in all parameters in near term driving forces*
- *Cost reduction*
  - **Design tools**
  - ***Reduced Test cost***
  - ***Competitive yield***
  - ***Reduced materials cost***
  - ***Increased equipment throughput***

Driving force for 3D Integration

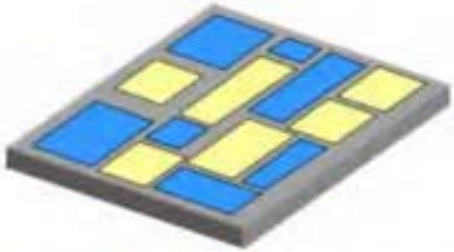
Why 3-D?

"More than MOORE"



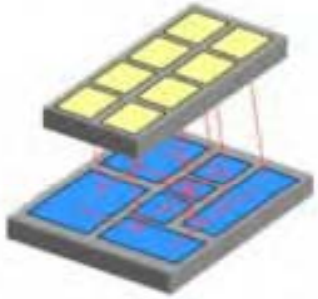
2D interconnect:

- Large form factor
- Long lines / shared bus



SOC solution:

- Reduced system size
- Increased performance
- Increased device cost



3D stack:

- Reduced system size
- Short interconnects
- Reduced packaging cost

EMC3D Estimations	
3.8mm X 2.9mm	
15%	Size Reduction
30%	Power/signal Improvement
5%	Cost Increase
35%	Size Reduction
40%	Power/signal Improvement
45%	Cost Reduction

What drives cost?

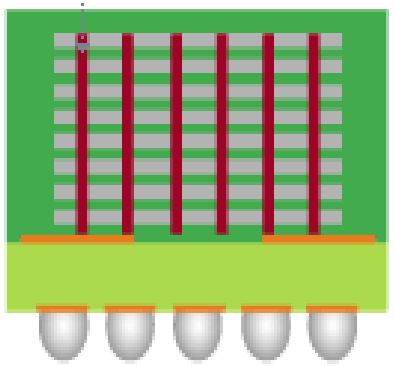
Factor	Conventional	WL-3D Integration
Materials	Lower cost but more material	+
Equipment	Less expensive with lower throughput	+
Labor	Lower parallelism in equipment requires more labor	0
Yield	Advantage disappears with learning curve	=

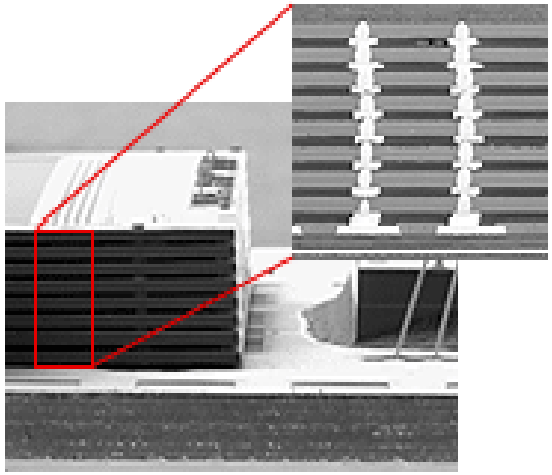
Every new packaging technology starts with a cost penalty and is ultimately adopted due to cost advantages.

3D Integration is not a new Vision

Cross-section

Through Silicon Via (TSV)





- Through Silicon Via Interconnection
- Micro-Bump Flip Chip Bonding
- Chip Direct (Cu Bump) Bonding

- High Density
- High Speed, High Performance
- Lower Profile
- Smaller Form-factor
- Less Power, Less Noise

※ High Density Storage, High Speed 3D DRAM, High Performance 3D SIP

3D Integration is not a new Vision

"we are at the doorstep of the largest shift in the semiconductor industry ever, one that will dwarf the PC and even the consumer electronics era".

Dr Chang-Gyu, Samsung April 2007

There are still some who think 3D is not ready for the mainstream

3-D devices based on TSVs, mainly CMOS image sensors, MEMS, and, to some degree, power amplifiers are shipping today. However…

- IBM has produced a power amplifier based on TSVs and several R&D processor projects with 3-D designs but a production-worthy device is not expected until 2012.
- Intel has not found a ''killer application'' for 3D.

3D Integration Presents Many Challenges

• Test access	⇒	▪ Bist chips in SiP
• Assembly yield	⇒	▪ Learning curve
• Interfacial adhesion	⇒	▪ New materials
• Thermal management	⇒	▪ Phase change microfluidics
• Stress management	⇒	▪ New materials
• Fracture toughness	⇒	▪ New materials
• Reliability	⇒	▪ Design margins

They all have solutions

New Materials will be required

Many are in use today

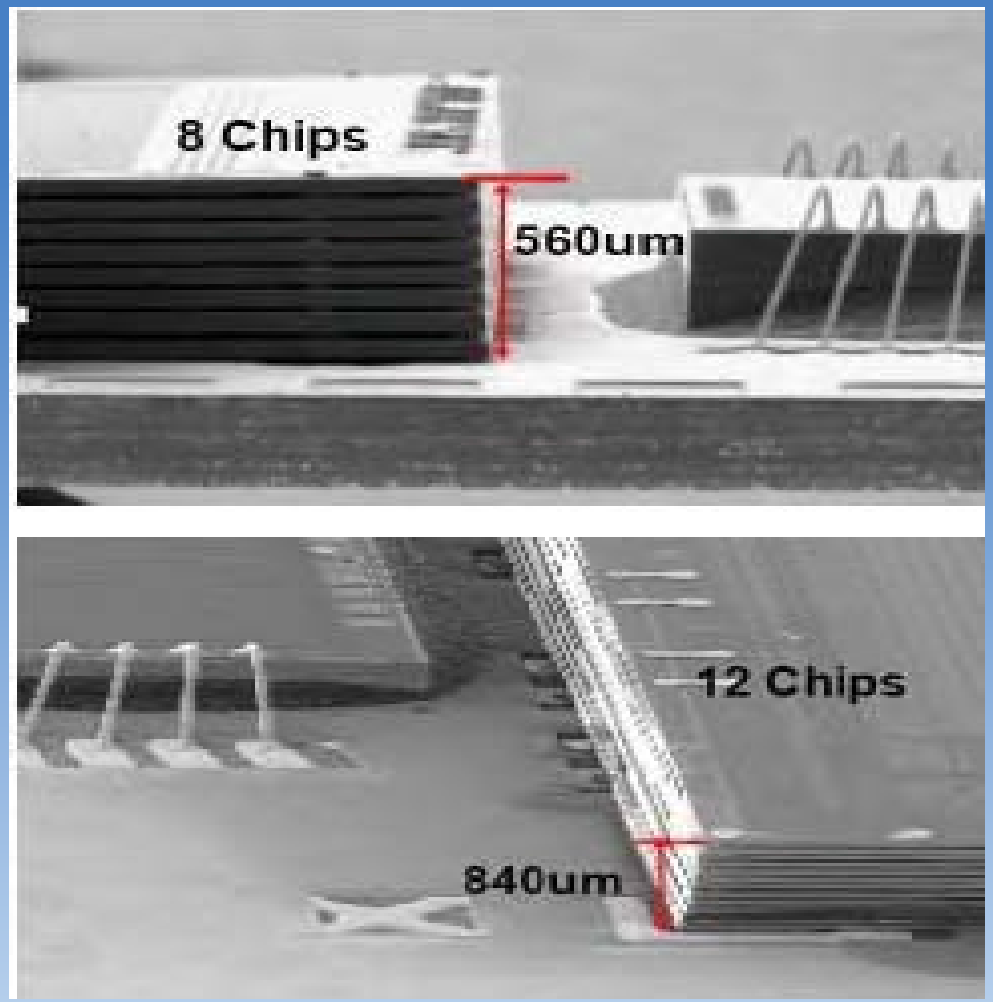
- Cu interconnect
- Ultra Low k dielectrics
- High k dielectrics
- Organic semiconductors
- Green Materials
  - Pb free
  - Halogen free

But improvements are needed

Many are in development

- **Nanotubes**
- **Nano Wires**
- **Macromolecules**
- **Nano Particles**
- **Composite materials**

Future Industry Growth Depends on the Success of 3D Integration



Future Industry Growth Depends on the Success of 3D Integration

Most solutions exist to realize the promise of 3D integration and work is underway to resolve the remaining difficult challenges and deliver reliable solutions at low cost

Changes in Test Quality requirement

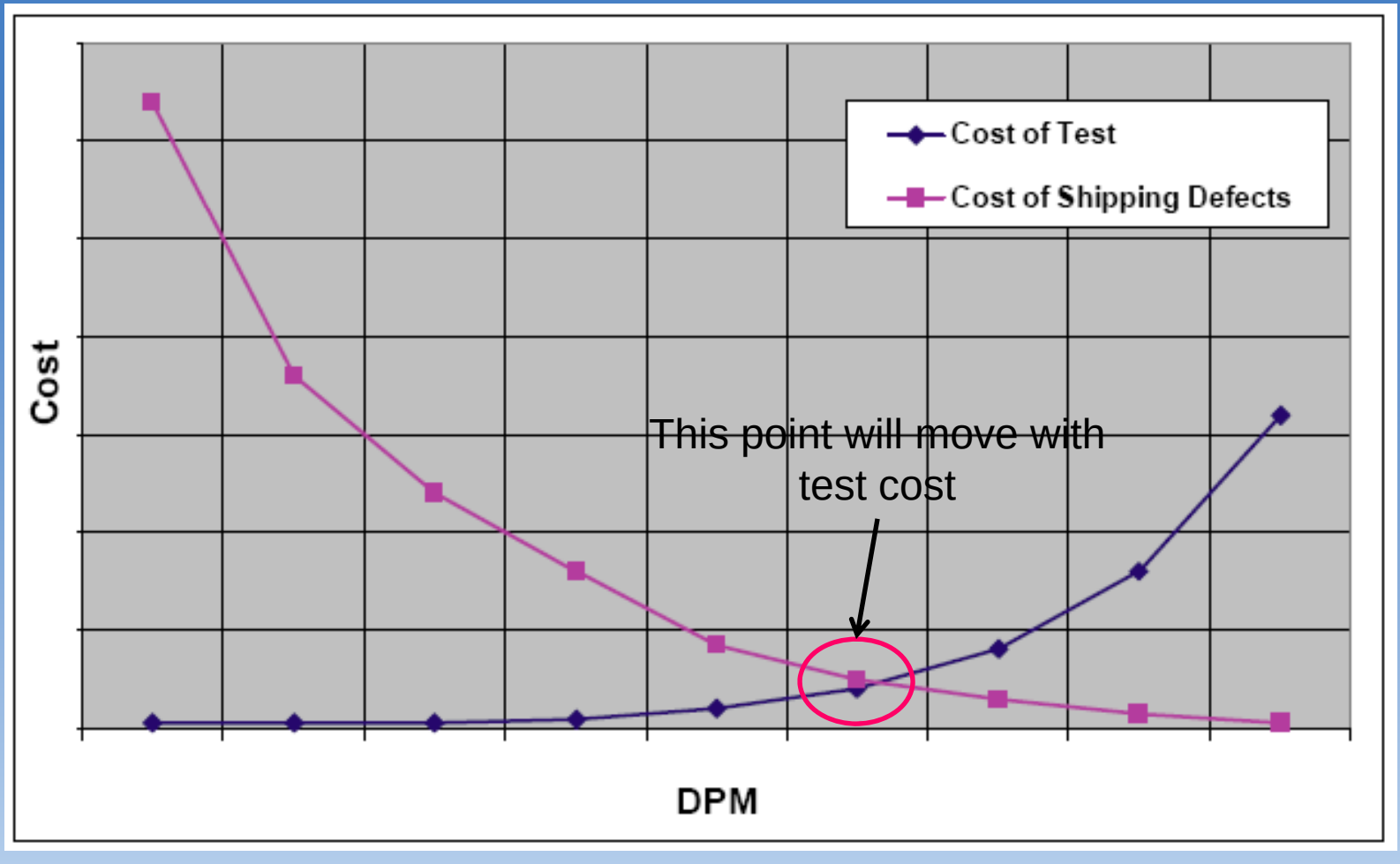
- Test paradigms are changing due to:
  - Billion transistor ICs
  - Incorporation of 3D IC structures
  - SoC architectures
  - SiP system integration
  - Wafer thinning
  - Smaller contact pads with tighter pitch
- These changes are driving increases in test cost

Changes in Test Quality requirement

- Test paradigms are changing due to:
  - Billion transistor ICs
  - SIP system in package
  - Wafer thinning
  - Smaller contact pads with tighter pitch
- These changes are driving increases in test cost

The concept of Known Good Die will be displaced by Probably Good Die for very complex systems

The Test Quality Tradeoff is already used in Manufacturing



Economics will limit Penetration of KGD as Test Access becomes more limited and probing is limited by probe damage of thinned die

- PGD will be enabled by
  - System Redundancy
  - Continuous test while running
  - Dynamic self repair
  - Graceful degradation

Interconnect has become the limiting factor in power requirement

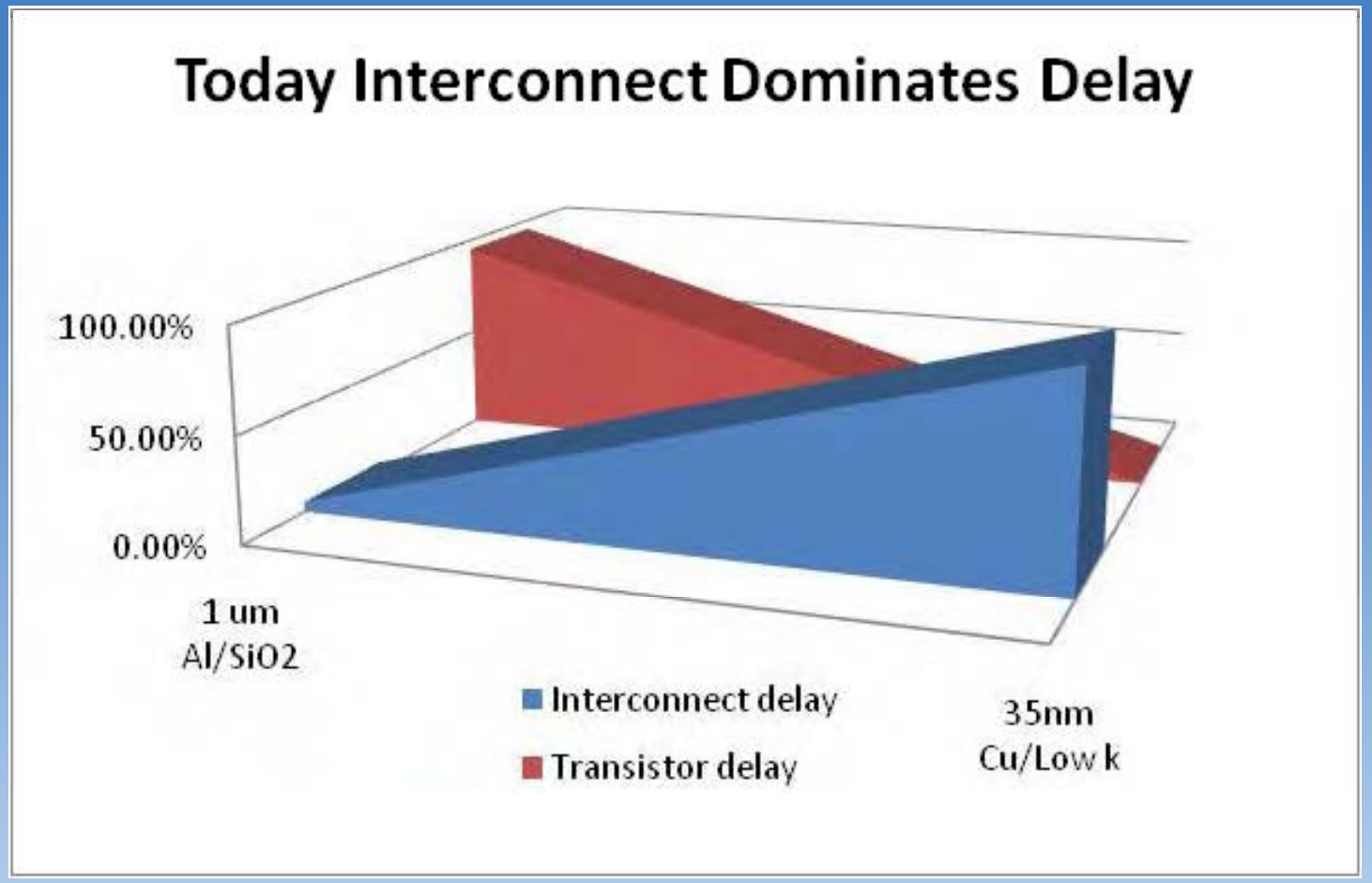
- Moore's law scaling has decreased transistor delay and power by three orders of magnitude while interconnect delay and power dissipation have been negatively impacted.

Change from Al/SiO_2 to Cu/Low k can solve the problem

For small dimensions metal resistivity increases rapidly due to sidewall and grain boundary scattering increasing RC delay

- For 1.0 um Al/SiO2 technology, transistor delay was 20 psec and RC delay for a 1 mm line was 1.0 psec
- For 35 nm Cu/low k technology, transistor delay will be 1.0 psec and RC delay for a 1 mm line is 250 psec

Interconnect will dominate delay and power dissipation



Drivers *for* Low-κ Dielectrics?

Circuit Interconnect delays have two major components: Resistance and Capacitance

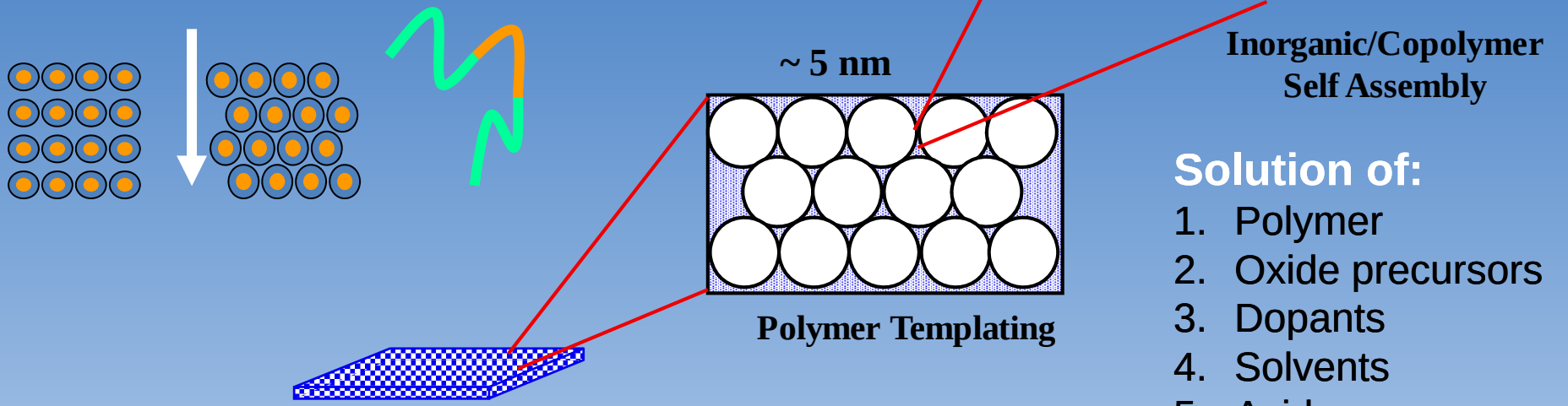
- Resistance is reduced by using copper
- Capacitance can only be reduced by
  - **Increasing interconnect spacing (die size)**
  - **Reducing interconnect size (increases resistance)**
  - **Increasing interlayer dielectric thickness**

… *or*, Lowering the dielectric constant

Technology

Chemically Tunable Liquid Formulations…

self-assembled to form engineered nano-composite structures with controlled structure and physical properties….



Unique "ordered" Material Structure

Solution of:

1. Polymer
2. Oxide precursors
3. Dopants
4. Solvents
5. Acids

Block Polymer Templated Inorganic Oxides

SBA's Materials meet ITRS Roadmap for Low κ Dielectric

Projections have slipped but the Roadmap turns RED at the same k=2.3-2.6

DRAM Interconnect Technology Requirements

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*
DRAM ½ Pitch (nm) (contacted)	*50*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*	*18*	*16*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*52*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*	*18*	*16*
MPU Physical Gate Length (nm)	*20*	*18*	*16*	*14*	*13*	*11*	*10*	*9*	*8*	*7*	*6*
Number of metal layers	4	4	4	4	4	4	4	4	4	4	4
Metal 1 wiring pitch (nm) *									40	36	32
Specific contact resistance (Ω-cm									3.40E-09	2.80E-09	2.34E-09
Specific contact resistance (Ω-cm									5.10E-09	4.30E-09	3.60E-09
Specific via resistance (Ω-cm^2)	3.50E-10	2.90E-10	2.50E-10	2.1[illegible]E-10	[illegible]70E-10	1.40E-10	1.20E-10	1.00E-10	8.40E-11	7.00E-11	5.81E-10
Conductor effective resistivity (μΩ-cm) assumes no scattering for Cu	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
[illegible]ic	3.1–3.4	3.1-3.4	2.7–3.0	[illegible].7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6
2005 ITRS Roadmap for low k	2.5-2.8	2.5-2.8	2.5-2.8	2.3-2.6	2.3-2.6	2.3-2.6	2.1-2.4	2.1-2.4	2.1-2.4	1.9-2.2	1.9-2.2
Roadmap Today?		2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	1.9-2.2	1.9-2.2

2008 ITRS Targets

SBA's Low k Materials integrate into existing fabs with no new equipment requirement

- Material is available for k=2.0, 2.2 and 2.4 through Sumitomo
- Shipped in the same containers as photoresist and uses any standard resist spin tools

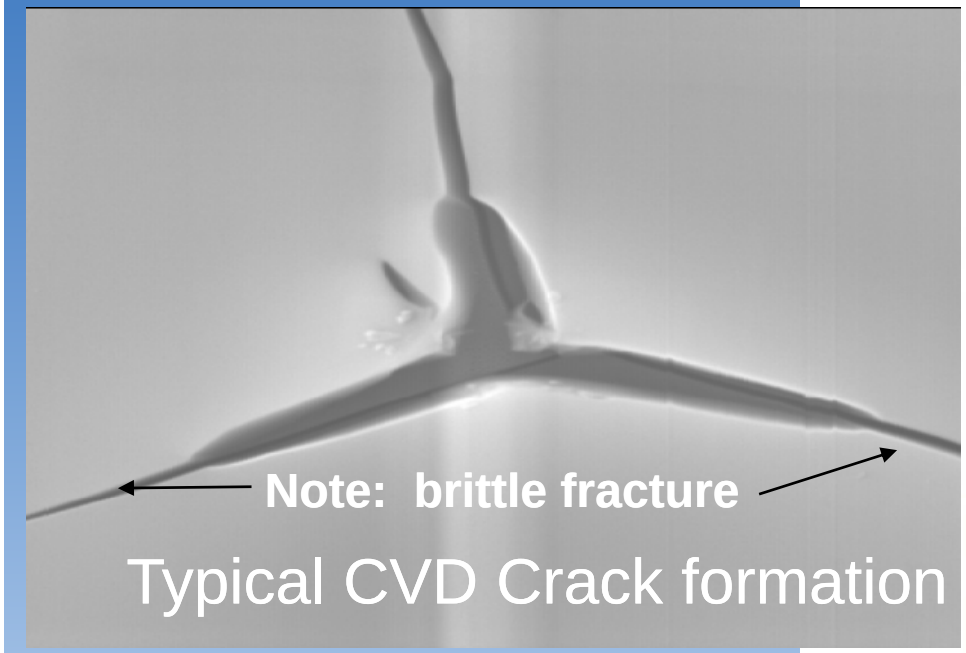
Roadmap Today?		2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	2.0-2.4	1.9-2.2	1.9-2.2

More than 30,000 300mm layers of SBA low k material have been fabricated in a production environment

Performance Differentiation

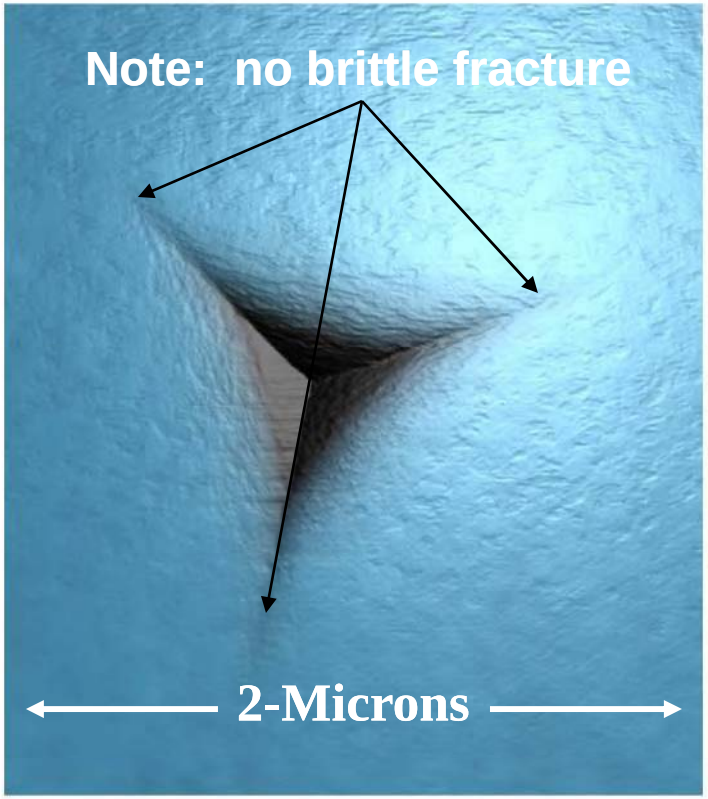
“Fracture tough” Mechanical Performance

CVD K=2.6 Material



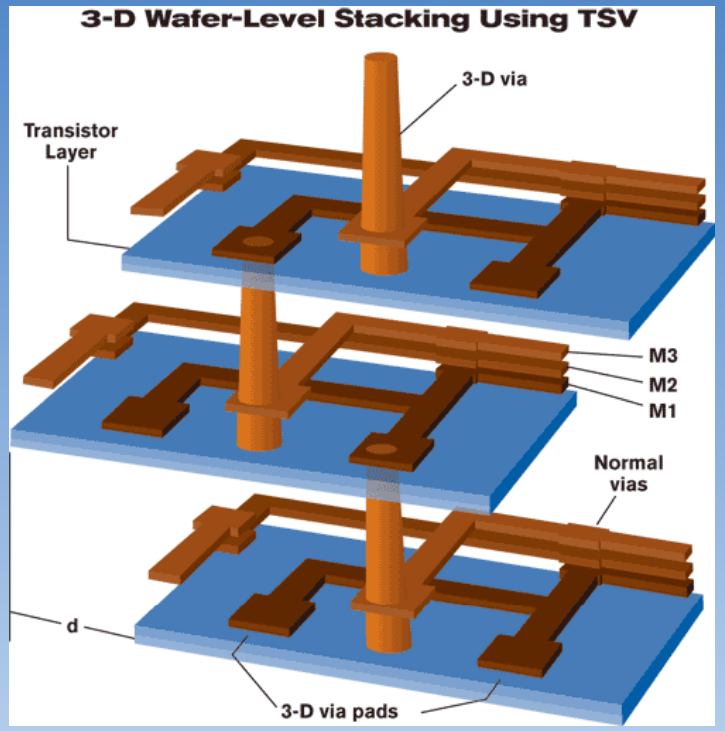
Typical CVD Crack formation

SBA K=2.0 Material



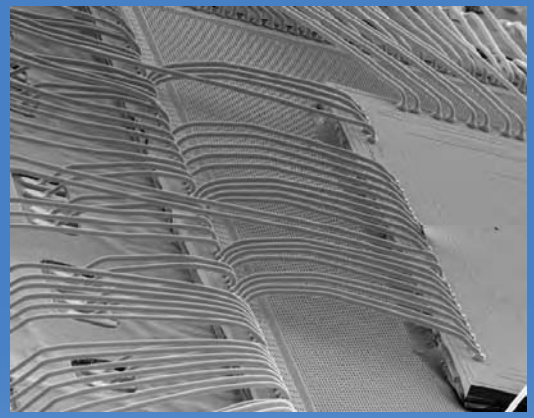
Technologies enabling 3D Integration

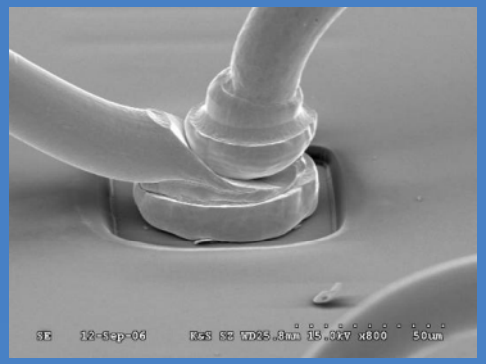
- Through Silicon Via – active wafer & interposers
- Two side wafer level Processes
  - RDL and MicroBumping
- Embedded Components (active & passive)
- Wafer thinning & Handling
- Wafer to Wafer Bonding
- Die to Wafer Bonding
- Micro bump assembly
- Design Tools
- Micro fluidics Cooling
- Assembly of TSV die
- Test of TSV Die

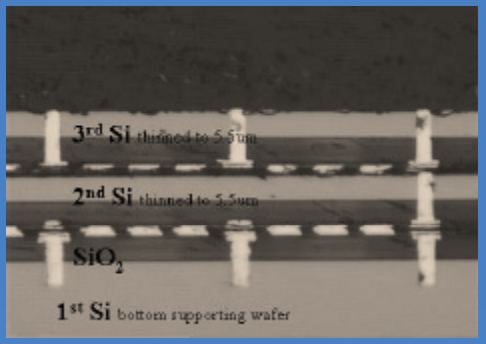


Source: Phil Garrou, 2009

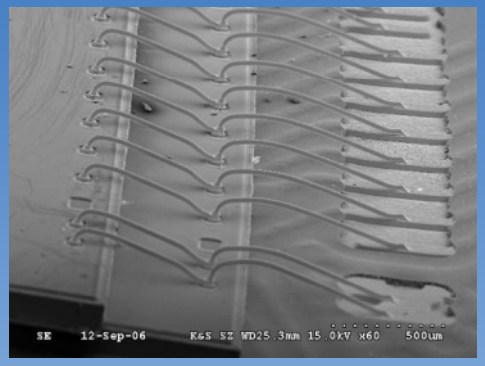
Multiple 3D Technologies are Available

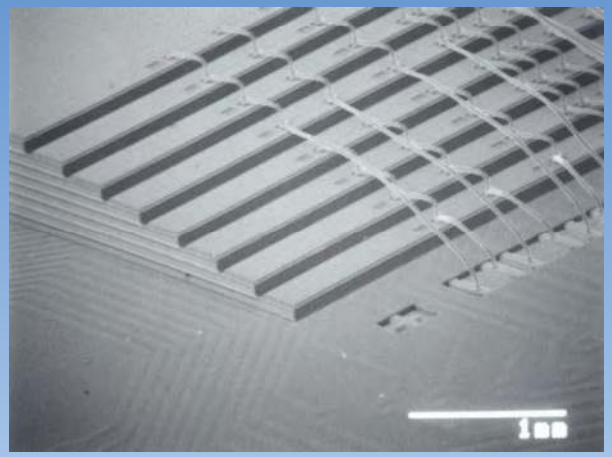


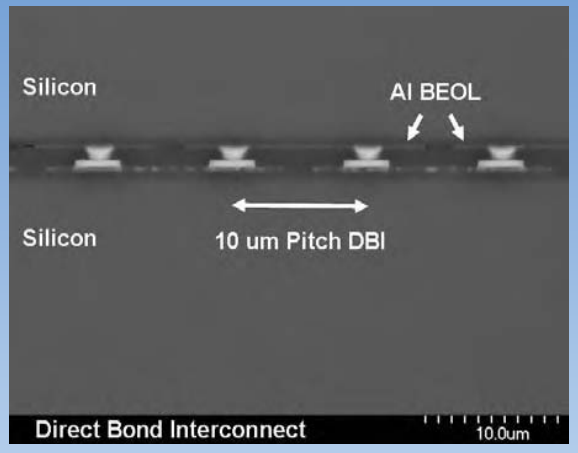




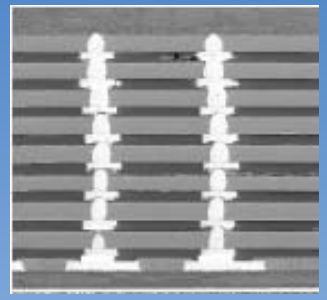
TSV of Tezzaron

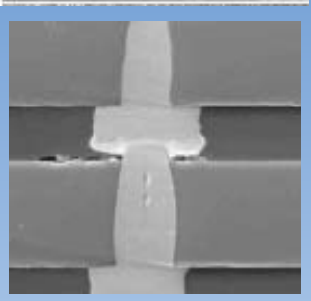






TSV of Ziptronix





Samsung TSV
50 micron thick

The Advantages of TSV

- Reduction in interconnect length
  - Faster circuit speed
  - Reduced power consumption
    - Standby power reduced by 75% compared to PoP and MCP packages
  - Smaller physical size

TSV Interconnection is Enabling

Through-Silicon-Via provides vertical connections that are the shortest, lowest inductance, lowest resistance and the most plentiful.

Higher density
Shorter Connections
Reduced RC Delays
Better heat dissipation
Enable miniaturization
Tighter I/O pitch
Lower Power

TSV interconnects provide solutions to many limitations of SiP and Chip Stacking methods.

Source: Semitool GBC conference

Challenges for 3D Integration

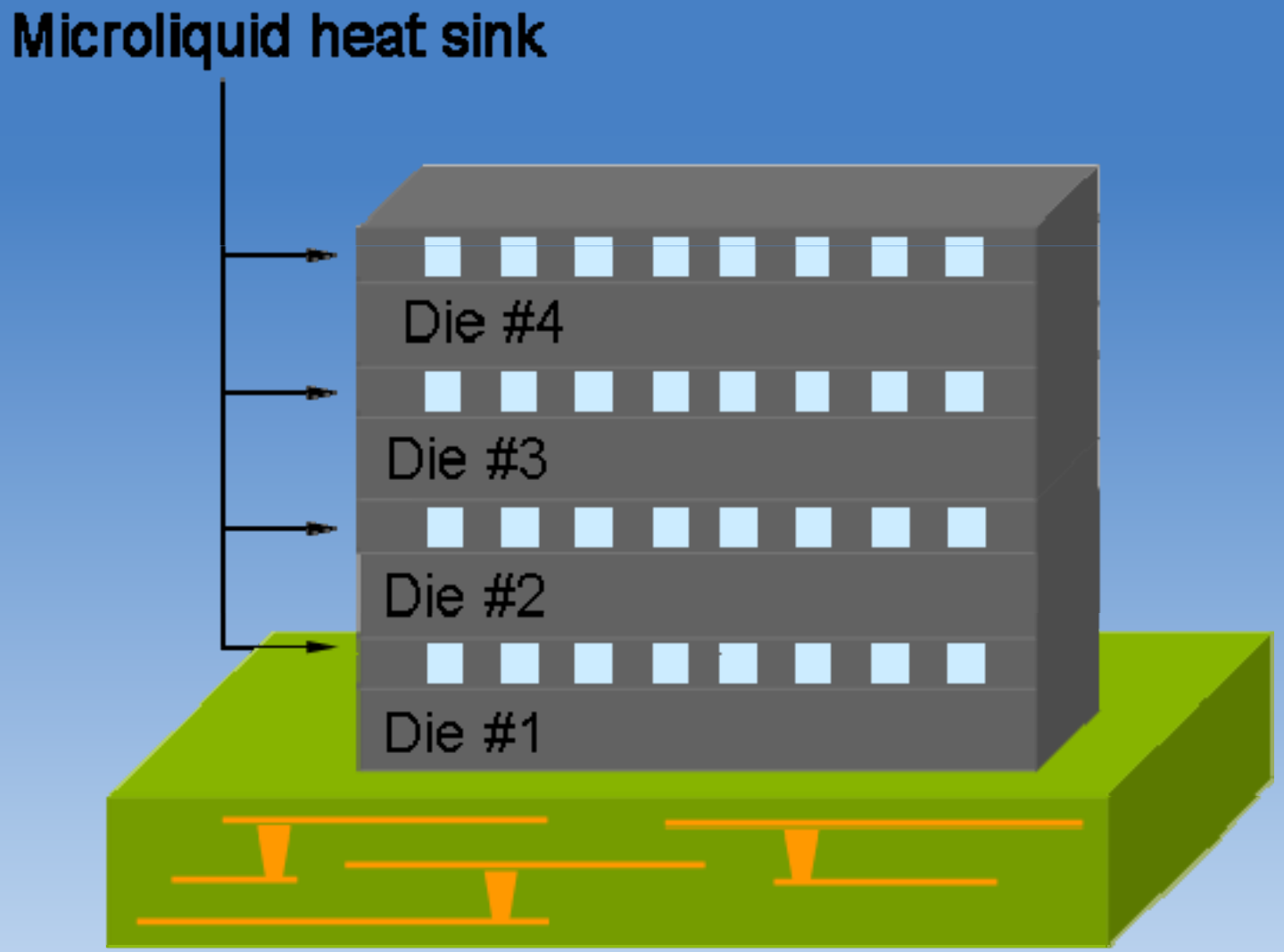
based on TSVs

- Limitations of design and simulation tools
- Complexity of designs for thousands of TSVs
- Thermal management for complex 3D designs
- Test for 3D Integration
- Manufacturing Infrastructure .
  - Will TSVs will be produced by the IDMs, foundries, IC-assemblers or Post-fab processing companies?
- Heterogeneous system integration.
  - The challenge is to integrate different chips--such as ''RF, memory and the MPU''--in one part
- Standards
  - SEMI has standards, Sematech has different specs. Others are moving in their own directions.

Managing the Thermal Density

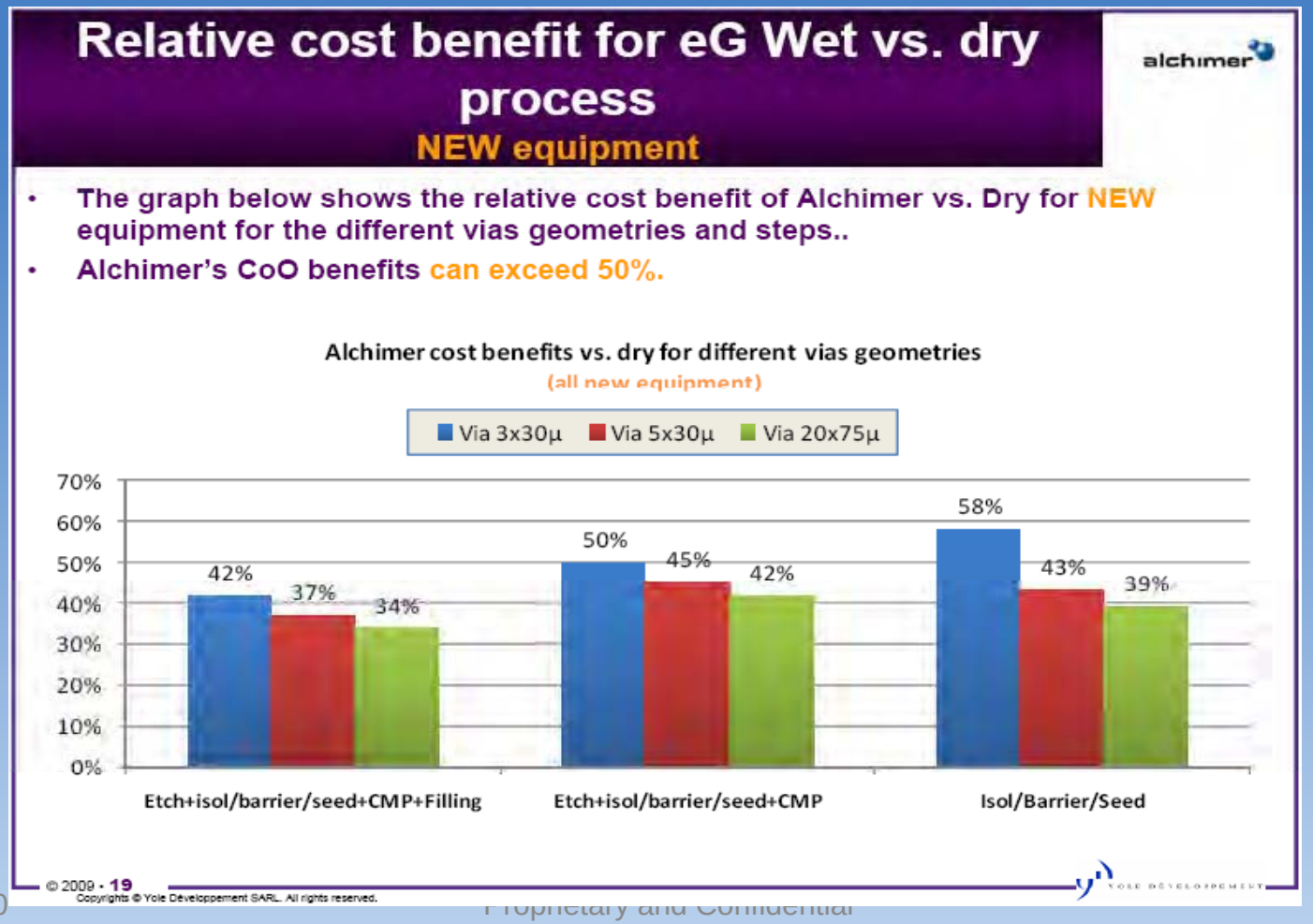
- Thermal management
  - New materials with improved thermal conductivity in all 3 dimensions
    - Nanotubes
    - Nanoparticle fillers of high conductivity materials
  - Reduction in thermal density by:
    - Reducing resistance, capacitance and inductance in the die and in the package
    - Reducing operating voltage
    - Reducing interconnect length through die stacking
  - Incorporation of microfluidics for improved heat removal
  - Incorporation of thermal vias in package and chip design

Interposer Based Microliquid Cooling for Stacked Die



Progress is being made: Cost

Electrografting technology improves properties and reduces cost.



Benefits of Electrografting

- Drastic reduction in Cost-of-Ownership by:
  - Eliminating all dry processing techniques
  - Reducing initial investment and consumable costs
  - Reducing the cost of adjacent process steps
- eG superior performance:
  - Best-in-class Step Coverage, Aspect Ratio, Conformality, Adhesion
  - Insensitive to scalloping, undercut, reentrant structures
  - Film properties meeting or exceeding current TSV requirements
- Save device real estate by reducing TSV diameters
  - More flexibility for designer

Wafer Thinning

It was easier than we thought.

Table 102a&b Thinned Silicon Wafer Thickness 200 mm/300 mm

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Min. thickness of thinned wafer (microns) (general product)	50	50	50	50	45	40	40	40	40
Min. thickness of thinned wafer (microns) (For extreme thin package ex. Smart card)*	20	20	15	15	10	10	10	10	8

Handling of Thinned wafers and die will be the limiting factor

Japan's NEDO 3D IC Project

New Energy and Industrial Development Organization

- Runs through March 2013
- Wafer thinning to 10(+/-1)um for 300mm
- 3D SiPs with TSV by 2012
  - 5 layer stack
  - >10,000 TSVs per chip

Japan's NEDO 3D IC Project

New Energy and Industrial Development Organization

Several of the Goals are already achieved:

- **Wafer thinning**
- **TSV interconnect for stacked die products**
- **>5 layer stacks**
- **>10,000 connections**
- **Improved electrical performance**
- **Reduced power requirement**

Accretech, a subsidiary of Tokyo Seimitsu, showed a thin wafer for TSV 3-D applications.

Difficult Challenges:
Low cost Handling of Thin Wafers

Low Cost Handling Concept: E-Chuck on Si-Wafer

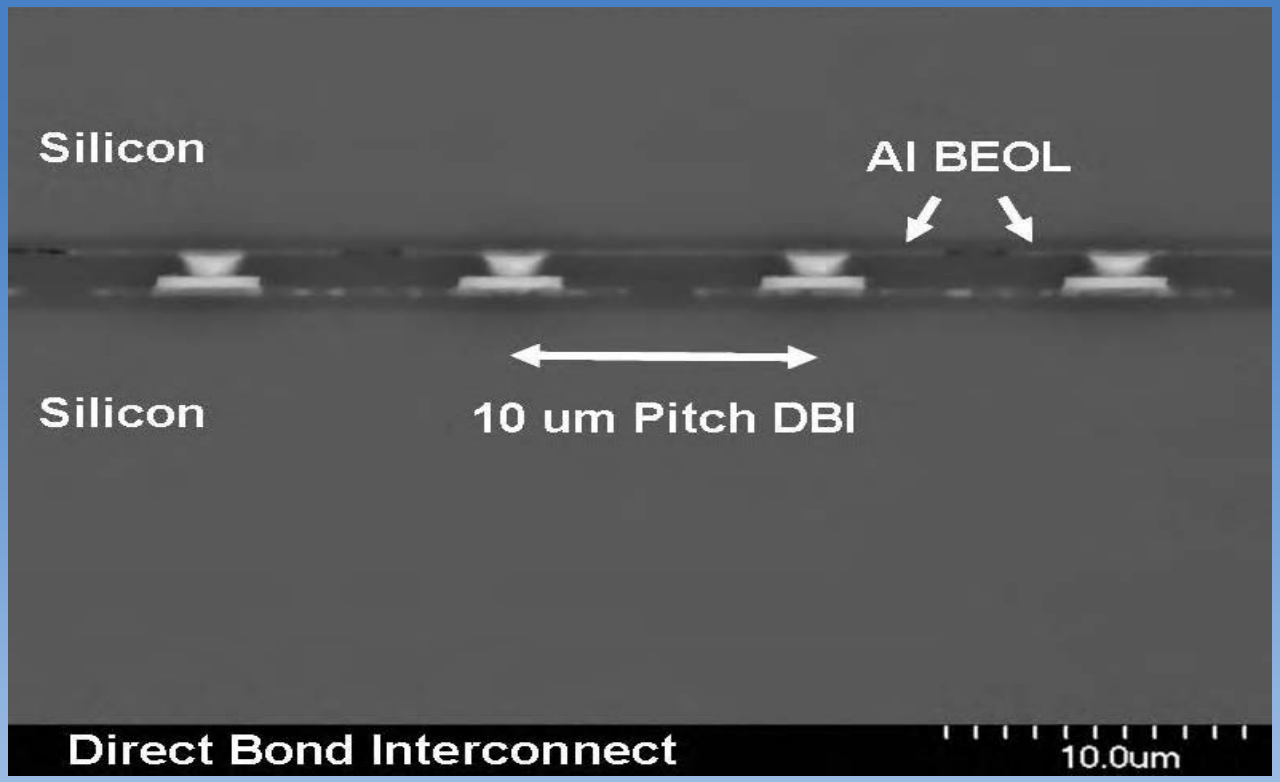
- Mobile electrostatic carrier
- Prototype Electrostatic Chuck successfully tested (200 mm)
- Chucking Principle: Bipolar electrostatic
- Built on Si-Wafers, CMOS compatible
- Chuck-Wafer Thickness:

  100 µm < d < 720 µm

Source: Fraunhofer IZM

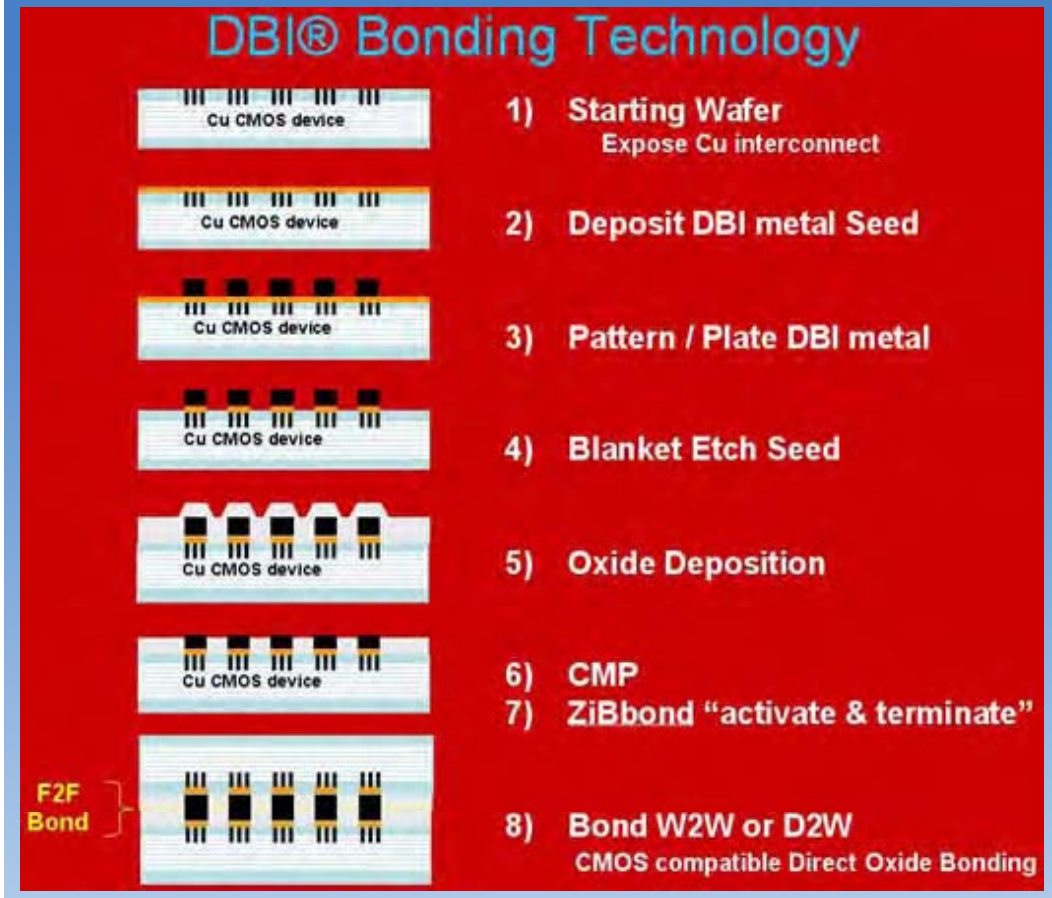
The Simplest Case

Face to Face Die to Wafer



TSV of Ziptronix

Direct Bond Interconnect Process Flow (Ziptronix)



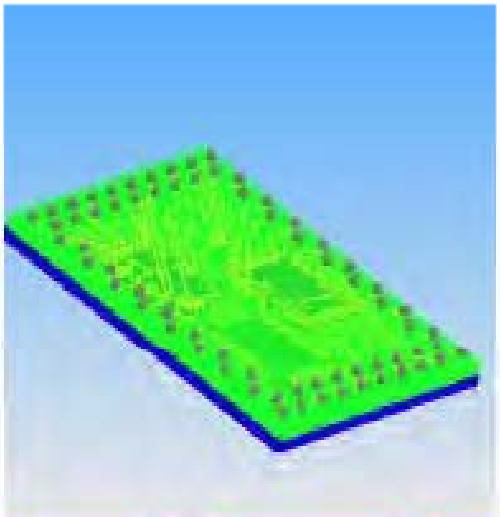
- Advantages
  - Faster process (up to 10X)
  - Improved bonding accuracy
  - Higher bond energy
  - Lower process temperature (100C)
  - Lower cost

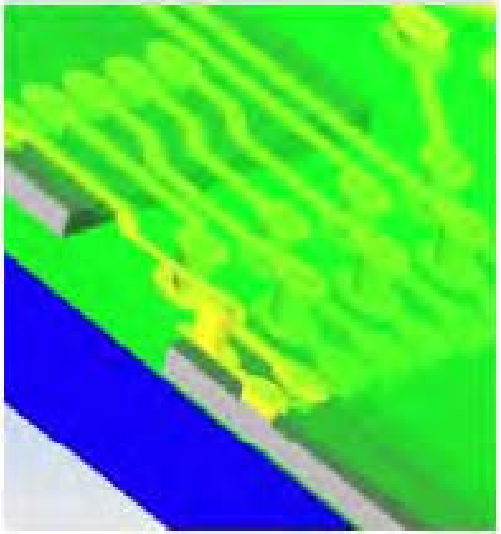
The ITRS and MIT's Microphotonics Center are Collaborating on Implementation of a 3D Integrated Computing SiP targeting 2015

The objectives are:

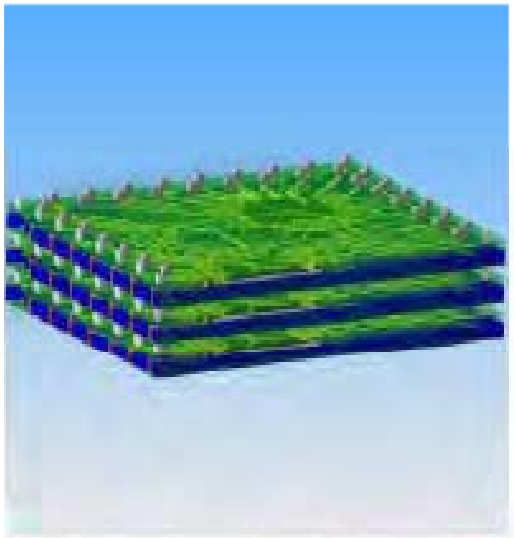
- Push the limits and identify the challenges not met by known technology
- Focus development efforts on the factors limiting speed, cost and power requirements for high performance SiP

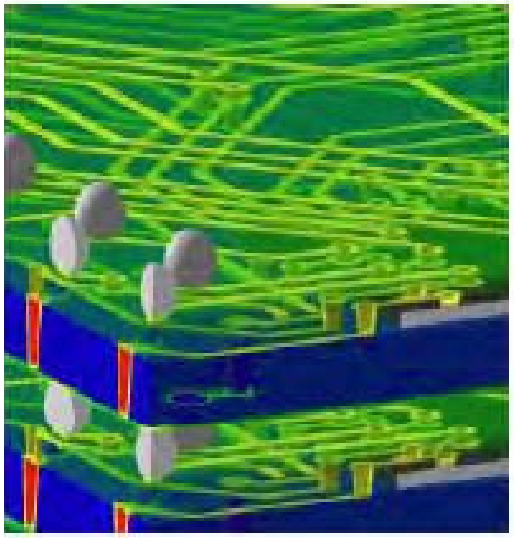
Initial Design Parameters





Target date for production:	**2015**
Number of Cores:	**100**
Core transistor speed:	**10GHz**
Electrical pins off-chip max:	**25GHz**
Optical connections per Package:	**1**
Power, ground and clock connections through substrate	**#TBD**
Total power per package:	**TBD**
Die size:	
Memory	**557mm^2**
Logic	**310mm^2**
Optical	**TBD**
Die thickness	
CPU:	**25um**
Memory:	**25um**
Total power per package:	**TBD**
Maximum power density:	**TBD**
Hot spot distribution:	**TBD**
Max. Junction temperature:	**~85^{o}C**
Operating Voltage:	**500mV**





The project has identified two limiting factors

- Thermal management for high power density
- Bandwidth density to meet the I/O requirements of a general purpose Teraflop computer (9 terabits/s)

Interconnects are the dominant contributors to both limiting factors

What is the solution?

- Multi-core designs can reduce frequency required for a given compute power to mitigate the problem.
- 3D interconnect decreases path lengths.

(For n stacked layers, this may reduce global interconnect path lengths by square root of n)

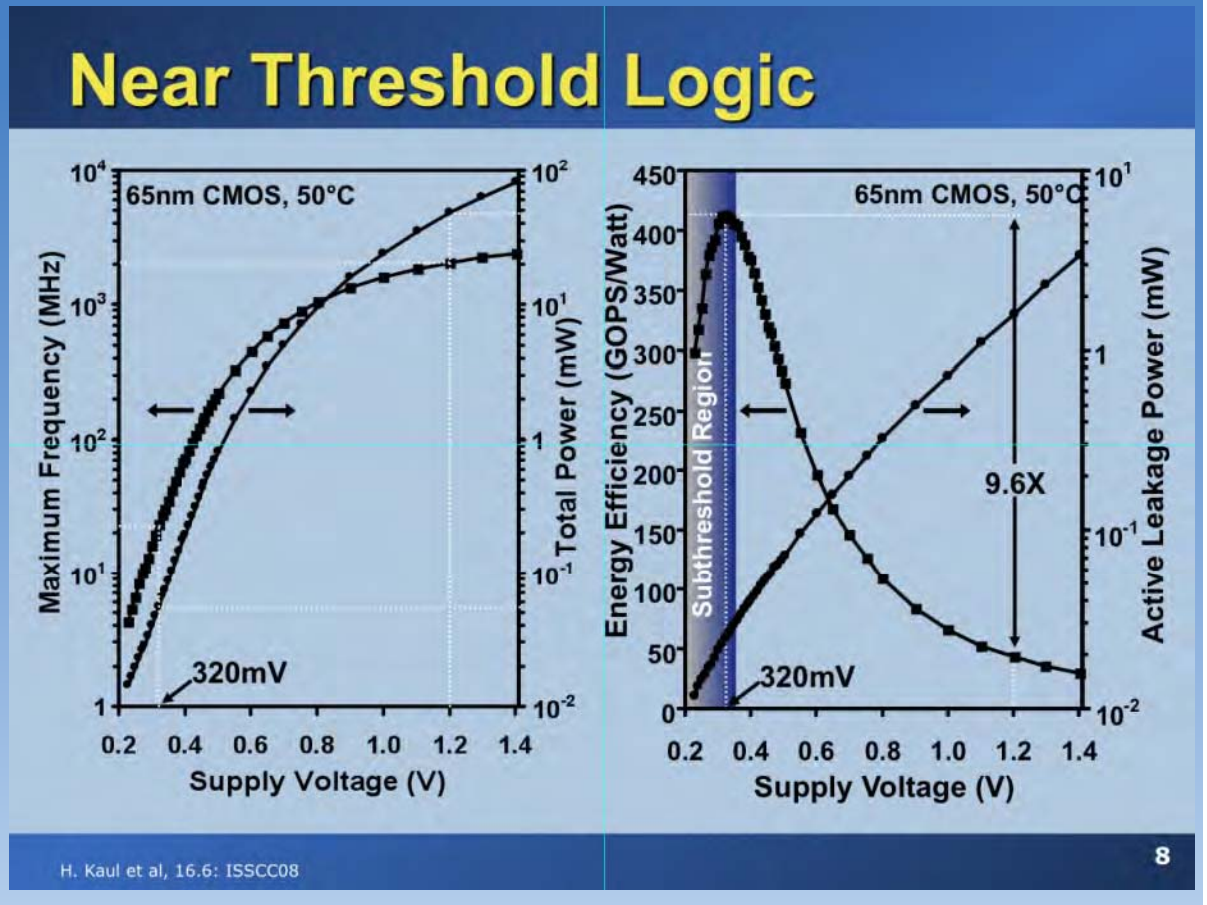
Power Efficiency is a Key Driver

- Maximum energy efficiency occurs near subthreshold boundary
- Maximum frequency rises slowly after 2X threshold voltage

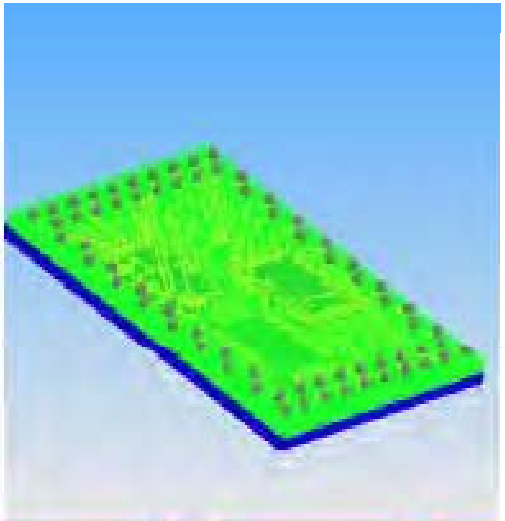
Therefore:

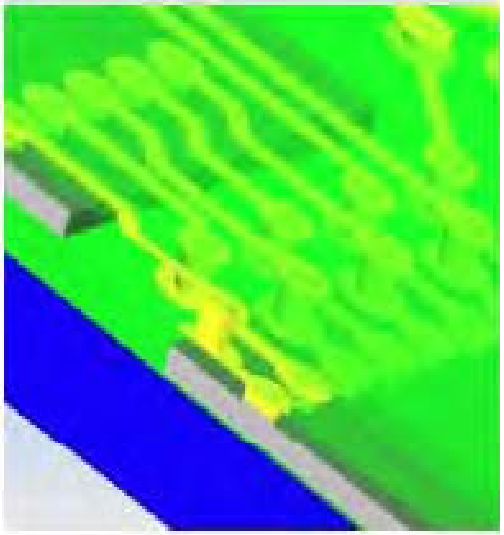
Greater parallelism is preferred over increasing frequency.

Power supply voltage should be as low as possible.

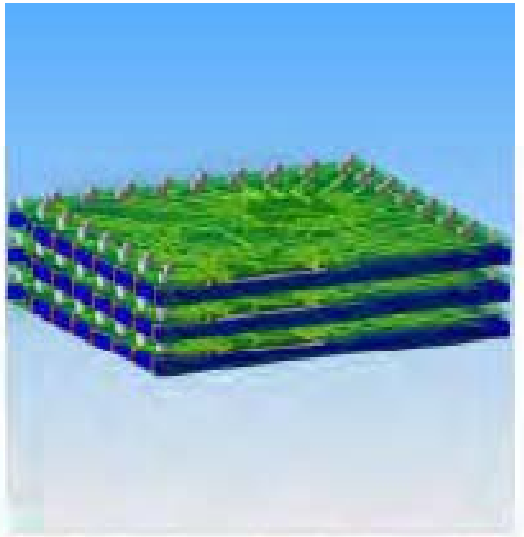


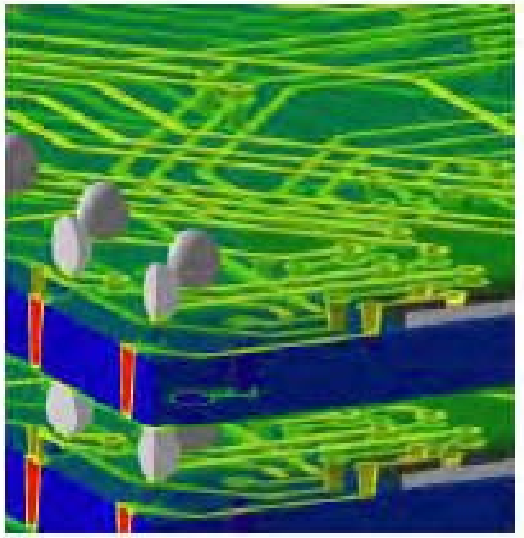
Revised Design Parameters





Target date for production:	**2015**
Number of Cores:	**1000**
Core transistor speed:	**1GHz**
Electrical pins off-chip max:	**25GHz**
Optical connections/ Package:	**1**
Optical bandwidth	**1Tbyte/S**
Power, ground and clock connections through substrate	**#TBD**
Total power per package:	**TBD**
Die size:	
Memory	**557mm^2**
Logic	**310mm^2**
Optical	**TBD**
Die thickness	
CPU:	**25um**
Memory:	**25um**
Total power per package:	**TBD**
Maximum power density:	**TBD**
Hot spot distribution:	**TBD**
Max. Junction temperature:	**~85^{o}C**
Operating Voltage:	**400mV**





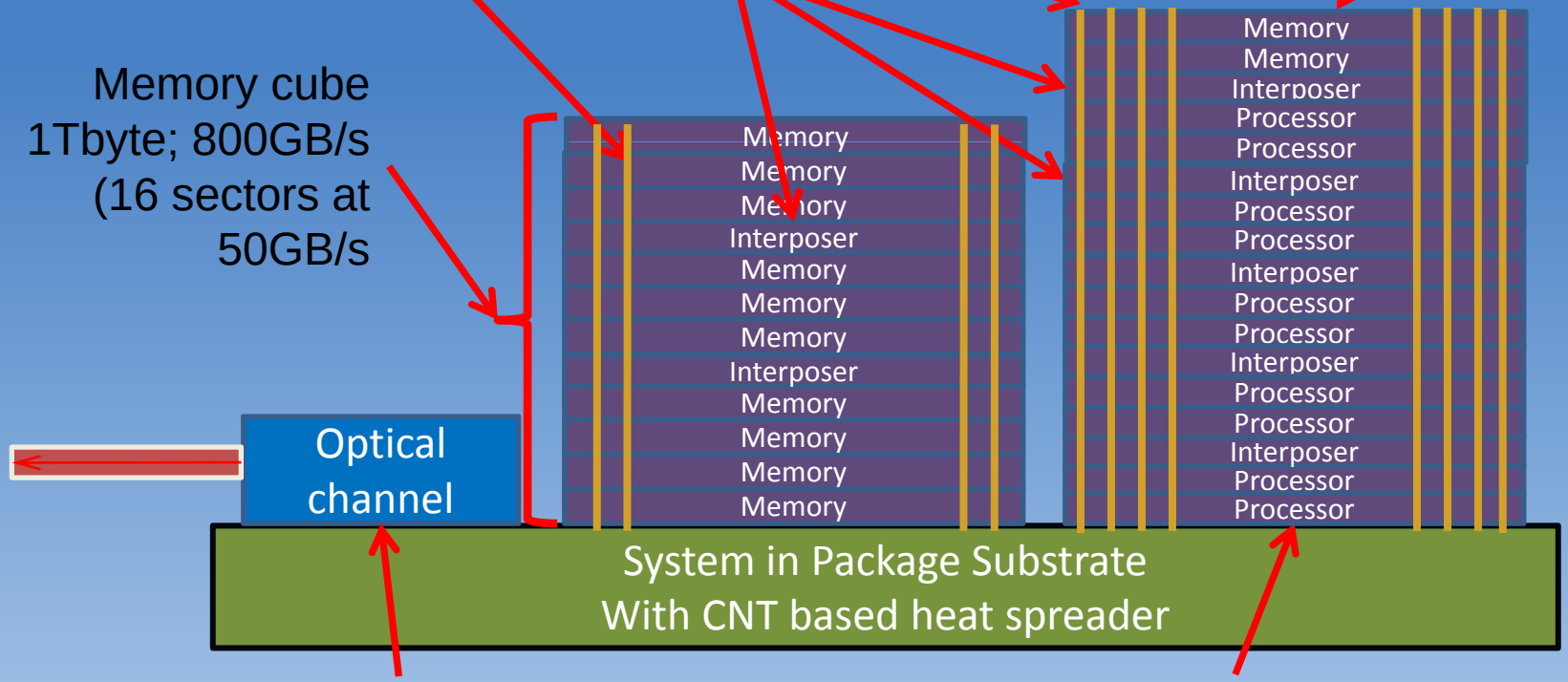
Tera-scale Computing by 2015

TSV die to die connection

Silicon Interposer with:
-Integrated thermal management
-Integrated Passive networks

200GB; 800GB/s memory
(16 sectors at 50GB/s)

Memory cube
1Tbyte; 800GB/s
(16 sectors at
50GB/s



2TB/s optical transceiver for:
- Off package communication
- On package routing

Processor with 1000 cores/10 layers
Core transistor speed 1GHz
25um thick wafer (~400mV power)

Tera-scale Computing by 2015

The Roadmap says we can make the components:

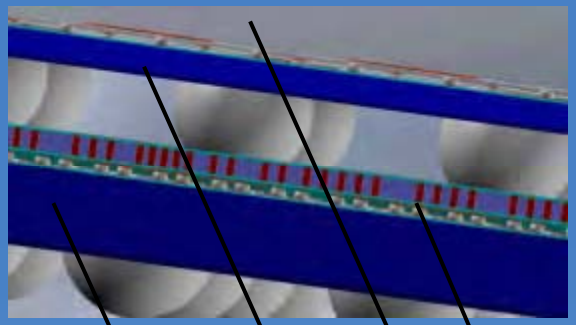
- 3D memory stack with TSV interconnect
- 25GHz electrical signaling
- Microfluidic based thermal management
- 1000 core processor with 1 GHz clock
- 100Gbyte memory die
- Optical transceivers at 2TB/S per channel

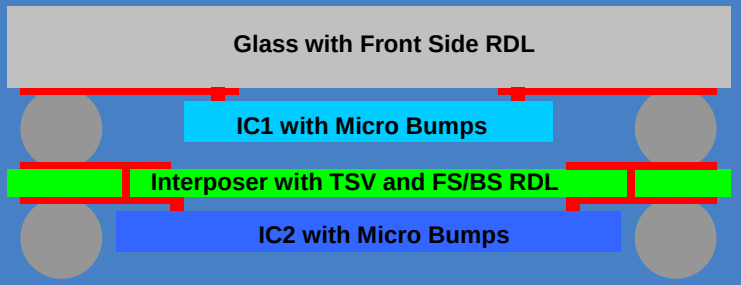
Tera-scale Computing by 2015

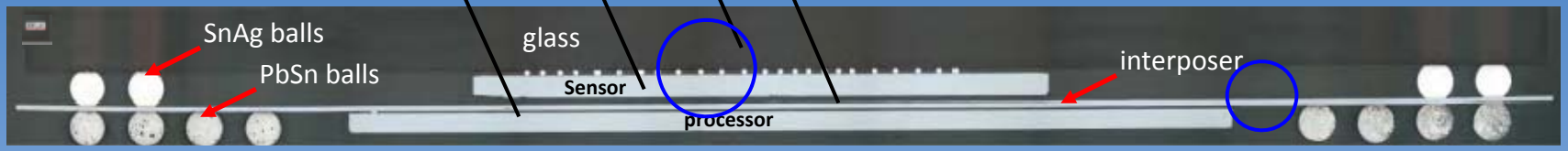
These design changes have reduced projected power requirement by more than 20X

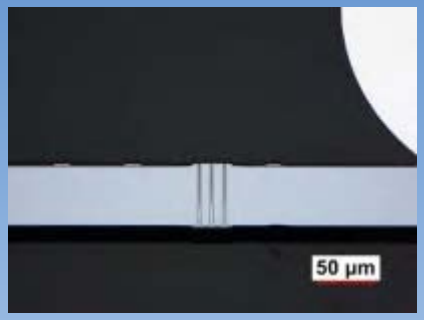
3D TSV are in Production today

Stacked Die 3D Camera Module





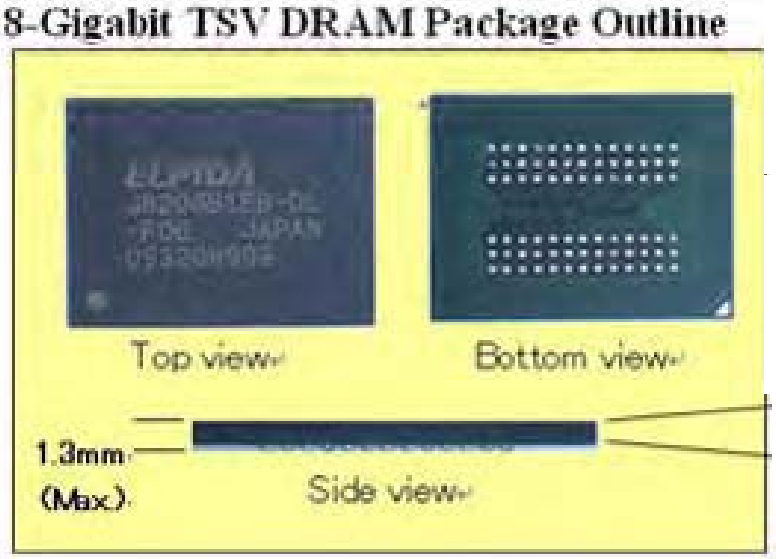




Cross section of the 3D camera stack with 3D stacking, functional diversification using TSV interconnect

Source: Fraunhofer IZM

Elpida has Introduced The First 3D TSV Memory Product

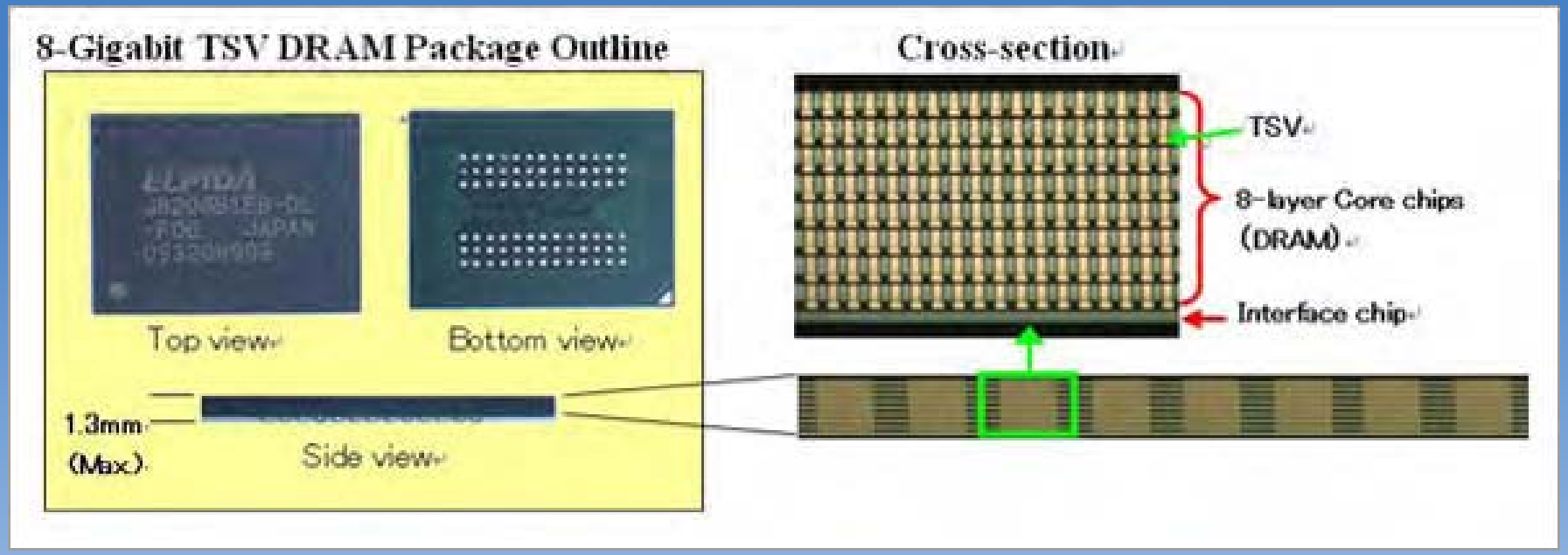


The first production TSV stacked die product for complex ICs:

- **Production shipments 2009**
- **16Gb version mid 2010**

This Product has been tooled for volume production at Elpida's Hiroshima Facility

Elpida has Introduced The First 3D TSV Memory Product



This Product has been tooled for volume production at Elpida's Hiroshima Facility

Elpida 8-Gigabit TSV DRAM

- 8-Gigabit DDR3 SDRAM (operating at 1,600Mbps)
- 1,030 connections between core layers
- 8,357 bump connections for a single package (including the interface layer)
- Package height: 1.3mm (eight core layers and one interface layer)

Predictions

- Moore's Law scaling is nearing it's end.
  - The CMOS technology has only 2 more technology nodes before fundamental change is required. (assuming 32 nm is here)
- All packaging and interconnect materials and most device materials will change during this decade.
  - **SiO_2 and Al ⇒ Cu and low k dielectric**
  - **SiGe, W, Ni, High K metal gates…**
- Half of the materials will change again in the next decade
  - **Nanotubes, Nanowires, Nanoparticles**
  - **New molecules**
  - **A replacement for the CMOS switch**

Predictions continued

- Wafer Level Packaging will expand in 2010 as cost and performance advantages become a reality
- 3D WLP will be enabled for complex systems as standards and new processes and materials are introduced
- 3D Integration will maintain the price elastic growth of the industry after Moore's Law Scaling reaches its limit
- Volume shipments of more complex 3D ICs will begin in 2010

Thank you