Design of High Density & 3D Packaging: Tools and Knowledge

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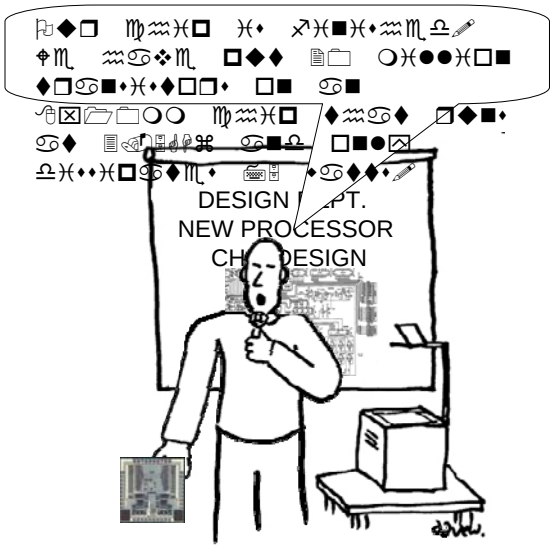
Outline

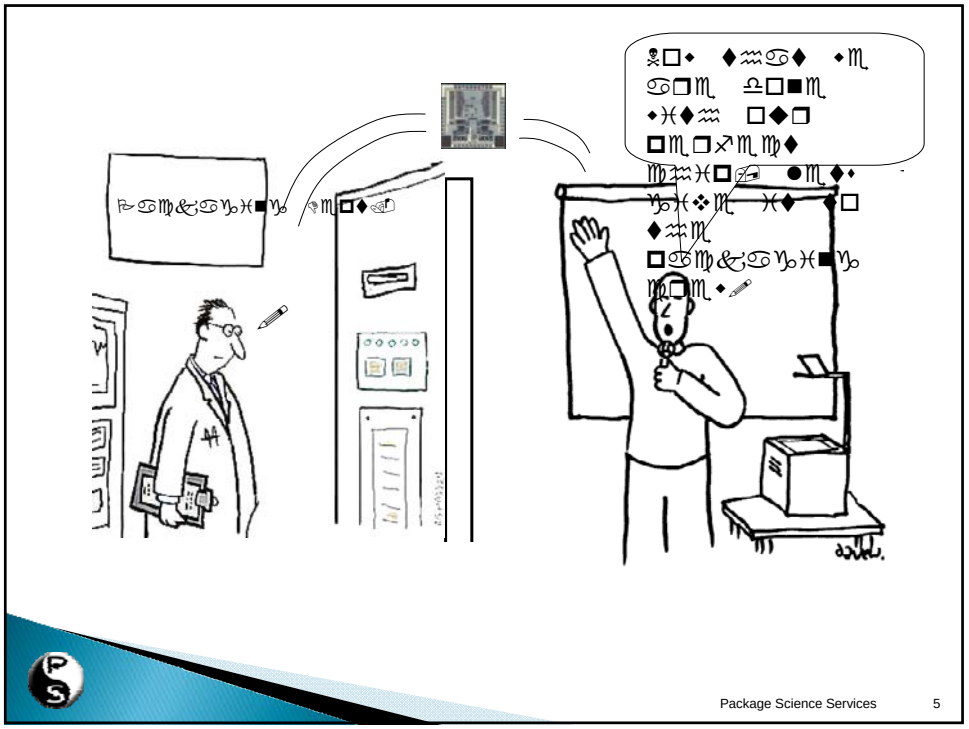
- Package Design Flow (the old way)
- Package Design Flow (the right way)
- Evolution of Packaging Sciences
- Package Selection
- Moore's Law, Miniaturization and Cost
- Chip Stacking and High-Density Designs
- Electrical Design and Analysis

- Conclusion

IC PACKAGING DESIGN FLOW

The Old Way

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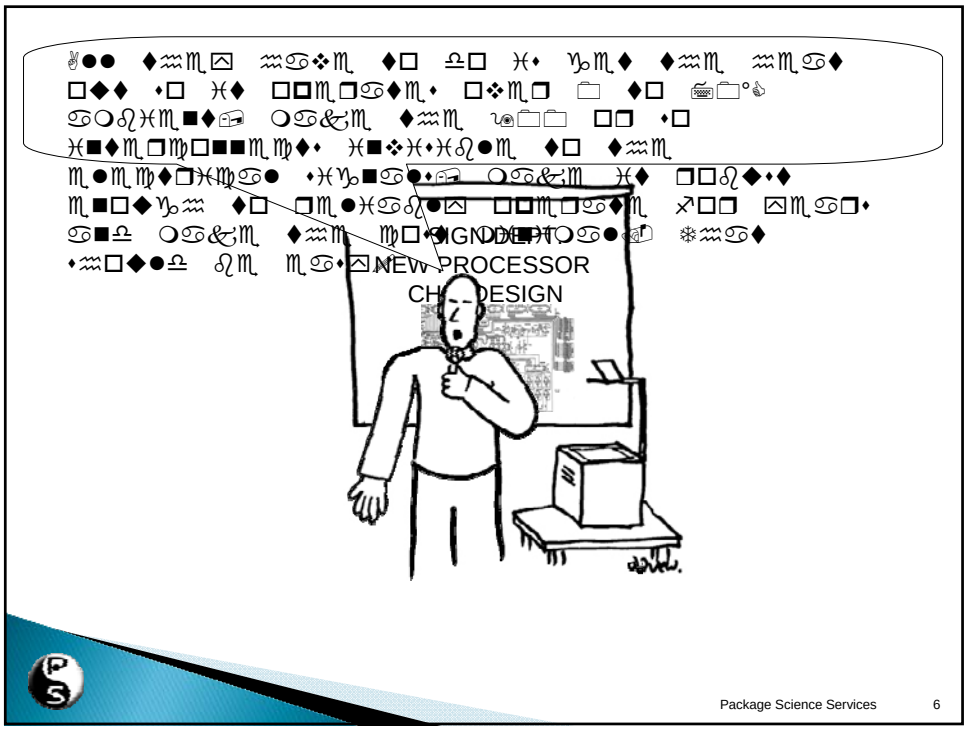

NEW PROCESSOR
Package Science Services 6

IC PACKAGING DESIGN FLOW

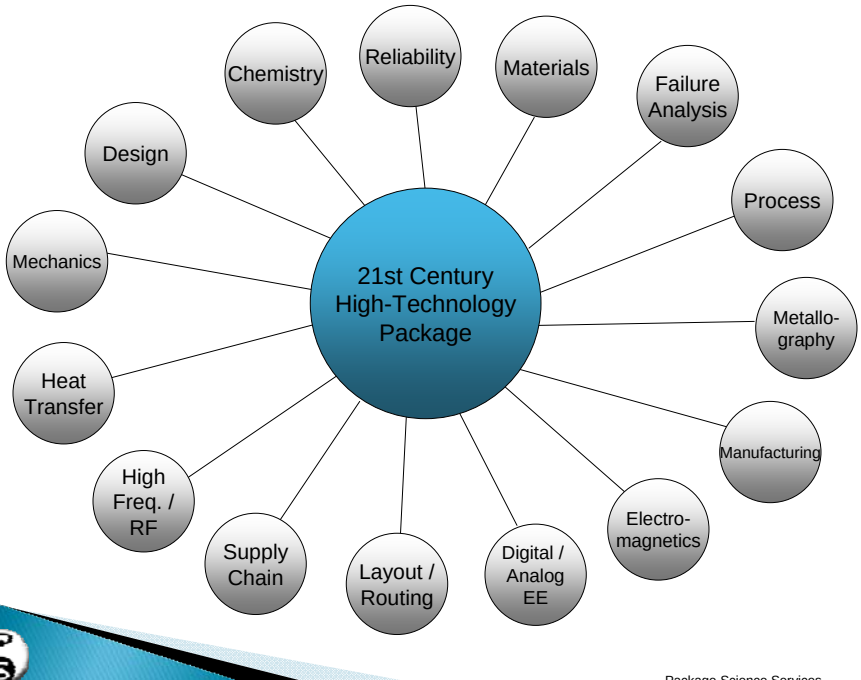
(The Right Way)

Evolution of Packaging Science

- The old model of creating the device and then packaging it is long gone
- Chip manufacturing has evolved to where simple, low-performance designs can be packaged in the millions and billions with high yield and extremely low cost
  - This presents the illusion that all packaging is simple and should be relatively easy and low cost
- Successful packaging of high technology devices requires consideration at the outset of the device design
  - Concurrent design practices for the device and package are mandatory for high performance products
- But the stigma remains

IC Packaging Science

- Packaging of complex silicon devices requires a deep knowledge of many aspects of high-technology engineering disciplines
  - As an example, packaging a high lead-count chip requires knowledge of electrical, thermal, mechanical, chemical, reliability and materials engineering
  - Taking the next step from prototype to mass-manufacture requires knowledge of manufacturing processes, materials, statistical methods (SPC), failure analysis and supply chain
- These disciplines must be known and used in the conceptualization, design and implementation of any package design



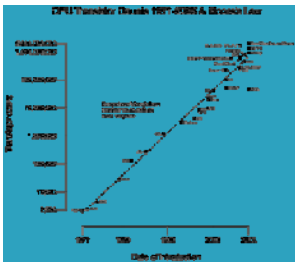
Package Types

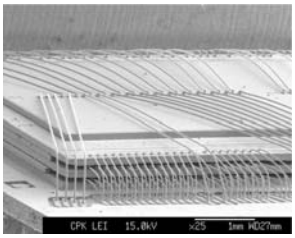
- Packaging has evolved with technology advances to meet the needs of high-performance, low-cost and specialty designs
- Selection of the best form factor must balance cost, performance and reliability
- Form factors range from two-lead packages with simple structure to multi-layer, high-leadcount structures, stacked chips and package-on-package formats
- Performance and I/O count have increased while the size of components and products have decreased
  - Drives the need for higher package integration
  - More functionality in a smaller space
  - Higher density and interconnectivity

Package Selection

- As with any product, the package must satisfy the need but also fit into a larger assembly with the best fit, form, function and cost
- Packaging Selection Criteria
  - Product specifications
  - Desired form factor
  - Cost targets
  - Chip size and number of interconnects/type
  - Electrical requirements
  - Cooling or temperature control requirements
  - Process limits or special handling

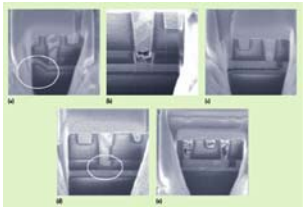
Moore's Law and packaging

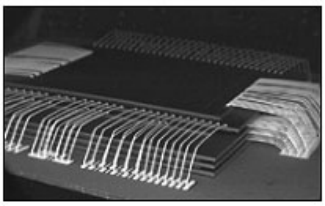


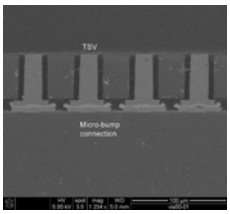


- The industry has been able to keep pace with Moore's Law by shrinking transistors
- Limitations to transistor gate size are an issue in the future and interconnect losses pose a serious problem for high speed chips now
- 3D packaging provides increased density and performance and is a key element to meeting/exceeding Moore's predictions

Miniaturization and Performance

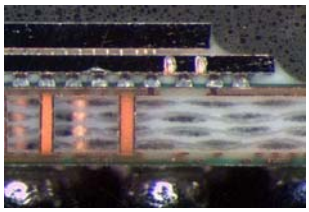






- High performance computing is limited by interconnect losses
- Interconnect scalability cannot keep pace with gate length
- Interconnect switching power can be 50% of overall dynamic power
- Stacking chips can reduce chip-to-chip interconnect length but does not address on-chip interconnect length
- Through-silicon vias help to reduce interconnect losses on-chip and chip-to-chip
- Challenges include coupling and substrate interaction

Cost



- Reducing cost or maintaining cost with more functionality is the number one priority
- Stacking packages and chips may be less costly than advancing lithography
- TSV and other 3D packaging technologies reduce real estate, material usage and back-end process costs

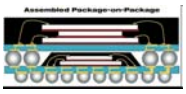
Increasing Packaging Density

- The need for higher integration is met by innovative package design

- Stacked chips
  - Initially used for memory applications
    - Same size memory chips stacked with spacers, offsets or alternating die orientations
- Later moved to functional blocks with memory, logic, ASIC and special function
  - Varied chip size stacked ‘wedding cake’ style
  - Combination of wirebond and flip-chip
  - Leadframe, BGA and SMT package types

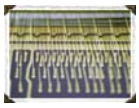
Stacked Packages

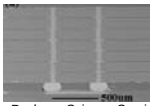
- In some cases, it is not practical or possible to stack all chips that make up a system into the same package but the need for miniaturization and connectivity remains
  - Cases where KGD are not available or connectivity for test is not practical or possible
  - Modules can be assembled with different devices for varied functionality or product mix
  - Temperature or process sensitivity
- Stacked packages meet these needs



Chip Stacking Considerations

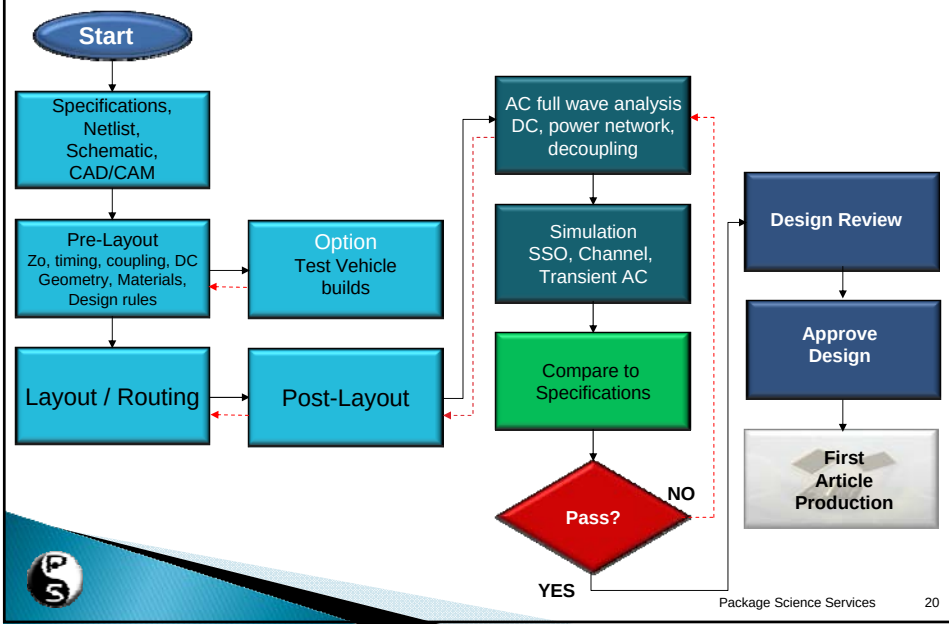
- Performance and interconnectivity are primary concerns when designing a stacked package
- When using same-type die, connectivity is not simple, but it is constrained
- When using multiple die to create a 3D system in package, connectivity is complex and requires intelligent software assistance
- Various combinations of die rotations, connections to the substrate and chip-to-chip are possible
- At this time, traditional tools are used to perform this function, but it is not by any means automated





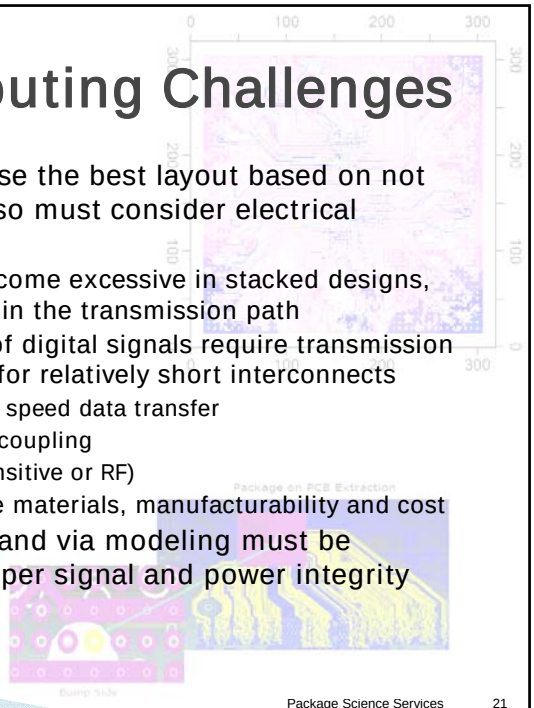
Electrical Design and Analysis

Electrical Design Flow



Layout and Routing Challenges

- The designer must choose the best layout based on not only connectivity, but also must consider electrical performance
  - Wire bond length can become excessive in stacked designs, increasing the parasitics in the transmission path
  - Frequency components of digital signals require transmission line design and analysis for relatively short interconnects
    - Differential pairs for high speed data transfer
    - Multiple power supply decoupling
    - Analog interconnects (sensitive or RF)
  - Design constraints include materials, manufacturability and cost
- Concurrent trace, plane and via modeling must be performed to assure proper signal and power integrity



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Connectivity and Circuit Analysis

- Toolsets for 3D design must create accurate connectivity netlists and allow interaction with modeling and simulation tools
  - Connectivity from chip-to-chip, chip-to-substrate and substrate-to-PCB must be maintained throughout the design cycle
    - Traditional 2D design tools may require concatenation of netlists to maintain proper connectivity
    - Contain limited 3D information
  - 3D tools must maintain connectivity while allowing substitutions or changes in individual chip, interposer or package layout or position in the stack
  - Interoperability
    - Must be able to interact with other tools
      - Import/ Export from chip/package/PCB CAD/CAM design tools
      - Direct export to 3D modeling and simulation tools
      - Import results from analysis tools for optimization and DRC
      - Export design layout data to manufacturing files

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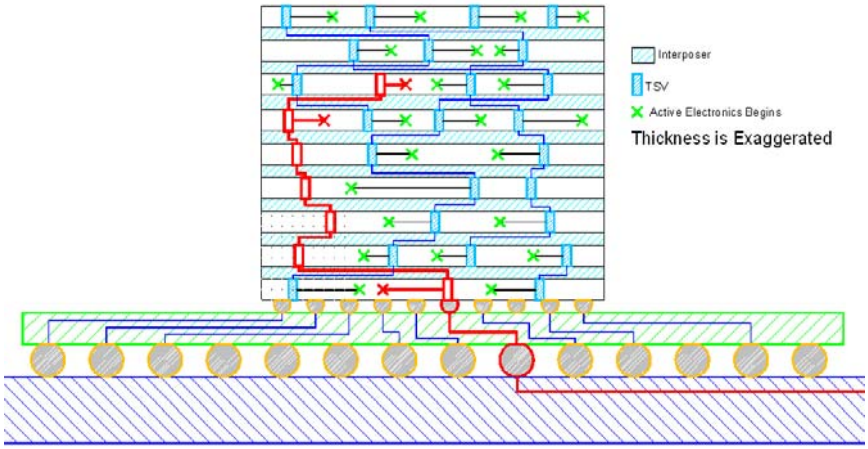
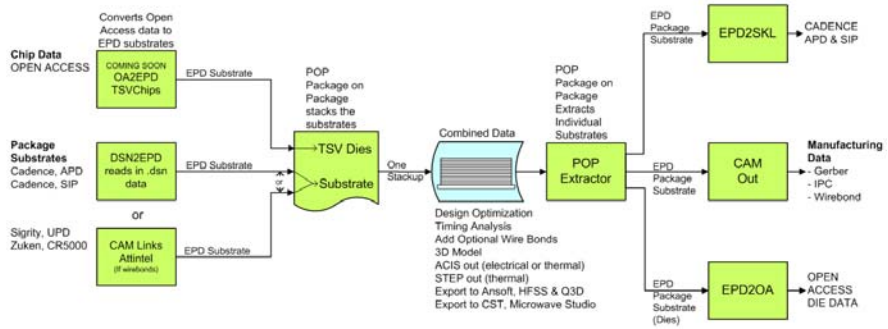
Circuit Path Example - TSV

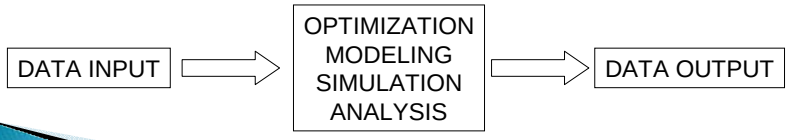


Example of a 3D Design Tool

CAD Design Software EPD
- Allows stacking of multiple substrates
  - Substrates may be chip, interposer, package, substrate, PCB
- Stack interconnected by bump, pillar, TSV, ball…
  - Creates a single composite substrate
    - Design, simulation and optimization of the entire assembly
  - Each component in the stack can be extracted as a single element
    - Distributed collaborative design
    - Sub-modeling, circuit simulation
    - Manufacturing, CAD/CAM files

EPD 3D Package Design Flow





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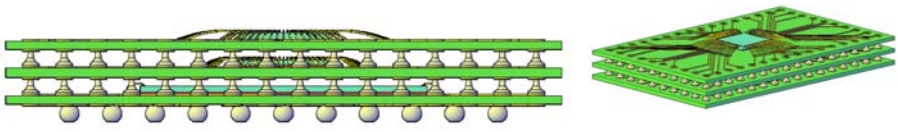
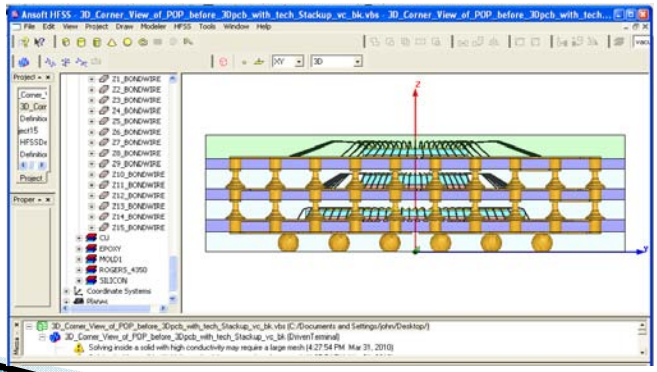
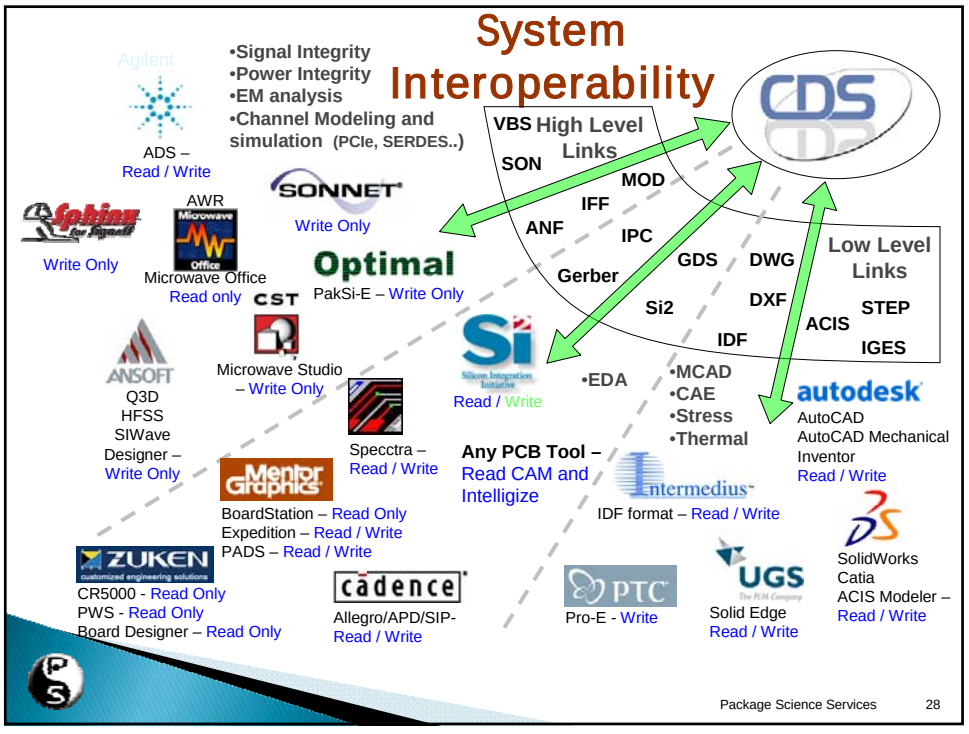
EPD 3D Model of POP





Package Science Services 26

Data in, Data Out
Interoperability
Modeling and Simulation



Tools

- Some commercial tools for electrical modeling and analysis
  - FEM, FDTD, PEEC, MOM and other solution methods
  - Typically include internal or third-party circuit generation and simulation engines
  - Output may be s-parameters, SPICE or HSPICE circuits, lumped or distributed circuit models

ANSOFT
Q3D
HFSS
SiWave
Designer

Microwave Office
Microwave Office

SONNET

CST
Microwave Studio

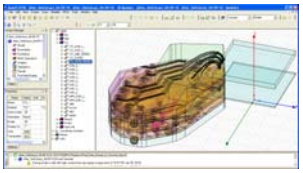
Sphinx

Optimal
PakSi-E

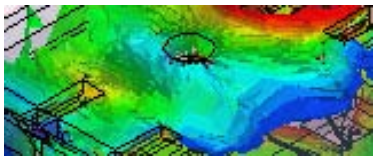
ADS

Full-Wave Solution

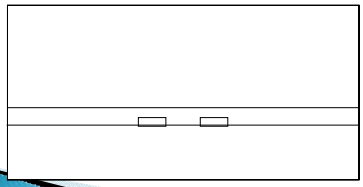
- Examples of results from full-wave solvers
- E field in EMI study, E field results for coupled transmission line

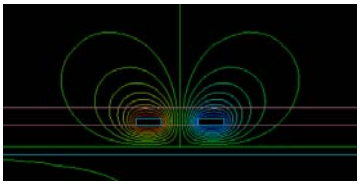


Geometry



Field Strength





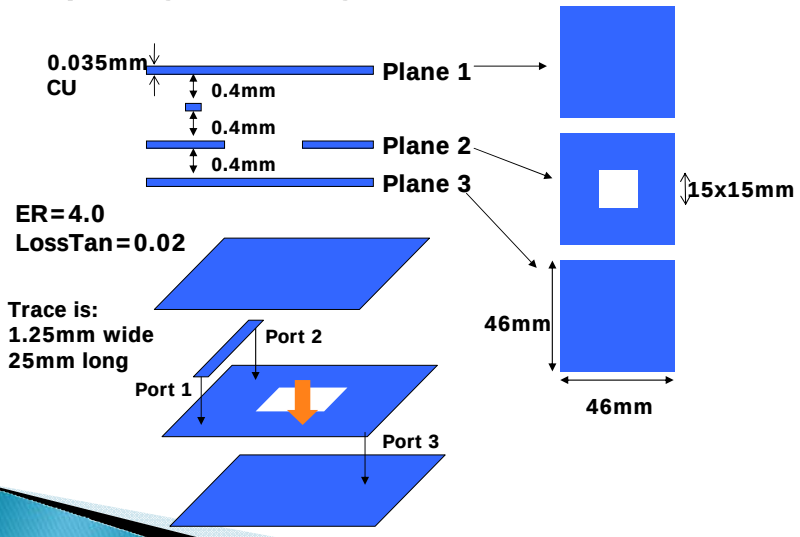
Plane Coupling and Discontinuities

- E-Systems SPHINX Signoff
  - Co-modeling and simulation of traces and planes
  - Multilayer Finite Difference Method
  - Extract frequency domain information, convert to circuit model, simulate
  - Allows concurrent design and optimization
    - Current/voltage distribution, decoupling requirements for power networks
    - Trace impedance, coupling from trace-to-trace, trace-to-plane
    - Effect of return path discontinuities (RPD)
      - Inconsistent planes (gaps, holes)
      - Layer-to-layer transition effects (vias, vertical connections)

Multilayer Modeling Example

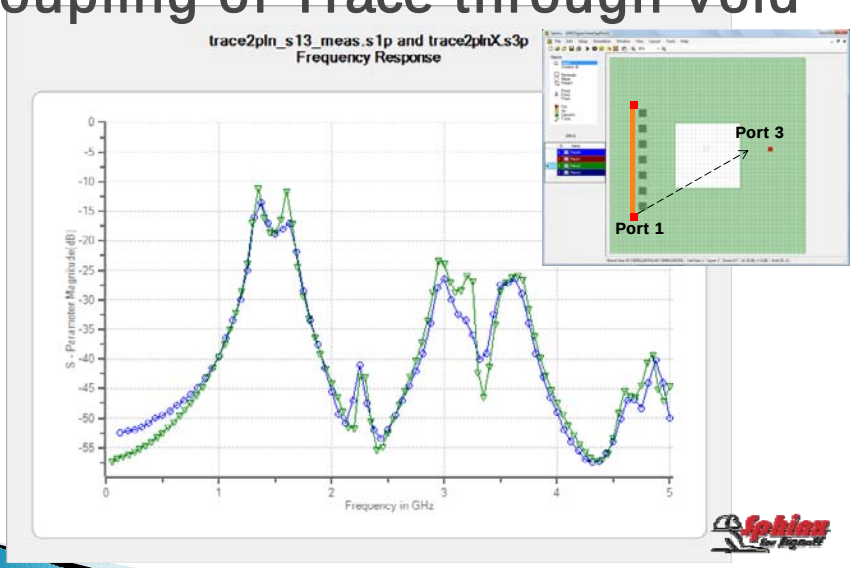
- Coupling of a trace through a void in a plane
  - Transmission paths are typically not 'straight through'
    - Changes in impedance due to gaps, voids, degassing holes, layer changes and trace-to-trace and trace-to-plane distances, microstrip to stripline
  - It is necessary to understand the effect of these aberrations in the signal path
  - Placement of decoupling elements

Objective: Accurately Capture Coupling through a Void in a Plane

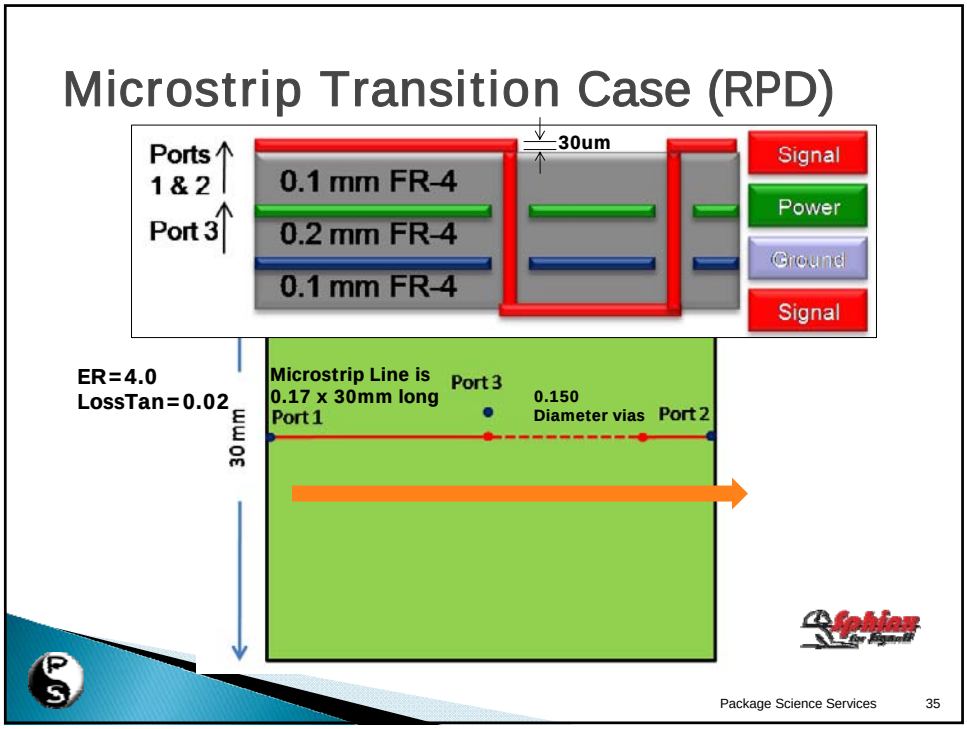


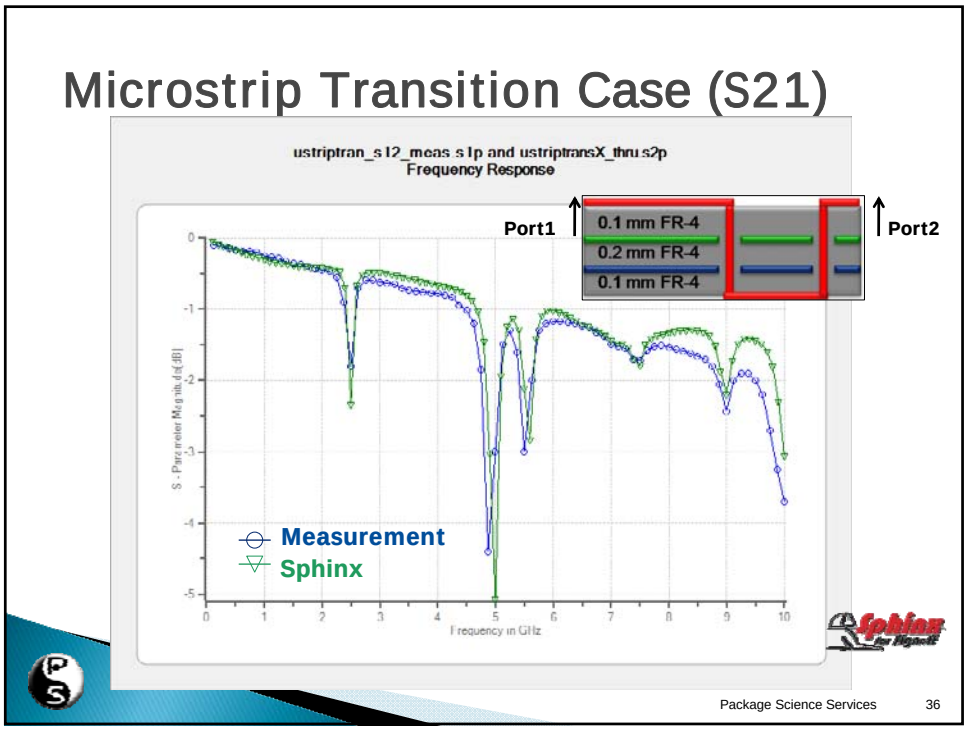
Package Science Services 33

Coupling of Trace through Void

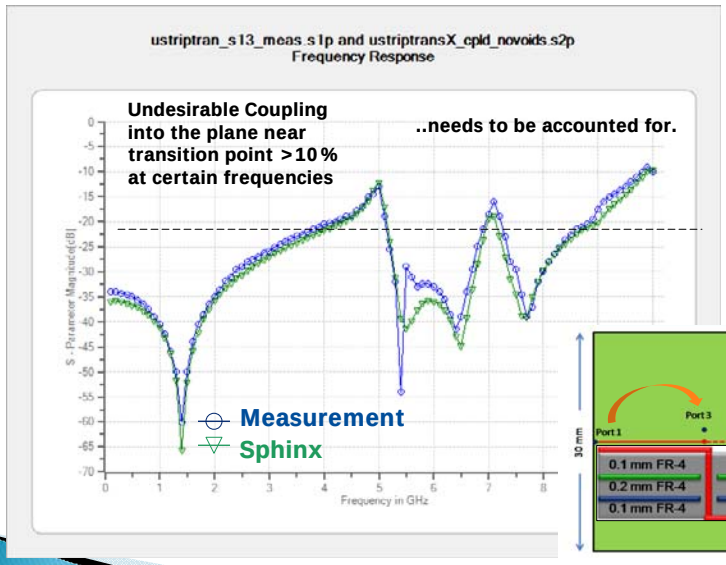


Package Science Services 34


Microstrip Transition Case (RPD)
Ports 1 & 2
Port 3
30um
0.1 mm FR-4
0.2 mm FR-4
0.1 mm FR-4
Signal
Power
Ground
Signal
ER=4.0
LossTan=0.02
30 mm
Microstrip Line is 0.17 x 30mm long
Port 1
Port 3
0.150 Diameter vias
Port 2
Package Science Services
35


Microstrip Transition Case (S21)
ustriptran_s12_meas s1p and ustriptransX_thru s2p
Frequency Response
Port1
Port2
0.1 mm FR-4
0.2 mm FR-4
0.1 mm FR-4
Measurement
Sphinx
Frequency in GHz
Package Science Services
36

Microstrip Via Transition Coupling to a Plane



Simulation

- Circuit models generated from s-parameter or time-domain or both
- Circuit model topology determined
- Circuit model subjected to stimulation
- Frequency response, signal distortion, eye diagram analysis
- SPICE, other simulation engines

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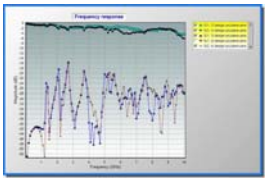
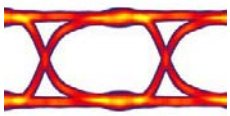
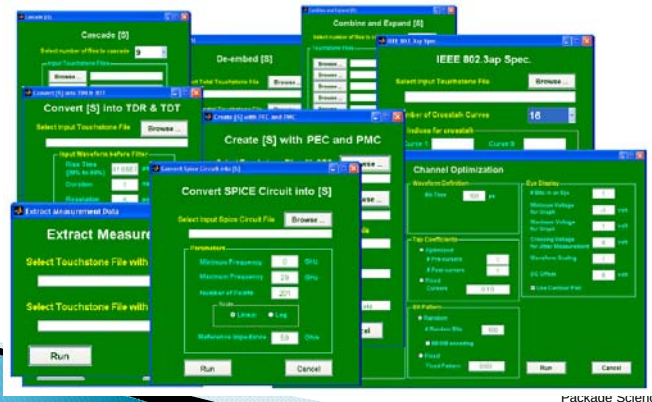


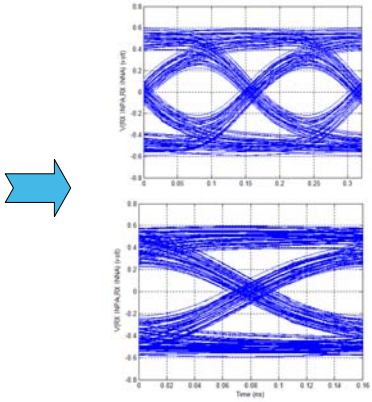


Simulation and Data Correlation

- AtaiTec ADK Advanced SI Design Kit
  - ADK is a toolkit which contains a multitude of tools for signal analysis, data correlation and correction, 2D extraction tools and simulation engines



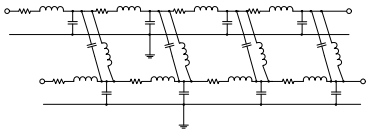
Simulation Example (ADK)



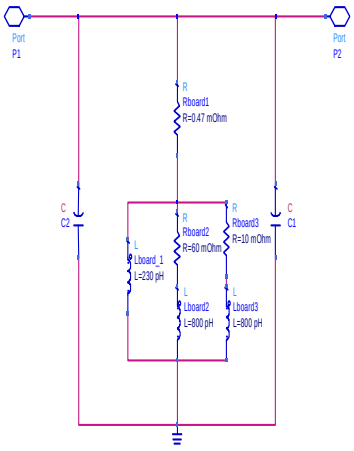
```
Maximum positive = 0.224461 volt at t = 0.0064 ns
Minimum negative = -0.21754 volt at t = 0.1584 ns
Maximum eye height = 0.441001 volt at t = 0.1584 ns
Eye height = 0.440938 volt at t = 0
Eye width = 0.109645 ns at greater than 0.1 volt p-p
Fuzz = 0.0356489 ns at 0 volt crossing
```

Circuit Topology and Results

- Circuit topology based on physical structure and number of elements needed to accurately describe behavior
- Optimize components and topology to obtain best fit

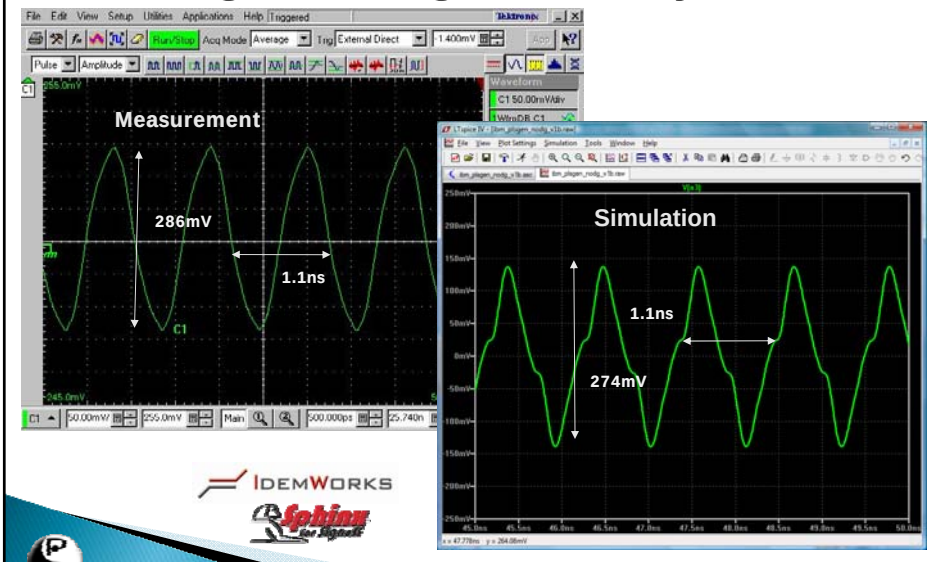


Distributed model



Chip Capacitor Equivalent Circuit

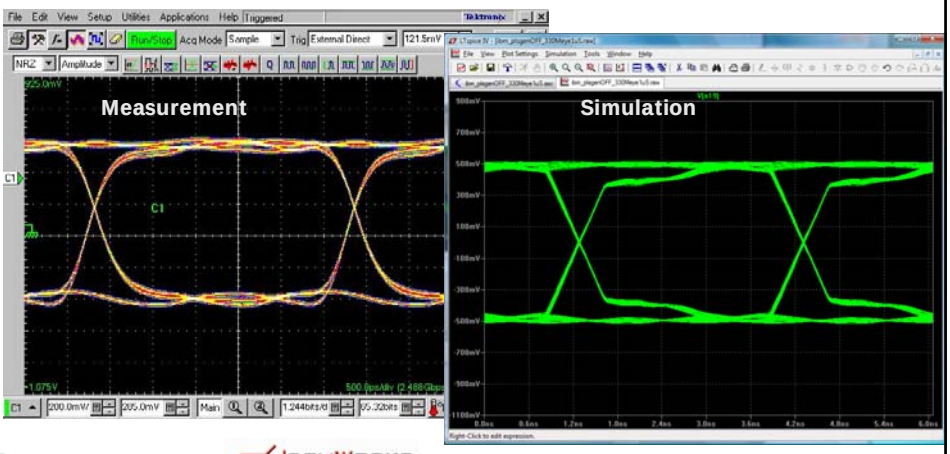
Timing and Signal Analysis



IdemWorks

Sphinx

Eye Diagram Analysis



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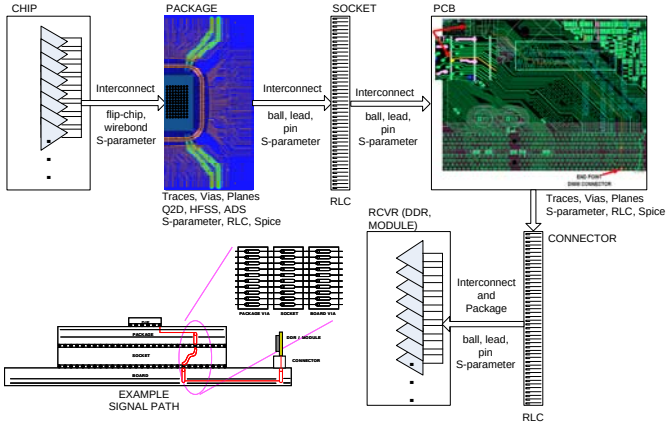
System Level Modeling and Simulation



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Conclusion

- High performance packaging requires many disciplines to select, design, characterize and manufacture
- Package design for high performance devices should be considered at the outset of chip design
- Electrical signal and power integrity are key to successful packaging of high speed digital products
- 3D tools for modeling and simulation are evolving to meet the needs of stacked packages and vertical interconnect methods such as TSV
- A series of lectures on measurement and modeling are planned for the future

THANK YOU!

Package Science Services LLC

Tom Tarter
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www.pkgscience.com

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