Greetings from Georgia Institute of Technology
3D Systems Packaging Research Center

Moore’s Law for System Integration
Focus of Last 50 Years; Moore’s Law for ICs
Focus of Next 50 Years; Moore’s Law for Systems

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Oct 12, 2010

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Joseph M. Pettit Endowed Chair
Professor in ECE & MSE

GT PRC

- Began as an NSF ERC
- Home for SOP Concept
- Integrated Approach to Research Education & Industry Collaboration

1. Leading Edge 3D Systems R&D
2. Educate Future Leaders
3. Collaborate with Global Industry & Academics
4. Enabled by $40M 300mm SOP Facility

3D Systems Center
Digital, RF & Bio Convergence
20 Academic & Research Faculty
70 Global Companies
GT PRC as An Academic Leader

- Economics
  - Generated $247M research and infrastructure dollars
  - Collaborated with 198 companies, 15 government agencies
  - Created 4 spin-out and 4 spin-in companies
  - Contributed $351M to State of Georgia economy

- Leading-Edge Research:
  - 1,200 refereed journal papers
  - > 249 invention disclosures
  - 36 patents awarded; 6 patents pending
  - 166 royalty/royalty-free licenses
  - 97 documented tech transfers
  - $40M state-of-the-art laboratories
  - Received 50 Best Paper awards

- Education
  - Granted 181 B.S, 283 M.S and 198 Ph.D. degrees
  - Designed 10 undergrad and 19 graduate cross-discipline courses
  - Published 4 text/reference books

Presentation Summary

- Si CMOS expected to reach limits due to:
  - Leakage and Performance
  - Potential Solutions: FD SOI, Fin FET, 3D ICs

- 3D ICs coupled with 2D ICs poised to be strategic

- Systems need more than 2D & 3D ICs for highest-functionality at lowest cost and in smallest size

- Moore's Law for System Integration (MLSI) addresses this bottleneck

- Quantum jump in systems requires more than run-of-the-mill manufacturing

- MLSI requires new and fundamental concepts in Electrical, Mechanical, Chemical, Thermal, Bio, Material Sciences, Engineering and Manufacturing

- MLSI provides unique and challenging opportunities in interdisciplinary research, education, and industry collaboration
Georgia Tech PRC Vision

SINGLE FUNCTION
Digital

MULTI-FUNCTION
Digital, RF, MEMS, analog, video

MEGA-FUNCTION-Vision of GT PRC
all the above and thousands of sensors


Functional Density or Component Density (cm³)

LG Video Phone Watch
- Featuring:
  - Full touch screen
  - Camera
  - Speaker
  - Bluetooth
- Bionic gadget can:
  - Play music
  - Take photos
  - Schedule appts
  - Read text messages
  - Make video calls

Apple's iPhone 4
- Featuring:
  - Multi-touch display
  - Dual cameras
  - Three-axis gyroscope
  - Camera and LED
- Bionic gadget can:
  - Play music, movies
  - Take photos
  - Record videos
  - Stream TV shows
  - Locate nearest Metro station in Paris
  - Over 200,000 applications
Georgia Tech-PRC Vision of 3D Systems

- Moore’s Law in 2D
- Packaging of 2D Devices

- Memory
- Logic
- Memory
- Power
- Sensors
- Logic
- Memory

Moore’s Law in 3D
Packaging of 3D ICs
Georgia Tech-PRC Vision of 3D Systems

- Moore's Law for System Integration
- Packaging of 3D Systems

- Discrete Components
- Organic Packages / Boards
- SMT

- Thin Film Passives
- Si / Glass Packages
- um SMT

- Nano Passives
- Nano TIM
- All Si System

Why 3D Integration?

- Interconnections on-chip
- High performance
- Low power
- High design and manufacturing cost

- MCM interconnections
- Lower
- Higher
- Lower

- Vertical interconnections
- Lower
- Higher
- Lower

- Shortest by TSV
- Higher
- lower

Source: Advanced Industrial Science and Technology (AIST)
Georgia Tech-PRC Vision of 3D Systems

- 3D Systems
- 90% System
- 600mm SOP

GT – PRC Focus

3D Systems

- 3D ICs - CMOS and non-CMOS
- 200-300 mm wafers
- 10% System Miniaturization

2D ICs

- CMOS ICs, 300nm Wafer Fabs

3D SYSTEMS
- Consumer
- Energy
- Automotive
- Healthcare
- Computer

Passives: R, L, C, Antennas

Power Sources

System Interconnections & Reliability

System Design Tools

MLSI Vision

- 2D ICs
- 3D ICs
- 3D Systems

MOORE’S LAW FOR SYSTEM INTEGRATION

- Highest functionality
- Smallest size
- Lowest cost
Difference between SIP, SOP and 3D ICs

SIP Means Stacked ICs and Packages (SIP)

SIP Stacked ICs
SIP Stacked Packages
3D ICs with TSV

2D and 3D ICs in MLSI

Moore’s Law for System Integration
Vision @ GT PRC

Ultra-Thin Silicon (30µm) with TPV

NANOMATERIALS
EMBEDDED COMPONENTS
INTERCONNECTIONS
SUBSTRATES & SYSTEM INTEGRATION

POWER & BATTERIES
MIXED SIGNAL ELECTRICAL DESIGN
THERMAL
MECHANICAL DESIGN FOR RELIABILITY

HIGH DENSITY I/O

IEEE Santa Clara Valley Chapter, Components, Packaging & Manufacturing Technology Society

10/12/2010
Grand Challenges in MLSI

- **Moore’s Law in 2D**
  - ICs beyond 22 nm and with ULK
  - Packaging of 2D ICs
  - Processor-driven Thermal challenges
- **Moore’s Law in 3D**
  - 3D ICs (with TSV) stack
  - TSV, Interconnections, Thermal
  - Interposer Packaging
- **Moore’s Law for System Integration**
  - Thin film Passives: miniaturized and better properties
  - Interconnections: Chip-level and Board-level
  - Thermal Technologies: Miniaturization-driven
  - Miniaturized and High-Density Batteries
  - Miniaturized Packages and Boards
  - System Design Tools

Grandparent

- There’s only one perfect grandchild in the world
- Every grandparent has it
Moore’s Law in 2D

- Challenges in 2D
  - Ultra-low Power and yet ultra-high Performance
  - ULK integrity
  - Si CMOS beyond 16nm
    - Performance
    - Leakage

Si CMOS beyond 16nm
- FD SOI and Fin FET
Grand Challenges in 3D Stack

- TSV: Cost and Manufacturing Infrastructure
- TSV to TSV interconnection @ 10 µm pitch
  - Materials and Processes
  - Underfill encapsulation
  - ULK reliability

PRC Strategy

1. Cu Pad
2. WL underfills
3. S-shaped TSV coatings
4. Bonding
5. Sin Sn
2D ICs vs. 2D Packages vs. 3D ICs

- Smallest form factor
- Increased electrical performance
  - Shortest interconnect length
- Reduced power consumption
- Heterogeneous integration of RF, memory, logic, MEMS, with optimized process nodes
3D IC Fundamentals

- 5-15µm Underfill
- Fine Pitch Interconnections
- TSV for Signal
- TSV for Power
- Power Delivery
- External Interface
- Interposer
  - Embedded LCR
  - 10X Flip-chip Interconnections
  - High-speed Signal
  - Lower Power Dissipation
  - Low Cost

Source: Advanced Industrial Science and Technology (AIST)

3D Packaging & Integration Evolution

**Past**
- Piggyback DIP: IBM, 1973
- Stacked TSOP: DST Modules, Inc.

**Recent**
- Chip Stack by Wirebonding: ChipPac
- POP + Chip Stack: Sharp
- POP + Chip-on-Chip: IMEC

**Emerging**
- Chip Stack by TSV: Bosch, TruSi etc.
- Ultra Thin W2W and D2W Stacking: IBM, Tohoku Univ, DARPA VISA, IMEC etc.
- Si Thru Via ASET
- Ultra Thin RF modules by EMAP by GT PRC
3D Package Integration Evolution

- Flip-Chip or Wire Bond: Mature
- Wire Bond: Mature
- PoP: Emerging
- Embedded: Emerging
- WLP: Emerging
- Edge Traces: Emerging
- TSV: Emerging

Source: Yole

3D ICs begin with Memory Stack with TSV

- eMMC memory package
- 8 memories + 1 controller

Source: Nokia
Si Interposer for ULK and wide I/O

- Silicon Interposer
  - Driven by
    - Die vs. substrate pitch
    - Ultra Low-k
  - Higher cost by wafer-based
  - Lower cost by panel base

- Wide IO Logic-Memory with TSV
  - Driven by
    - Performance
    - Bandwidth
    - Smaller power consumption
    - Size
  - Higher cost by wafer-based
  - Lower cost by panel base

Source: Nokia

Future 3D IC Applications

- Hetero-integration & SoC Partition
  - Driven by performance requirements
  - Interconnect density
  - New partitioning choices
  - Trace length reduction
  - Power distribution
  - “More than Moore”
  - KGD needed
  - Future technology

- “True 3D IC”
  - Driven by size and performance, the ultimate integration
  - Overall cost needs to be in place
  - KGD and Standards needed
  - Future technology

Source: Nokia
Interposers for Packaging 3D ICs

- Challenges
  - High I/Os @ less than 30 um pitch
  - Low cost/I/O

IC Package Technology Trend

- 1970s: Leadframe
- 1980s: Ceramics
- 1990s: Organics WLP
- ~2013: Silicon & Glass Packages
WLP vs. Panel-Based Interposer

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>WLP</th>
<th>Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large Wafer or Panel</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Miniaturized Components</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Low-cost Materials and Processes</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>High-throughput Tools</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Low-cost Facilities</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Smallest Package Size</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Thermal Performance</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Ideal Properties of a Package Material

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Ideal Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td>High resistivity, Low loss</td>
</tr>
<tr>
<td>Physical</td>
<td>Smooth surface finish, Large area availability, Ultra thin</td>
</tr>
<tr>
<td>Thermal</td>
<td>High Conductivity, CTE matched to Si</td>
</tr>
<tr>
<td>Mechanical</td>
<td>High strength, High modulus</td>
</tr>
<tr>
<td>Chemical</td>
<td>Resistance to process chemicals</td>
</tr>
<tr>
<td>Processability</td>
<td>Ease of Via formation and metallization</td>
</tr>
<tr>
<td>Cost</td>
<td>Low cost per I/O at 25um pitch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Materials</th>
<th>Glass</th>
<th>Silicon</th>
<th>Plastic</th>
<th>Metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal</td>
<td>Good</td>
<td>Poor</td>
<td>Fair</td>
<td>Poor</td>
</tr>
<tr>
<td>Properties</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Why Panel-based Glass & Si Packages?

- Ceramic
- Organic
- Silicon Interposer
- Panel-based Glass & Si Packages

Cost/I/O vs. I/O Pitch (µm)

3D ICs

2D ICs

10x

50 100 150 225

Multichip SaGI Interposer Module

- Large Si-interposer and size

Source: Nokia
Combine Interposer and Package into One

GT Packaging R&D

1. Electrical Design
2. Mechanical Design
3. 2Ds and 3D ICs
4. Package Substrates
5. Components
6. Interconnections
7. Thermal
8. System Integration
### Superiority of Glass Over Silicon

#### EM Model

![EM Model](image1)

#### TPV

<table>
<thead>
<tr>
<th>Material</th>
<th>Insertion Loss (dB) @5.4GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>GLASS</td>
<td>0.74</td>
</tr>
<tr>
<td>Si 1000 Ω-cm (High Resistivity)</td>
<td>2.02</td>
</tr>
<tr>
<td>Si 10 Ω-cm (Low Resistivity)</td>
<td>15.35</td>
</tr>
</tbody>
</table>

#### 3D View of a Filter

![3D View of a Filter](image2)

#### Glass and Silicon Resistivity

![Glass and Silicon Resistivity](image3)
Capacitor & Inductor Components in Glass

Stitched Capacitors

- Parallel Plate: $2.98 \times 0.64 \times 0.25 = 0.65 \text{ nF}$
- Vertically stitched: $2.65 \times 0.29 = 0.78 \text{ nF}$
- Horizontally stitched: $2.79 \times 0.31 = 0.86 \text{ nF}$

Via Based Inductors

- Reduced Shunt Parasitics
- Ease of design and routability
- Miniaturization

1st Demonstration of Glass Package with TPV Metallization

- TPV fill 50µm pitch vias
  - Via entrance: 150 µm
  - Via exit: 50 µm
  - TPV pitch: 250 µm
  - Glass thickness: 175 µm

- TPV fill 250µm pitch vias
  - Via entrance: 35 µm
  - Via exit: 22 µm
  - TPV pitch: 50 µm
  - Glass thickness: 175 µm

V.Sridhran, GTPRC
Glass Substrate R&D To-date

- Glass IPD (ST)
- Photonic System-in-Package (IZM)
- Glass Substrates (Longborough)
- Glass Wafer (NEC Schott)
- 3D Thin Film Interposer Based on TGV (IZM)
- Photosensitive Glass (Life Bioscience)

Through Package Via in Glass

- Mechanical Drilling in 200mm Glass (GT PRC)
- Photosensitive Glass (Life Bioscience)
- Schott Glass (NEC-Schott)
- Laser Ablation (GT PRC)
- Chemical (Natl Inst R&D of Microelectronics)
Miniaturized Boards

- Converge Packages and Boards into Miniaturized System Packages
- Develop Micro SMT

MLSI Must Eliminate the Gap

![Graph showing lithographic dimension (nm) over time from 1970 to 2020 with gaps indicated for IC System and Package.]
IC Level Interconnections

- Challenges
  - 10-100X more than Flipchip
  - Ultra-short interconnections
  - ULK reliability without underfill

Chip and Board Level Interconnections

IC-to-Packaging Interconnection

- Wirebond
- Flip-Chip
- Chip-First
- Chip-Last
- TSV

Package-to-Board Interconnection

- PGA
- LGA
- BGA
- Zero-Stress Interconnect
Why Embedding?

- I/O Density/mm³
  - Wire Bond ➔ Flip Chip ➔ 10X Flip Chip ➔ 100X Flip Chip

- Functional Density/mm³
  - Smart Phone Functionality ➔ Mega-functionality

- Heterogeneous Integration Density/mm³
  - Digital CMOS ➔ RF, Optical, Analog, Sensor

Embedded Strategy for I/O Density

- HVM - Flip-Chip
  - Organic Package
  - Flex
  - Molded
  - New Infrastructure
  - New Business Model
  - 10x flip chip
  - Reworkable

- LVM - 10x flip Chip
  - New Infrastructure
  - New Business Model

- R&D - Chip-First IC
  - 10x flip chip
  - Reworkable
  - Existing Infrastructure
  - Heterogeneous Integration

I/O Density (per chip area)

1x ➔ ~4x ➔ ~10-40x
1. Embedded MEMS, Activies and Passives (EMAP)
2. 9X higher I/O density than flip chip
3. Subsystem embedding
4. ULK compatible
5. Existing manufacturing infrastructure
6. Compatibility with activities, MEMS, and power components
### Two Approaches to Embedded Actives

<table>
<thead>
<tr>
<th></th>
<th>Flip-Chip</th>
<th>Chip-First</th>
<th>Chip-Last @ GT PRC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Schematic</strong></td>
<td><img src="image1" alt="Flip-Chip Schematic" /></td>
<td><img src="image2" alt="Chip-First Schematic" /></td>
<td><img src="image3" alt="Chip-Last Schematic" /></td>
</tr>
<tr>
<td><strong>Substrate</strong></td>
<td>Laminate</td>
<td>Carrier / Mold / Tape</td>
<td>Laminate</td>
</tr>
<tr>
<td><strong>Interconnect</strong></td>
<td>C4 100-150µm, 50-80µm</td>
<td>RDL via 40-80µm, 3-10µm</td>
<td>Cu-Cu bonding 30-50µm, 5-15µm</td>
</tr>
<tr>
<td><strong>Assembly</strong></td>
<td>Solder reflow</td>
<td>RDL process</td>
<td>Thermocompression</td>
</tr>
<tr>
<td><strong>Testability</strong></td>
<td>Known good die and substrate</td>
<td>Known good die and known good package challenges</td>
<td>Known good die and substrate</td>
</tr>
<tr>
<td><strong>Reworkability</strong></td>
<td>Yes</td>
<td>Challenge</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Manufacturing Infrastructure</strong></td>
<td>Existing</td>
<td>New infrastructure</td>
<td>Existing</td>
</tr>
<tr>
<td><strong>Wirebond die</strong></td>
<td>Needs redistribution</td>
<td>Can be used as is</td>
<td>Can be used as is</td>
</tr>
<tr>
<td><strong>MEMS Integration</strong></td>
<td>No cavity, surface only</td>
<td>Challenge</td>
<td>Cavity readily allows</td>
</tr>
</tbody>
</table>

#### 9X Flip-chip with 2000 Cycle Reliability

- **Ultra-Thin, Low CTE & Low Loss Organic Substrate**
- **Fine Pitch I/O Wiring with High Reliability**
- **Precise Laser Cavity for Ultra-Fine Pitch IC Embedding**
- **High Reliability Cu Microbump Interconnect at 30µm Pitch & 10µm Height**

- **High Isolation for Embedded Actives using EBGs**
- **High-Q Embedded Filters**
- **Embedded Die Reliability Demonstration**
1. Embedded MEMS, Actives and Passives (EMAP)
2. 9X higher I/O density than flip chip
3. Subsystem embedding
4. ULK compatible
5. Existing manufacturing infrastructure
6. Compatibility with activies, MEMS, and power components

Recent R&D at PRC

- 100 µm pitch lead-free flip-chip reliability
- 30um pitch chip-last interconnections
- G-Helix compliant interconnections
- Nano-Cu I/Os at 50um pitch
Board-Level Interconnection Challenges

- Challenges
  - SMT Pitch 400m, single biggest barrier to MLSI
  - Two Options
    - Converge Package and Board
    - Reduce pitch to 200m, 100m, 50m

Thermal

- Challenges
  - SOC or 2D Level
    - ULP devices
    - Nano thermal interfaces
  - 3D IC Level
    - Microfluidics for high power applications
    - High-K Interposers for consumer applications
  - System level
    - ULP devices
Thermal Management

- **Hand-Held**
  - Up to 60 W/cm² locally
  - TIM, Heat slugs and Heat Spreaders

- **Automotive**
  - 250 W/cm² projected
  - Reliability at 100-200°C

- **High-Performance**
  - 100-150 W/cm²
  - Fluidic Cooling

- **Cost-Performance**
  - 20-50 W/cm² at local hot spots
  - Cost constraints limit to air cooling

Thermal Interface Materials

- **BLT**
  - μm

- **Heat spreaders**

- **TIM1**

- **TIM2**

- **Thermal grease**

- **Indium**

- **Nanocomposite**

- **W/mK**

- **100**

- **500**

- **250**

- **10**
CNTs as TIM
Solder-assisted CNT Transfer

- Grow on silicon
- Aligned CNT bundles

- Reflow and remove Si

Source: C.P. Wong, GT - PRC
C.P. Wong, L. Zhu (U.S. Patent pending)

Thin film Passives

- From NMDC 2-4 slides
Miniaturized & High Storage Batteries

Packaging Materials: Yesterday and Tomorrow

<table>
<thead>
<tr>
<th>Materials</th>
<th>Current</th>
<th>Future</th>
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</thead>
<tbody>
<tr>
<td>Battery</td>
<td>Cylindrical Lithium-ion Battery</td>
<td>Nano porous silicon for</td>
</tr>
<tr>
<td></td>
<td></td>
<td>super-charged Li batteries</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lithium Titanium Oxide arrays</td>
</tr>
</tbody>
</table>

Nano porous silicon for super-charged Li batteries

Lithium Titanium Oxide arrays
MLSI Electrical Challenges

- Glass and Silicon Package
- Signal and Power Integrity
- Embedded Passive Design
- Mixed Signal Design and Tools
- TPV Design
- Interconnection Design

MLSI Mechanical Challenges

- Design-for-Reliability of Individual Failure Mechanisms
- Material Length Scale Effects in Mechanical Design & Modeling
- System-Design for Reliability with Chip-Package-System Interaction
GT PRC Global Industry Partnership

Europe
- ATOTECH
- BOSCH
- EPCOS
- INFINEON
- NXP SEMICONDUCTORS
- ST MICROELECTRONICS

China
- HUAWEI
- SAMEER
- TAMIC
- UNIMICRON

India
- SAMEER
- SAMSUNG
- HYNIX

Japan
- AGC ELECTRONICS
- DISCO
- IBIDEN
- MITSUBISHI
- MITSUBISHA GAS CHEMICAL
- NAMICS
- NGK-NTK
- OAK-MITSUI
- PANASONIC
- SONY
- SONY CHEMICAL
- TECNISCO
- ZEON CHEMICAL

U.S.A.
- ANVIK
- AMD
- BREWER SCIENCE
- BTU
- CORNING
- DOW
- DOW CHEMICAL
- DRAFTER LABS
- DUPONT
- ECI
- EVGROUP
- ENDICOTT INTERCONNECT
- GOULD
- HENKEL
- IBM

MEMBER COMPANIES
INTERESTED COMPANIES

Thank You

Prof. Rao R. Tummala
Director, 3D Systems Packaging Research Center
Joseph M. Pettit Endowed Chair
Professor in ECE & MSE