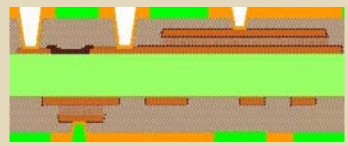
Embedded Passives

Packaging Paradigm of the Future?

Jason Ferguson

NSWC Crane

November 10, 2010



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Harnessing the Power of Technology for the Warfighter 1

Embedded Passives

Outline

- Overview of Crane
- Embedded Passives: What are they?
- Benefits of EP Technology
- What is slowing the adoption of EP Technology?
- EP Materials
- Emulator Project: Lessons Learned

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Harnessing the Power of Technology for the Warfighter 2


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WARFARE CENTERS
CRANE
CRANE DIVISION
NAVAL SURFACE WARFARE CENTER
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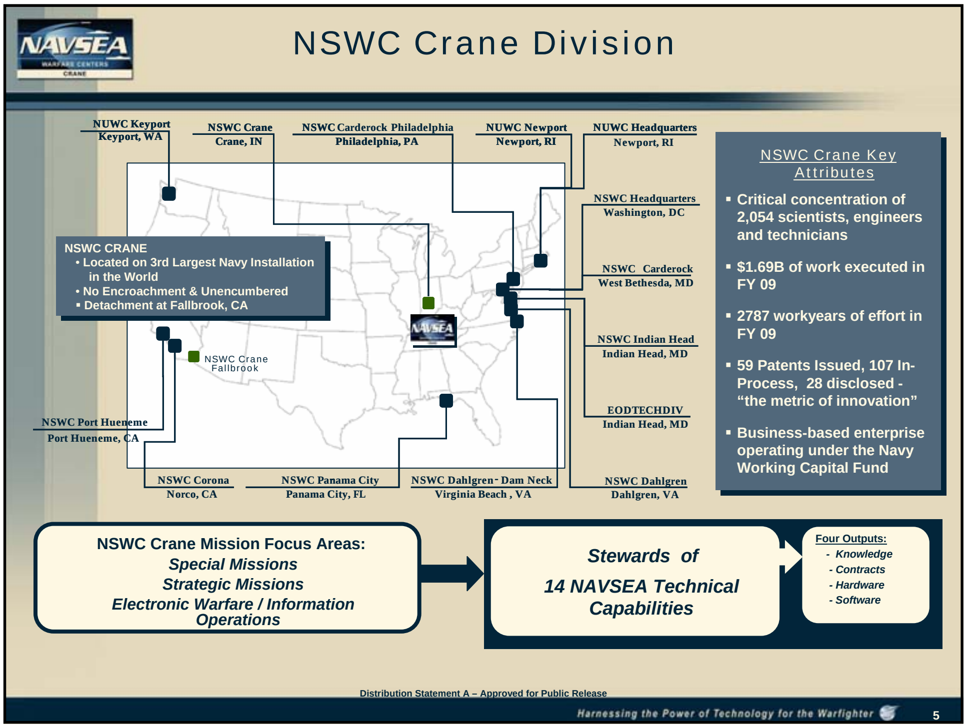
812-854-1210
Mr. Duane Embree
Technical Director
Duane.embree@navy.mil
812-854-3666
Harnessing the Power of Technology for the Warfighter
3


NAVSEA
WARFARE CENTERS
CRANE
SUPPORTING
THE WARFIGHTER
Harnessing the Power of Technology for the Warfighter


NAVSEA
NSWC Crane Division
NUWC Keyport
Keyport, WA
NSWC Crane
Crane, IN
NSWC Carderock Philadelphia
Philadelphia, PA
NUWC Newport
Newport, RI
NUWC Headquarters
Newport, RI
NSWC Headquarters
Washington, DC
NSWC Carderock
West Bethesda, MD
NSWC Indian Head
Indian Head, MD
EODTECHDIV
Indian Head, MD
NSWC Dahlgren
Dahlgren, VA
NSWC Dahlgren - Dam Neck
Virginia Beach , VA
NSWC Panama City
Panama City, FL
NSWC Corona
Norco, CA
NSWC Port Hueneme
Port Hueneme, CA
NSWC Crane Fallbrook
NSWC CRANE
• Located on 3rd Largest Navy Installation in the World
• No Encroachment & Unencumbered
• Detachment at Fallbrook, CA
NSWC Crane Key Attributes
▪ Critical concentration of 2,054 scientists, engineers and technicians
▪ $1.69B of work executed in FY 09
▪ 2787 workyears of effort in FY 09
▪ 59 Patents Issued, 107 In-Process, 28 disclosed - "the metric of innovation"
▪ Business-based enterprise operating under the Navy Working Capital Fund
NSWC Crane Mission Focus Areas:
Special Missions
Strategic Missions
Electronic Warfare / Information Operations
Stewards of
14 NAVSEA Technical Capabilities
Four Outputs:
- Knowledge
- Contracts
- Hardware
- Software
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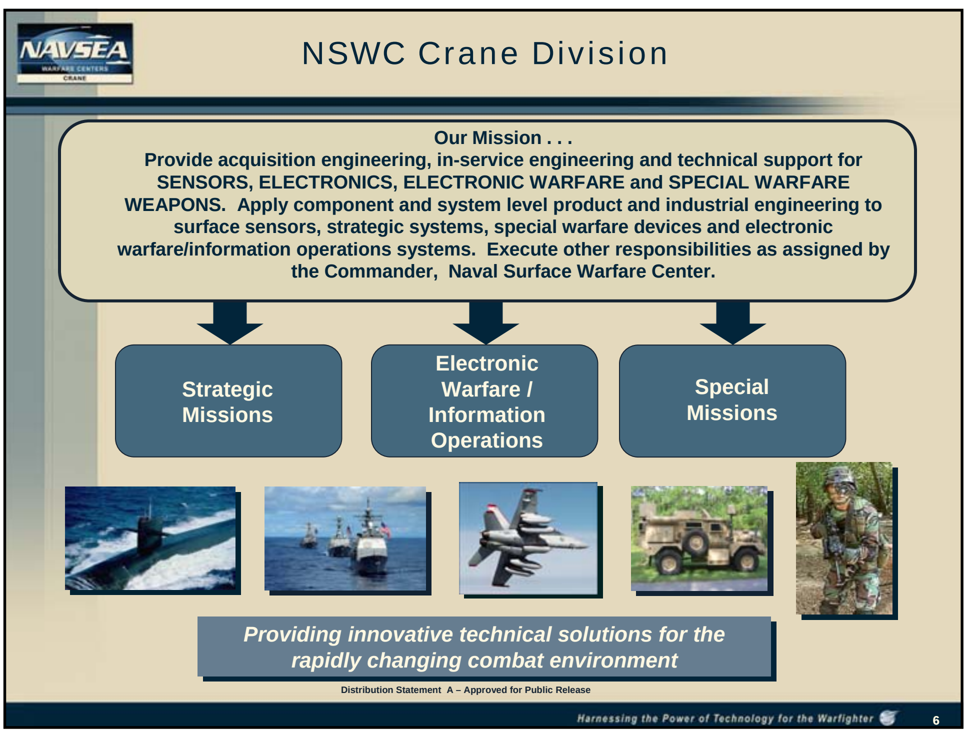
5


NAVSEA
NSWC Crane Division
Our Mission . . .
Provide acquisition engineering, in-service engineering and technical support for SENSORS, ELECTRONICS, ELECTRONIC WARFARE and SPECIAL WARFARE WEAPONS. Apply component and system level product and industrial engineering to surface sensors, strategic systems, special warfare devices and electronic warfare/information operations systems. Execute other responsibilities as assigned by the Commander, Naval Surface Warfare Center.
Strategic Missions
Electronic Warfare / Information Operations
Special Missions
Providing innovative technical solutions for the rapidly changing combat environment
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6


NAVSEA
STRATEGIC MISSIONS
DETER
DEFEND
DEFEAT
Harnessing the Power of Technology for the Warfighter
7


NAVSEA
Strategic Missions
Products and Thrust Areas
Crane provides a broad range of systems engineering expertise for the sustainment and modernization of the Land Based, Sea Based and Space Based Ballistic Missile Early Warning Sensors
Threat Detection
Every AEGIS BMD platform carries key components either designed, developed, tested or sustained at NSWC Crane.
MDA lead for Anti-Tamper technologies
Integrated Missile Defense
Experts in advanced missile technology, NSWC Crane leads the way in the design, development, production and sustainment of ballistic missile electronics
Global Strike
DoD resource for Critical Product Technologies including High Reliability, Radiation Hardened Electronics, Power Sources, High Power RF Devices and Printed Wiring Boards
Critical Technology Innovation Center
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8

Leadership

- DoD Executive Agent Microwave Devices
- DoD Executive Agent for Printed Circuit Boards
- STANDARD Missile Battery Technical Direction Agent for Power Systems
- CGX Acquisition Missile Defense Radar System Engineering Lead
- Leadership in Hardened Electronics And Radiation Technology
- Missile Defense Agency (MDA) Lead for Anti-Tamper Technology

Strategic Missions Capabilities

Resources

- Over 800 Technical Professionals
- 210,000 Sq Ft of StM Facilities
- World's most Powerful LINAC
- Premier facilities for FA/MA
- Full spectrum power system facility
- High power radar module facility
- Anti-tamper laboratory
- Critical Technology Innovation Center (CTIC)

Services

- Flight Engineering
- Radiation Science Technology
- Acquisition Engineering
- Missile Defense Components
- Power & Energy Solutions
- Failure & Materials Analysis
- Advanced RF Systems
- Anti-tamper Science
- Modeling and Simulation of Electronics

Partners

- Alliant Tech Systems
- Boeing
- Lockheed Martin
- Raytheon
- Indiana University
- Penn State University
- Purdue University
- Texas A&M
- Vanderbilt University

Recent Successes

- Advanced Electron-Photo Facility
- Hubble Telescope batteries
- SBX Radar Transition
- PrCB Executive Agent
- CWI TWT test capability


NAVSEA
WARFARE CENTERS
CRANE
ELECTRONIC WARFARE/
INFORMATION OPS
CONTROL THE SPECTRUM
CONTROL THE FIGHT
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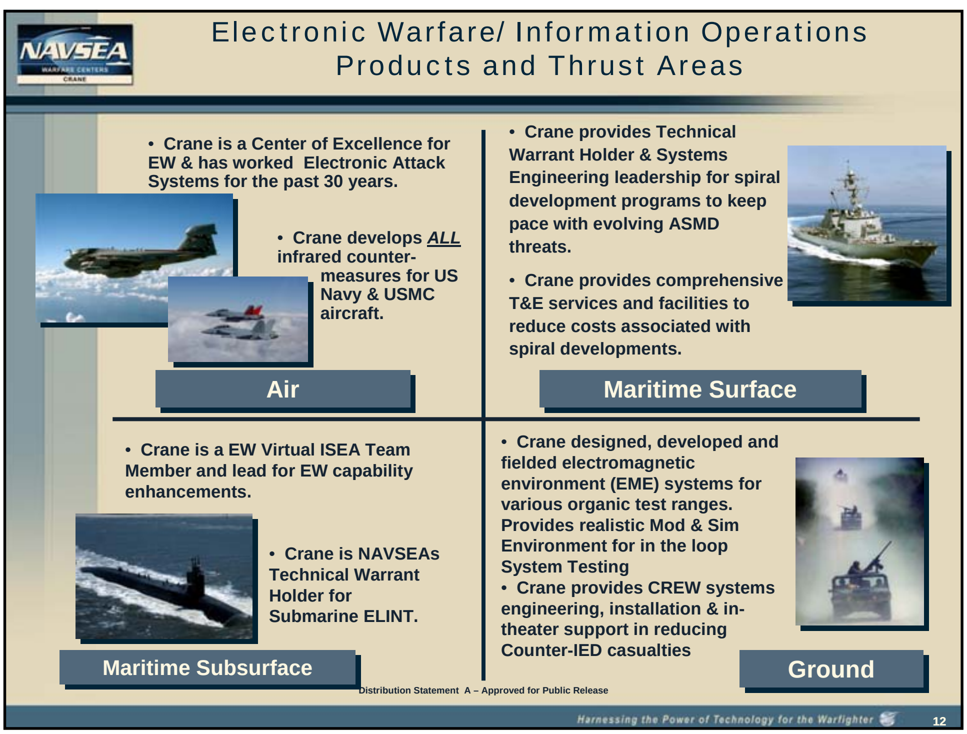
NAVSEA
WARFARE CENTERS
CRANE
Electronic Warfare/ Information Operations
Products and Thrust Areas
• Crane is a Center of Excellence for EW & has worked Electronic Attack Systems for the past 30 years.
• Crane develops ALL infrared counter-measures for US Navy & USMC aircraft.
Air
• Crane provides Technical Warrant Holder & Systems Engineering leadership for spiral development programs to keep pace with evolving ASMD threats.
• Crane provides comprehensive T&E services and facilities to reduce costs associated with spiral developments.
Maritime Surface
• Crane is a EW Virtual ISEA Team Member and lead for EW capability enhancements.
• Crane is NAVSEAs Technical Warrant Holder for Submarine ELINT.
Maritime Subsurface
• Crane designed, developed and fielded electromagnetic environment (EME) systems for various organic test ranges. Provides realistic Mod & Sim Environment for in the loop System Testing
• Crane provides CREW systems engineering, installation & in-theater support in reducing Counter-IED casualties
Ground
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12

Leadership

- NATO IRCM and Seeker Exercise Support
- DoDs Largest EW Footprint - Only government facility that is multi-spectral/multi-domain
- COMOPTEVFOR Trusted Agent for Surface Ship EW Test & Evaluation
- OPNAV Next Generation Jammer AoA Technical IPT Lead
- Navy Network Warfare Command (NNWC) EWIIP Technology IPT Lead
- ONR Next Generation Jammer Airborne Electronic Attack (AEA) Principal Investigator
- Naval EW Technology Integration Center (NEWTIC):

  - The Navy's Technology Transition Agent to the Fleet

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Harnessing the Power of Technology for the Warfighter 13

EW / IO Capabilities

Resources

- 1,588 Skilled Personnel
- 320,000 sq ft EW Complex
- Secure MILCON facilities
- Naval EW Technology Integration Center
- Information Operations Range
- Unique Nulka Round Assembly Facility

Services

- EW Modeling & Simulation
- Threat Analysis & Effectivity testing
- Anti-Ship Missile Defense
- Intelligence, Surveillance & Reconnaissance Support
- Airborne Infra-Red Countermeasures
- Electro-Optics/Infra-Red System Support
- Systems Engineering
- EW Modeling & Simulation

Partners

- Naval Research Lab
- Air Force Research Lab
- Army Research Lab
- Purdue
- Penn State
- Ohio State University
- Georgia Tech Research Institute
- Numerous OEMs

Recent Successes

- AN/SLQ-32(V) General Receiver Improvement Program Concept Demonstration
- JCREW Fielding
- JCREW 3.1 Field Operational Assessment in OEF
- JCREW 3.3 Preliminary Design Review
- CEASAR Testing

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NAVSEA
WARFARE CENTERS
CRANE
SPECIAL MISSIONS
RAPID RESPONSE
PROVEN SOLUTIONS
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NAVSEA
WARFARE CENTERS
CRANE
Special Missions
Products and Thrust Areas
Crane designed, built and fielded the first Counter-Sniper Enclosure for USAF Force Protection HMMWVs in 6 weeks
Mobility & Maneuverability
Crane is USSOCOM's PM for the development, acquisition, fielding and sustainment of the SOF Combat Assault Rifle (SCAR)
Special Munitions & Weapons
Crane integrates sensors on a variety of ground platforms for special missions
Sensors & Communications
To date Crane has provided Small Arms operations & maintenance training to 1641 personnel
Training
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16

Leadership

- Joint & Special Operations Program Management Office
  - Project Management support for USSOCOM, ASAF,USN and USMC
- Advanced Systems and Concepts (AS&C) TRUSTED AGENT for Non-Traditional Assessments & Technology Transition for Office of Secretary of Defense (OSD)
- Electro-Optics (EO) & Infrared (IR) Sensing Systems Leadership
- Small Arms and Weapons Technical Leadership
- Extensive Multi-Site Testing Capability
  - Camp Atterbury
  - Muscatatuck Urban Training Center (MUTC)
  - Multi-Site Ordnance Test Complex, Hawthorne, NV
  - Special Weapons Assessment Range
  - Glendora Lake Test Facility

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Special Missions Capabilities

Resources

- Extensive test facilities for expeditionary warfare, electro-optics, environmental, weapons and ballistics
- Over 1.3M sq ft of RDT&E facilities
- 720 person government workforce
- Realistic Ground Range Facility
- EO / IR Test Facility

Services

- Weapons, Sensors & Comm platform Integration
- Small Arms Weapons and Integration
- Rapid Standard and Non-Traditional Testing and Assessment Capability
- Broad In-Theater Support Capability
- Laser Test & Evaluation
- Pyrotechnics / Demolition Product Support

Partners

- Indiana National Guard
- Naval Research Lab
- US Army Night Vision & Electronic Sensors Directorate
- Penn State, Purdue
- Marine Corps Programs Office, Hawthorne, NV
- Joint Services Small Arms Synchronization Team
- Multiple Industry Partners

Recent Successes

- Mobile Technology Complex
- Shipboard Protection System
- Non-Traditional Test JCTDs
- Completed Electo-Optic Technology Roadmap
- 235,000 weapons accessories fielded to date

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Harnessing the Power of Technology for the Warfighter 18

Technical Assignments

NAVSEA Technical Warrants

Electro-Optics (EO) & Infrared (IR) Sensing Systems (except submarines)
Anti-Tamper Implementation
Electronic Warfare and SIGINT Programs (including Ground EW and Intelligence Collection Equipment)
Small Arms and Weapons
Shipboard Anti-Terrorism and Force Protection

DOD Executive Agent

Microwave Power Tube Industry
Printed Circuit Board Technology

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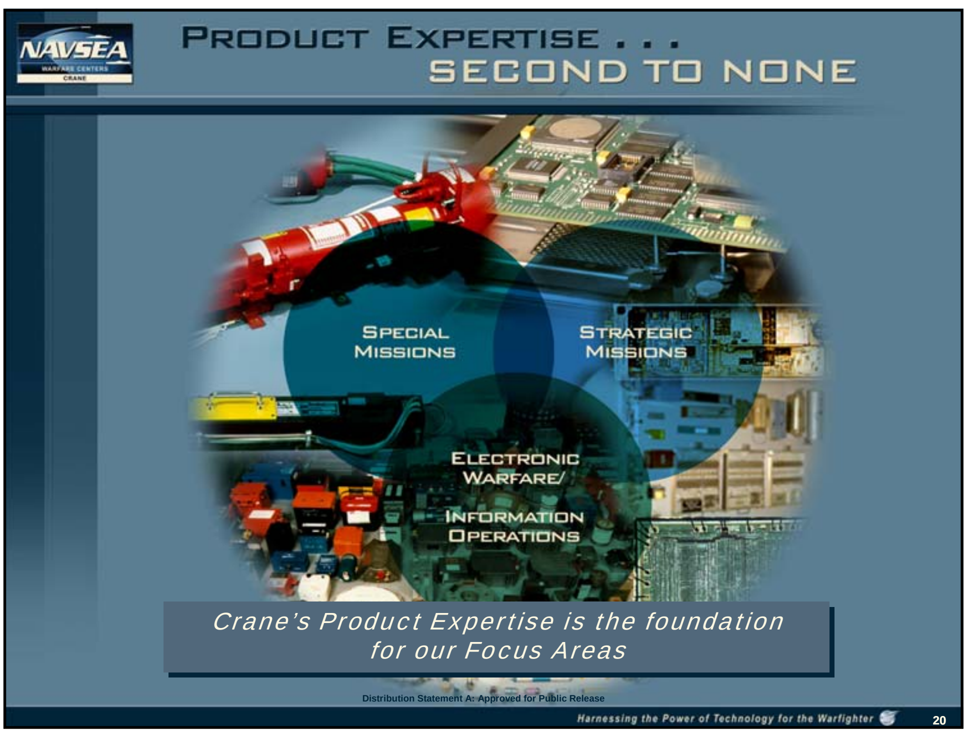

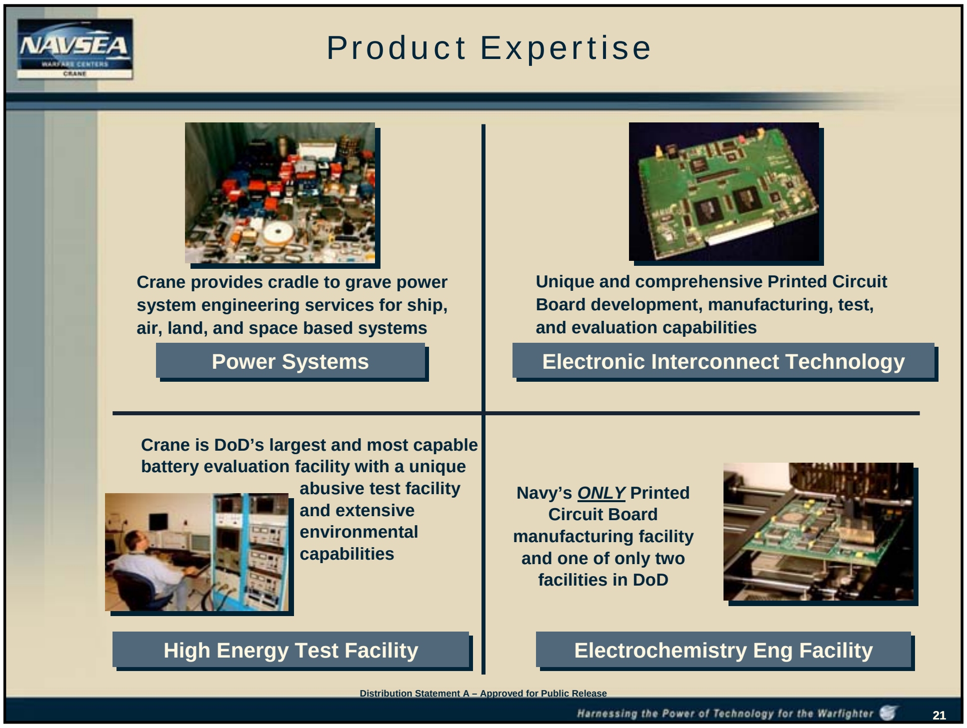
NAVSEA
WARFARE CENTERS
CRANE
Product Expertise
Crane provides cradle to grave power system engineering services for ship, air, land, and space based systems
Power Systems
Unique and comprehensive Printed Circuit Board development, manufacturing, test, and evaluation capabilities
Electronic Interconnect Technology
Crane is DoD's largest and most capable battery evaluation facility with a unique abusive test facility and extensive environmental capabilities
High Energy Test Facility
Navy's ONLY Printed Circuit Board manufacturing facility and one of only two facilities in DoD
Electrochemistry Eng Facility
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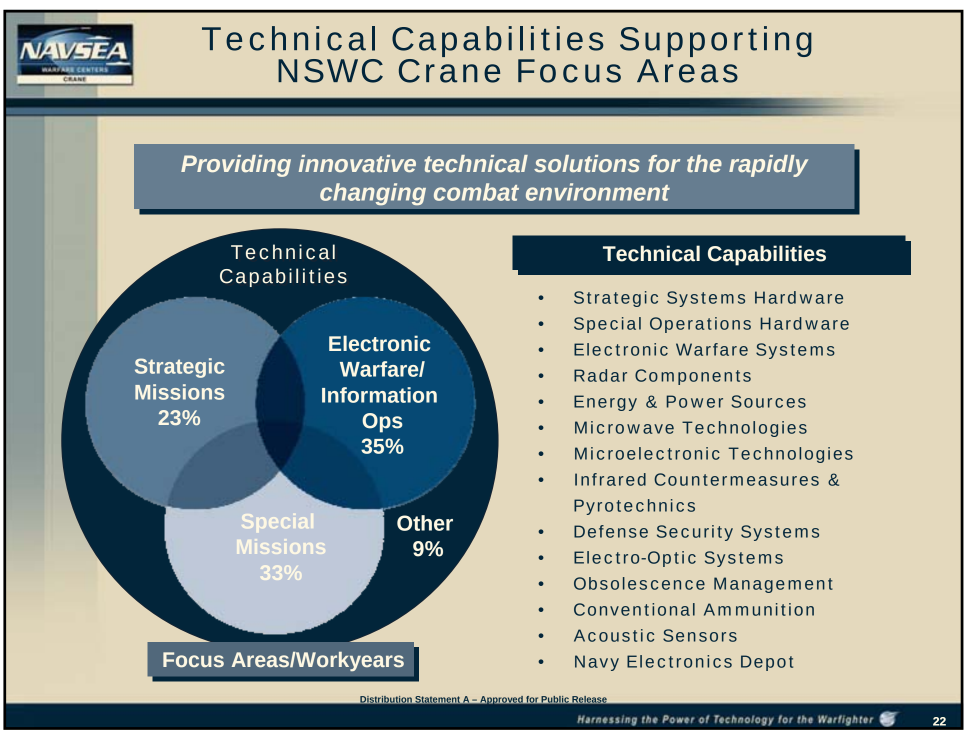
21


NAVSEA
WARFARE CENTERS
CRANE
Technical Capabilities Supporting NSWC Crane Focus Areas
Providing innovative technical solutions for the rapidly changing combat environment
Technical Capabilities
Strategic Missions 23%
Electronic Warfare/ Information Ops 35%
Special Missions 33%
Other 9%
Focus Areas/Workyears
Technical Capabilities
• Strategic Systems Hardware
• Special Operations Hardware
• Electronic Warfare Systems
• Radar Components
• Energy & Power Sources
• Microwave Technologies
• Microelectronic Technologies
• Infrared Countermeasures & Pyrotechnics
• Defense Security Systems
• Electro-Optic Systems
• Obsolescence Management
• Conventional Ammunition
• Acoustic Sensors
• Navy Electronics Depot
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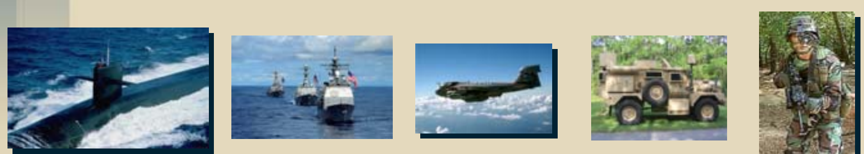
22

Summary

- NSWC Crane is critical to the Department of Defense, providing technical engineering solutions and total lifecycle leadership for many of the systems that protect and enable our Warfighters
- NSWC Crane's total focus is to support the Warfighter by leveraging our technical capabilities to provide innovative, leading-edge technical solutions for the rapidly changing combat environment
- Our employees honor the Crane core values to provide the diverse knowledge, skills and abilities to support the installation's technical capabilities
- This team of skilled professionals puts technical solutions directly into the hands of the Warfighter, ensuring safer missions and saving lives while practicing continuous process improvement every day
- NSWC Crane supports the NAVSEA Goals of building an Affordable Future Fleet, Sustaining Today's Fleet Efficiently and Effectively, and by Enabling our People.



Keeping America's Navy #1 in the World

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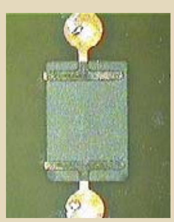
Embedded Passives

What are they?



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Embedded Passives

What are they?

Passive Components
- •Resistors and capacitors (for this discussion)
- •Provide/absorb energy
  - – Maintain constant V or A
- •Filter signals
- •Control impedance
- •Sense signals
- •Delay or synchronize signals

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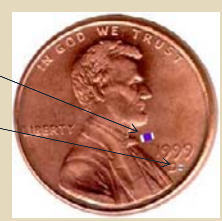
Embedded Passives

Where are they?

0402 resistor:
- • (It's the same size as President Lincoln's bow tie)

0201 capacitor:

Now inspect 2000 parts like this on one board.



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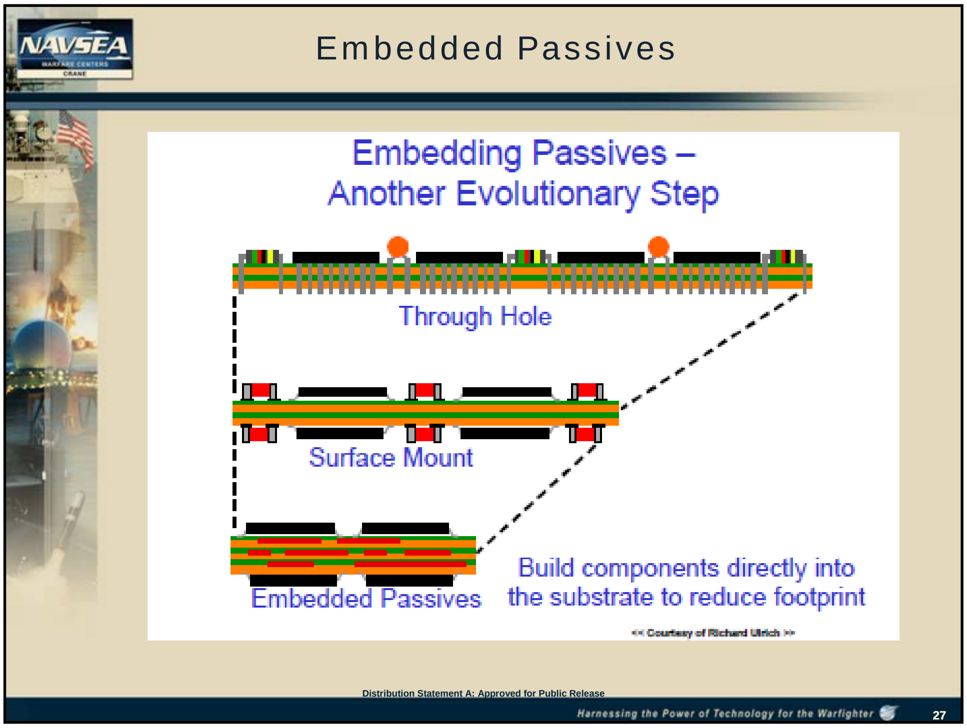
Embedded Passives
Embedding Passives –
Another Evolutionary Step
Through Hole
Surface Mount
Embedded Passives
Build components directly into
the substrate to reduce footprint
<< Courtesy of Richard Ulrich >>
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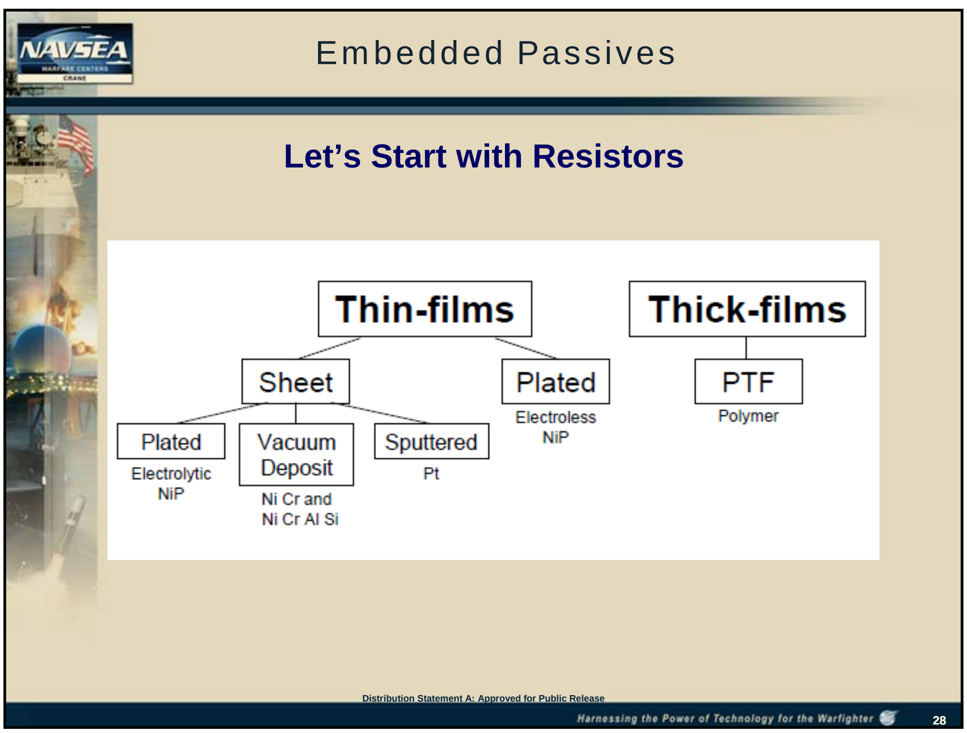
27


Embedded Passives
Let's Start with Resistors
Thin-films
Thick-films
Sheet
Plated
Electroless
NiP
PTF
Polymer
Plated
Electrolytic
NiP
Vacuum
Deposit
Ni Cr and
Ni Cr Al Si
Sputtered
Pt
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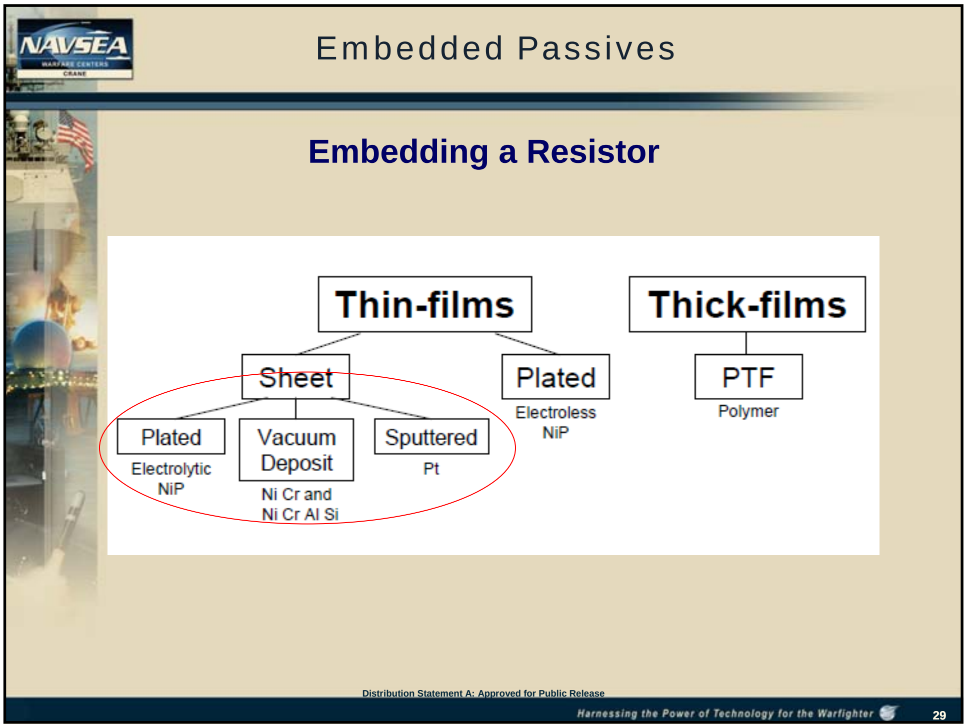
28


Embedded Passives
Embedding a Resistor
Thin-films
Thick-films
Sheet
Plated
Electroless NiP
PTF
Polymer
Plated
Electrolytic NiP
Vacuum Deposit
Ni Cr and Ni Cr Al Si
Sputtered
Pt
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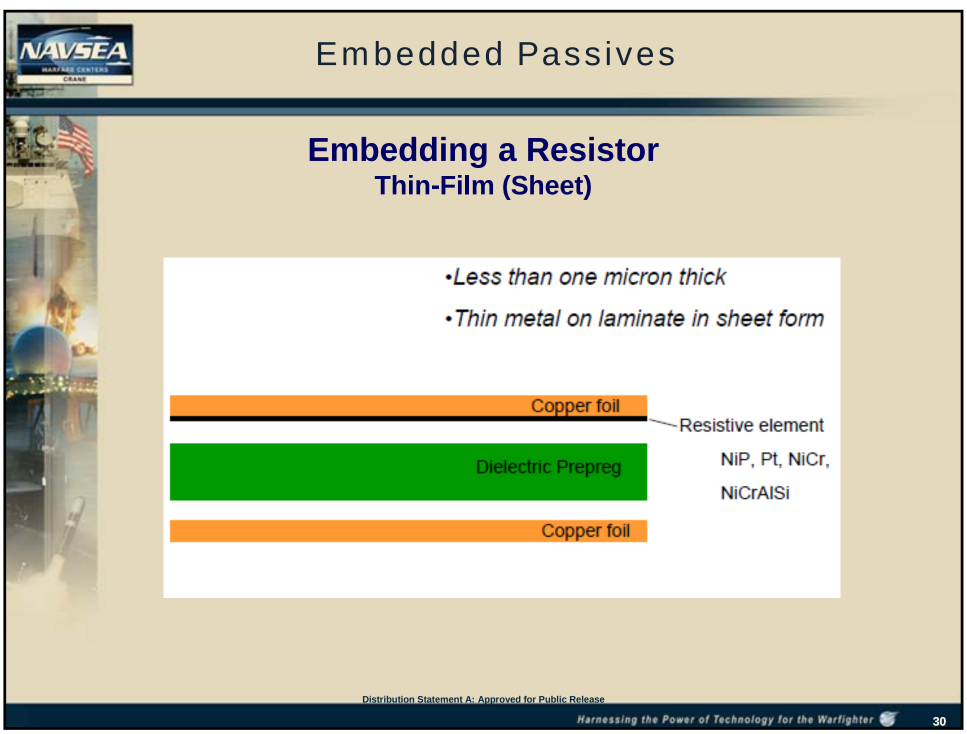
Embedded Passives
Embedding a Resistor
Thin-Film (Sheet)
•Less than one micron thick
•Thin metal on laminate in sheet form
Copper foil
Resistive element
NiP, Pt, NiCr, NiCrAlSi
Dielectric Prepreg
Copper foil
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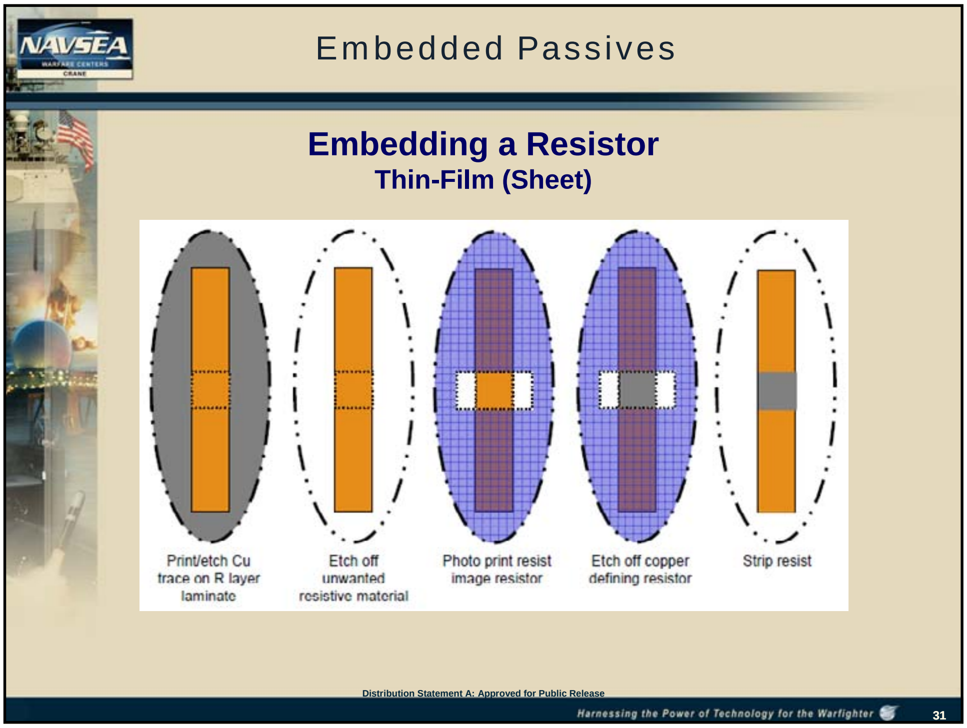
30


Embedded Passives
Embedding a Resistor
Thin-Film (Sheet)
Print/etch Cu trace on R layer laminate
Etch off unwanted resistive material
Photo print resist image resistor
Etch off copper defining resistor
Strip resist
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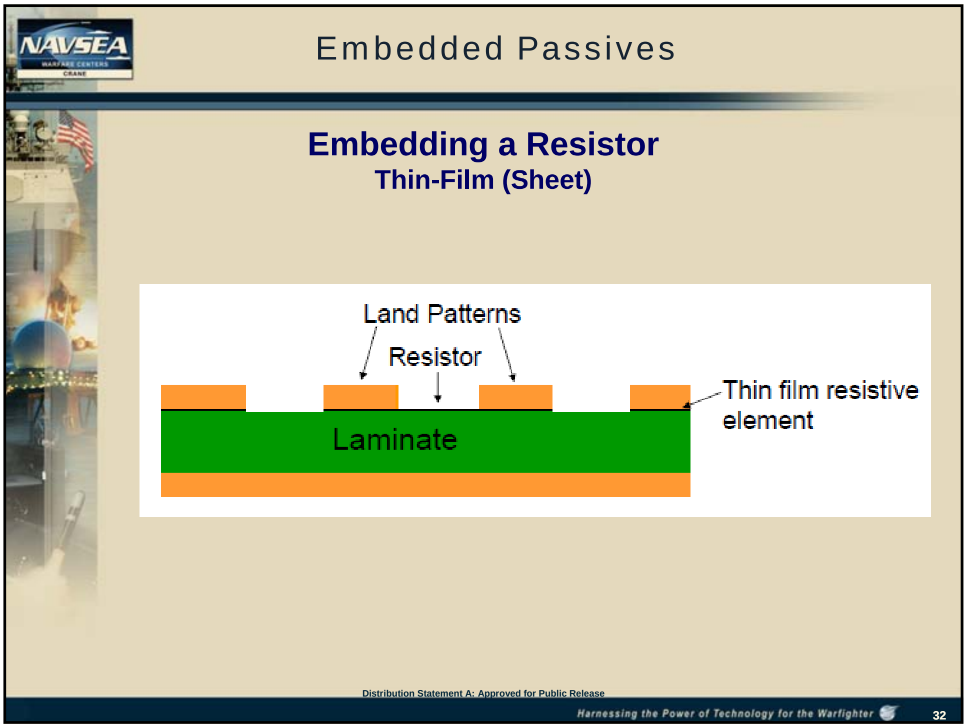
31


Embedded Passives
Embedding a Resistor
Thin-Film (Sheet)
Land Patterns
Resistor
Thin film resistive element
Laminate
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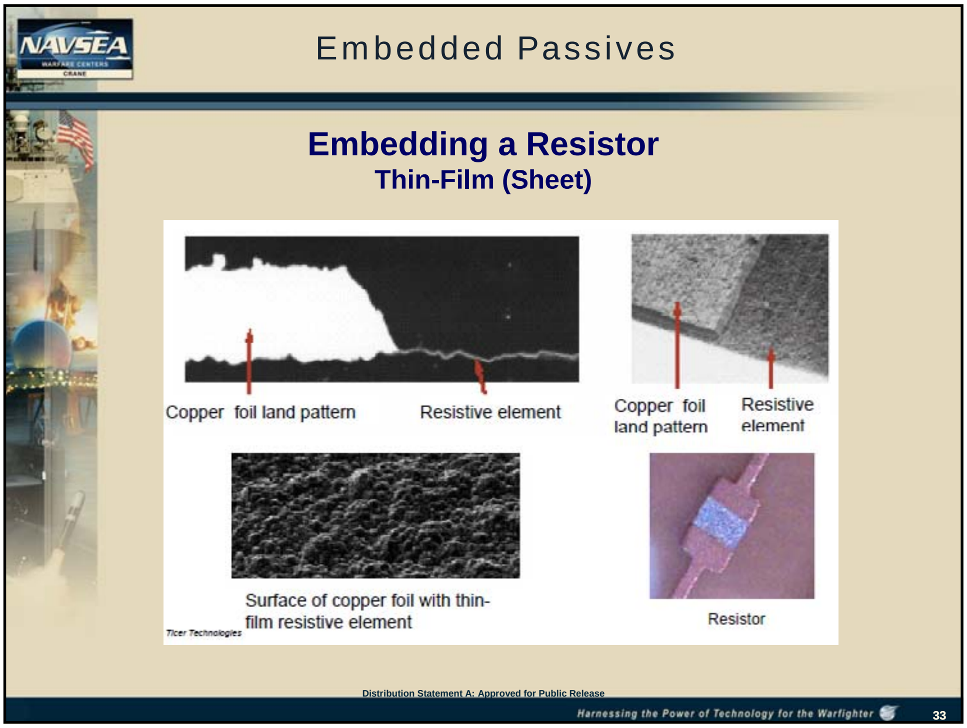
32


Embedded Passives
Embedding a Resistor
Thin-Film (Sheet)
Copper foil land pattern
Resistive element
Copper foil land pattern
Resistive element
Surface of copper foil with thin-film resistive element
Ticer Technologies
Resistor
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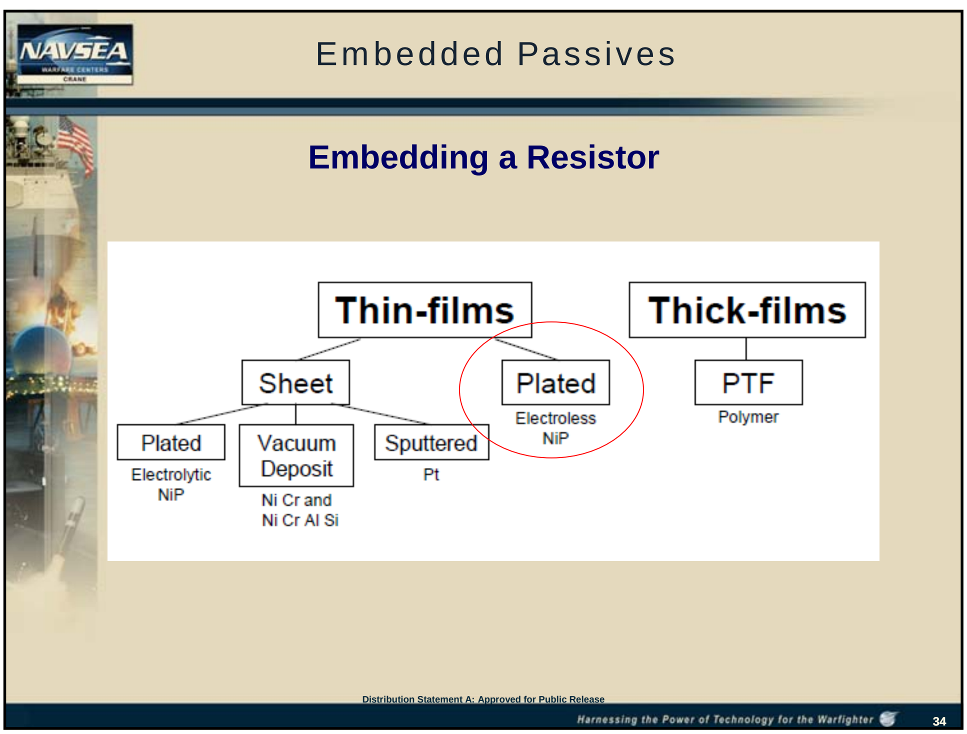
Embedded Passives
Embedding a Resistor
Thin-films
Thick-films
Sheet
Plated
Electroless NiP
PTF
Polymer
Plated
Electrolytic NiP
Vacuum Deposit
Ni Cr and Ni Cr Al Si
Sputtered
Pt
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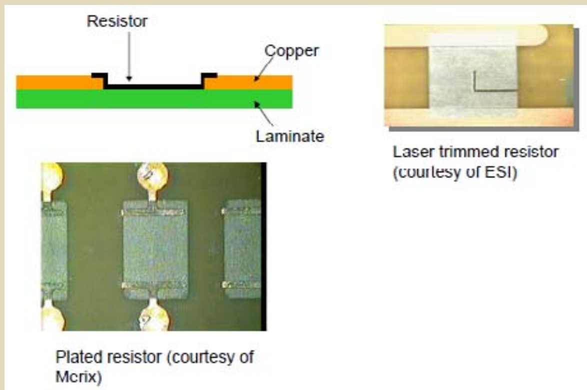
34

Embedded Passives

Embedding a Resistor

Thin-Film (Plated)



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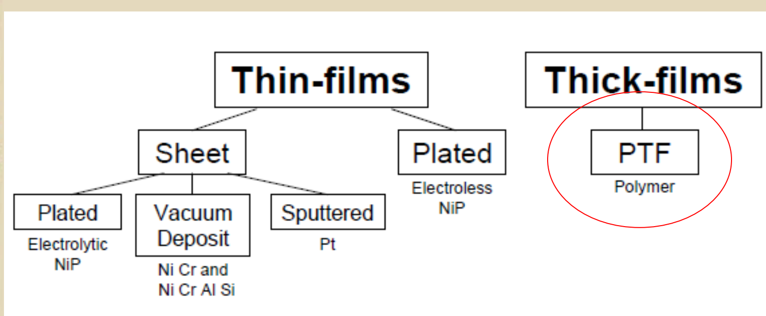
35

Embedded Passives

Embedding a Resistor



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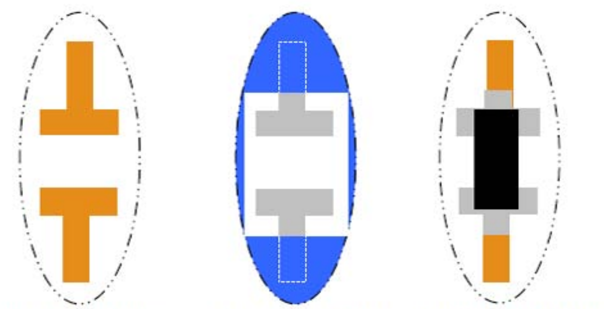
36

Embedded Passives

Embedding a Resistor
Polymer Thick Film



Print/etch/oxide Cu traces/land pattern on resistor layer laminate

Print/silver plate copper land pattern area

Screen print/cure resistors. Test/trim as required

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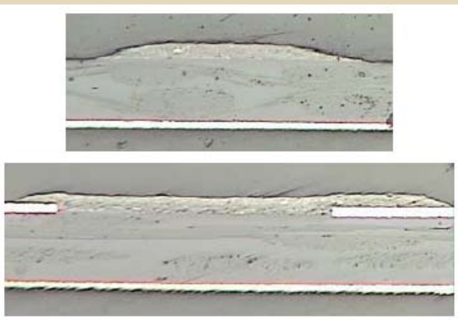
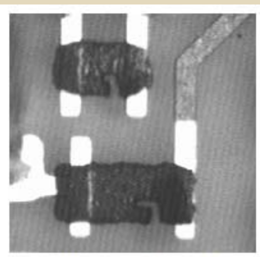
Embedded Passives

Embedding a Resistor
Polymer Thick Film



Screened PTF resistor cross sections



PTF resistor, trimmed

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Embedded Passives

How to achieve a value?

- Resistor material is specified in Ohms per square (OPS)
- The more squares in a series, the larger the resistance value in Ohms.
- Assume 50 OPS mat'l (and a perfect square)

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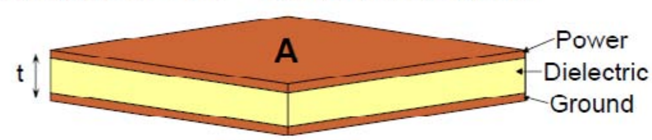
Embedded Passives

Now, let's look at capacitors

Parallel planes in PCBs – a very common situation



$$C = \frac{A*D_k*K}{t}$$

Where:

C = Capacitance (Farads)

A = Area of plates

D_k = Dielectric constant of material between plates

K = Constant

t = Thickness between plates

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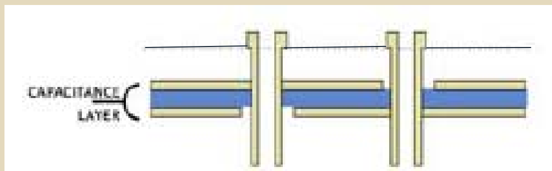
Embedded Passives

Embedded Capacitor

Distributed or Planar



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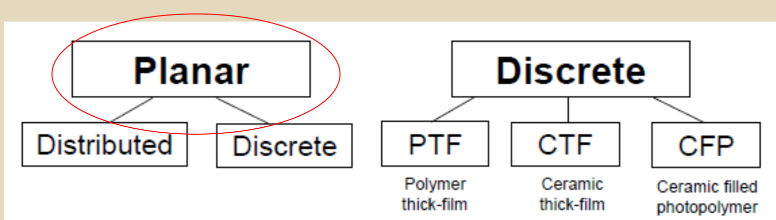
Embedded Passives

Embedding a Capacitor



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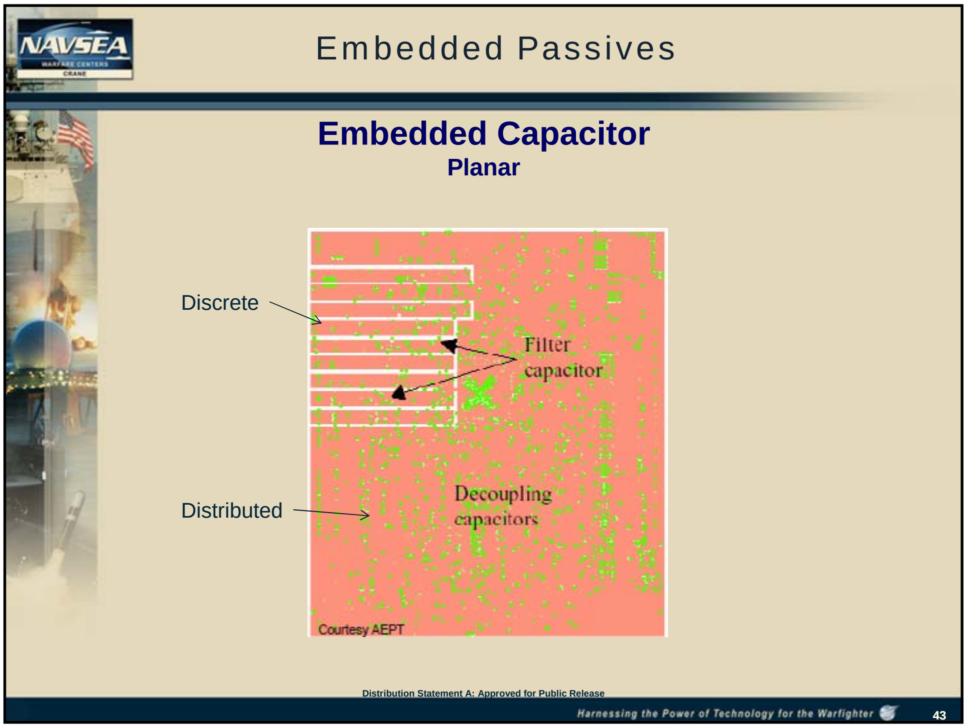
NAVSEA
Embedded Passives
Embedded Capacitor
Planar
Discrete
Filter capacitor
Distributed
Decoupling capacitors
Courtesy AEPT
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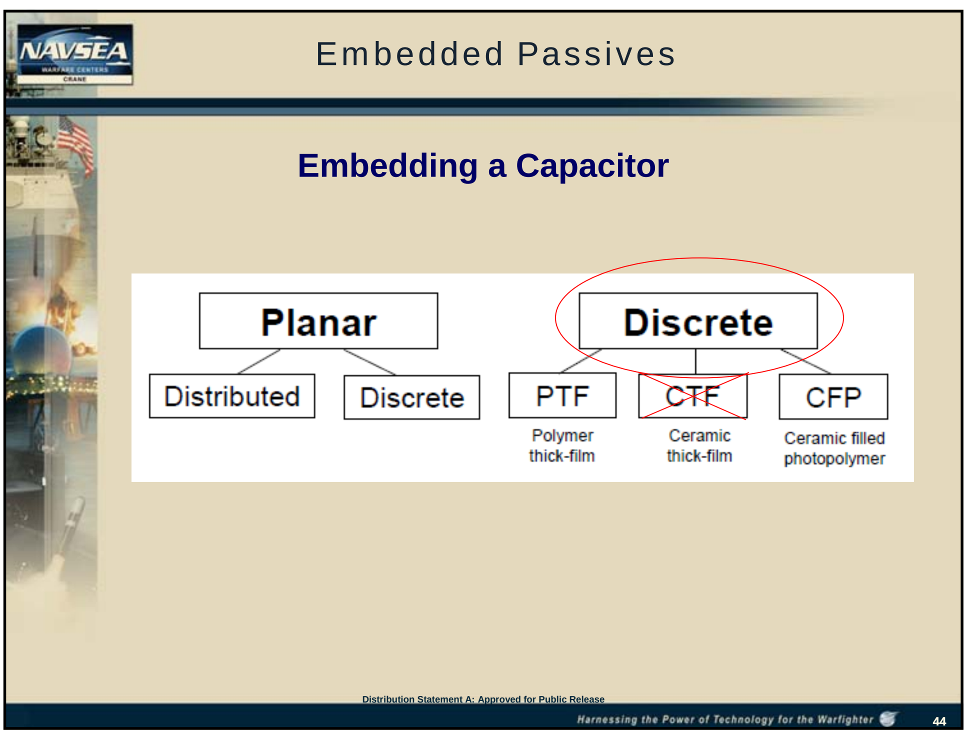
NAVSEA
Embedded Passives
Embedding a Capacitor
Planar
Distributed
Discrete
Discrete
PTF
Polymer thick-film
CTF
Ceramic thick-film
CFP
Ceramic filled photopolymer
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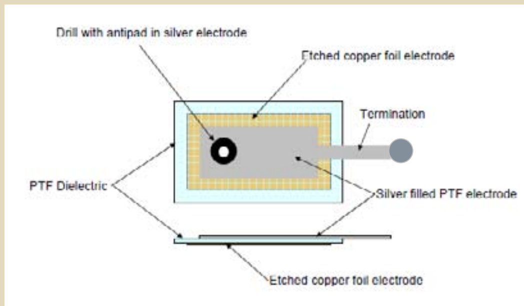
Embedded Passives

Embedded Capacitor

Discrete (Polymer Thick Film)

- Screen printing process
  - – Very similar to PTF resistors
  - – PTF Dielectric screened on previously etched copper electrode and cured (bottom capacitor plate)
  - – PTF Silver filled conductor screened on dielectric and cured (top capacitor plate)



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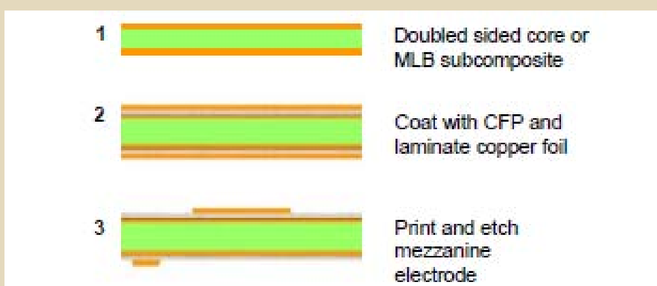
Embedded Passives

Embedded Capacitor

Discrete (Ceramic Filled Photodielectric)



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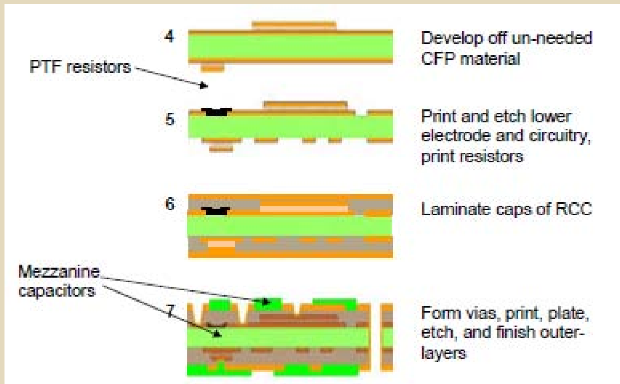
Embedded Passives

Embedded Capacitor

Discrete (Ceramic Filled Photodielectric)



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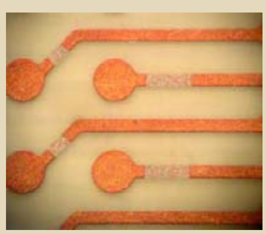
Embedded Passives

Benefits of EP Technology



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Embedded Passives

Benefits

- Frees Up Real Estate on the Surface, Which Means
  - More IC space, possible added functionality
  - Or reduction in size of the board
    - More boards per panel in manufacturing
- Improved performance
  - Reduction in loop inductance
  - Reduction in EMI
- Reliability
  - Less solder joints to SMT passives
  - Less vias
- Cost
    - Fewer parts to mount

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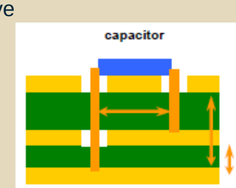
Harnessing the Power of Technology for the Warfighter 49

Embedded Passives

Benefits in Performance

- Large Electrolytic Capacitors
  - Lower impedance at lower frequencies
  - Parasitic inductance makes them have higher impedance at higher frequencies
- Small surface-mount caps
  - Less capacitance
  - Higher Z at lower F
  - Less inductance
  - Lower Z at higher F
- Board plane capacitance
  - Even less capacitance, less inductance
  - Less vias to connect to SMT parts means less inductance attributed to vias
  - Eliminates mounting inductance of SMT parts



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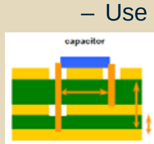
Power Distribution Network Benefits of Plane Capacitance

- Only means of reducing board PDN impedance at higher frequencies
- The future will have higher operating frequencies
- Can increase capacitance by
  - Increase in plane size
  - Increase Dk between planes
  - Decrease distance between planes

Benefits with HDI

- Less vias going through entire board
  - Smaller reduction in copper on planes from via antipads
  - Antipads reduce plane capacitance
- More copper available to deliver current
- Vias closer together, planes closer to caps
  - Less inductance for decoupling capacitors
- Planes closer together
  - Larger embedded board capacitance
  - Use of special dielectric materials



NAVSEA WARFARE CENTERS CRANE

Embedded Passives

What is slowing the adoption of EP Technology?

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Embedded Passives

Barriers

- Software Computer Aided Design Tools
  - Mentor Graphics
  - Zuken
- Tolerancing
  - SMT can achieve +/-0.01%
  - Embedded have to fight to achieve +/-1.0%
  - Maintainability
  - Incapable of repair
  - Standards
  - Manufacturability

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Embedded Passives

Standards

- IPC – 4821Specification for Embedded Passive Device Capacitor Materials
- IPC – 4811 Specification for Embedded Passive Device Resistor Materials
- IPC – 2316 Design Guide for Embedded Passive Device Printed Boards
- IPC – 6017 Qualification and Performance Specification for Printed Boards Containing Embedded Passives
- IPC – 2227 Sectional Design Standard for Embedded Passive Printed Boards (under construction)

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Embedded Passives

Manufacturability

- Most boardshops will not want to invest without big return on investment
- Boardshops will have to learn
  - How to scale resistors
  - How to panelize and assign nomenclature to layers
  - Handling of thin core materials that are <16 um thick
  - Laser trimming of resistors
  - Possibly new process chemistries

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Embedded Passives

Manufacturability (Scaling Resistors)

- **CAM operators will scale the designed resistors**
- **Purpose: Achieve a final post-manufactured resistance value that meets design spec**
- **What will change resistance value in manufacturing?**
  - Trimming (of course)
  - Surface Treatment, prior to lamination (alt oxide, black oxide, etc)
  - Multilayer Lamination
  - Hot Air Solder Level or Reflow

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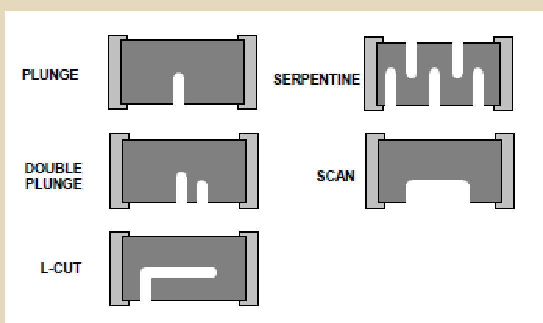
Embedded Passives

Trimming



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Embedded Passives

EP Materials

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Embedded Passives

Resistor Material Suppliers

Photo-print and etch			
	Thin-film		
		Ohmega Industries - OhmegaPly	10, 25, 100 & 250 ohms/sq
		Rohm & Haas - Insite	500 & 1000 ohms/sq
		Ticer Technologies	25, 50, 100, 250 & 1000 ohms/sq
Photo-print and plate			
	Thin-film		
		MacDermid - M Pass	25 to 100 ohms/sq
Screen-print			
	Polymer thick-film (PTF)		
		Electra, Asahi & others	1 ohm to 1 megohm/sq
		~~DuPont - Interra~~	~~1 to 10,000 ohms/sq~~

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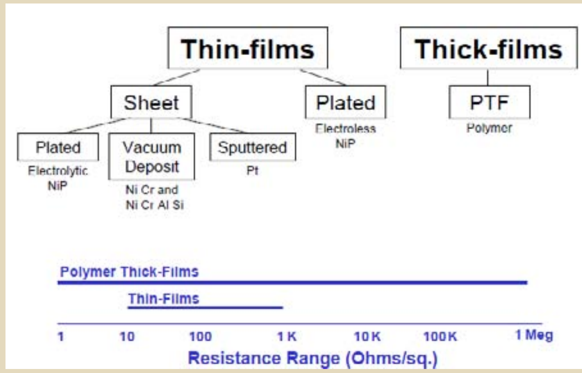
Embedded Passives

Resistor Materials



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Harnessing the Power of Technology for the Warfighter

Embedded Passives

Thin-Film Resistor Materials

Properties of Thin-Film Resistors in PCB Substrates

Resistance	Sheet resistance tolerance	CV (coeffecient of variance)	TCR (themperature coeffecient of resistance)	Solder float	Temperature exposure	Humidity exposure
(Ω/□ nominal)	(%)	(%)	–65° C to +125° C (ppm/°C)	(%Δ R) after 20 sec @ 260°C	(%ΔR) after 1000 hrs @ 70°C	(%Δ R) after 240 hrs.@ 40°C and 95% RH
10	+/-3	+/-3	-5	-0.02	NA	0.25
25	+/-5	+/-5	-50 to 110	0.5	0.5	0.5
50	+/-5	+/-5	-60	0.75	0.75	0.75
100	+/-5	+/-5	-80	1.0	1.0	1.0
250	+/-10	+/-10	100	0.5	1.0	2.0
500	+/-10	NA	100	NA	NA	NA
1000	+/-10	NA	100	NA	NA	NA

Note: Properties vary depending on the resistive material, foil used, resistor value range, aspect ratio, type of substrate, termination design, and other manufacturing conditions. Reported data is limited. The above is a summary extracted from technical articles and vendor data sheets.

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NAVSEA WARFARE CENTERS CRANE

Embedded Passives

Polymer Thick-Film Resistor Materials

Properties of Polymer Thick-Film Resistors in PCB Substrates

Resistance range	Sheet resistance tolerance	CV (coeffecient of variance)	TCR (themperature coeffecient of resistance)	Solder dip	Temperature exposure	Humidity exposure	Humidity exposure
(Ω)	(%)	(%)	-30^0 C to $+100^0$ C (ppm/^{0}C)	(%Δ R) after 3X260^{0}C	(%ΔR) after 1000 hrs @ 100^{0}C	(%Δ R) after 1000 hrs.@ 40^{0}C and	(%Δ R) after 500 hrs.@ 85^{0}C and
10 to100	+/-10	2 to 6	250	-2 to 2.5	0 to -2.5%	0 to 2%	-3 to 5%
10K to1Meg	+/-10	2 to 8	750	-5 to 2.5	0 to -5%	0 to 5%	0 to 5%

Note: Properties vary depending on the material source, resistor value range, thickness, aspect ratio, cure, type of substrate, termination design and finish, and other manufacturing and design conditions. Reported data is limited. The above is a summary extracted from several technical articles and vendor data sheets.

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NAVSEA WARFARE CENTERS CRANE

Embedded Passives

Capacitor Material Suppliers

Planar	
Unfilled and filled dielectrics	
SCI-Sanmina (licensor) - BC2000	78 & 140 pF/sq cm
3M - C-Ply	850 pF/sq cm
Oak-Mitsui - FaradFlex	155 to 1700 pF/sq cm
DuPont - Interra HK	125 to 700 pF/sq cm
~~Ticer Technologies~~	~~110 & 215 pF/sq cm~~
Discrete (Screen print)	
Polymer thick-film (PTF)	
Electra - ElectraΩD'OR	75 to 3,000 pF/sq cm
Ceramic thick-film (CTF) (Soon to be commercialized)	
~~DuPont - Interra EPC~~	~~93,000 pF/sq cm~~
Discrete (Photo image)	
Unfilled and filled dielectrics	
Any of the planar materials	See above
Ceramic filled photodielectric (CFP)	
Motorola (licensor) - Mezzanine	1,550 pF/sq cm

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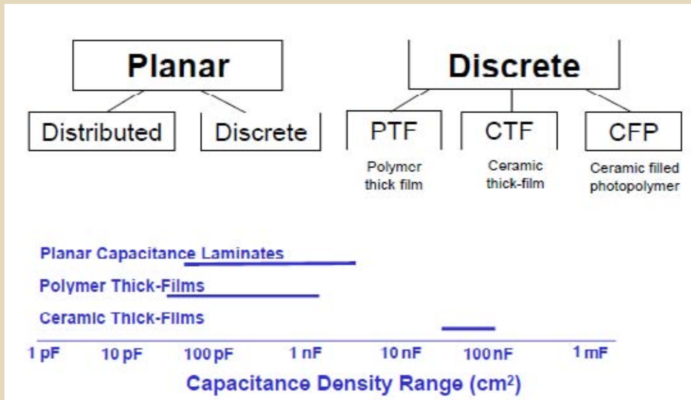
Embedded Passives

Capacitor Materials



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Embedded Passives

Planar Capacitor Materials

Properties of Planar Laminate Capacitor Materials for PCB Substrates

Property	Units	Method	Property range (*)
Dielectric thickness	µ	Nominal	8 to 50
Capacitance density @ 1MHz	nF/in^2	IPC TM 650 2.5.5.3	0.5 to 11
	pF/cm^2		78 to 1700
Dk @ 1 MHz		IPC TM 650 2.5.5.5	4.4 to 30
Loss tangent @ 1 MHz		IPC TM 650 2.5.5.5	0.003 to 0.02
Dielectric strength	KV/mil	IPC TM 650 2.5.6.3	1.2 to 7.3
Electrical migration (85^{0}C, 85%RH, 35V)	Hours		>1000
HiPot (VDC)			100 to 500
(*) this represents the ranges of 14 different products manufactured by 5 companies			

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Embedded Passives

PTF Discrete Capacitor Materials

Properties of Polymer Thick-Film Capacitors in PCB Substrates

PROPERTY	UNITS	TYPICAL VALUE	TEST METHOD
Dielectric thickness	mils	0.5 - 1	NA
Capacitance	nF/in^2	0.5 - 20	NA
Dielectric constant	--	4 - 60	ASTM-D-150
Loss tangent	--	NA	NA
Dielectric strength	V/mil	>1000	ASTM-D-149
Temperature coefficient of capacitance	%	NA	NA
Bias test: 85%RH/85^{0}C/5V/1000hr	Pass/Fail	NA	NA
Insulation resistance	Ohms	$>10^{12}$	JIS Z 3197
Temperature coefficient of expansion	ppm / ^{0}C	NA	NA

Note: Technical reports and data for PTF capacitors is very limited. The above information was compiled from supplier data sheets.

Embedded Passives

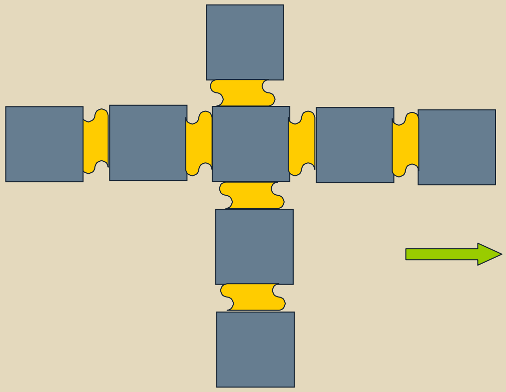
Emulator Project

Lessons Learned

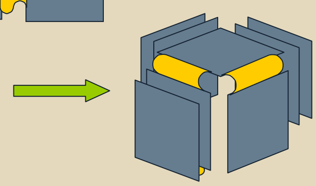
Embedded Passives

JPL Emulator

- Eight Petal Rigid Flex Design
- Motor Controller Board



- Folds Around Motor



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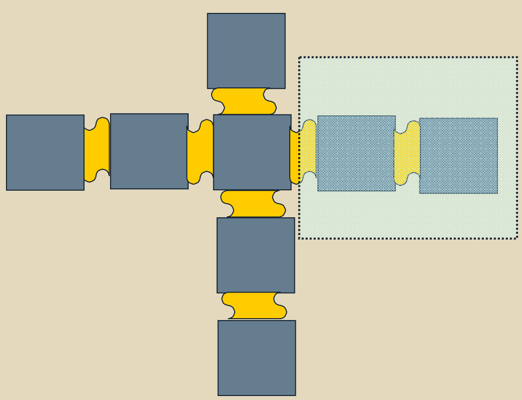
Embedded Passives

JPL Emulator

- Two petals selected to redesign



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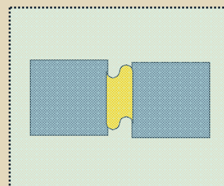
Embedded Passives

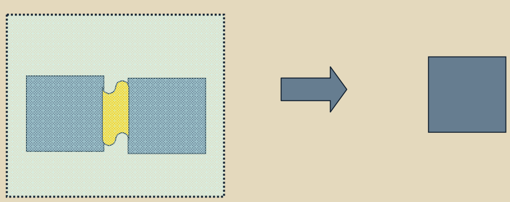
JPL Emulator

- Objectives:
  – Maintain same layer count (12)
  – Reduce number of decoupling capacitors, while maintaining or decreasing noise
  – Possibly reduce area
  – Embed resistors
  – Maintain electrical performance



Embedded Passives

JPL Emulator

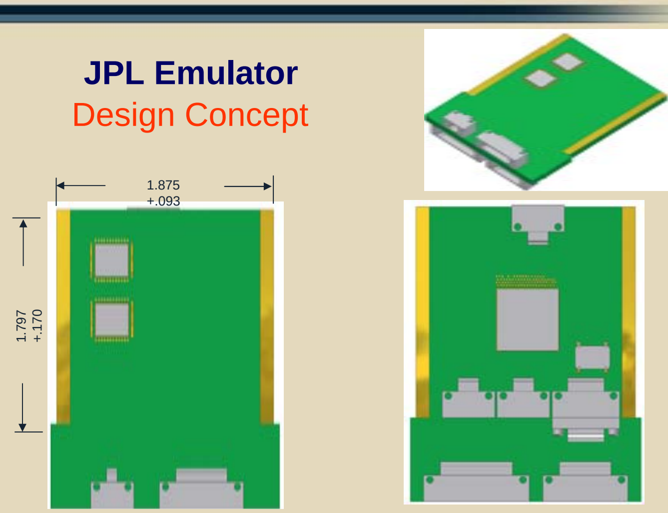


From two

To one

Embedded Passives

JPL Emulator
Design Concept



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Embedded Passives

Stackup A (with 3M C-Ply)

Layer	Description	Thickness (mils)	Material	Via Structure
	Mask	0.70		
	Plating	1.00		
1	Signal	0.35	1/4 oz ABC Foil	
	Prepreg	1.80	Arlon 1x38N8060 (106)	
2	Analog Plane (Ground)	1.40	1 oz Cu	
	Capacitor Dielectric	0.56	C-Ply (14um)	
	Resistor Metal	0.00	1000 Ohm Ticer CrSiO	
3	Analog Plane (Power)	1.40	1 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
	Core Dielectric	10.00	[illegible]	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
4	Analog Signal	0.70	1/2 oz Cu	
	Capacitor Dielectric	2.00	DuPont Polyimide Pyralux (APR)	
	Resistor Metal	0.00	25 Ohm Ticer NiCrAlSi	
5	Analog Signal	0.70	1/2 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
	Core Dielectric	5.00	[illegible]	
6	Analog Plane (Ground)	0.70	1/2 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
7	Digital Plane (Ground)	0.70	1/2 oz Cu	
	Core Dielectric	5.00	[illegible]	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
8	Digital Signal	0.70	1/2 oz Cu	
	Resistor Metal	0.00	25 Ohm Ticer NiCrAlSi	
	Capacitor Dielectric	2.00	DuPont Polyimide Pyralux (APR)	
9	Digital Signal	0.70	1/2 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
	Core Dielectric	10.00	[illegible]	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
10	Digital Plane (Power)	1.40	1 oz Cu	
	Resistor Metal	0.00	1000 Ohm Ticer CrSiO	
	Capacitor Dielectric	0.56	C-Ply (14um)	
11	Digital Plane (Ground)	1.40	1 oz Cu	
	Prepreg	1.80	Arlon 1x38N8060 (106)	
12	Signal	0.35	1/4 oz ABC Foil	
	Plating	1.00		
	Mask	0.70		
	Overall	73.62		
	Target Spec	72.00		

Upper Composite Core

Lower Composite Core

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Harnessing the Power of Technology for the Warfighter 74

Embedded Passives

Stackup B (with DuPont HK-04)

Layer	Description	Thickness (mils)	Material	Via Structure
	Mask	0.70		
	Plating	1.00		
1	Signal	0.35	1/4 oz ABC Foil	
	Prepreg	1.80	Isola P26	
2	Analog Plane (Ground)	0.70	1/2 oz Cu	
	Flex Dielectric	1.00	DuPont Polymide Pyralux (APR)	
	Resistor Metal	0.00	1000 Ohm Ticer CrSiO	
3	Analog Plane (Power)	0.70	1/2 oz Cu	
	Prepreg	3.00	Isola P26	
	Core Dielectric	10.00	Isola P26	
	Prepreg	3.00	Isola P26	
4	Analog Signal	0.70	1/2 oz Cu	
	Capacitor Dielectric	2.00	DuPont Polymide Pyralux (APR)	
	Resistor Metal	0.00	25 Ohm Ticer NiCrAlSi	
5	Analog Signal	0.70	1/2 oz Cu	
	Prepreg	3.00	Isola P26	
	Core Dielectric	5.00	Isola P26	
6	Analog Plane (Ground)	0.70	1/2 oz Cu	
	Prepreg	3.00	Isola P26	
7	Digital Plane (Ground)	0.70	1/2 oz Cu	
	Core Dielectric	5.00	Isola P26	
	Prepreg	3.00	Isola P26	
8	Digital Signal	0.70	1/2 oz Cu	
	Resistor Metal	0.00	25 Ohm Ticer NiCrAlSi	
	Capacitor Dielectric	2.00	DuPont Polymide Pyralux (APR)	
9	Digital Signal	0.70	1/2 oz Cu	
	Prepreg	3.00	Isola P26	
	Core Dielectric	10.00	Isola P26	
	Prepreg	3.00	Isola P26	
10	Digital Plane (Power)	0.70	1/2 oz Cu	
	Resistor Metal	0.00	1000 Ohm Ticer CrSiO	
	Flex Dielectric	1.00	DuPont Polymide Pyralux (APR)	
11	Digital Plane (Ground)	0.70	1/2 oz Cu	
	Prepreg	1.80	Isola P26	
12	Signal	0.35	1/4 oz ABC Foil	
	Plating	1.00		
	Mask	0.70		
	Overall	71.70		
	Target Spec	72.00		

Upper Composite Core

Lower Composite Core

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Harnessing the Power of Technology for the Warfighter

Embedded Passives

JPL Emulator

- Design Status – Type II HDI
  - Embedded resistors
    - On Layers 3 and 10
      - 100 resistors
      - 1K Ω/□ Ticer CrSiO
      - 1K to 15K Ω Values
    - On Layers 5 and 8
      - 55 resistors
      - 25 Ω/□ Ticer NiCr
      - 10 to 499 Ω Values
  - Eliminated decoupling caps
    - Stackup A – Using C-Ply (14um) dielectric
    - Stackup B – DuPont Pyralux (25 um) dielectric

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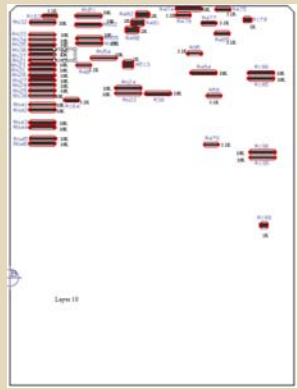
Harnessing the Power of Technology for the Warfighter

Embedded Passives

JPL Emulator

Layer 3

Layer 10



Embedded Passives

JPL Emulator

Layer 5

Layer 8

Embedded Passives

JPL Emulator

- Design Lessons Learned
  - Do not locate resistors directly under IC's (great possibility of increasing inductance loop because of circuits return path)
  - Pay attention to resistor power ratings
    - Enlarged 10 Ohm resistors with 0.2 Watt rating
  - Maintain surface bulk capacitors for low and midrange frequencies to dampen noise
  - Add contingent capacitors at corners of ASIC
  - Design software does not compensate resistors

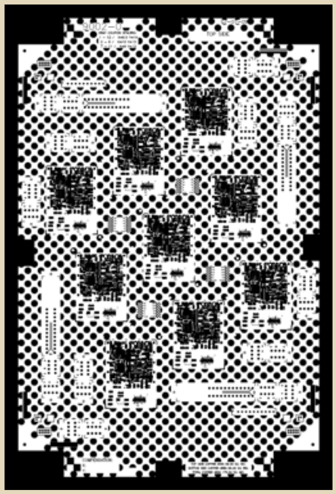
Embedded Passives

JPL Emulator

- Fabrication Lessons Learned
  - Stagger board patterns on panel
  - Copper etching compensation factors
  - Resistivity variations of materials
  - Alternative Oxide effects
  - Compensation due to material movement
  - Geometry compensation for trimming
  - Resistance change during lamination
  - Resistance change during reflow
  - Drilling parameters

Embedded Passives

JPL Emulator



- Panelization
  - Stagger boards
  - Include resistor coupons
  - Local scaling of laser drill
  - Scaling of resistor geometries
  - Compensating layers

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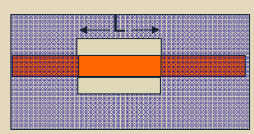
Embedded Passives

JPL Emulator

- Cu Etch Compensation
  - Grow trace widths by
    - .0010” for L3 and L10
    - .0009” for L5 and L8
  - Reduce length of resistor mask by
    - .001” for L3 and L10
    - .0015” for L5 and L8



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Harnessing the Power of Technology for the Warfighter 82

Embedded Passives

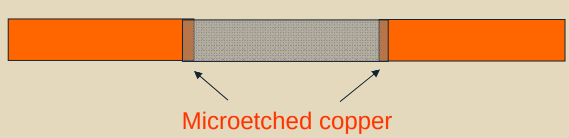
JPL Emulator

- Resistivity variations on materials
  - C-Ply ~1000 OPS
  - DuPont ~1300 OPS
  - For the two stackups
    - Resistor geometries (length and width) between the two materials on L3 and L10 will be different in order to compensate for this variation in resistivity
  - Changed in CAM

Embedded Passives

JPL Emulator

- Alternative Oxide Effects
  - Rise in resistance due to lengthening of resistor
    - NiCr w/0.5 oz Cu – increase of 0.3 to 0.8 mils
    - CrSiO w/0.5 oz Cu – increase of 0.9 to 1.7 mils
  - Predictable
    - Copper is microetched at both ends of resistor
    - Resistor metal is unharmed by etchant
  - For wide resistors, values are less affected



Embedded Passives

JPL Emulator

- Alternative Oxide
  - Wide resistor's value is less affected

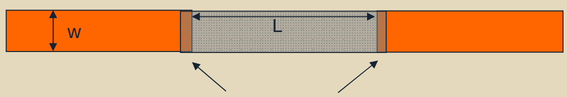
Wide Resistor
w = 0.100"
L_0 = 0.100"
L_1 = 0.1008"
ρ= 50 Ω/□

Narrow resistor
w = 0.015"
L_0 = 0.015"
L_1 = 0.0158"
ρ= 50 Ω/□

$$R = \rho \times \frac{L}{w}$$

Wide resistor:
R_0 = 50.0 Ω
R_1 = 50.4 Ω

Narrow resistor:
R_0 = 50.0 Ω
R_1 = 52.7 Ω



Microetched copper

Embedded Passives

JPL Emulator

- Scaling Due to Material Movement
  - Contributors
    - Etching material
    - Lamination
  - Results after 1st lamination
    - Layers 4/5 and 8/9
      - Grow layers by 430 ppm (x and y)
    - Layers 2/3 and 10/11
      - DuPont HK-04
        - » Grow layers by 1235 ppm (x and y)
      - 3M C-Ply
        - » Grow layers by 910 ppm (x and y)

Embedded Passives

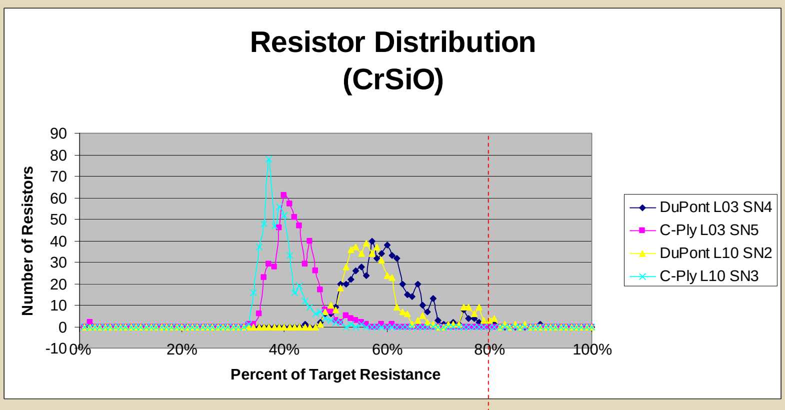
JPL Emulator

- Resistor geometry compensation for trimming
  - Layer 5 and Layer 8 (25 OPS NiCr)
    - Target 80% of final value
  - Layer 3 and Layer 10 (1300 OPS CrSiO on HK04)
    - Target 50% of final value
  - Layer 3 and Layer 10 (1000 OPS CrSiO on C-Ply)
    - Target 70% of final value

    (Purpose: Hopefully, allow all resistors to be created to a value that is less than pre-surface treatment value)

Embedded Passives

JPL Emulator



Trim Boundary

Embedded Passives

JPL Emulator

- Resistance Change Due to Lamination
  - Layer 5 and Layer 8 (25 OPS NiCr)
    - No change
  - Layer 3 and Layer 10 (1300 OPS CrSiO on HK04)
    - 1.5 percent increase
  - Layer 3 and Layer 10 (1000 OPS CrSiO on C-Ply)
    - 1.5 percent increase

Embedded Passives

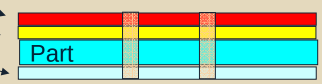
JPL Emulator

- Resistance Change Due to Reflow
  - Layer 5 and Layer 8 (25 OPS NiCr)
    - 0.1 to 0.2 percent increase
  - Layer 3 and Layer 10 (1300 OPS CrSiO on HK04)
    - 1.1 percent increase
  - Layer 3 and Layer 10 (1000 OPS CrSiO on C-Ply)
    - More testing needed (one data set, to date)

Embedded Passives

JPL Emulator

- Mechanic Drill Parameters (L2-L6 and L7-L11 cores)
  - Speed – 110,000 rpm
  - Infeed – 23 in/min
  - Retract rate – 300 in/min
  - Entry material
    - Bulls-eye material
    - .005” FR-4
  - Exit material - Slickback



Embedded Passives

JPL Emulator

- Resistor Stages

CrSiO on HK04 Layer 3 or Layer 10 example

Stage	Etched	Trimmed	Surface Prep	Lamination	Reflow
Percent change	-	+20 to +220	+1.5	+1.5	+1.1
Resistance (Ohms)	3,000 to 8,000	9598	9745	9891	10,000

Layer 5 or Layer 8 example

Stage	Etched	Trimmed	Surface Prep	Lamination	Reflow
Percent change	-	+8 to +39	+1.5	0	+1.1
Resistance (Ohms)	70 to 90	97.4	98.9	98.9	100

Embedded Passives

Acknowledgments

- Richard Snogren
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- Joel Peiffer
- Dave McGregor
- Richard Ulrich

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93

Embedded Passives

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94