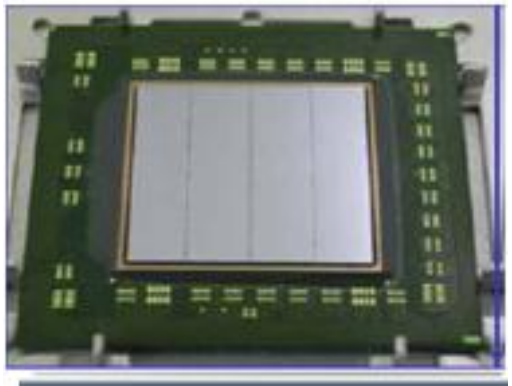
IEEE Components, Packaging, and Manufacturing
Technology Chapter, Santa Clara Valley

XILINX®

3D IC Development and Key Role of Supply Chain Collaboration

Suresh Ramalingam
Xilinx Inc.

IEEE CPMT, April 28, 2011



Agenda

- Background and Motivation
- Stacked Silicon Interconnect Technology
- Supply Chain Collaboration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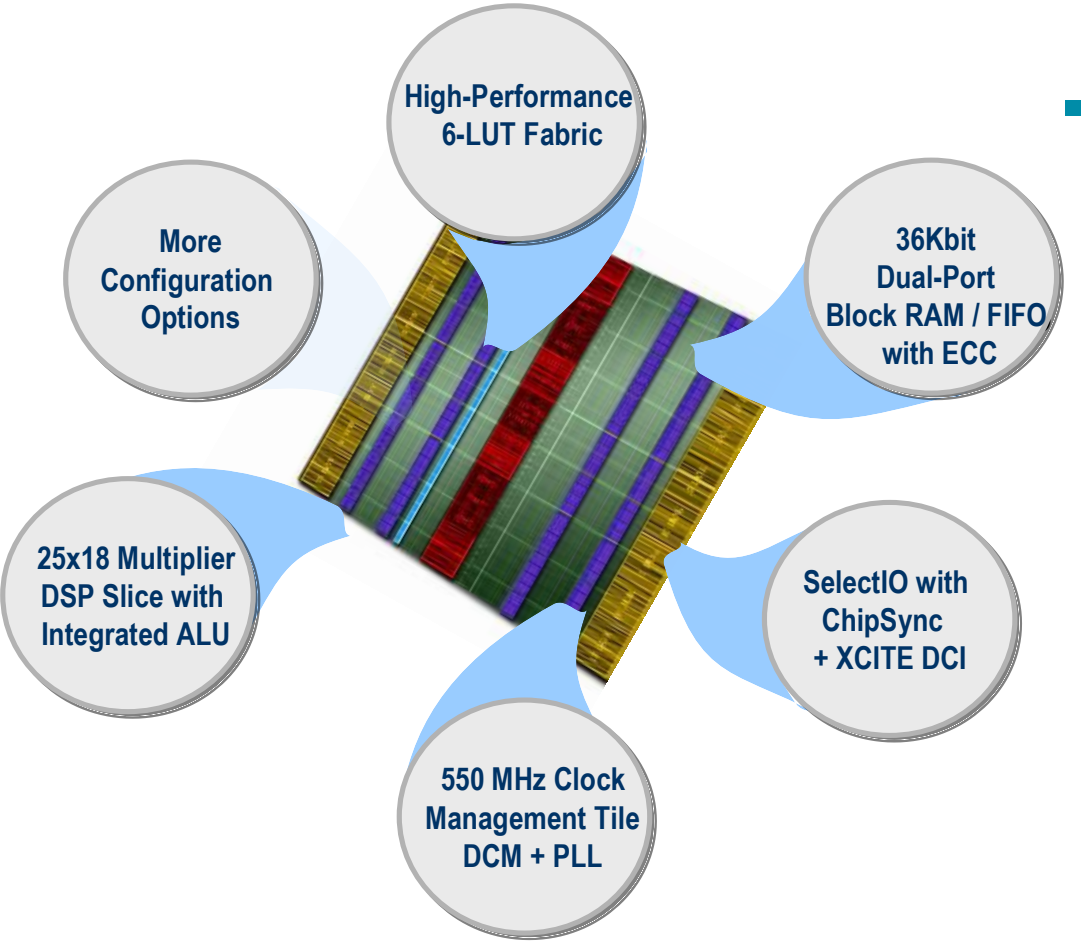
Background and Motivation

Background: FPGA



- **Building Blocks**
  - Configurable Logic Block (CLB)
    - Configuration memory
    - Programmable switches
    - Interconnect drivers
  - Hard IP (DSP, EMAC, etc.)
  - Block RAM
  - Configurable IOs
  - High-speed transceivers

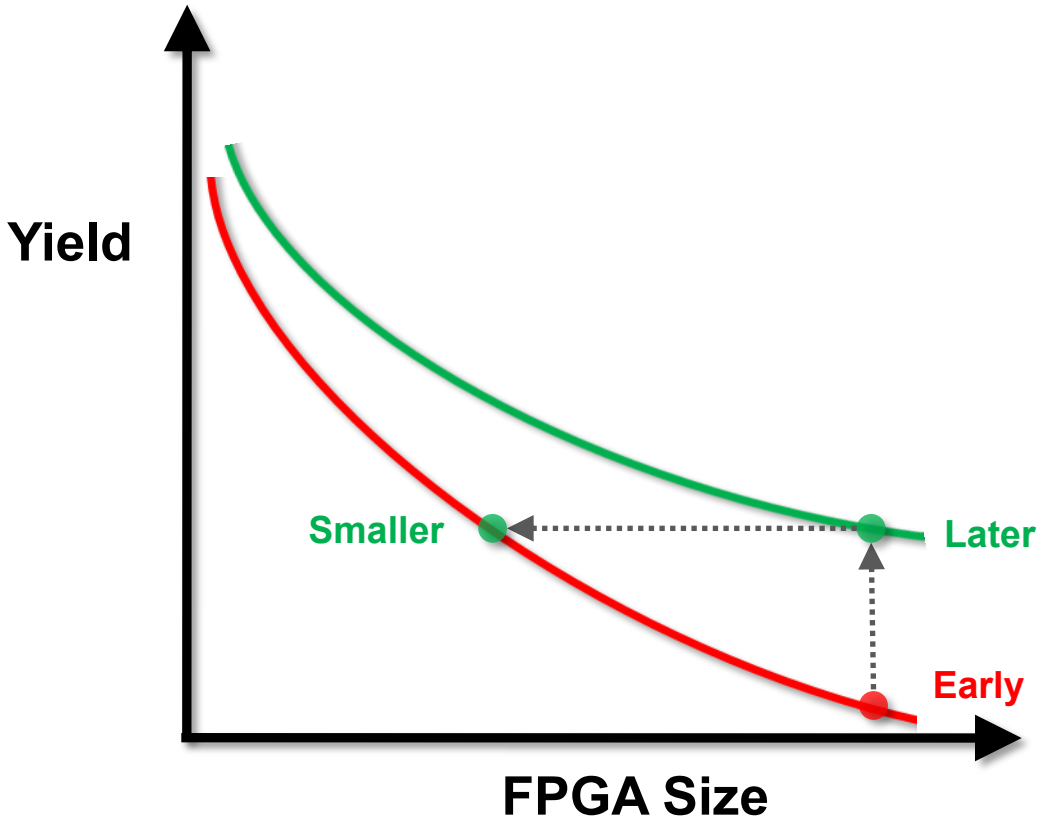
Programmable SoC of logic, memory, and analog circuits

Customers Are Asking for More

- More than 2X today's logic capacity…
- Many more high-speed serial transceivers…
- Many more processing elements…
- Much more internal memory to store data…

Challenge 1: Availability and Capability

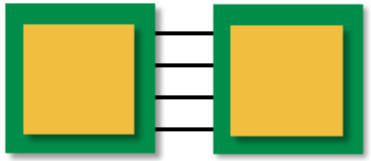
Largest FPGAs only viable later in the life cycle



Challenge 2: Power and Bandwidth

Traditional mitigation techniques are no longer adequate

Large Monolithic FPGA



Multiple FPGAs on PCB or MCM

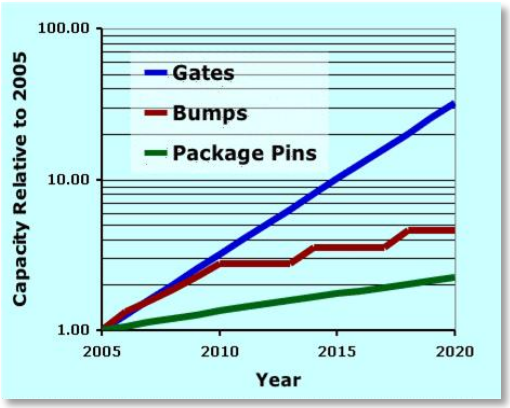
Chip-to-Chip via Standard I/Os and SerDes

More total gates, sooner, but…

Resources Not Scaling

1. Not enough I/Os
2. I/O latencies too high
3. Wasted I/O power

Innovation Needed



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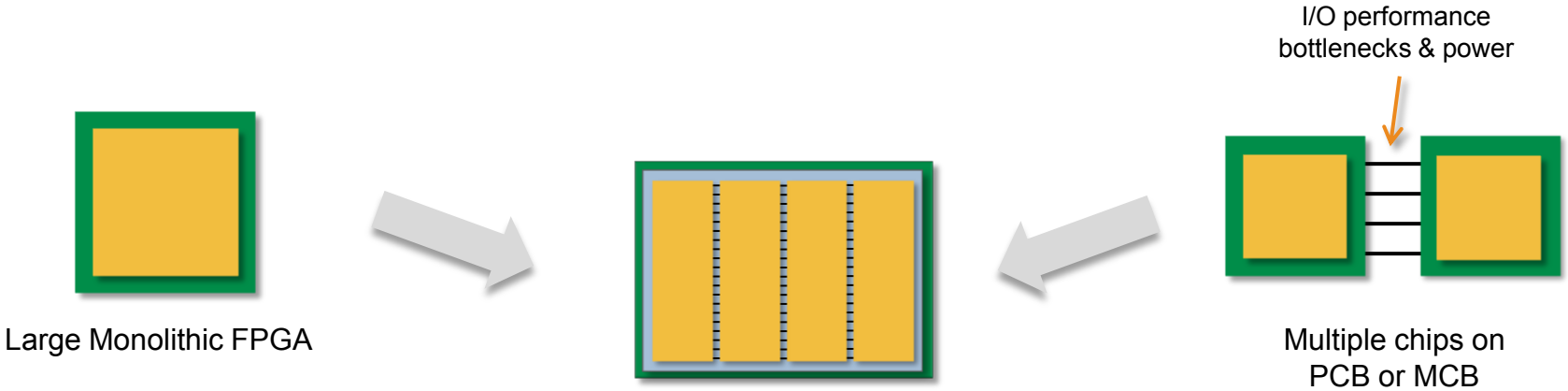
Introducing Stacked Silicon Interconnect Technology

High Bandwidth, Low Latency, Low Power



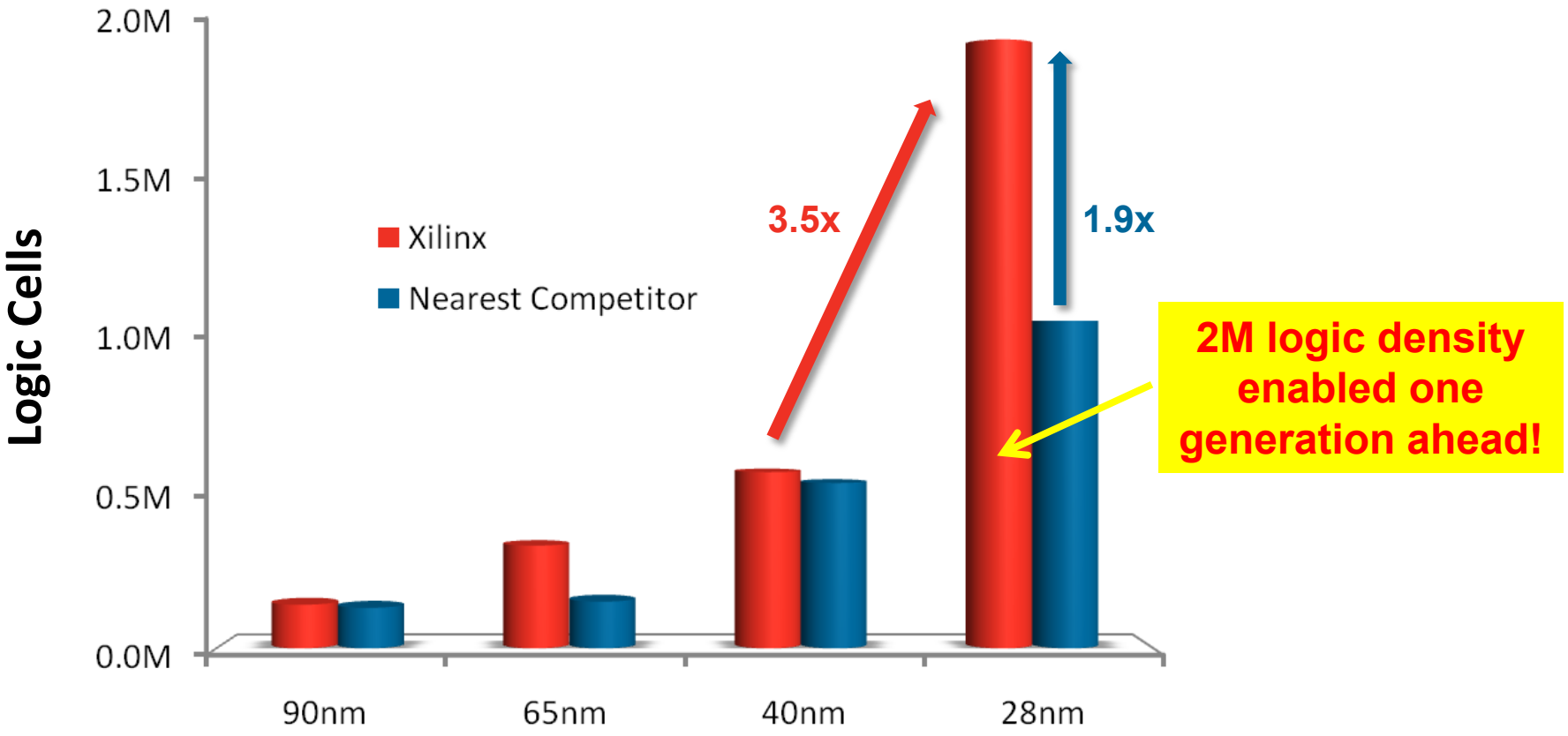
Xilinx Innovation

- ✓ Massive number of low latency, die-to-die connections
- ✓ Earlier in time
- ✓ No wasted I/O power
- ✓ Over five years of R&D

Delivers the Best of Both Worlds: High and Usable Capacity

Delivers Resource-Rich FPGAs

Largest Device with Transceivers



For the Most Demanding FPGA Applications

Next Gen Wired Communications

Next Gen Wireless Communications

VIRTEX 7

Industry's Highest System Performance and Capacity

High Performance Computing

Medical Imaging

Aerospace & Defense

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Summary

- **SSIT Addresses IO Bottleneck**
  - 100X better BW/W over traditional IOs/SerDes
- **Can offer Next Generation Density Now**
- **SSIT Platform Enables**
  - Optimal Partitioning
    - Digital and analog blocks
    - IP/IC reuse
  - Heterogeneous Integration
    - Digital, mixed signal, & optical
    - FPGA & memory

Stacked Silicon Interconnect Technology

- Technology Overview
- Supply Chain Collaboration
- Summary

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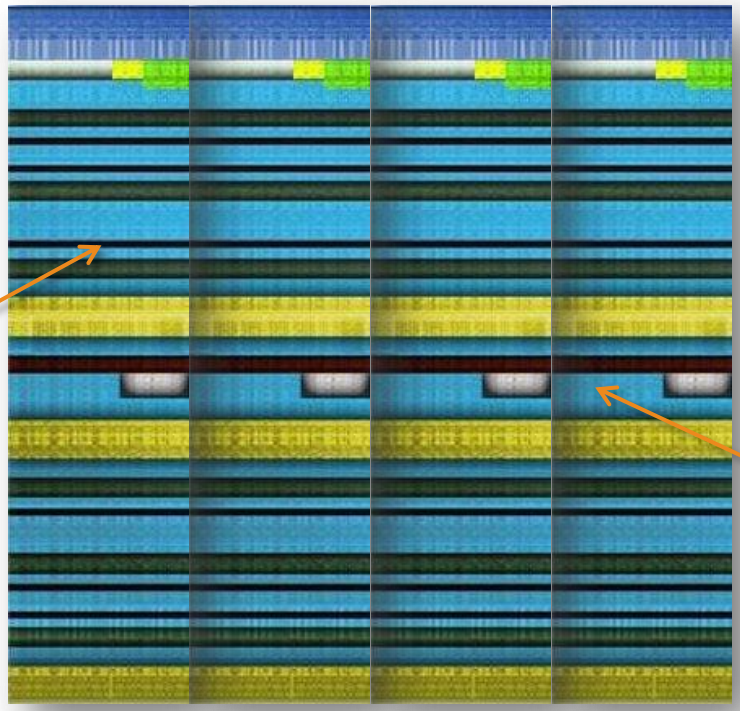
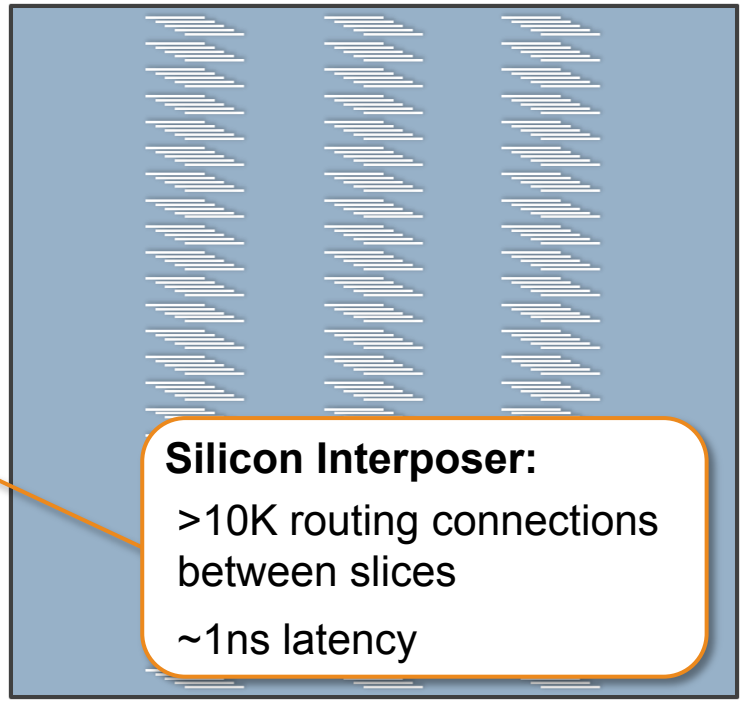
Xilinx FPGA Architectural Innovations
At the Heart of the Technology



ASMBL Optimized FPGA slice

FPGA Slices Side-by-Side



Silicon Interposer:

>10K routing connections between slices

~1ns latency

Silicon Interposer

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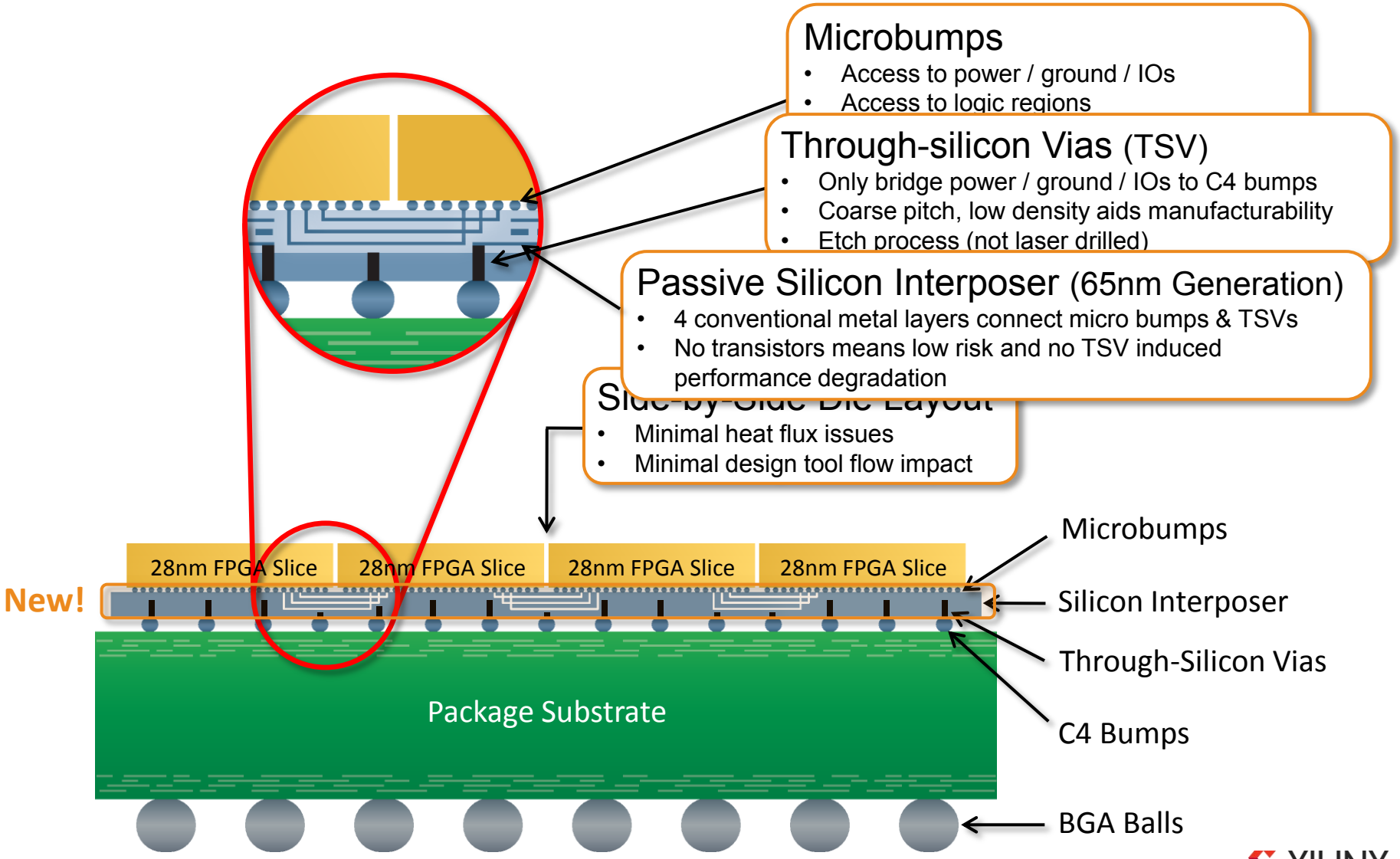
Harnesses Proven Technology in a Unique Way



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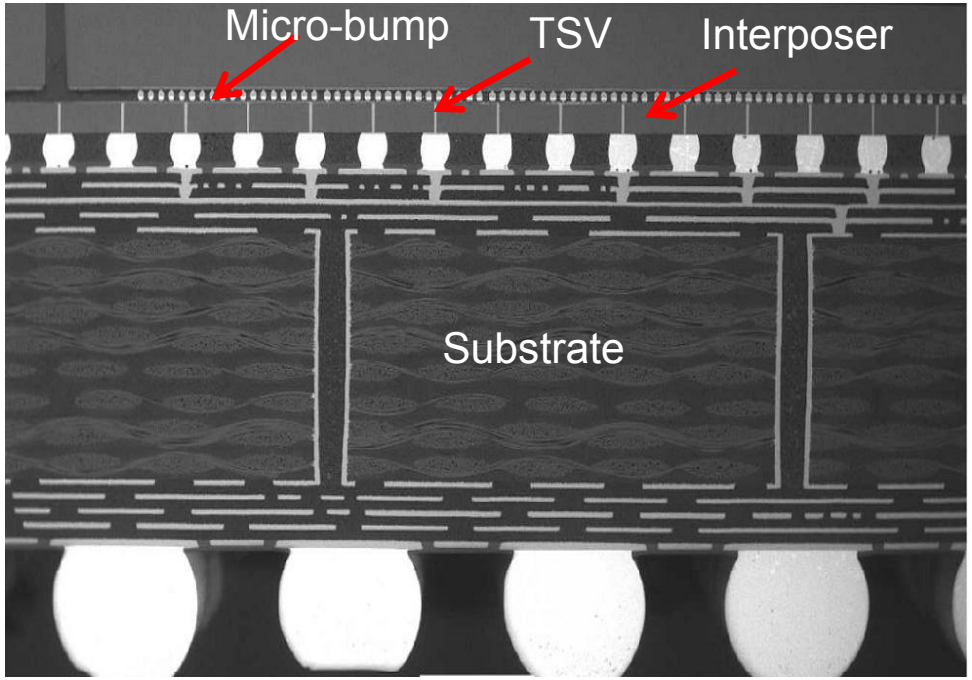
Virtex-7 SSIT uses 28 nm FPGA and 65 nm Interposer

28nm Test Vehicle + 65 nm Interposer



Courtesy of Xilinx, TSMC, Amkor

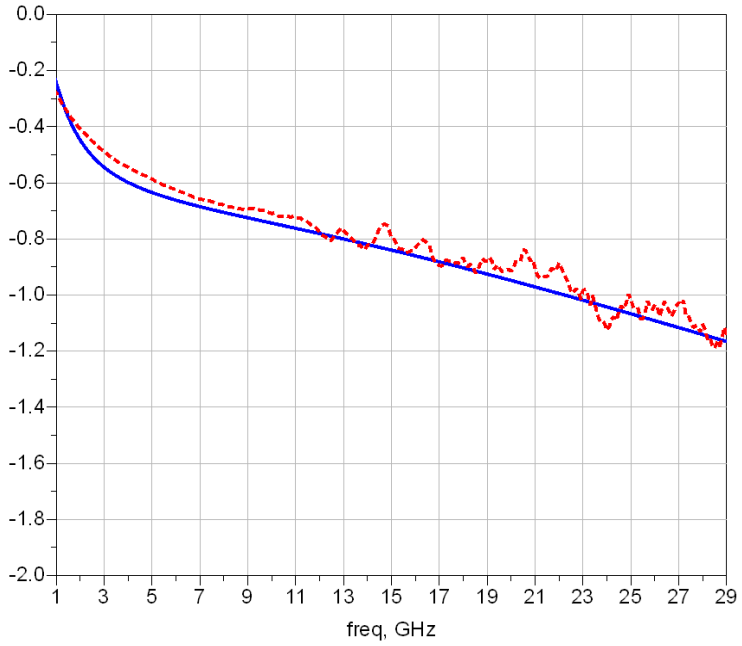
Technology	Specs
M1-M4	2um pitch 4 4X layers
TSV	>10 um diameter & 210um pitch
Micro-bump	45um pitch
C4	210um pitch
Package	4-2-4 Layer, 1.0 mm BGA pitch

- **Low risk approach to integrate TSV & u-bump**
  - Passive silicon interposer with 65nm interconnects & coarse-pitch TSV
- **High density micro-bump for 10K-30K chip-to-chip connections**
- **Better FPGA low-k stress management with silicon interposer**

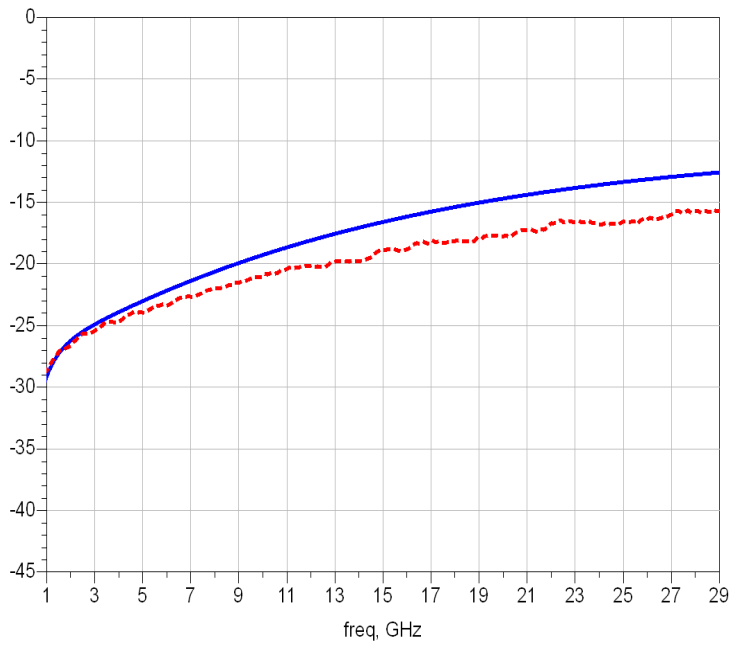
Correlation between Measurement and Simulation

Through transmission structure using two TSVs

Insertion Loss S21 [dB]



Return Loss S11 [dB]



Dotted Red Trace – Measurement
Solid Blue Trace - Simulation

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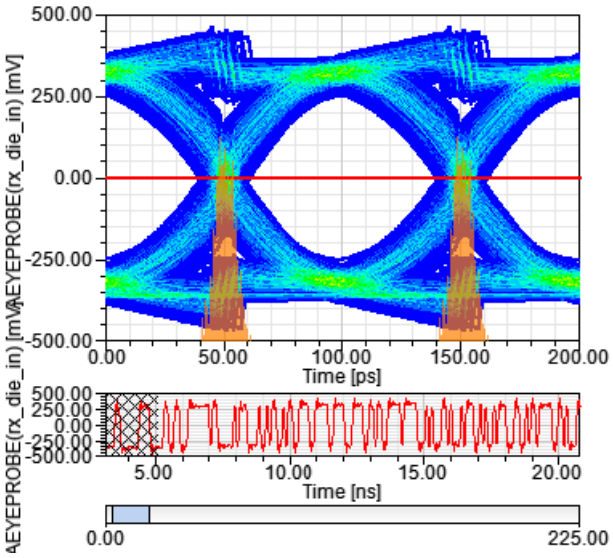
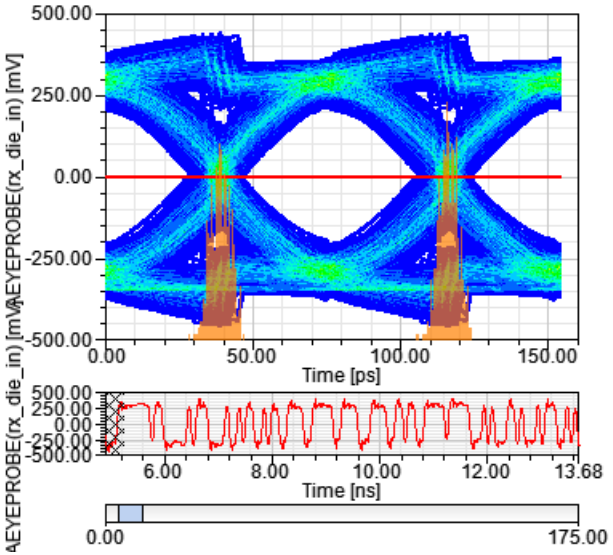
Eyes After TSV Optimization

w/o Interposer



10Gbps



13Gbps

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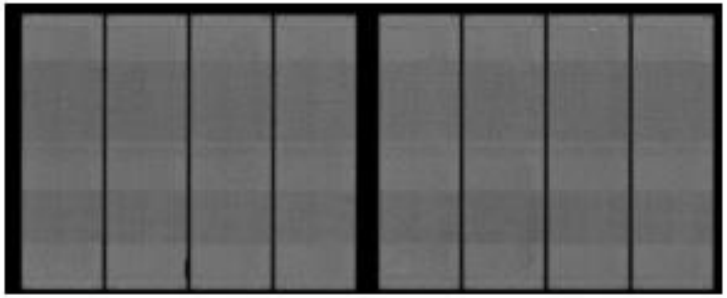
Reliability Validation Status

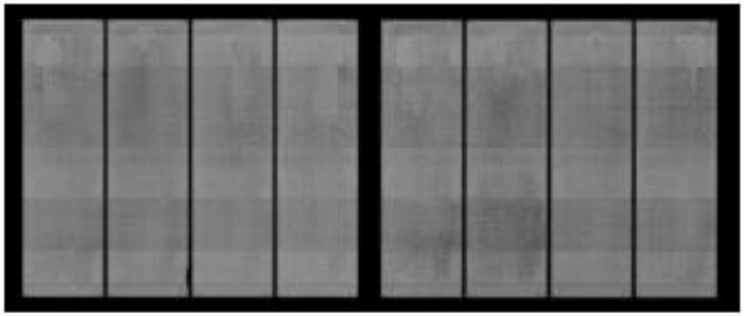
Reliability Tests	Focus Areas	Results
Package Level L4 Precon and TCB	TSV and C4	Passed 1000 TCB
Wafer Level TCB	TSV& Interposer Interconnects	Passed 1000 TCB
Electro-migration	Micro-bump Joint	Passed 0.1% CDF for 10 years
High Temperature Storage	Micro-bump Joint	Passed 1000 hours
Package Level L4 Precon and TCB – 1st Leg	Micro-bump Joint, TSV, C4 Interconnects	Passed L4 and 500 TCB (CSAM)
Package Level L4 Precon and TCB – 2st Leg	Micro-bump Joint, TSV, C4 Interconnects	In progress
Package Technology Qualification *- L4 Precon, TCB, THB, HTOL, HTS*	Micro-bump Joint, TSV, C4, Silicon, Package	In planning

Underfill

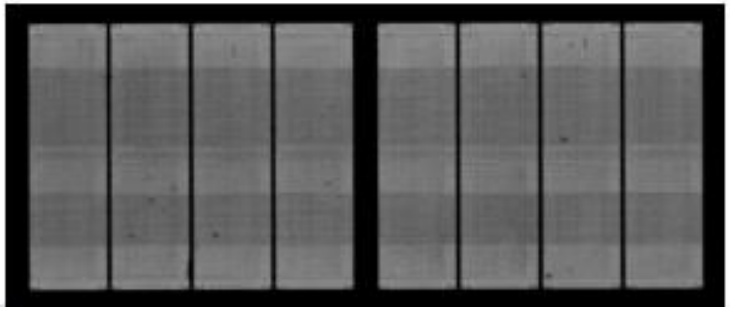
Initial Underfill



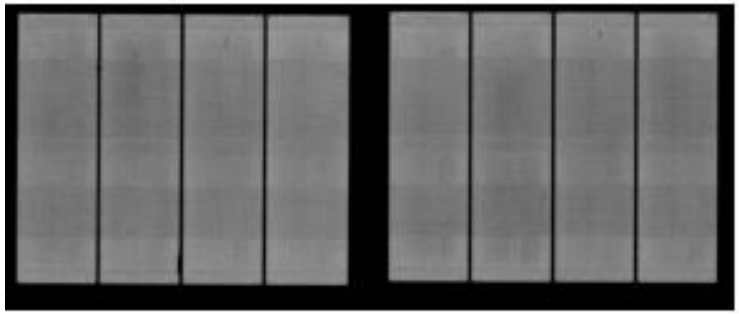
MRT L5/250



HAST 48 Hours



HAST 264 Hours

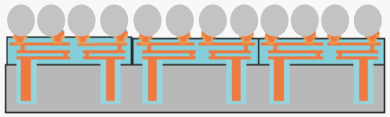


Courtesy of Xilinx, TSMC, Amkor

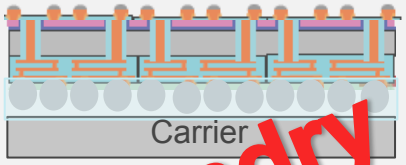
No Delamination, Post HAST: 110C, 85% RH, 264 Hours

Establishing a Supply Chain Flow

Die-to-Substrate



Wafer with TSV
C4 bump, Probe

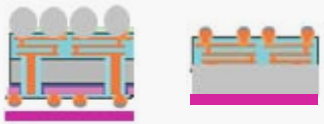


Carrier Mount
Thin & TSV Reveal
RDL & u-bump

Foundry

OSAT

Carrier De-mount
To Film Frame



Dice

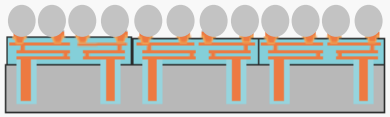
3D-Package Assembly

OSAT

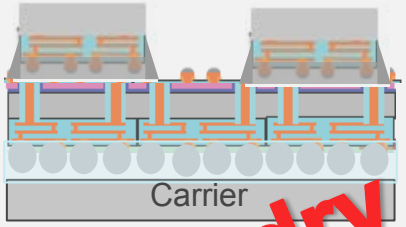
Considerations

- Product and Cost Requirements
- Scalable Business Model
- Design Rules (Foundry vs. OSAT)
- Heterogeneous Die integration

Die-to-Wafer



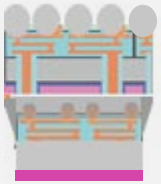
Wafer with TSV
C4 bump, Probe



Carrier Mount
Thin & TSV Reveal
RDL & u-bump
Die-to-wafer

Foundry

OSAT



Dice

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Benefits from Collaboration with Other Technology Leaders

- ✓ Leading fabless & fablite companies
- ✓ Equipment manufacturers
- ✓ Fabs and OSAT
- ✓ Industry consortia

imec

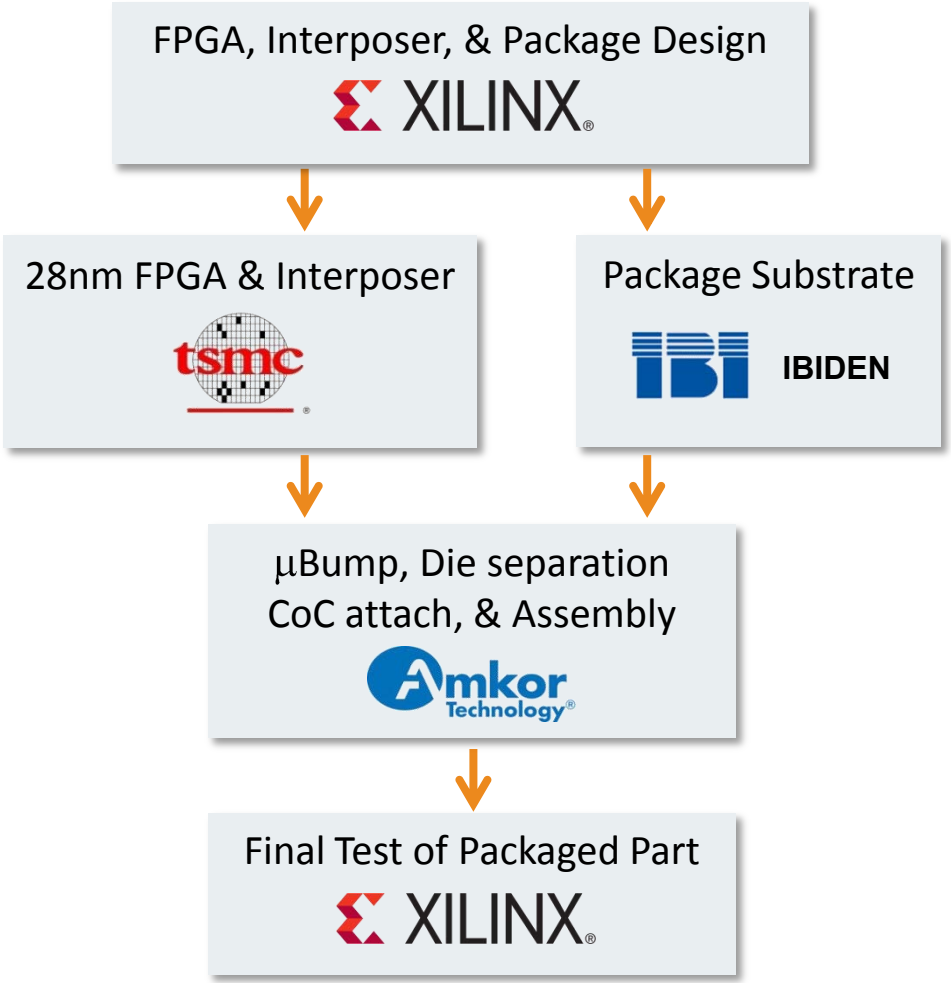
SEMATECH
Accelerating the next technology revolution.

semi

- Requirements alignment
- Industry standards setting
- Best practice sharing

Xilinx has a Robust Supply Chain

Leading foundry and OSAT partners

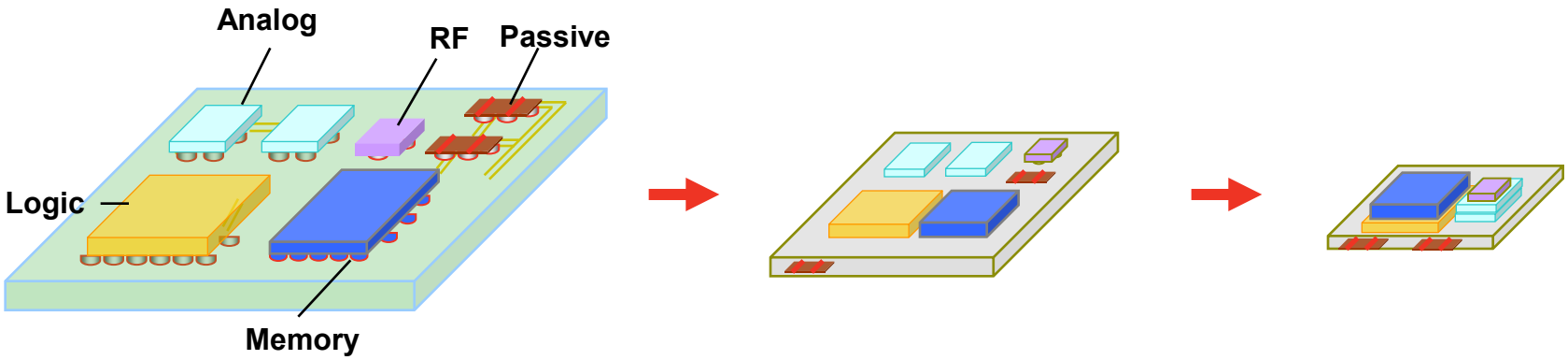


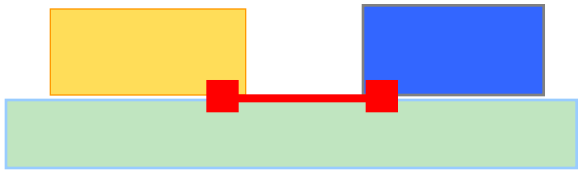
TSMC Discusses Stacked Silicon Interconnect

Dr. Shang-Yi Chiang

Senior Vice President, R&D, TSMC

System Migration Trend



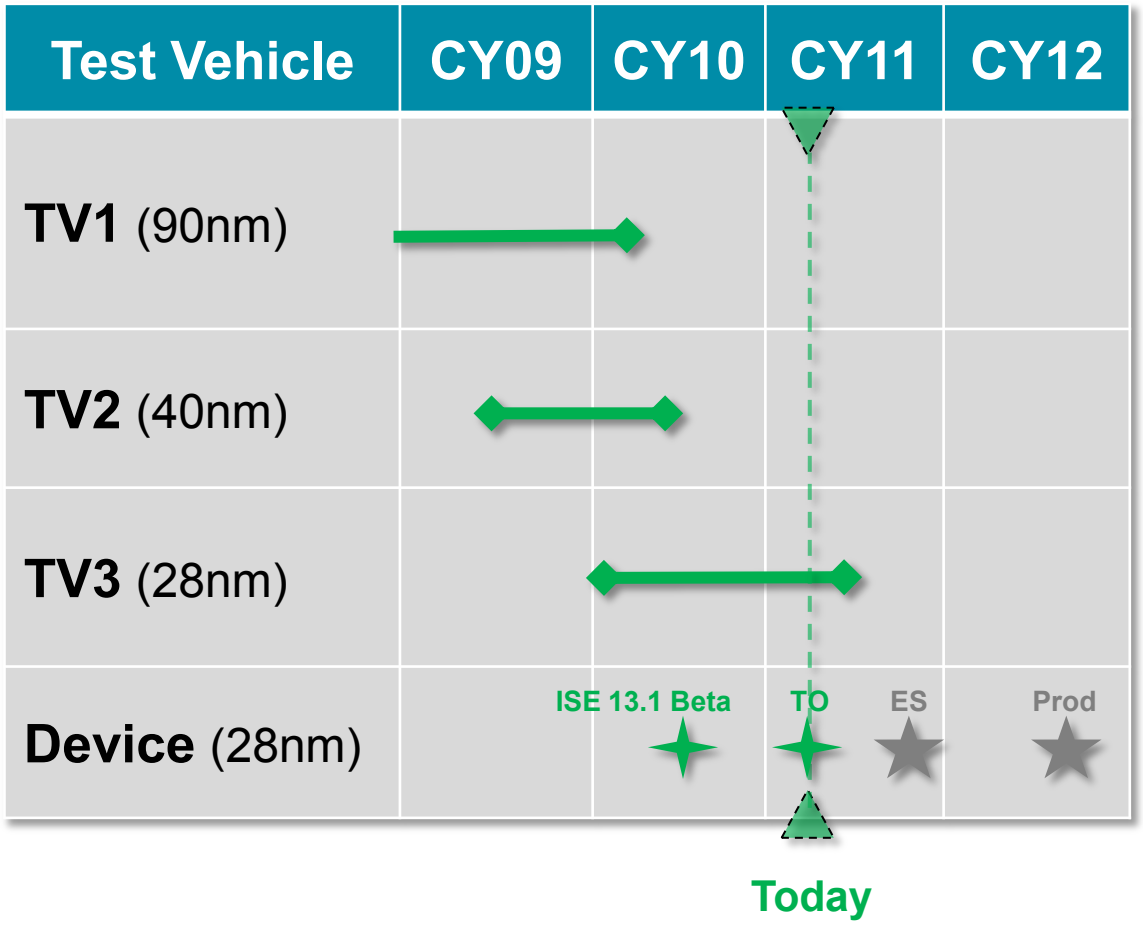


Traditional

Silicon Interposer

3D

Xilinx Is Well on the Way to Volume Production



Module Development ✓
Process Integration ✓
Reliability Assessment ✓
Supply Chain Validation ✓

Design Enablement ✓

Design Validation ✓
Process Qualification

EA Design Tools ✓
Initial Sampling

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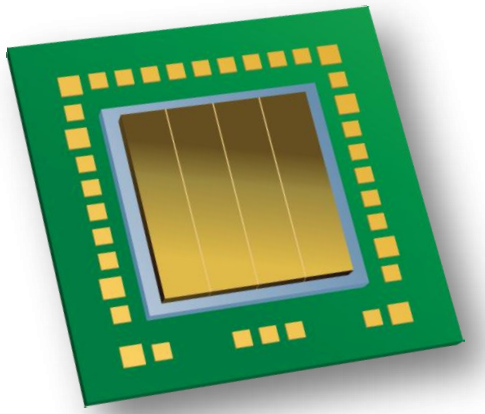
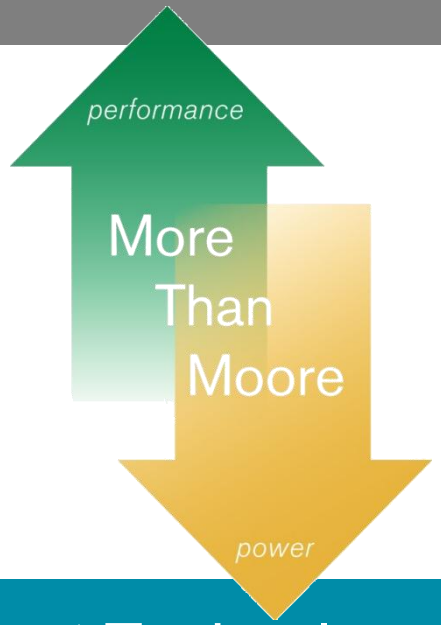
Summary

Xilinx leads industry with **Stacked Silicon Interconnect** technology delivering breakthrough capacity, bandwidth and power efficiency





Stacked Silicon Interconnect Technology

- 2X FPGA capacity advantage at each process node
- Core part of Virtex-7 family
- Supported by standard design flows