Alpha Particle Induced Soft Error Rates for FF Designed in a 28 nm Bulk CMOS Process

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Perturbation in E field due to an ion hit
Soft Errors in Advanced Technologies

- Charge collection mechanisms are different
  - Multiple node charge collection is the norm
- Circuit-level parameters are changing
  - Operating frequency
  - Layout restrictions
- Flipflop hardness can not be guaranteed
Designers Perspective

- Designers currently use data from two generations back to estimate FIT rates for soft errors
  - For 28 nm designs, designers are using data from 65 nm or earlier technology
- No single mechanism dominates SER
  - Charge collection, charge sharing, pulse quenching mechanisms strongly influence SER
- Data from older technologies may not be applicable to newer technologies
  - For example, DICE FF is no longer a reliable option at 40 nm technology

MUST EVALUATE FF DESIGNS AT 28 NM NODE
Test ICs were designed and tested
TEST IC Design Details

- FF testing will be done through shift registers
- PLL and RPG are shared by all designs
- 40 shift register designs on the test ICs

Clock Block

RPG Block

N-bit shift register #1 with error detection

N-bit shift register #2 with error detection

N-bit shift register #3 with error detection

N-bit shift register #40 with error detection
Storage Cells Testing

- Arrays of storage cell designs or Circuit for Radiation Effects Self-Test (CREST) may be used for direct measurement of error rates
- On-chip error detection to facilitate high frequency testing
- Allows for meaningful comparison of different flip-flop designs
Flip-Flop Designs

- 40 different flip-flop designs from multiple design houses were used
- Varying soft error hardness ranging from conventional DFF to hardened DICE FF
- Varying range of power, speed, area
- FF were designed with standard $V_t$, low $V_t$, and high $V_t$ transistors
- Layouts were generated for dual-well and triple-well structures
Fabrication and Test Process Details

- 28 nm commercial bulk CMOS process was targeted
- Two different die of 3 mm X 2 mm size were used
- Flip-flop designs were divided evenly between the die

- Each die was functionally tested to ensure full functionality
- Each die was exposed to Alpha source separately
Alpha source was characterized in air and in vacuum.
Alpha Test Results

- Alpha source was less than 8 mm away from the die
- Alpha flux was estimated to be about 300 alpha/mm²/sec
- FIT rates are calculated for 0.002 particles/cm²/hour
- FIT rates reported in the next slides are per MB
### Alpha Test Results : 28 nm Node

- The following FIT numbers are in FIT/Mbit
- The range of FIT observed was 2852 to 0
- The median FIT value was 995
- The average FIT value was 927

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Alpha Test Results: 28 nm Node

The following FIT numbers are in FIT/Mbit.
Comparison Between 40 and 28 nm Nodes

For 28 nm node
- The range of FIT observed was 2852 to 0
- The median FIT value was 995
- The average FIT value was 927

For 40 nm node (not necessarily for the same FF designs)
- The range was 1384 to 0
- The median was 796
- The average was 622

Cisco FF with identical design except shrinkage showed 4X increase in FIT rates at 28 nm node compared with 40 nm node
Discussion

- Compared to 40 nm, 28 nm FF designs show higher median and average FIT rates

- FIT rates observed for a Cisco FF was 400% higher at 28 nm node compared to 40 nm node – the design was identical except shrinkage

- Lower critical charge values have strong effect on FIT rates

- Lower transistor sizes can not overcome increased vulnerability due to lower critical charge