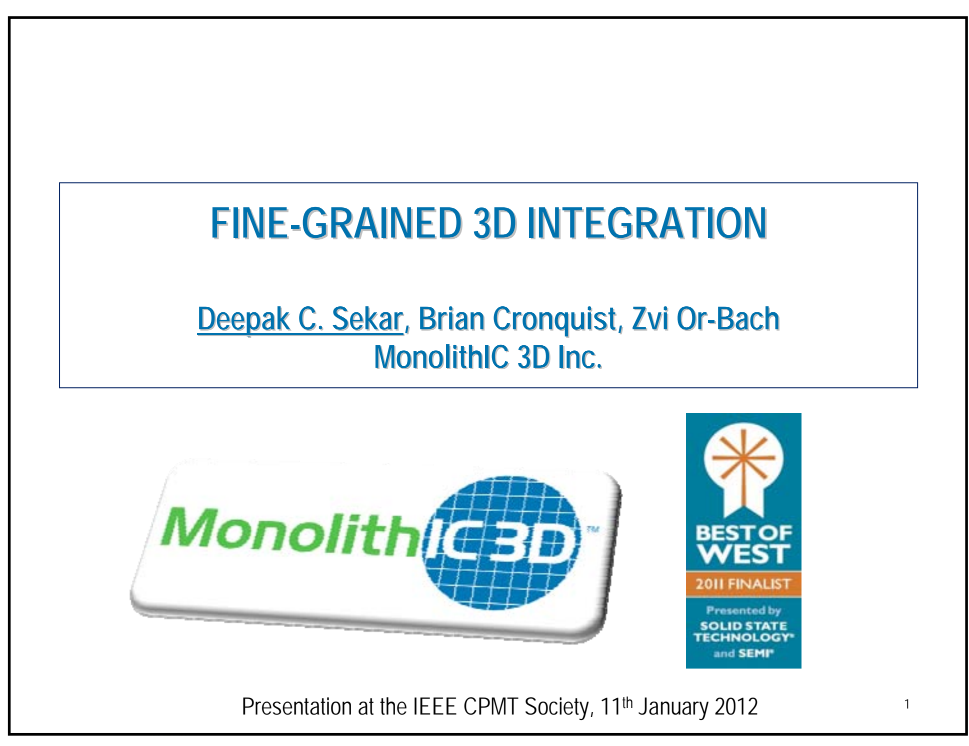
FINE-GRAINED 3D INTEGRATION
Deepak C. Sekar, Brian Cronquist, Zvi Or-Bach
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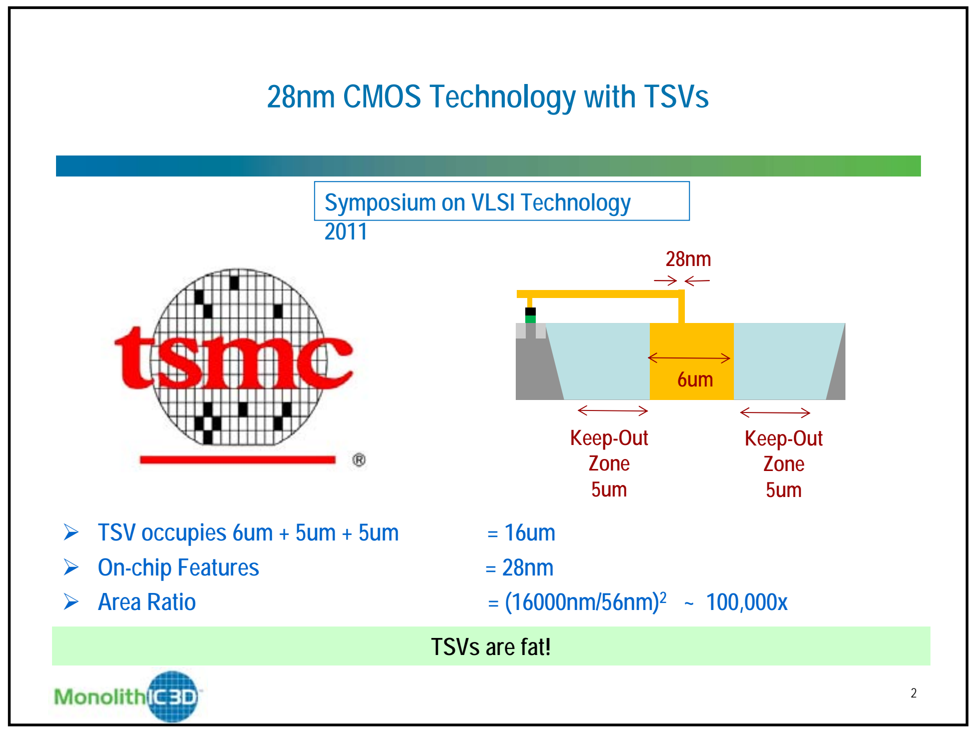
BEST OF WEST
2011 FINALIST
Presented by SOLID STATE TECHNOLOGY and SEMI
Presentation at the IEEE CPMT Society, 11th January 2012
1


28nm CMOS Technology with TSVs
Symposium on VLSI Technology 2011
tsmc
28nm
6um
Keep-Out Zone 5um
Keep-Out Zone 5um
TSV occupies 6um + 5um + 5um = 16um
On-chip Features = 28nm
Area Ratio = (16000nm/56nm)2 ~ 100,000x
TSVs are fat!
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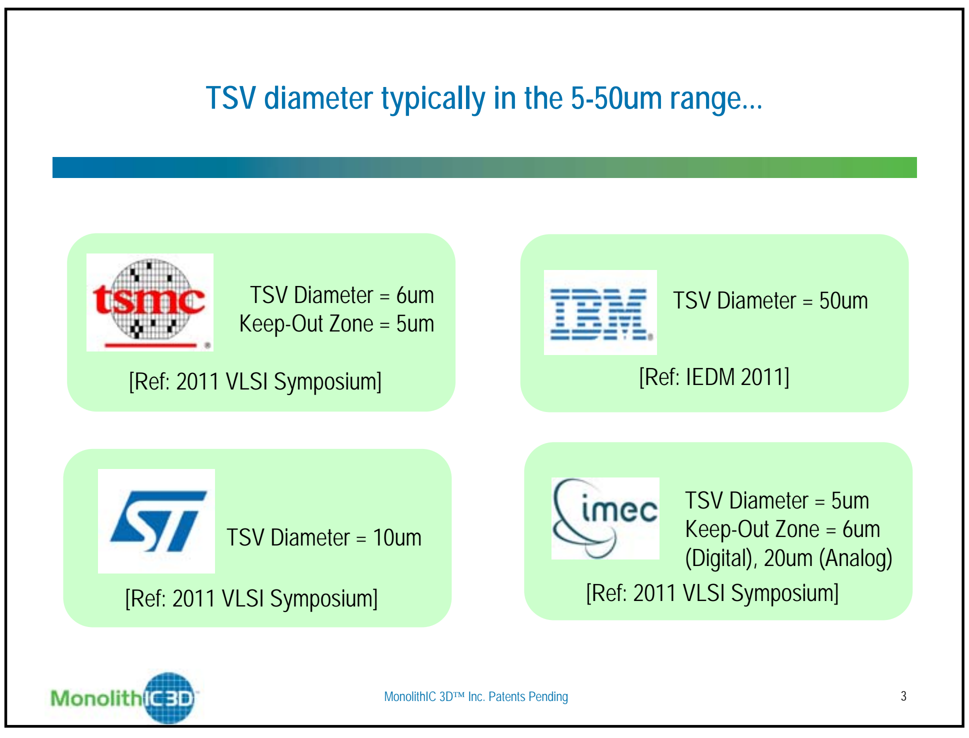
TSV diameter typically in the 5-50um range…
TSV Diameter = 6um
Keep-Out Zone = 5um
[Ref: 2011 VLSI Symposium]
TSV Diameter = 50um
[Ref: IEDM 2011]
TSV Diameter = 10um
[Ref: 2011 VLSI Symposium]
imec
TSV Diameter = 5um
Keep-Out Zone = 6um
(Digital), 20um (Analog)
[Ref: 2011 VLSI Symposium]
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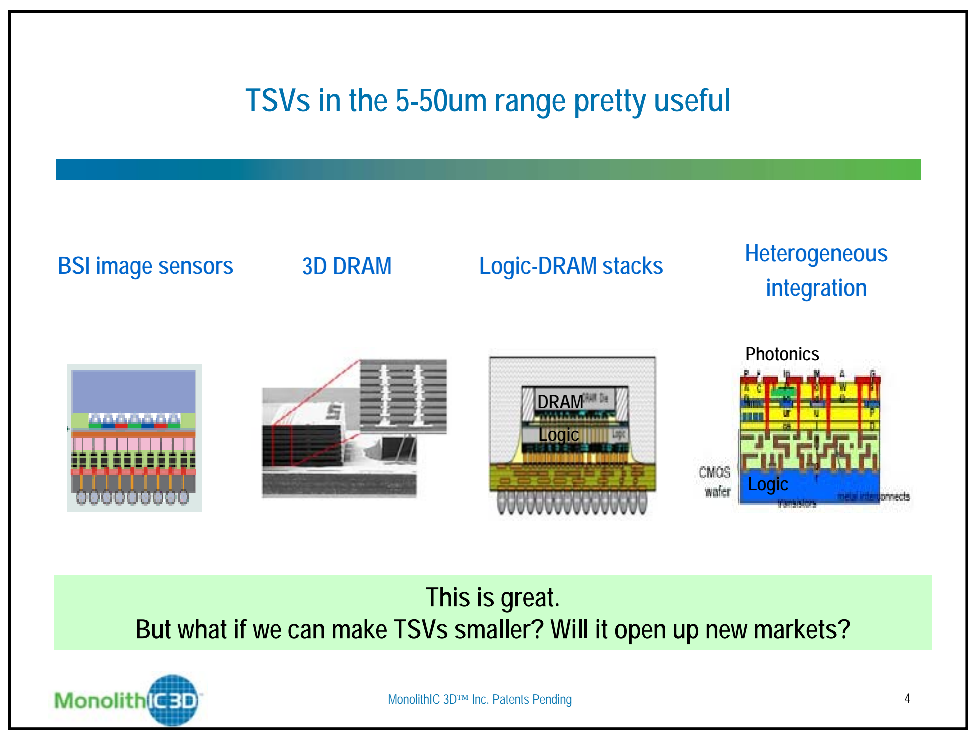
TSVs in the 5-50um range pretty useful
BSI image sensors
3D DRAM
Logic-DRAM stacks
Heterogeneous integration
DRAM
Logic
Photonics
CMOS wafer
Logic
This is great.
But what if we can make TSVs smaller? Will it open up new markets?
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Fine-Grained 3D
Definition: Small TSV diameter, in the 20nm-250nm range

Outline of this Presentation

- Motivation for Fine-Grained 3D
- How can we make TSVs smaller?
  - Evolutionary Methods
  - Revolutionary Methods

Note: Face-to-back approaches will be the focus of this presentation as they are extendable to more than two dice

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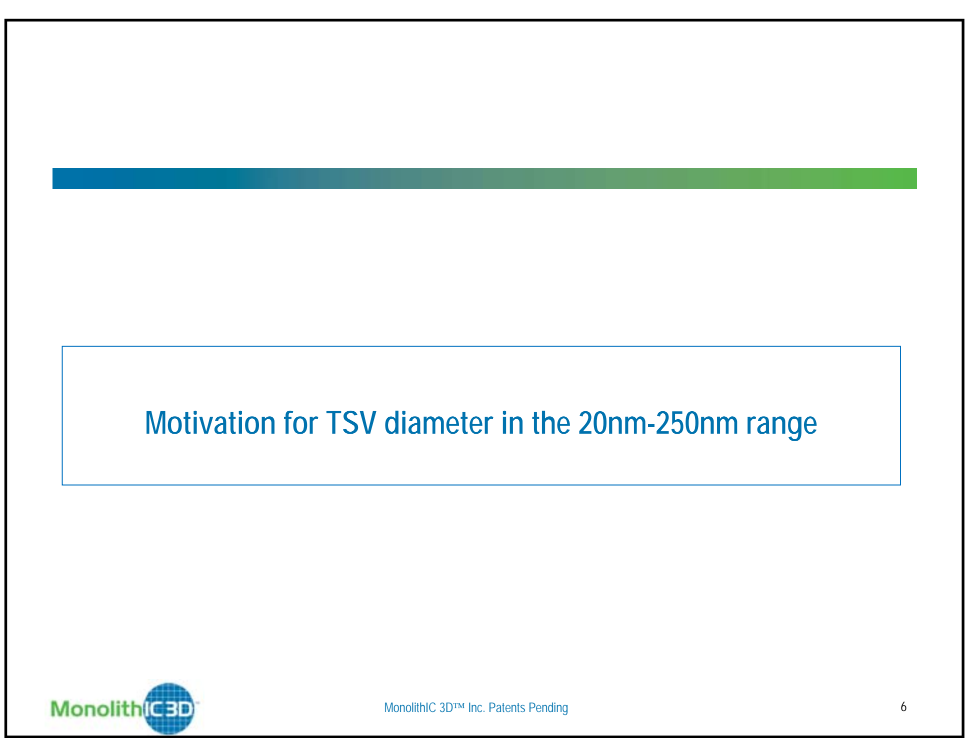

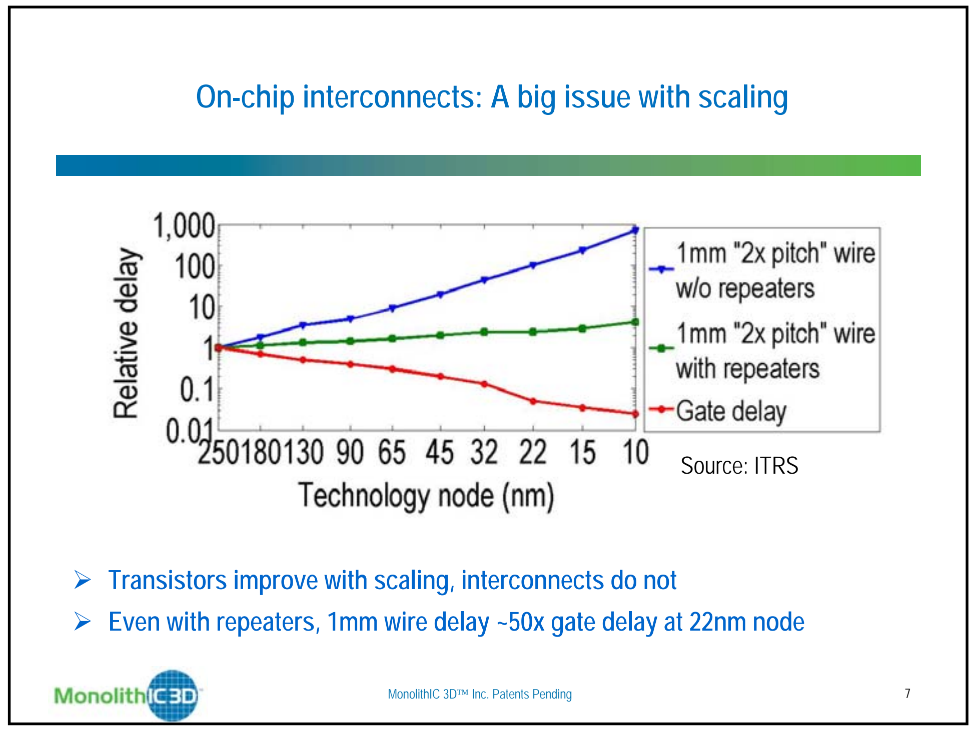
On-chip interconnects: A big issue with scaling
Relative delay
1,000
100
10
1
0.1
0.01
250 180 130 90 65 45 32 22 15 10
Technology node (nm)
1mm "2x pitch" wire w/o repeaters
1mm "2x pitch" wire with repeaters
Gate delay
Source: ITRS
➢ Transistors improve with scaling, interconnects do not
➢ Even with repeaters, 1mm wire delay ~50x gate delay at 22nm node
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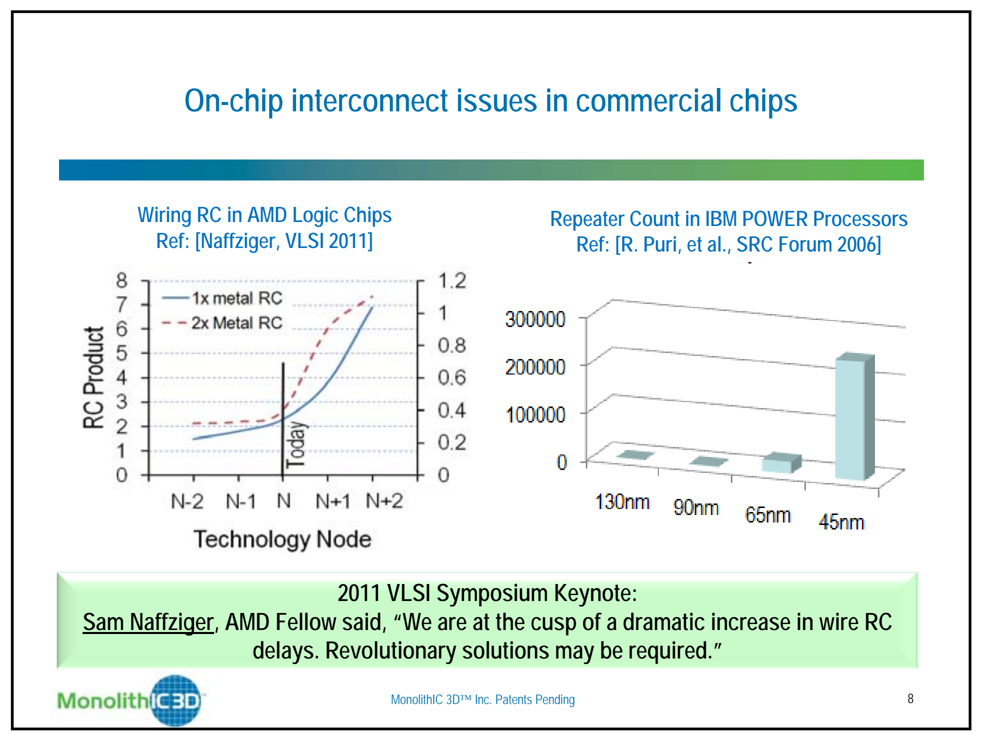
On-chip interconnect issues in commercial chips
Wiring RC in AMD Logic Chips
Ref: [Naffziger, VLSI 2011]
RC Product
1x metal RC
2x Metal RC
Today
N-2 N-1 N N+1 N+2
Technology Node
Repeater Count in IBM POWER Processors
Ref: [R. Puri, et al., SRC Forum 2006]
300000
200000
100000
0
130nm 90nm 65nm 45nm
2011 VLSI Symposium Keynote:
Sam Naffziger, AMD Fellow said, "We are at the cusp of a dramatic increase in wire RC delays. Revolutionary solutions may be required."
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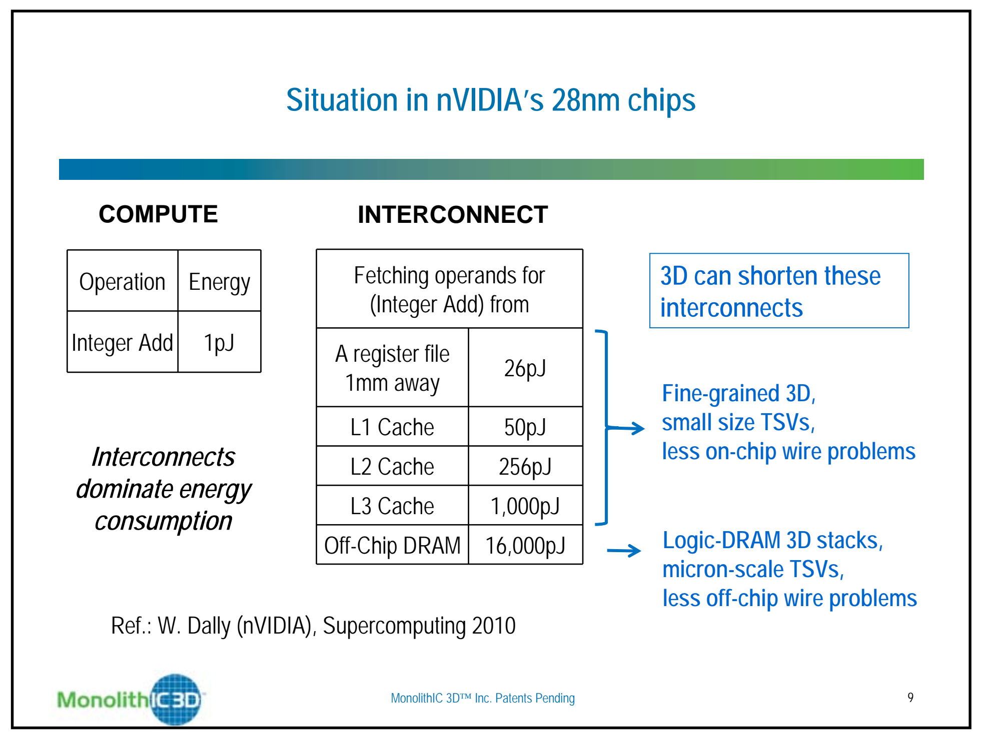
Situation in nVIDIA's 28nm chips
COMPUTE
INTERCONNECT
Operation
Energy
Integer Add
1pJ
Fetching operands for (Integer Add) from
A register file 1mm away
26pJ
L1 Cache
50pJ
L2 Cache
256pJ
L3 Cache
1,000pJ
Off-Chip DRAM
16,000pJ
Interconnects dominate energy consumption
3D can shorten these interconnects
Fine-grained 3D, small size TSVs, less on-chip wire problems
Logic-DRAM 3D stacks, micron-scale TSVs, less off-chip wire problems
Ref.: W. Dally (nVIDIA), Supercomputing 2010
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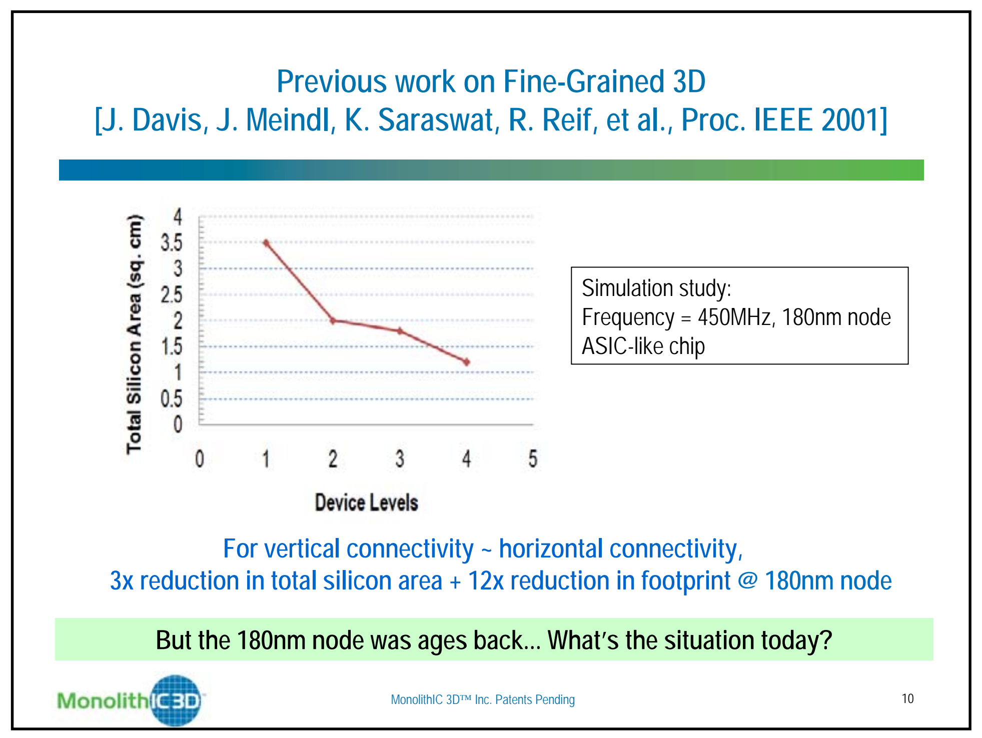
Previous work on Fine-Grained 3D
[J. Davis, J. Meindl, K. Saraswat, R. Reif, et al., Proc. IEEE 2001]
Total Silicon Area (sq. cm)
4
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
5
Device Levels
Simulation study:
Frequency = 450MHz, 180nm node
ASIC-like chip
For vertical connectivity ~ horizontal connectivity,
3x reduction in total silicon area + 12x reduction in footprint @ 180nm node
But the 180nm node was ages back... What's the situation today?
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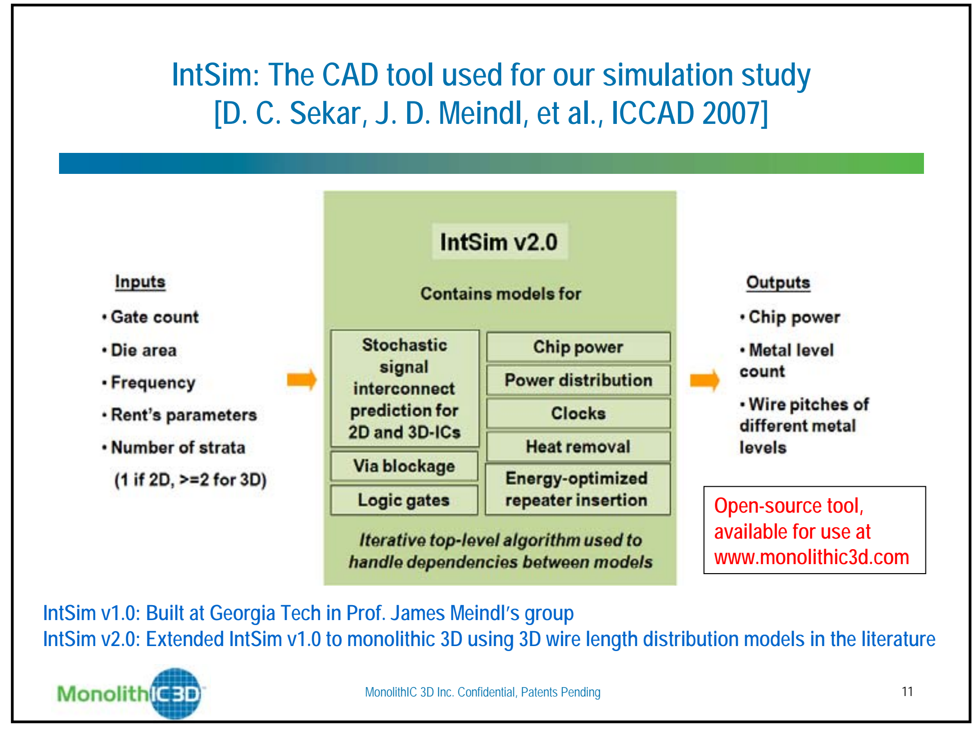

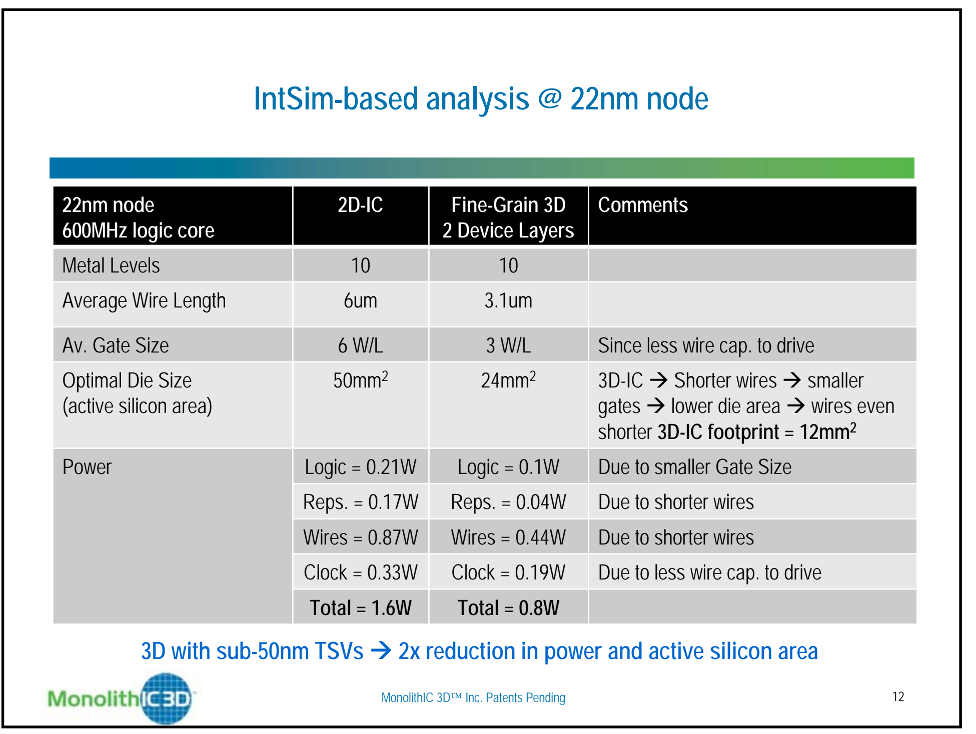

22nm node 600MHz logic core	2D-IC	Fine-Grain 3D 2 Device Layers	Comments
Metal Levels	10	10	
Average Wire Length	6um	3.1um	
Av. Gate Size	6 W/L	3 W/L	Since less wire cap. to drive
Optimal Die Size (active silicon area)	50mm^2	24mm^2	3D-IC → Shorter wires → smaller gates → lower die area → wires even shorter **3D-IC footprint = 12mm^2**
Power	Logic = 0.21W	Logic = 0.1W	Due to smaller Gate Size
	Reps. = 0.17W	Reps. = 0.04W	Due to shorter wires
	Wires = 0.87W	Wires = 0.44W	Due to shorter wires
	Clock = 0.33W	Clock = 0.19W	Due to less wire cap. to drive
	Total = 1.6W	**Total = 0.8W**	

Scaling with 3D or conventional 0.7x scaling?

Analysis with IntSim v2.0 Same logic core scaled	2D-IC @22nm	2D-IC @ 15nm	Fine-Grained 3D 2 Device Layers @ 22nm
Frequency	600MHz	600MHz	600MHz
Metal Levels	10	12	10
Footprint	50mm^2	25mm^2	12mm^2
Total Silicon Area (a.k.a "Die size")	**50mm^2**	**25mm^2**	**24mm^2**
Average Wire Length	6um	4.2um	3.1um
Av. Gate Size	6 W/L	4 W/L	3 W/L
Power	**1.6W**	**0.7W**	**0.8W**

- Fine-Grained 3D could provide similar benefits to a generation of scaling
- Without the need for costly lithography upgrades
- Let's understand this better…

Theory: 2D Scaling vs. 3D Scaling

	2D Scaling (0.7x scaling)		Fine-Grained 3D Scaling (2 device layers)
	Ideal	Today, V_{dd} scales slower	
Chip Footprint	0.5x		0.25x-0.5x (see slide 12)
Long wire length $\alpha \sqrt{Footprint}$	0.7x		0.5x-0.7x
Long wire capacitance	0.7x		0.5x-0.7x
Long wire resistance	*>1.4x*		0.5-0.7x
Gate Capacitance	0.7x		Same
Driver (Gate) Resistance (Vdd/Idsat)	Same	Increases	Same

Overall benefits seen with IntSim have basis in theory

- 2D scaling scores: Gate capacitance
- 3D scaling scores: Wire resistance, driver resistance, wire capacitance

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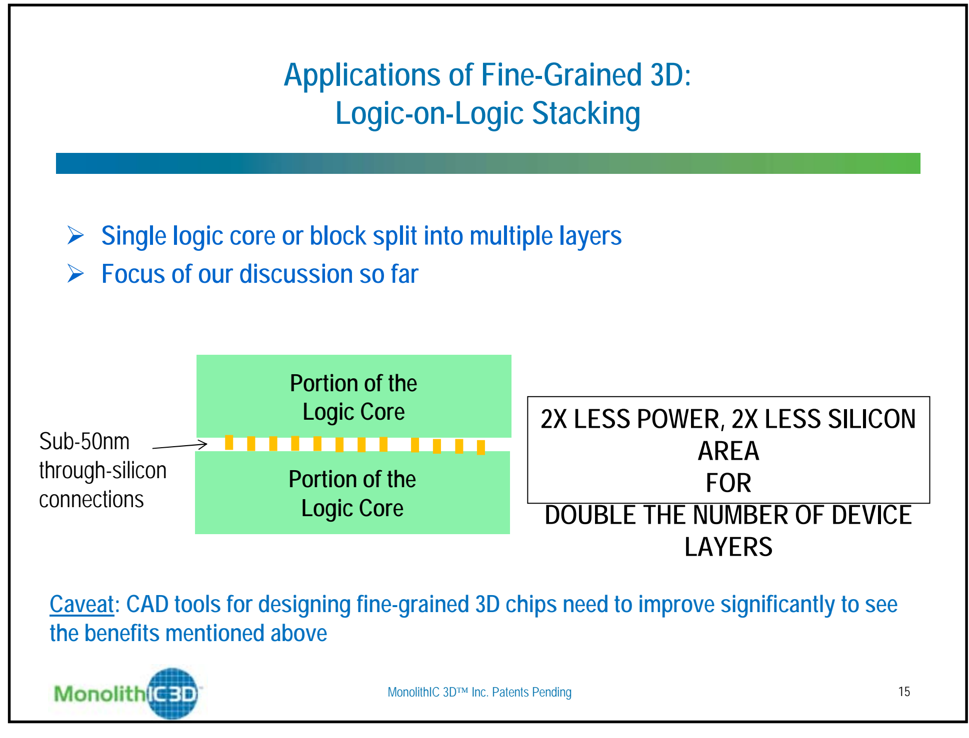
Applications of Fine-Grained 3D:
Logic-on-Logic Stacking
Single logic core or block split into multiple layers
Focus of our discussion so far
Portion of the Logic Core
Sub-50nm through-silicon connections
Portion of the Logic Core
2X LESS POWER, 2X LESS SILICON AREA FOR DOUBLE THE NUMBER OF DEVICE LAYERS
Caveat: CAD tools for designing fine-grained 3D chips need to improve significantly to see the benefits mentioned above
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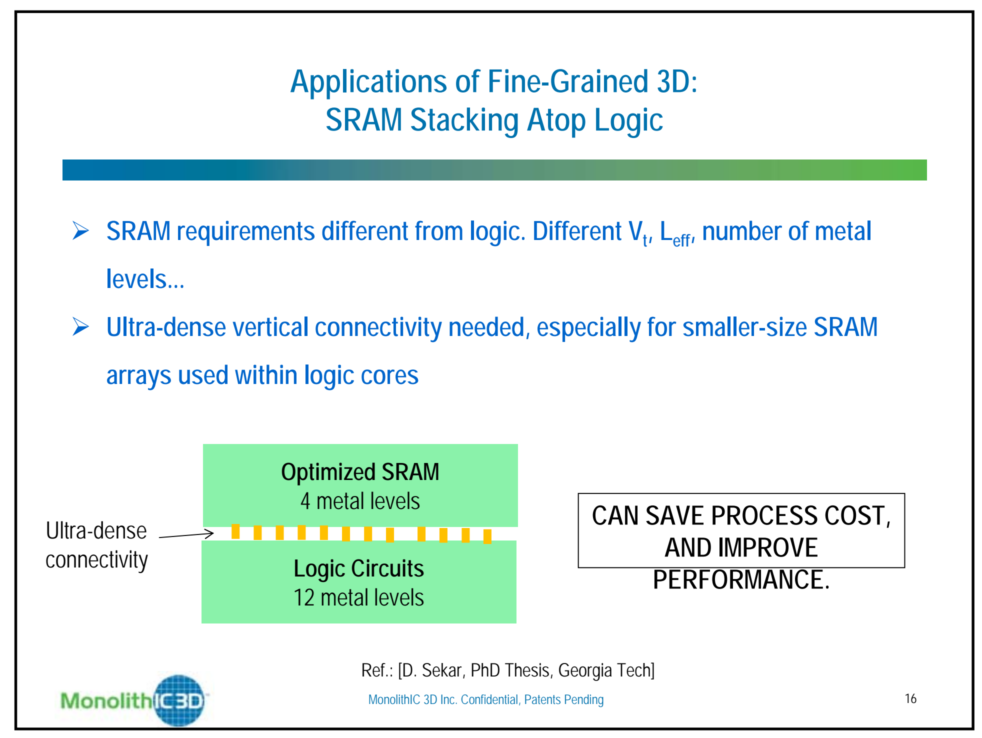
Applications of Fine-Grained 3D:
SRAM Stacking Atop Logic
SRAM requirements different from logic. Different V_t, L_{eff}, number of metal levels...
Ultra-dense vertical connectivity needed, especially for smaller-size SRAM arrays used within logic cores
Optimized SRAM
4 metal levels
Ultra-dense connectivity
Logic Circuits
12 metal levels
CAN SAVE PROCESS COST, AND IMPROVE PERFORMANCE.
Ref.: [D. Sekar, PhD Thesis, Georgia Tech]
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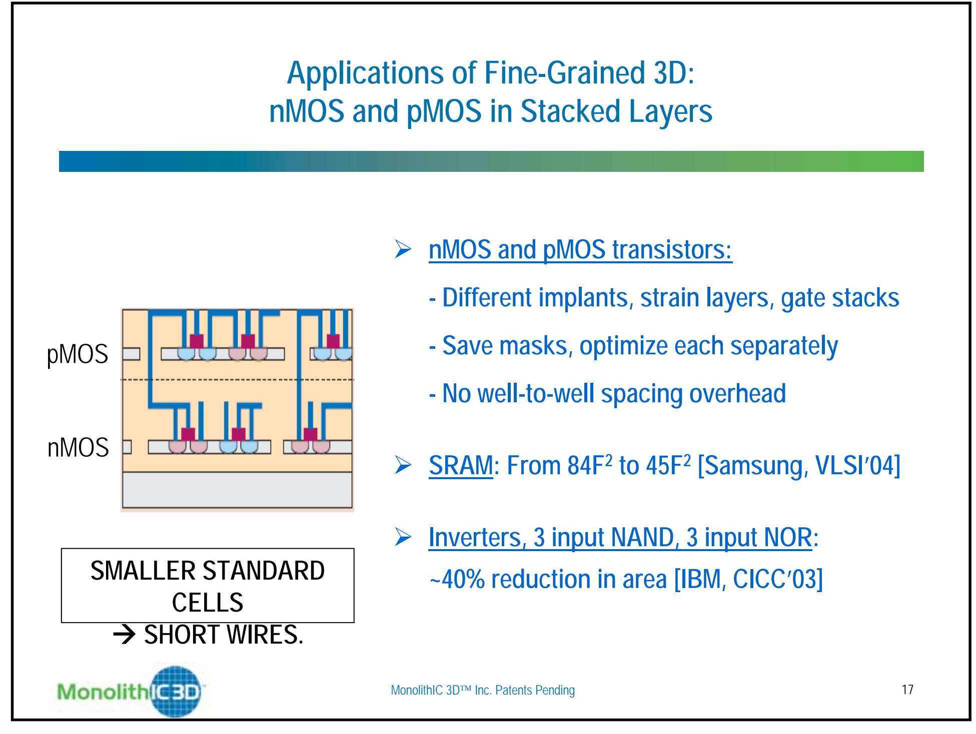
Applications of Fine-Grained 3D:
nMOS and pMOS in Stacked Layers
pMOS
nMOS
SMALLER STANDARD CELLS
→ SHORT WIRES.
nMOS and pMOS transistors:
- Different implants, strain layers, gate stacks
- Save masks, optimize each separately
- No well-to-well spacing overhead
SRAM: From 84F² to 45F² [Samsung, VLSI'04]
Inverters, 3 input NAND, 3 input NOR:
~40% reduction in area [IBM, CICC'03]
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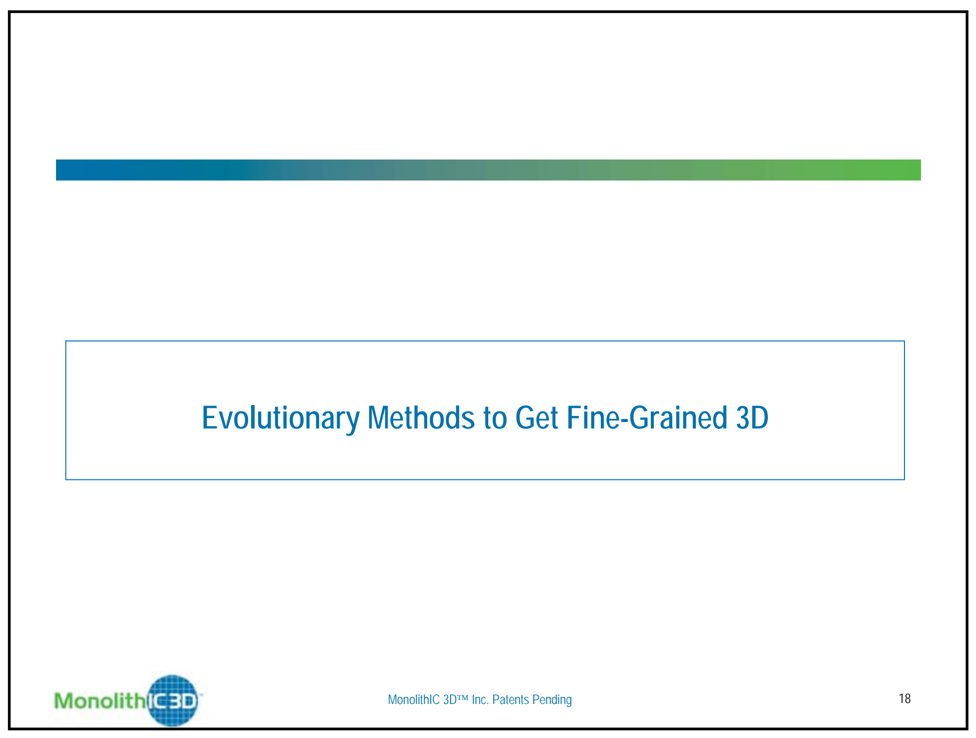
Evolutionary Methods to Get Fine-Grained 3D
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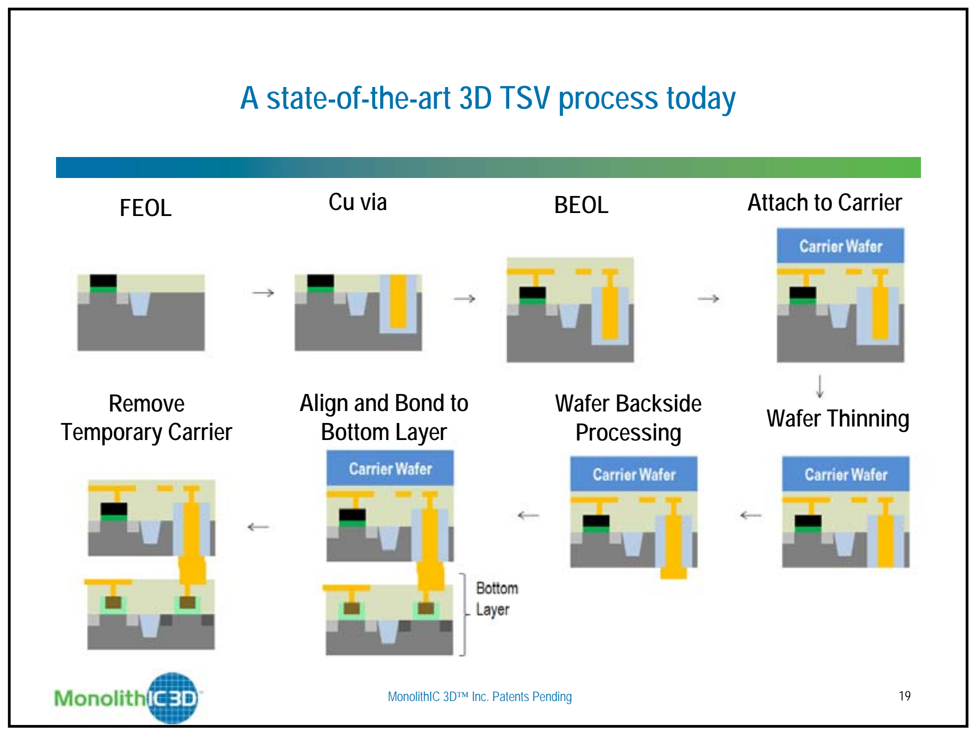
A state-of-the-art 3D TSV process today
FEOL
Cu via
BEOL
Attach to Carrier
Carrier Wafer
Wafer Thinning
Carrier Wafer
Wafer Backside Processing
Carrier Wafer
Align and Bond to Bottom Layer
Carrier Wafer
Bottom Layer
Remove Temporary Carrier
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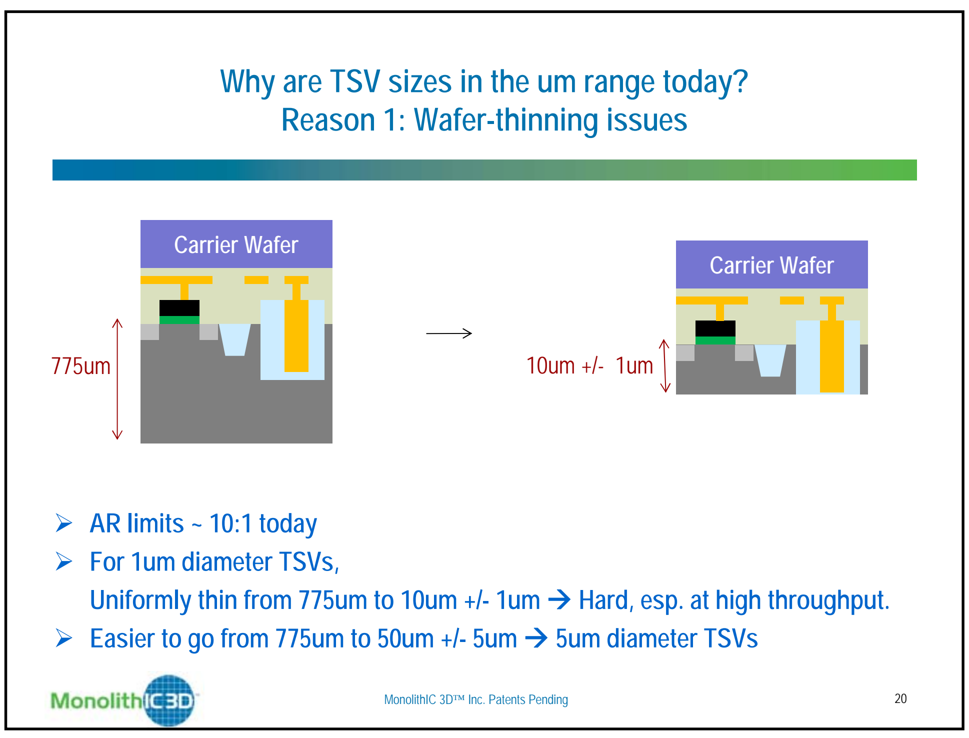
Why are TSV sizes in the um range today?
Reason 1: Wafer-thinning issues
Carrier Wafer
775um
Carrier Wafer
10um +/- 1um
AR limits ~ 10:1 today
For 1um diameter TSVs,
Uniformly thin from 775um to 10um +/- 1um → Hard, esp. at high throughput.
Easier to go from 775um to 50um +/- 5um → 5um diameter TSVs
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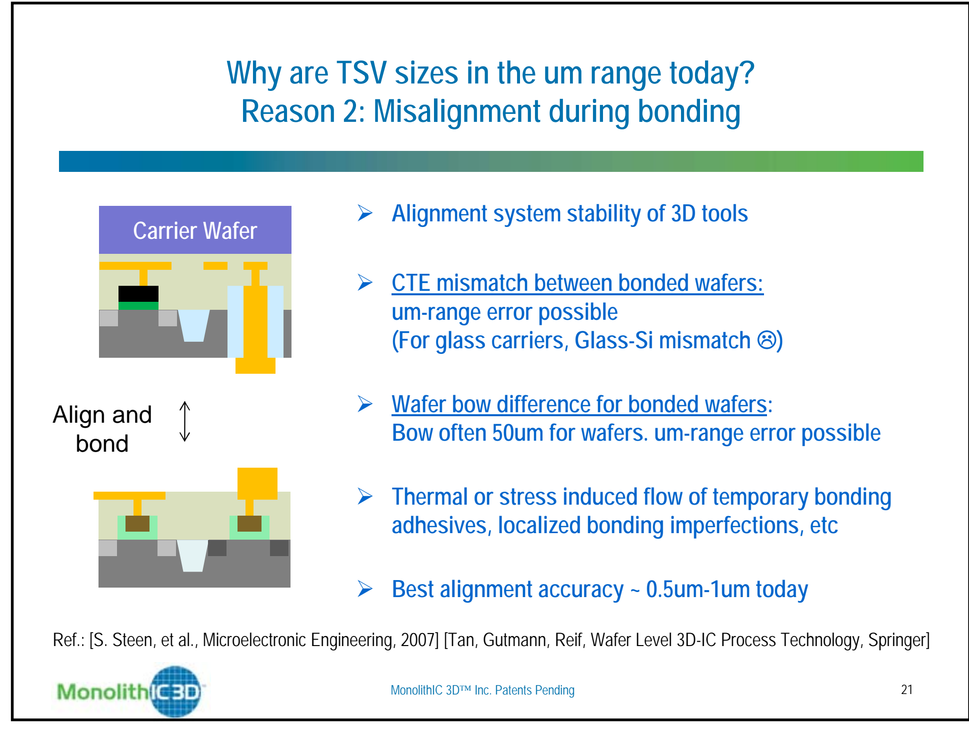
Why are TSV sizes in the um range today?
Reason 2: Misalignment during bonding
Carrier Wafer
Align and bond
Alignment system stability of 3D tools
CTE mismatch between bonded wafers:
um-range error possible
(For glass carriers, Glass-Si mismatch ☹)
Wafer bow difference for bonded wafers:
Bow often 50um for wafers. um-range error possible
Thermal or stress induced flow of temporary bonding adhesives, localized bonding imperfections, etc
Best alignment accuracy ~ 0.5um-1um today
Ref.: [S. Steen, et al., Microelectronic Engineering, 2007] [Tan, Gutmann, Reif, Wafer Level 3D-IC Process Technology, Springer]
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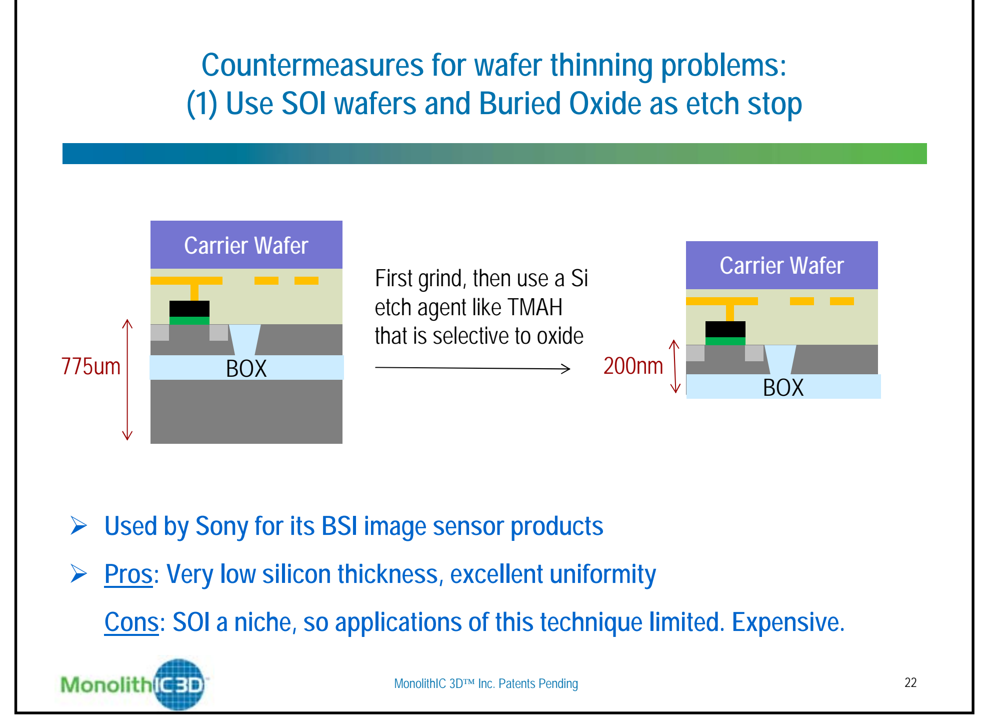
Countermeasures for wafer thinning problems:
(1) Use SOI wafers and Buried Oxide as etch stop
Carrier Wafer
775um
BOX
First grind, then use a Si etch agent like TMAH that is selective to oxide
Carrier Wafer
200nm
BOX
Used by Sony for its BSI image sensor products
Pros: Very low silicon thickness, excellent uniformity
Cons: SOI a niche, so applications of this technique limited. Expensive.
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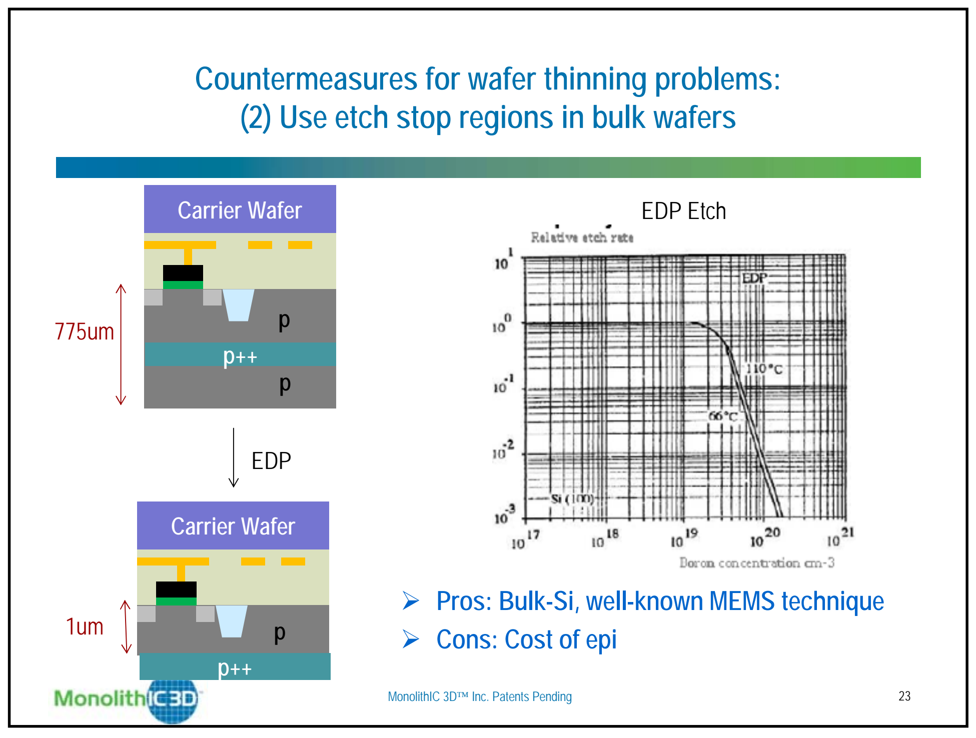
Countermeasures for wafer thinning problems:
(2) Use etch stop regions in bulk wafers
Carrier Wafer
775um
p
p++
p
EDP
Carrier Wafer
1um
p
p++
EDP Etch
Relative etch rate
EDP
110°C
66°C
Si (100)
Boron concentration cm-3
Pros: Bulk-Si, well-known MEMS technique
Cons: Cost of epi
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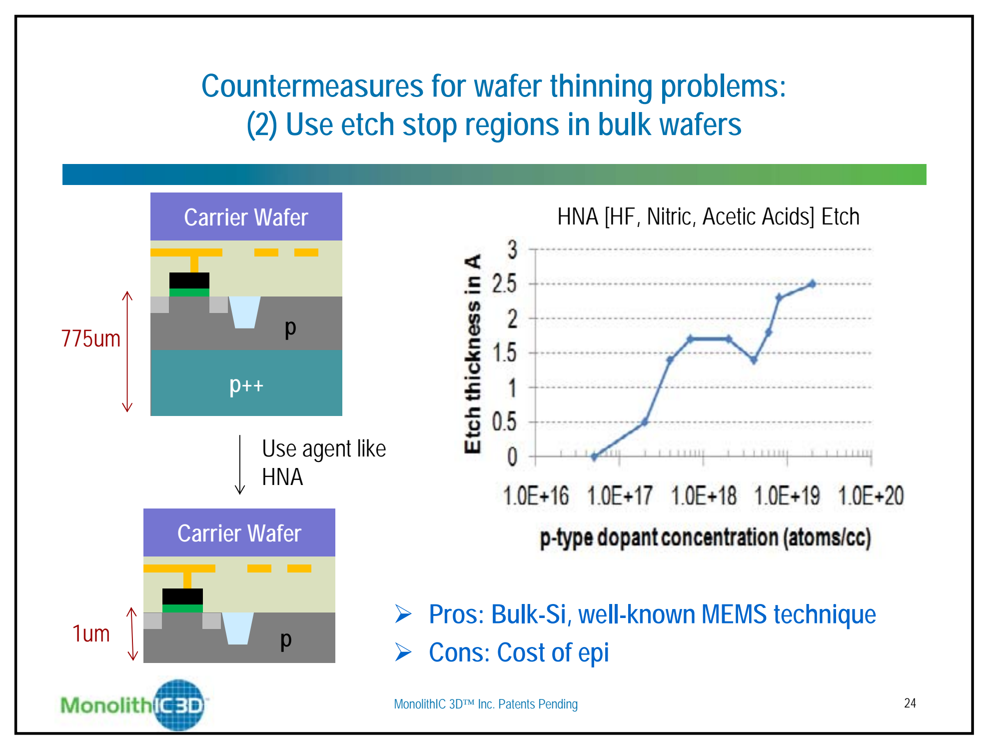
Countermeasures for wafer thinning problems:
(2) Use etch stop regions in bulk wafers
Carrier Wafer
775um
p
p++
Use agent like HNA
Carrier Wafer
1um
p
HNA [HF, Nitric, Acetic Acids] Etch
Etch thickness in A
3
2.5
2
1.5
1
0.5
0
1.0E+16 1.0E+17 1.0E+18 1.0E+19 1.0E+20
p-type dopant concentration (atoms/cc)
Pros: Bulk-Si, well-known MEMS technique
Cons: Cost of epi
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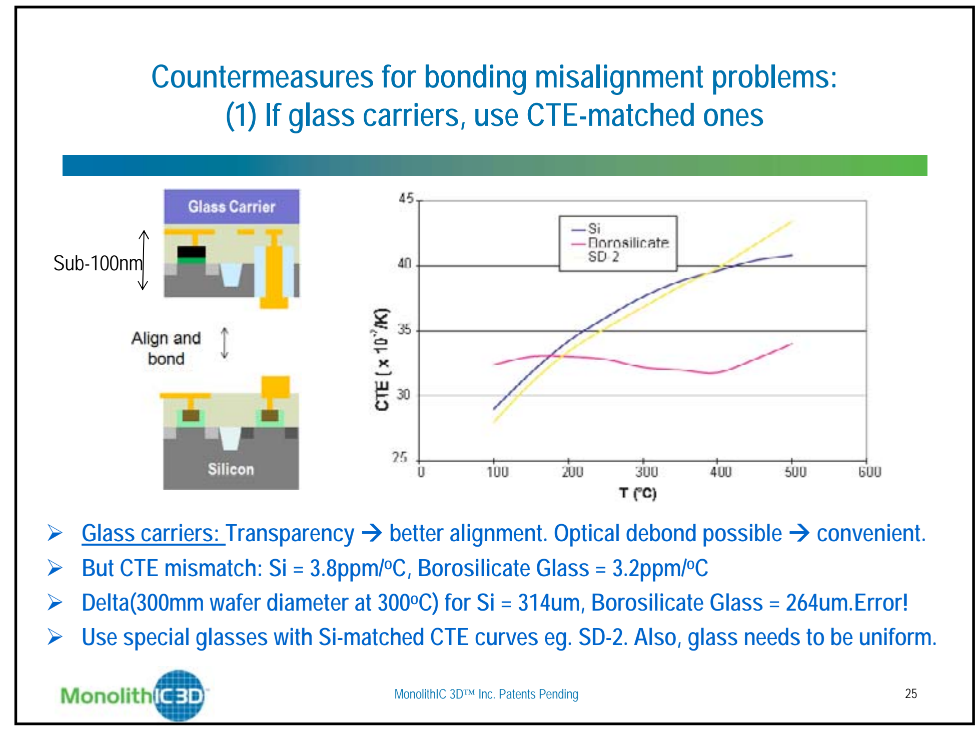
Countermeasures for bonding misalignment problems:
(1) If glass carriers, use CTE-matched ones
Glass Carrier
Sub-100nm
Align and bond
Silicon
Si
Borosilicate
SD 2
CTE (x 10⁻⁷/K)
T (°C)
Glass carriers: Transparency → better alignment. Optical debond possible → convenient.
But CTE mismatch: Si = 3.8ppm/°C, Borosilicate Glass = 3.2ppm/°C
Delta(300mm wafer diameter at 300°C) for Si = 314um, Borosilicate Glass = 264um.Error!
Use special glasses with Si-matched CTE curves eg. SD-2. Also, glass needs to be uniform.
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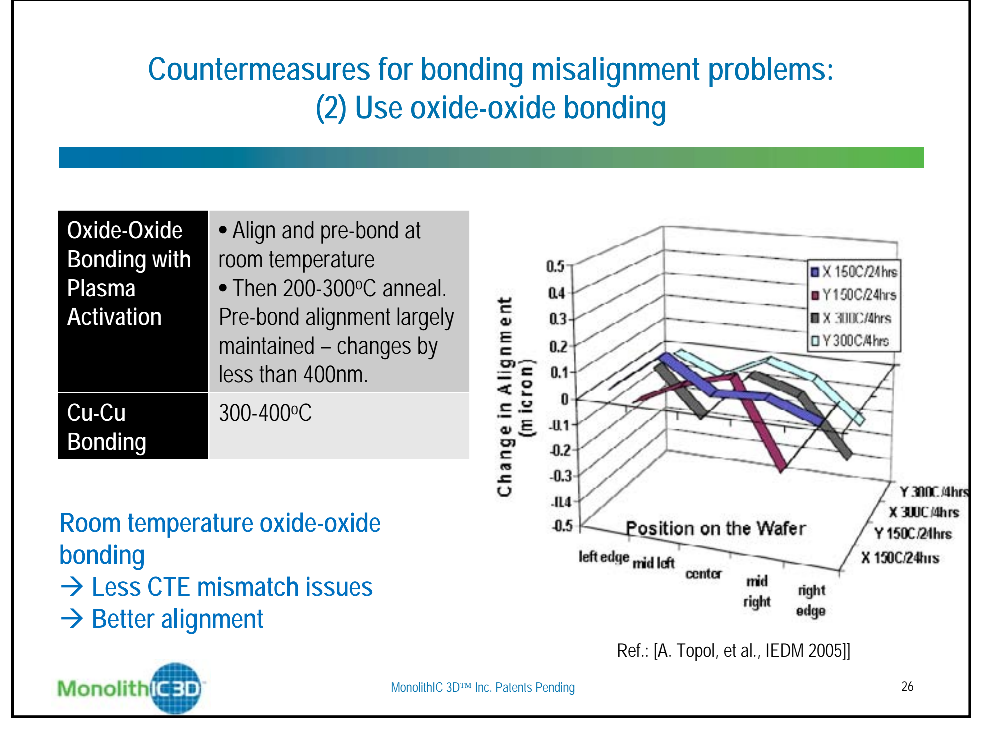
Countermeasures for bonding misalignment problems:
(2) Use oxide-oxide bonding
Oxide-Oxide Bonding with Plasma Activation
• Align and pre-bond at room temperature
• Then 200-300°C anneal. Pre-bond alignment largely maintained – changes by less than 400nm.
Cu-Cu Bonding
300-400°C
Room temperature oxide-oxide bonding
→ Less CTE mismatch issues
→ Better alignment
Change in Alignment (micron)
X 150C/24hrs
Y 150C/24hrs
X 300C/4hrs
Y 300C/4hrs
Position on the Wafer
left edge
mid left
center
mid right
right edge
Ref.: [A. Topol, et al., IEDM 2005]]
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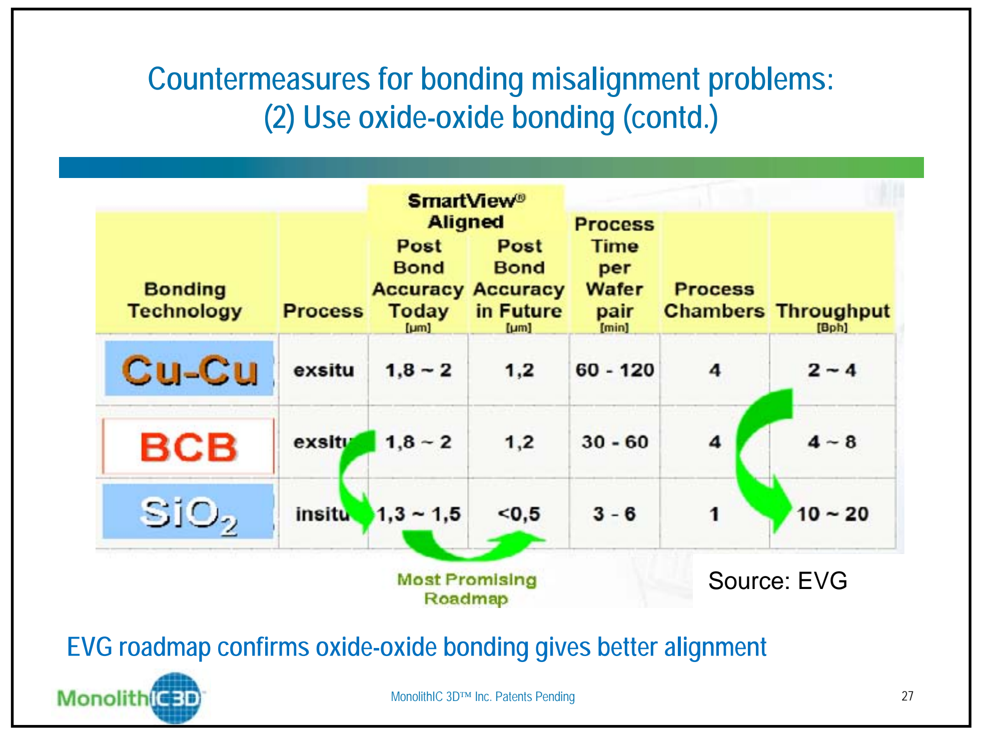
Countermeasures for bonding misalignment problems:
(2) Use oxide-oxide bonding (contd.)
SmartView® Aligned
Bonding Technology
Process
Post Bond Accuracy Today [µm]
Post Bond Accuracy in Future [µm]
Process Time per Wafer pair [min]
Process Chambers
Throughput [Bph]
Cu-Cu
exsitu
1,8 ~ 2
1,2
60 - 120
4
2 ~ 4
BCB
exsitu
1,8 ~ 2
1,2
30 - 60
4
4 ~ 8
SiO2
insitu
1,3 ~ 1,5
<0,5
3 - 6
1
10 ~ 20
Most Promising Roadmap
Source: EVG
EVG roadmap confirms oxide-oxide bonding gives better alignment
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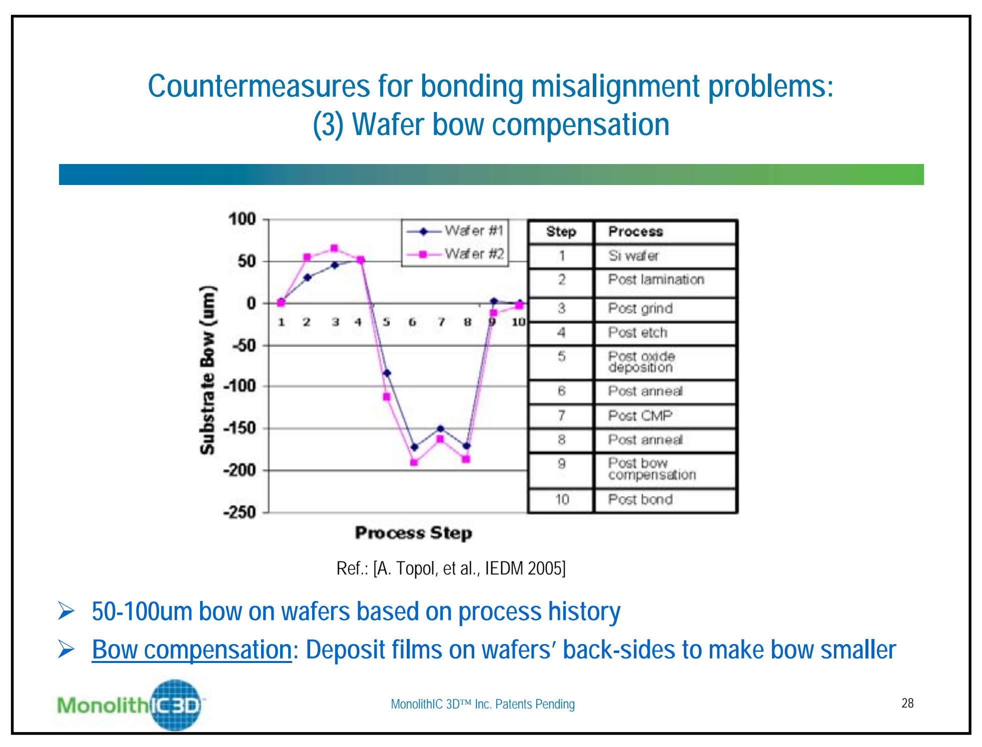
Countermeasures for bonding misalignment problems:
(3) Wafer bow compensation
Substrate Bow (um)
100
50
0
-50
-100
-150
-200
-250
1 2 3 4 5 6 7 8 9 10
Process Step
Wafer #1
Wafer #2
Step
Process
1 Si wafer
2 Post lamination
3 Post grind
4 Post etch
5 Post oxide deposition
6 Post anneal
7 Post CMP
8 Post anneal
9 Post bow compensation
10 Post bond
Ref.: [A. Topol, et al., IEDM 2005]
50-100um bow on wafers based on process history
Bow compensation: Deposit films on wafers' back-sides to make bow smaller
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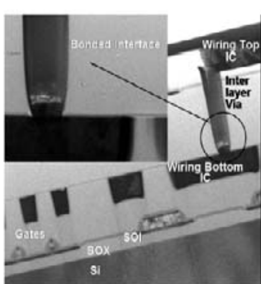
IBM's work in this area
[S. Koester, et al. IBM Journal R&D, 2008] [A. Topol, et al., IEDM 2005]



- Borofloat glass carrier – ok CTE match, transparent
- Thinning with SOI wafers and BOX etch stop
- Low temperature oxide-oxide bonding
- Wafer bow compensation

- Best demo so far = 6.7um pitch.
- IBM: "2um pitch possible if bonder with sub-0.5um misalignment available"

Research Opportunities: Silicon Temporary Carriers for High-Density TSVs?

Reasons for historic preference towards glass

- Transparent. Look through and align. Less error.
- Temporary bonding adhesives optically de-bondable. Withstand 300-350°C bumpless bonding.

Why silicon has promise

- CTE
- Cheap, highly smooth
- Emerging high T stable temporary bonding adhesives for silicon
- Alignment tools for non-transparent carriers improving fast
- $$$ invested in silicon temporary carriers for bump-based 3D-TSV

Research Opportunities in the High-Density TSV Space

- Throughput and cost optimization for all process steps
- Improved wafer bow compensation schemes
- Bonders with better alignment capabilities. A number of ideas from regular litho can be applied to 3D.
- Lower thermal budget for bonding
- Temporary bonding adhesives

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Revolutionary Methods to Get Fine-Grained 3D

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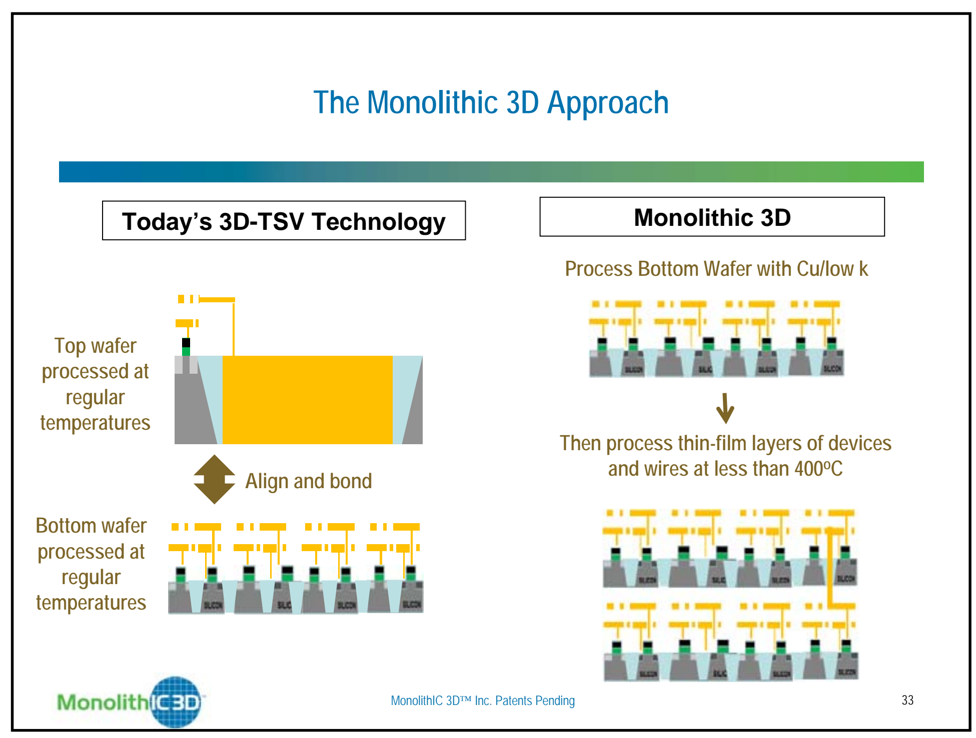
The Monolithic 3D Approach
Today's 3D-TSV Technology
Monolithic 3D
Process Bottom Wafer with Cu/low k
Top wafer processed at regular temperatures
Align and bond
Then process thin-film layers of devices and wires at less than 400ºC
Bottom wafer processed at regular temperatures
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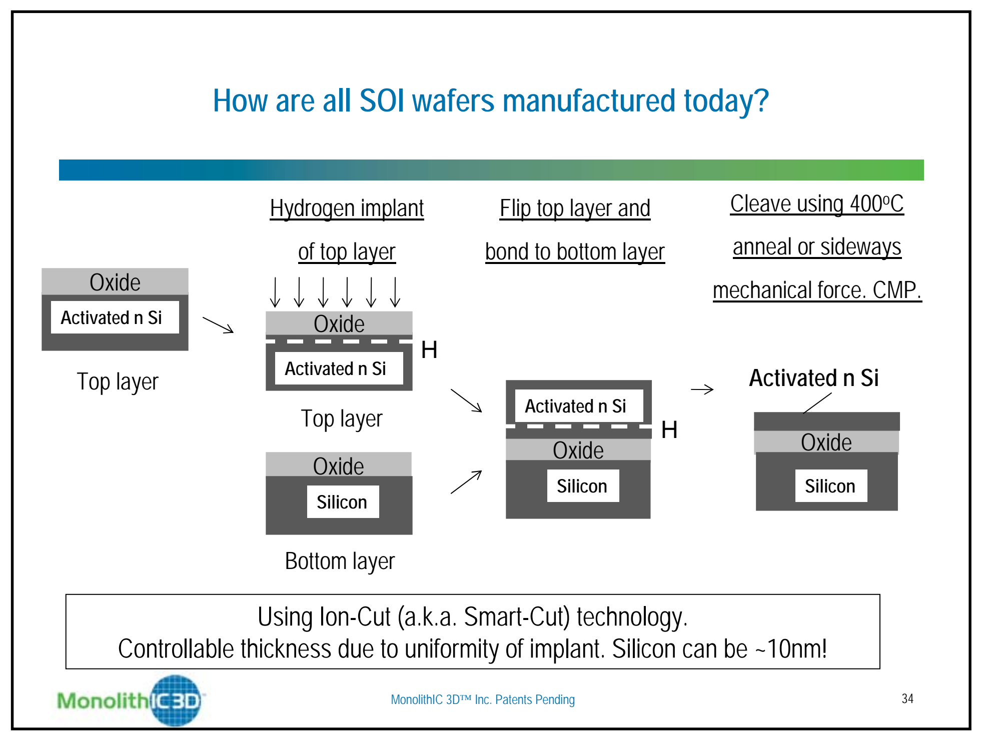
How are all SOI wafers manufactured today?
Hydrogen implant of top layer
Flip top layer and bond to bottom layer
Cleave using 400ºC anneal or sideways mechanical force. CMP.
Oxide
Activated n Si
Top layer
H
Silicon
Bottom layer
Using Ion-Cut (a.k.a. Smart-Cut) technology.
Controllable thickness due to uniformity of implant. Silicon can be ~10nm!
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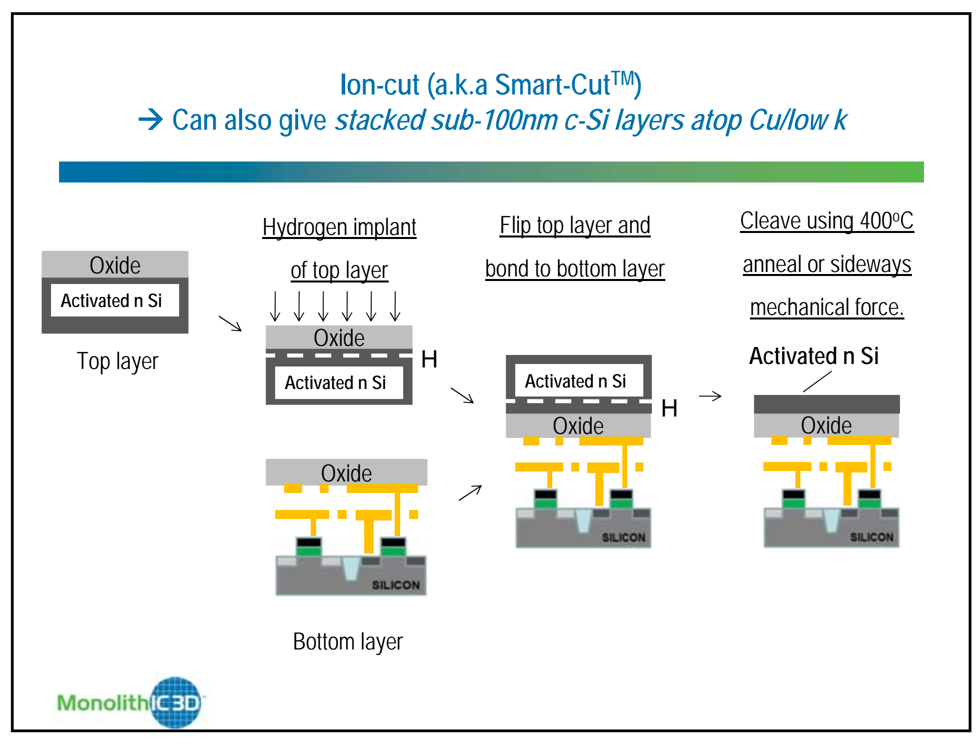
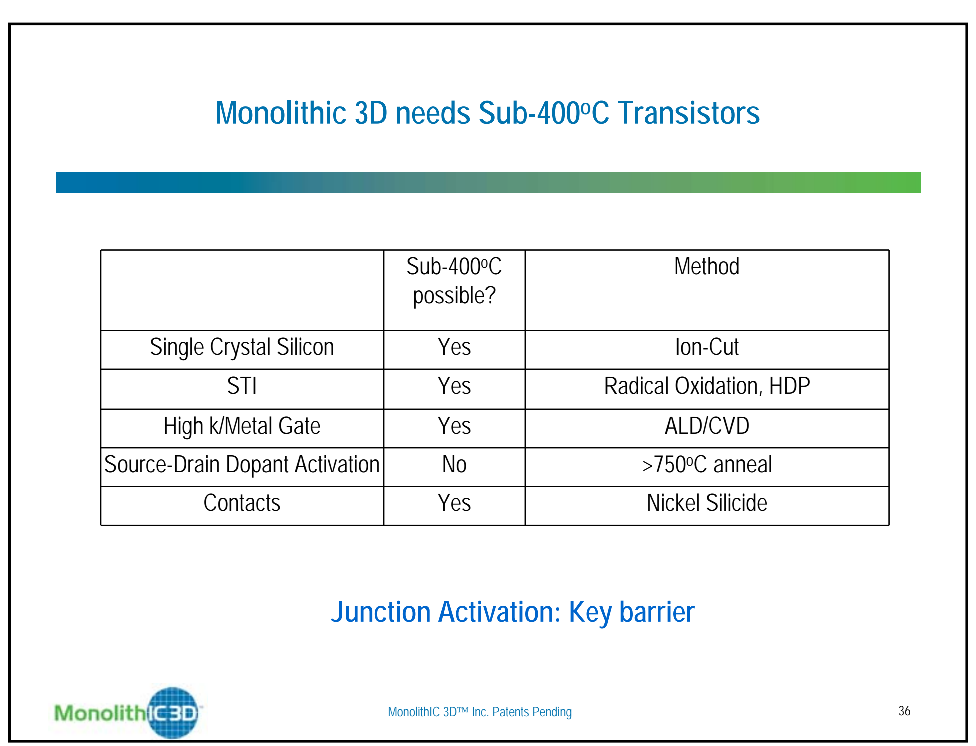
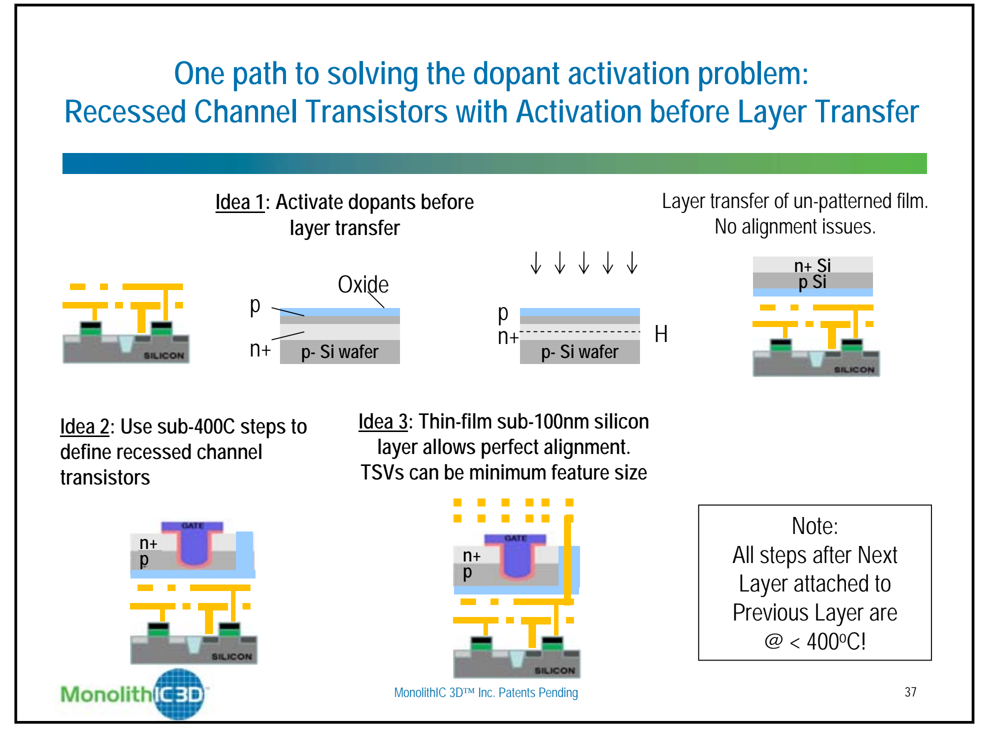




	Sub-400°C possible?	Method
Single Crystal Silicon	Yes	Ion-Cut
STI	Yes	Radical Oxidation, HDP
High k/Metal Gate	Yes	ALD/CVD
Source-Drain Dopant Activation	No	>750°C anneal
Contacts	Yes	Nickel Silicide


One path to solving the dopant activation problem:
Recessed Channel Transistors with Activation before Layer Transfer
Idea 1: Activate dopants before layer transfer
Layer transfer of un-patterned film.
No alignment issues.
Oxide
p
n+
p- Si wafer
H
n+ Si
p Si
SILICON
Idea 2: Use sub-400C steps to define recessed channel transistors
Idea 3: Thin-film sub-100nm silicon layer allows perfect alignment.
TSVs can be minimum feature size
Note:
All steps after Next Layer attached to Previous Layer are @ < 400ºC!
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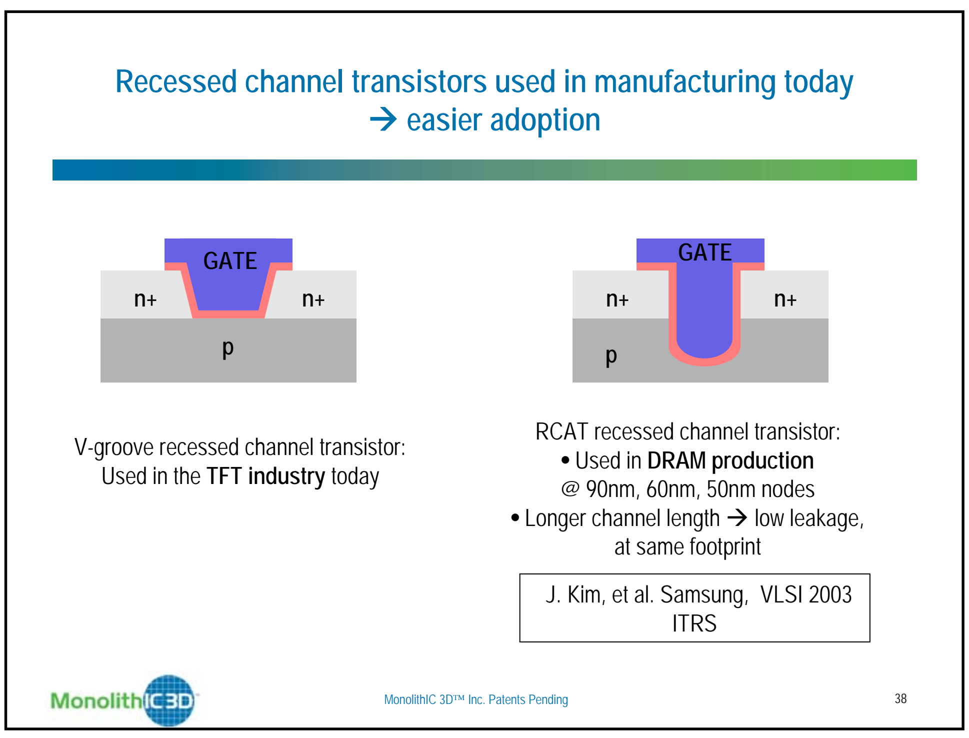
Recessed channel transistors used in manufacturing today
→ easier adoption
GATE
n+
n+
p
V-groove recessed channel transistor:
Used in the TFT industry today
RCAT recessed channel transistor:
• Used in DRAM production
@ 90nm, 60nm, 50nm nodes
• Longer channel length → low leakage,
at same footprint
J. Kim, et al. Samsung, VLSI 2003
ITRS
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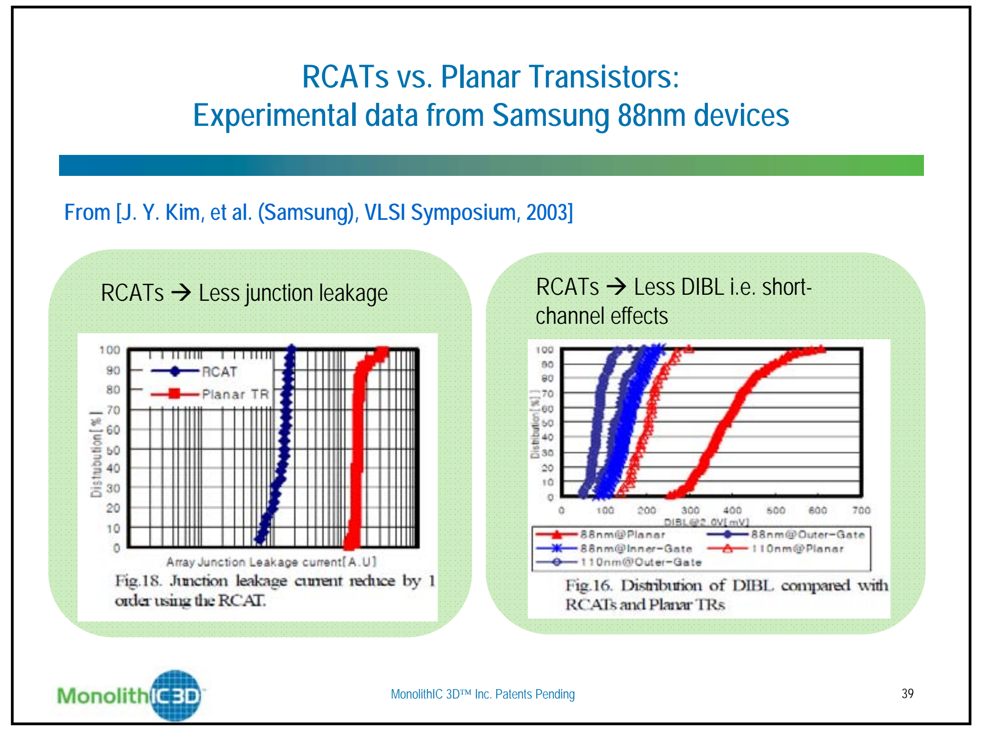
RCATs vs. Planar Transistors:
Experimental data from Samsung 88nm devices
From [J. Y. Kim, et al. (Samsung), VLSI Symposium, 2003]
RCATs → Less junction leakage
RCAT
Planar TR
Array Junction Leakage current[A.U]
Fig.18. Junction leakage current reduce by 1 order using the RCAT.
RCATs → Less DIBL i.e. short-channel effects
88nm@Planar
88nm@Outer-Gate
88nm@Inner-Gate
110nm@Planar
110nm@Outer-Gate
Fig.16. Distribution of DIBL compared with RCATs and Planar TRs
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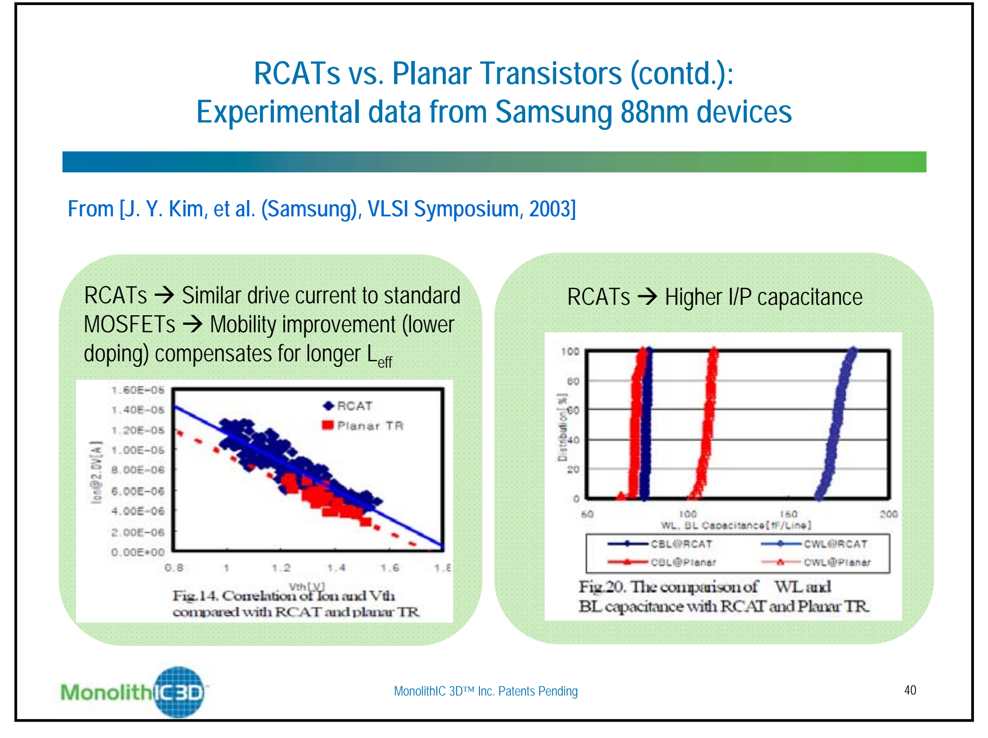
RCATs vs. Planar Transistors (contd.):
Experimental data from Samsung 88nm devices
From [J. Y. Kim, et al. (Samsung), VLSI Symposium, 2003]
RCATs → Similar drive current to standard MOSFETs → Mobility improvement (lower doping) compensates for longer Leff
RCAT
Planar TR
Ion@2.0V[A]
Vth[V]
Fig.14. Correlation of Ion and Vth compared with RCAT and planar TR
RCATs → Higher I/P capacitance
WL, BL Capacitance[fF/Line]
CBL@RCAT
CWL@RCAT
CBL@Planar
CWL@Planar
Fig.20. The comparison of WL and BL capacitance with RCAT and Planar TR.
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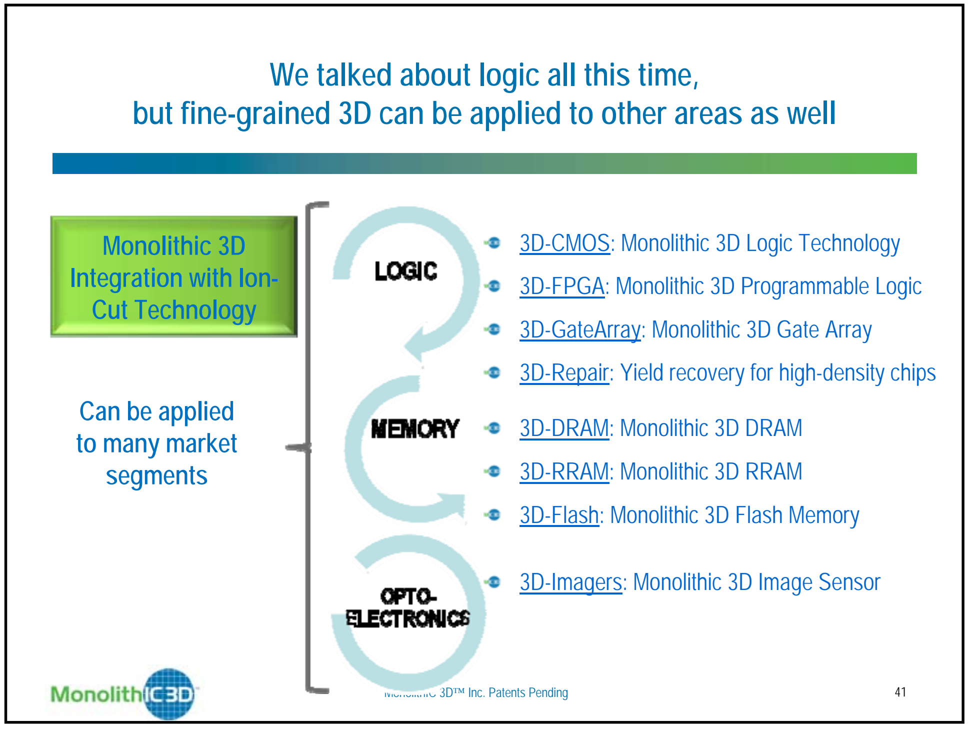
We talked about logic all this time,
but fine-grained 3D can be applied to other areas as well
Monolithic 3D Integration with Ion-Cut Technology
Can be applied to many market segments
LOGIC
MEMORY
OPTO-ELECTRONICS
3D-CMOS: Monolithic 3D Logic Technology
3D-FPGA: Monolithic 3D Programmable Logic
3D-GateArray: Monolithic 3D Gate Array
3D-Repair: Yield recovery for high-density chips
3D-DRAM: Monolithic 3D DRAM
3D-RRAM: Monolithic 3D RRAM
3D-Flash: Monolithic 3D Flash Memory
3D-Imagers: Monolithic 3D Image Sensor
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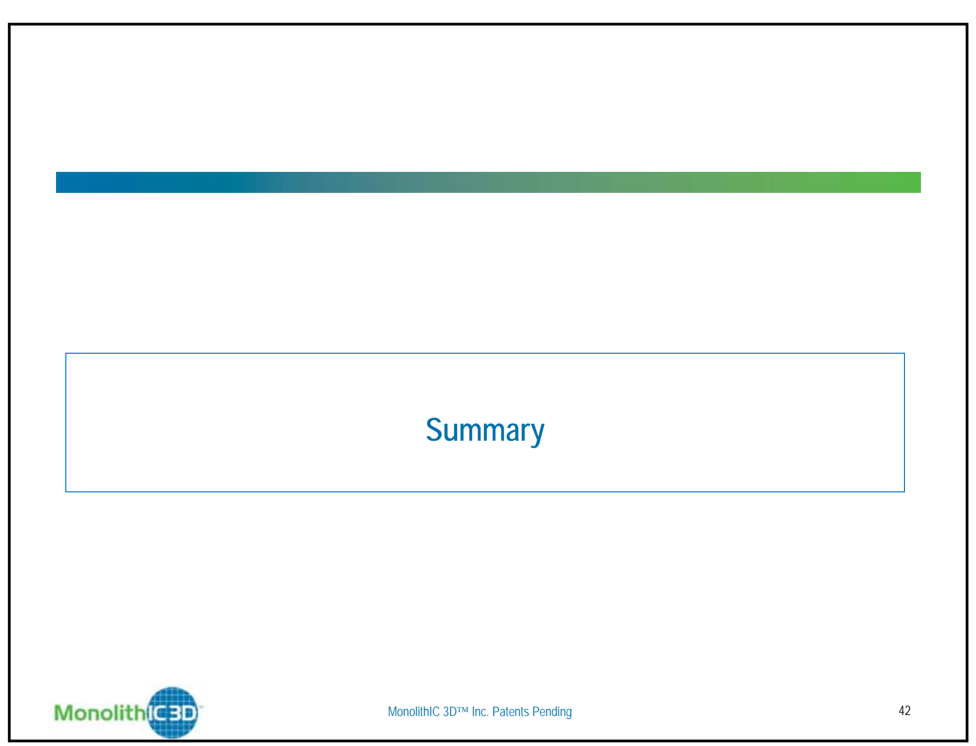
Summary
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Summary

- Today ~5um TSV diameter. Fine-Grained 3D: 20nm-250nm TSV diameter.
- Applications:

  Tackles on-chip interconnect problems

  Logic core split into 2 stacked layers: 2x power, 2x die area savings possible

  SRAM stacking with logic, nMOS and pMOS stacking
- How Fine-Grained 3D?

  Evolutionary extension of 3D-TSV: 2um pitch possible now, could reduce further

  Monolithic 3D: Sub-100nm TSV diameter...

Before we end, a couple of trivia questions...

Trivia Question 1

Commercialization of Fine-Grained 3D:

(A) Is 2 years away

(B) Is 5 years away

(C) Is 10 years away

(D) Will never happen

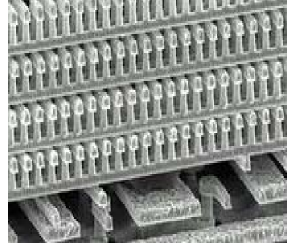
Answer:

Fine-Grained 3D was commercialized 8 years back!

(Trick question ☺)

Fine-Grained 3D was commercialized by Matrix Semiconductor in 2003

- 4-8 monolithically constructed memory layers
- 130nm commercial product
  TSV sizes smaller than 180nm
- Non-volatile memory:
  Multiple layers of poly diodes in series with antifuses
- Startup acquired by SanDisk in 2006



Trivia Question 2

Will you be buying a Fine-Grained 3D product in 4 years?

(A) Yes

(B) No

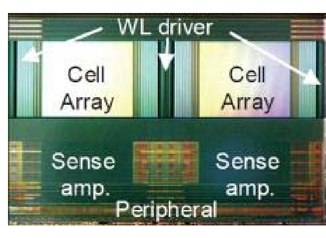
(C) Possibly. Is it on someone's roadmap?

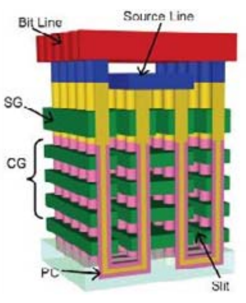
(D) Another trick question?

Answer:

(C) Fine-Grained 3D appears on Toshiba and Samsung's flash memory product roadmaps within 4 years. Maybe you'll see it in your next iPhone? Product roadmaps rarely stick to schedule though. So the answer is maybe.

Toshiba's 32Gb Fine-Grained 3D Prototype
Scheduled to go to production within 4 years





- 16 layers of poly-based monolithic 3D NAND flash memory
- 60nm feature sizes

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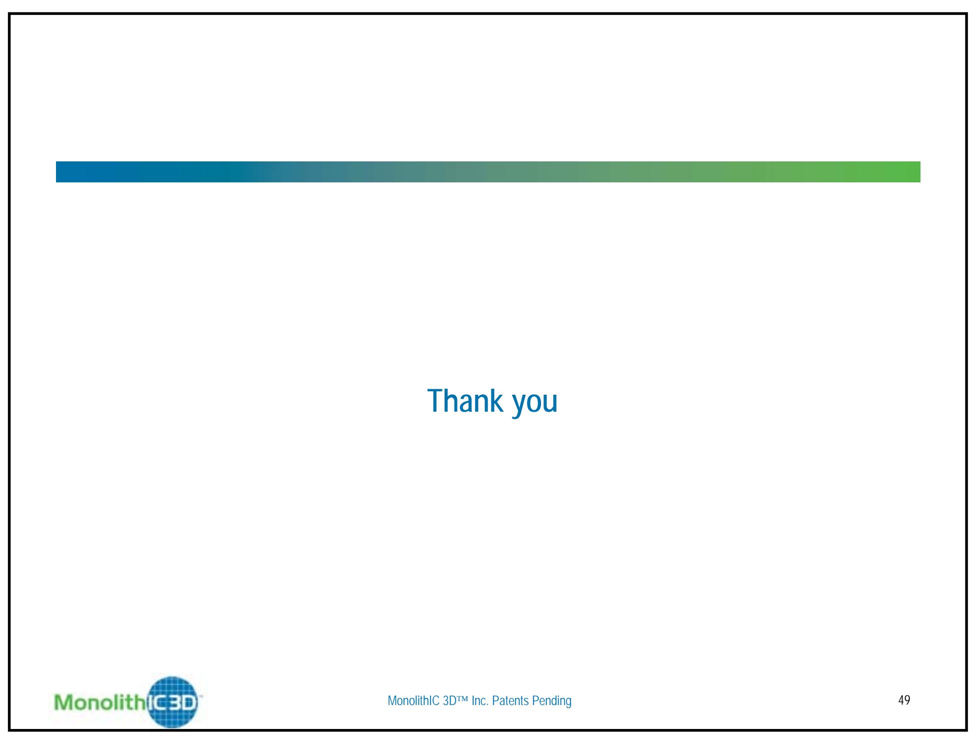
Thank you
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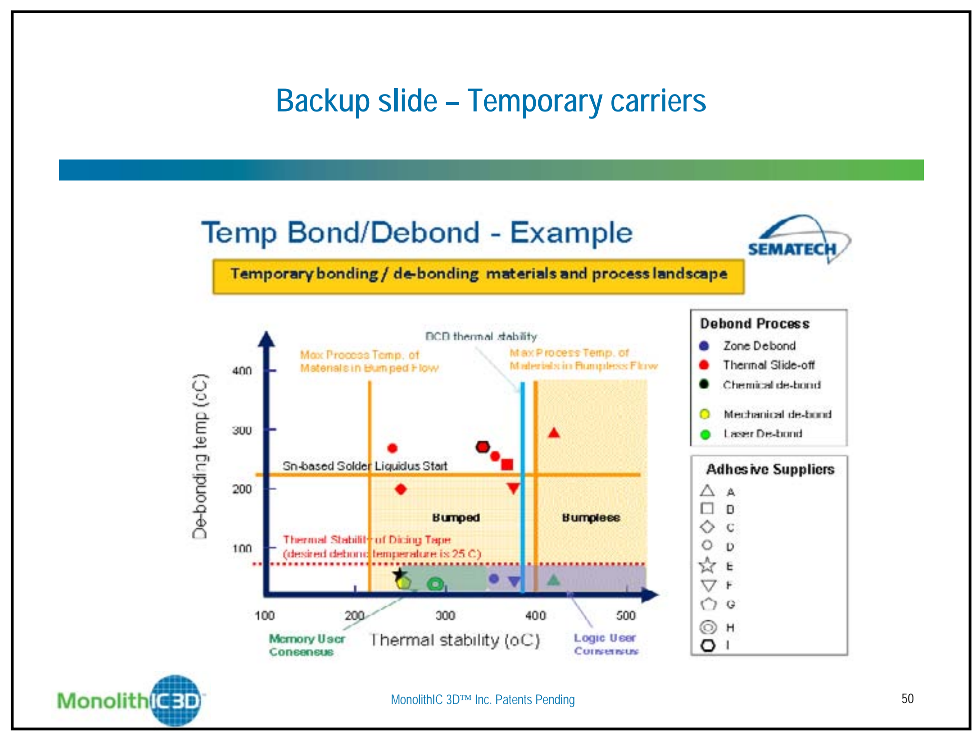
Backup slide – Temporary carriers
Temp Bond/Debond - Example
SEMATECH
Temporary bonding / de-bonding materials and process landscape
Debond Process
Zone Debond
Thermal Slide-off
Chemical de-bond
Mechanical de-bond
Laser De-bond
Adhesive Suppliers
A
D
C
D
E
F
G
H
I
De-bonding temp (oC)
400
300
200
100
Max Process Temp. of Materials in Bumped Flow
Max Process Temp. of Materials in Bumpless Flow
Sn-based Solder Liquidus Start
Bumped
Bumpless
Thermal Stability of Dicing Tape (desired debond temperature is 25 C)
100
200
300
400
500
Thermal stability (oC)
Memory User Consensus
Logic User Consensus
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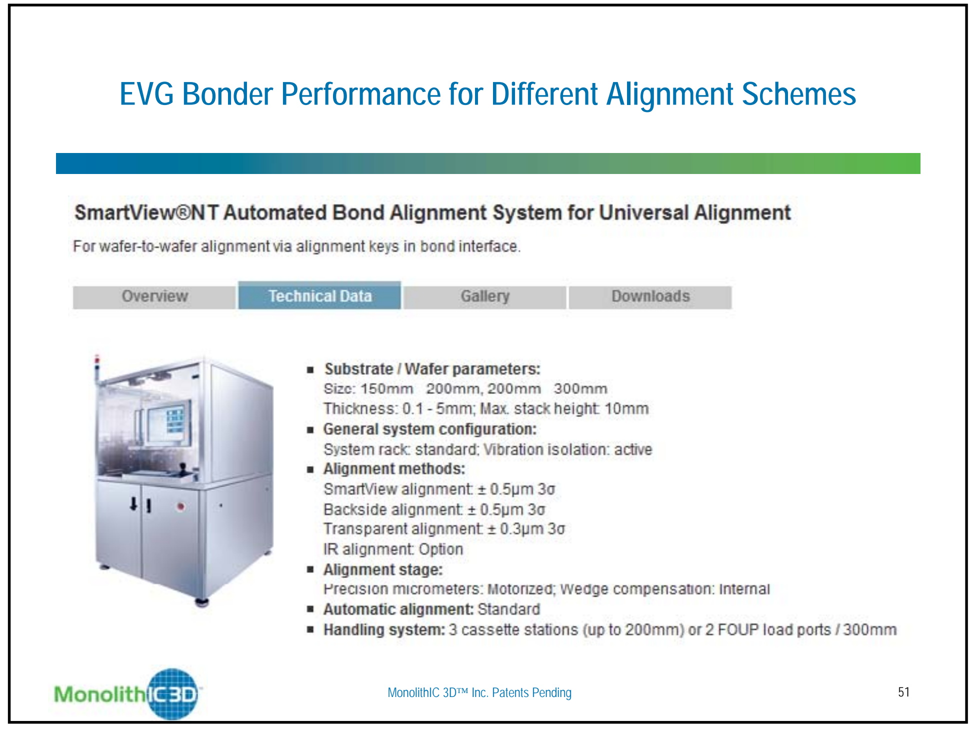
EVG Bonder Performance for Different Alignment Schemes
SmartView®NT Automated Bond Alignment System for Universal Alignment
For wafer-to-wafer alignment via alignment keys in bond interface.
Overview
Technical Data
Gallery
Downloads
Substrate / Wafer parameters:
Size: 150mm 200mm, 200mm 300mm
Thickness: 0.1 - 5mm; Max. stack height: 10mm
General system configuration:
System rack: standard; Vibration isolation: active
Alignment methods:
SmartView alignment: ± 0.5µm 3σ
Backside alignment: ± 0.5µm 3σ
Transparent alignment: ± 0.3µm 3σ
IR alignment: Option
Alignment stage:
Precision micrometers: Motorized; Wedge compensation: Internal
Automatic alignment: Standard
Handling system: 3 cassette stations (up to 200mm) or 2 FOUP load ports / 300mm
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