



Combining Accurate Measurement with Thermal Simulation

Thermal Characterization of Electronic Components

John Wilson
Application Engineering Manager
Mechanical Analysis Division

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Agenda

- Combining Accurate Measurement with Thermal Simulation
 - Validated Thermal Model
 - JESD15-4:Delphi Compact Thermal Model (CTM)
 - Enhanced 2 Resistor Compact Thermal Model (CTM)
 - Difficulties in Junction-To-Case measurement
 - JESD 51-1 Electrical test method: Z_{th} , Structure Functions
 - JESD51-14 Transient Dual Interface Method Overview
 - Use Cases:Leveraging JESD51-14 for System Thermal Design
 - Summary

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Detailed Model Validation and Delphi CTM of IC Device Packages

- CFD (Computational Fluid Dynamics) models of packages are compared to measurements
- Validated CFD model used to generate DELPHI compact models for system level thermal analysis
- Alternatively the validated 3D thermal model may be used directly in the analysis tool

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Linking Test to System Thermal Design Compact Thermal Model

- Compact Thermal Models allow:
 - System designers to predict device operating temperatures
 - Vendors to provide only thermal characteristics

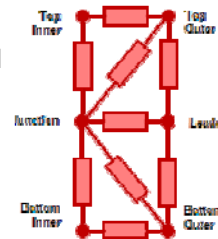
Compact thermal models (CTM) are essential when developing a valuable predictive System Thermal Model

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Characteristics of Method

- Validated Detailed Thermal
 - No standard requirements for validation (R_{ja} , R_{jma} , etc..)
 - Material properties (k , ρ , C_p) not easily obtained
 - Detailed model computationally expensive to include in system level (CFD) analysis
- Delphi model
 - Obtained only from computational analysis
 - Boundary Condition Independent predictive model
 - Useful for Steady State analysis only
 - Requires fairly sophisticated mathematical optimization to determine thermal resistances
 - Computationally efficient in system level (CFD) analysis
 - JESD15-4: Guidelines for model generation



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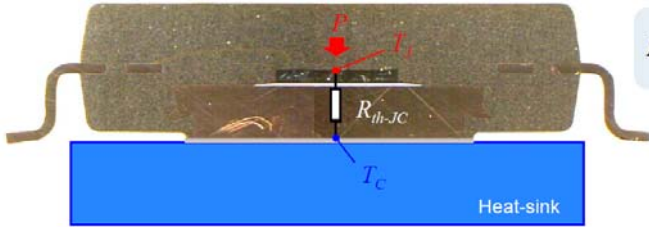
RTH-JC: SIMPLE IN CONCEPT, YET...

Some material courtesy of Dirk Schweitzer & Heinz Pape, Infineon

Rth-JC JEDEC JESD51-1 Definition

- Thermal Resistance, Junction-to-Case:


“The thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when the same surface is properly heat sunk so as to minimize temperature variation across that surface.” (JESD51-1)



$$R_{th-JC} = \frac{T_J - T_C}{P}$$

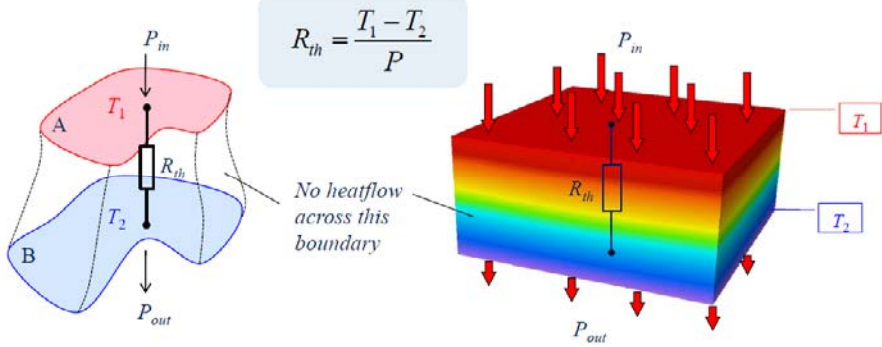
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Rth-JC The Concept of Thermal Resistance


- Conditions under which thermal resistance is well defined:
 - Heatflow between two isothermal surfaces A (T1) and B (T2).
 - The whole power that enters the volume V through surface A leaves the volume through surface B: (i.e. Pin = Pout = P)



$$R_{th} = \frac{T_1 - T_2}{P}$$

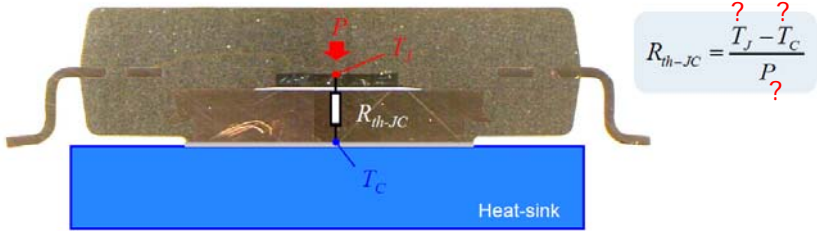
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Rth-JC Problems with the Definition

- Neither junction nor case temperature are truly uniform
 - What is T_J ? What is T_C ? Maximum, average, or ... temperature?
- Not all of the power dissipation P generated in the junction leaves the package through the case... So:
- Rth-JC is neither well-defined nor unambiguous!

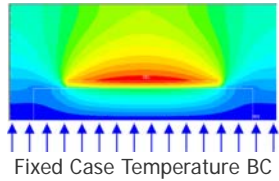


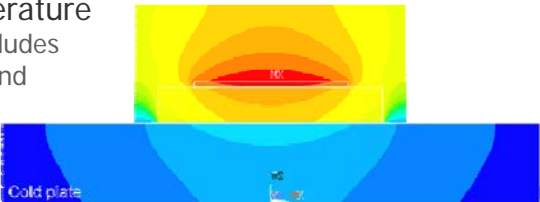
$R_{th-JC} = \frac{T_J - T_C}{P}$

Heat-sink

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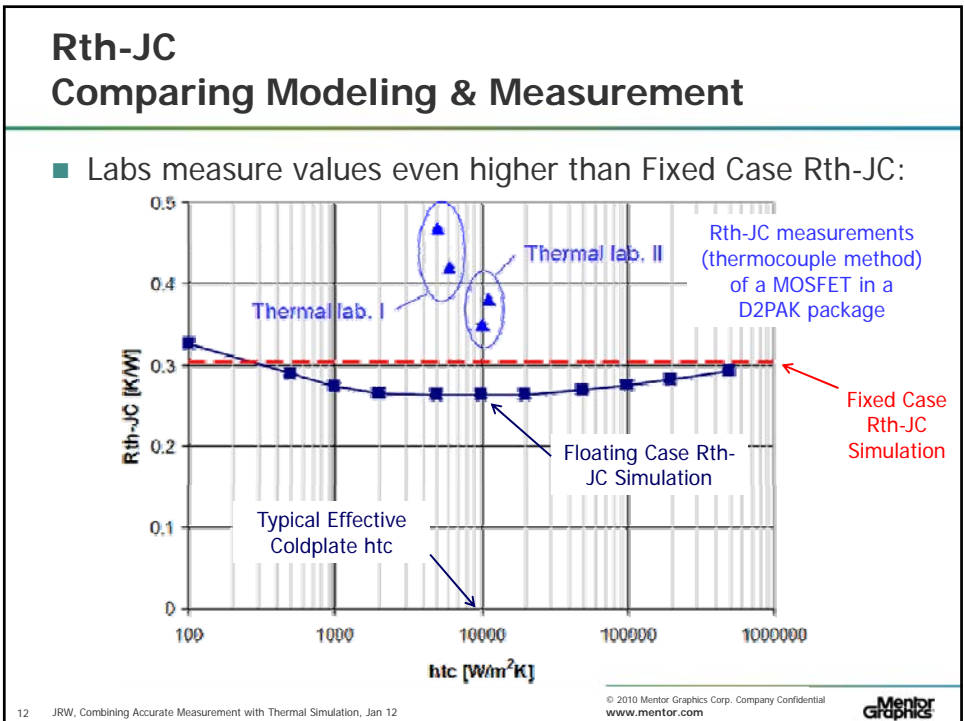
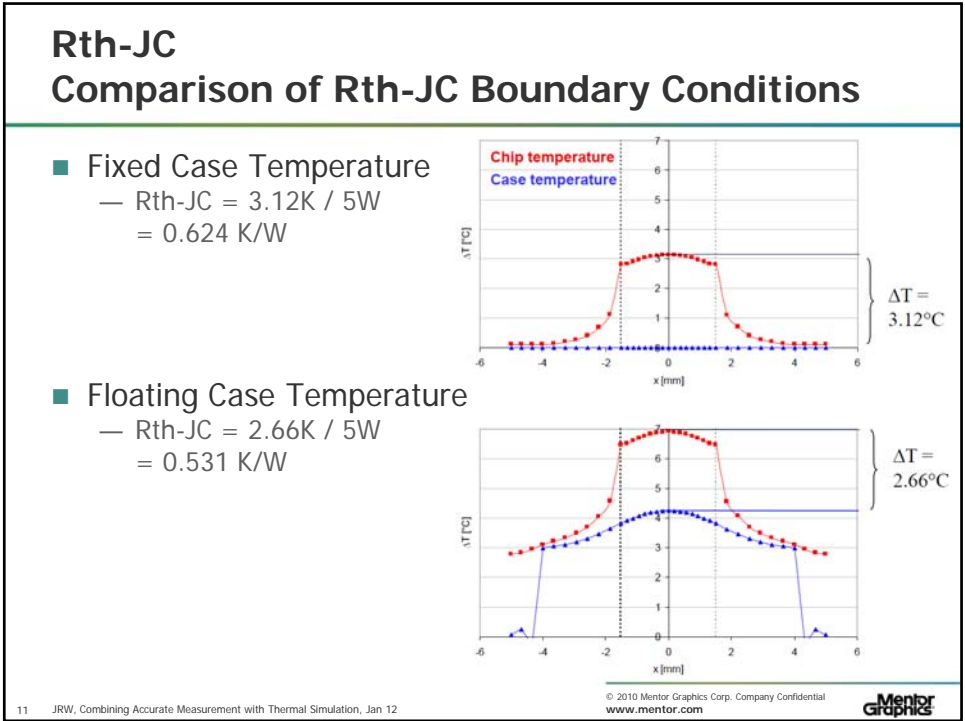
Rth-JC Two Ways to Compute Rth-JC

- Fixed Case Temperature
 - The bottom case temperature is kept constant
 - Ideal heatsink case
 - Closest to definition as T_2 is isothermal

Fixed Case Temperature BC
- "Floating" Case Temperature
 - The thermal model includes thermal grease layer and cold-plate.
 - A temperature profile is allowed to develop in the heatsink
 - Non-ideal (physical) heatsink; realizable in practice.

Cold plate

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Rth-JC Thermocouple Issues

- The reason has been thoroughly investigated by Infineon.
 - There is a temperature gradient down the thermocouple bead
 - The TC drill hole also affects the temperature in the coldplate

$T_C = 304.6 \text{ K (31.6}^\circ\text{C)}$
 $T_{TC\text{-}ip} = 303.9 \text{ K (30.9}^\circ\text{C)}$
 $T_{TC\text{-}bot} = 301.6 \text{ K (28.6}^\circ\text{C)}$

grease

Chromel Alumel
 $T_{TC\text{-}bot}$
 ΔV_1 ΔV_2
 Chromel wire Alumel wire
 T_{Ref}
 $V_{out} = \Delta V_2 - \Delta V_1$



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Rth-JC Conclusions

- Rth-JC appears conceptually simple, but
- It's definition is somewhat ambiguous, and
- It's very tricky to measure:
 - Thermocouple measurement tends to overestimate Rth-JC
 - Thermal simulations predict a possible measurement error of 50% and more!
 - This might explain why the TC-measurement often returns Rth-JC values which are (much) higher than those obtained by simulation

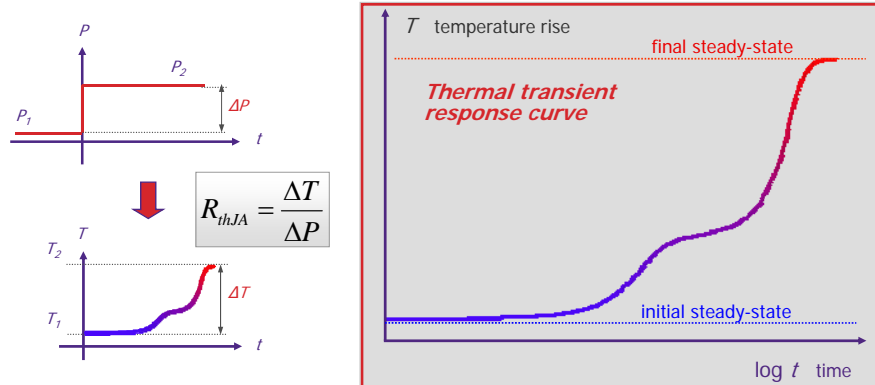
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Transient Test Methods Implementing The Electrical Test Method	
<ul style="list-style-type: none">■ The JESD51-1 standard lists two modes of measurement:■ Dynamic mode - pulsed heating■ Static mode - continuous heating■ Both methods rely on using a Temperature Sensitive Parameter (TSP) to relate voltage to temperature, e.g.:<ul style="list-style-type: none">— Voltage drop across a forward-biased diode.	<p>EIA/JEDEC STANDARD</p> <hr/> <p>Integrated Circuits Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)</p> <hr/> <p>EIA/JESD51-1</p> <hr/> <p>DECEMBER 1995</p> <hr/> <p>ELECTRONIC INDUSTRIES ASSOCIATION ENGINEERING DEPARTMENT</p> 
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Transient Test Methods JEDEC "Static" Test Method

- Switch power on (or off) in **initial steady state** and wait
- While waiting for **final steady state**, measure (record) the real transient *continuously*, as it takes place.



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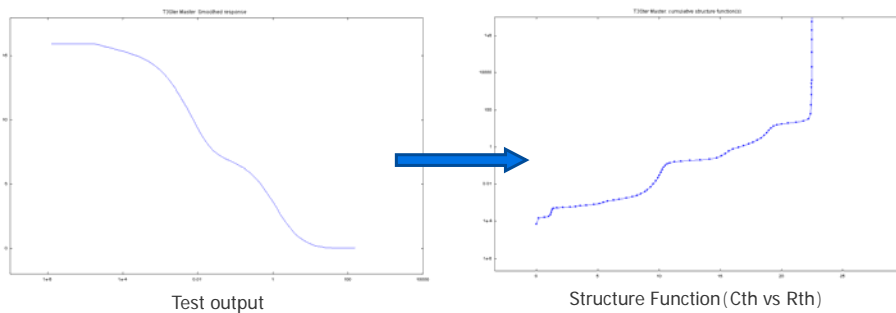
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Analyzing the Structure

- Test output can be mathematically processed to determine the "Structure Function"
 - Identify the thermal resistances and capacitances along the heat transfer path



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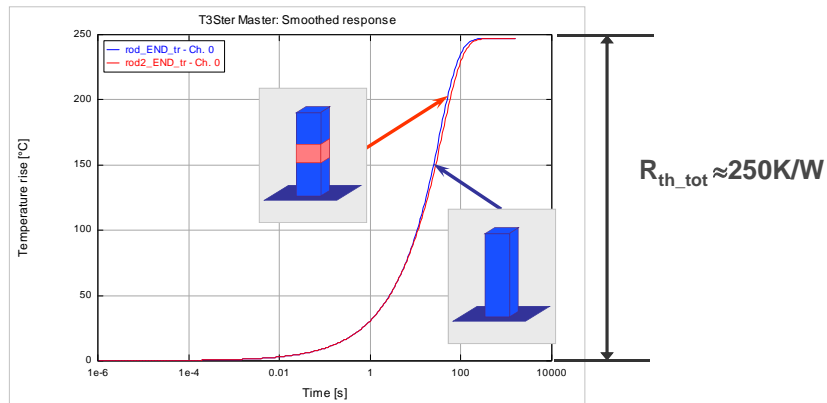
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Structure Function: Why is it important?

- Consider a Cu rod of 1x1mm² cross-sectional area
 - Rod 1: 100mm (λ, C_v)
 - Rod 2: 40mm (λ, C_v), 20mm ($\lambda, 2xC_v$), 40mm (λ, C_v)



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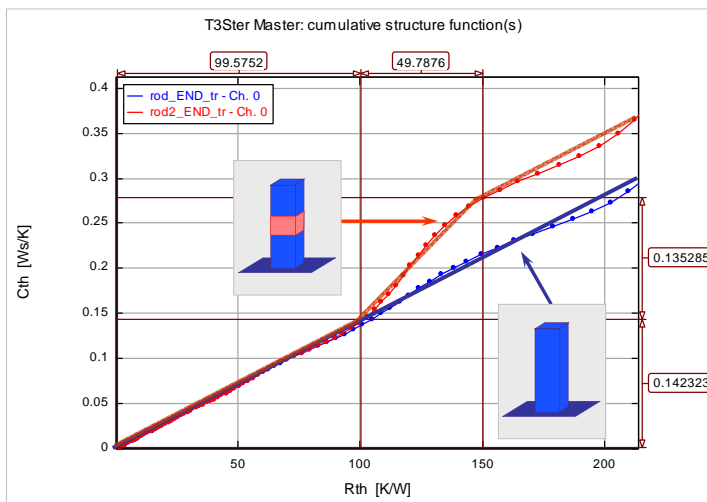
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Structure Function: Why is it important?

- The difference in the structures is well seen



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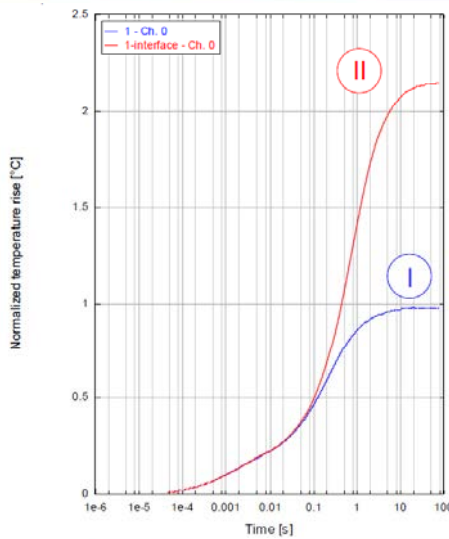
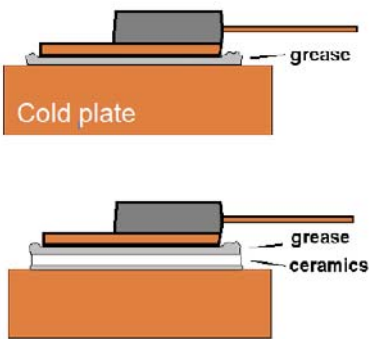


MEASURING RTH-JC TRANSIENT DUAL THERMAL INTERFACE METHOD (JESD51-14)

Some material courtesy of Dirk Schweitzer & Heinz Pape, Infineon

Transient Dual Interface (TDI) Method Background: Original Approach by MicReD


- Original approach pioneered by MicReD:
 - P. Szabo et. al., Proc. 10th THERMINIC, 2004



Time [s]	Normalized temperature rise [°C] (Ch. 0)	Normalized temperature rise [°C] (1-interface - Ch. 0)
1e-6	0.00	0.00
1e-5	0.00	0.00
1e-4	0.00	0.00
0.001	0.05	0.05
0.01	0.30	0.30
0.1	0.90	0.90
1	1.00	1.50
10	1.00	2.00
100	1.00	2.10

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Transient Dual Interface (TDI) Method Background: Original Approach by MicReD

- Proposed approach used comparison of 'structure functions' to determine Rth-JC

Cold plate

grease

ceramics

Differential Structure Function

K [W2s/K2]

Rth [K/W]

Rth-JC ≈ 0.35K/W

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Transient Dual Interface (TDI) Method Background: Original Approach by MicReD

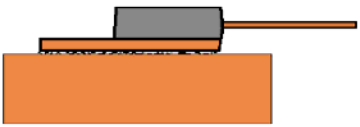
- Peaks and valleys of differential structure function correspond to different layers of the heatflow path.
 - Interface surfaces represented by inflexion points.
 - Rth-JC can be identified as the first inflexion point following the separation of the structure functions
- Structure functions should in principle be identical as long as the heat flow paths are equal...
- BUT: Identical path in **both** measurements includes first grease layer
 - structure functions might separate "too late" as it will be after the glue layer.

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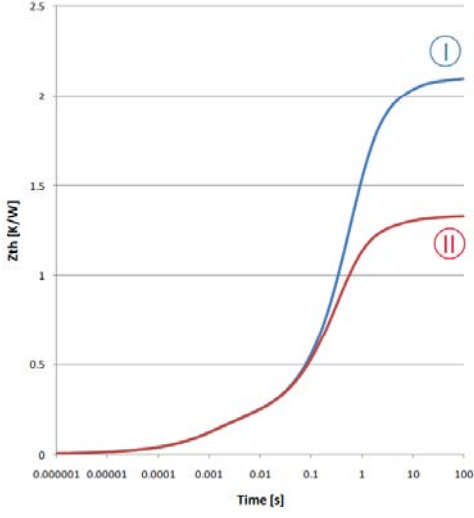
Transient Dual Interface (TDI) Method Background: Infineon Proposal

- Perform two Zth-measurements on the same device:
 - Without thermal grease:



- With thermal grease:





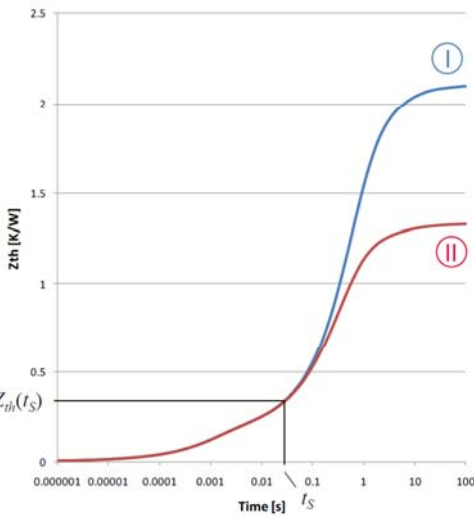
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Transient Dual Interface (TDI) Method Background: Infineon Proposal

- Infineon proposed an alternative evaluation method based on the separation point of the Zth-curves instead of the structure functions
- Found strong correlation between Zth-value $Z_{th}(t_S)$ and R_{th-JC}^* :


$$R_{th-JC} \approx Z_{th}(t_S)$$



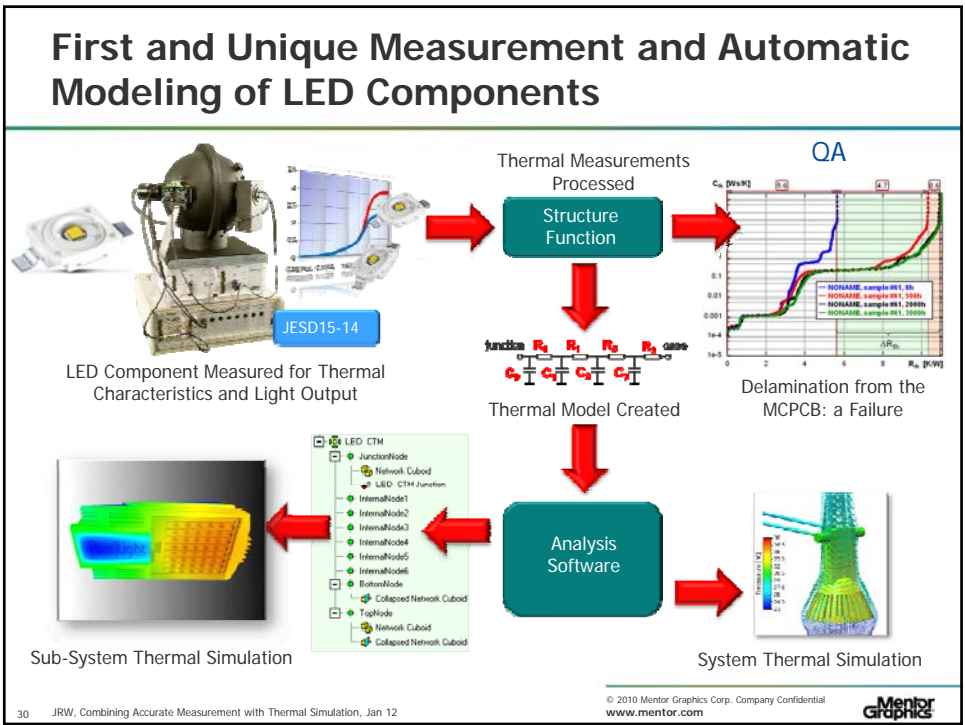
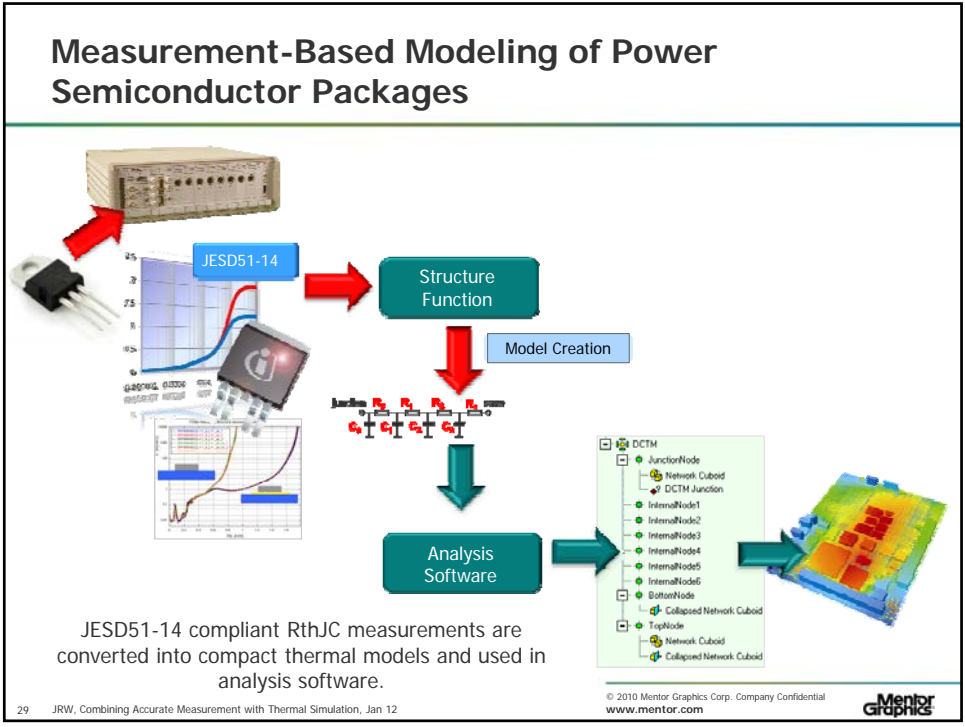
* Not valid for devices with an internal heat flow barrier such as a low conductivity glue, where the structure function approach works better.

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<h2>Transient Dual Interface (TDI) Method Summary</h2>	
<ul style="list-style-type: none">■ JESD51-14 has a number of advantages over the original MIL-Std 883 1983, which suffered from:<ul style="list-style-type: none">— Low reproducibility:— Thermocouple bead not sufficiently insulated from cold plate— High clamping pressure causes delaminations within the package— Influence of thermocouple drill hole■ But:<ul style="list-style-type: none">— Result interpretation is not so straightforward without dedicated software.	<p>JEDEC STANDARD</p> <hr/> <p>Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path</p> <hr/> <p>JESD51-14</p> <p>NOVEMBER 2010</p> <hr/> <p>JEDEC SOLID STATE TECHNOLOGY ASSOCIATION</p> <p>JEDEC</p> <hr/> <p><small>© 2010 Mentor Graphics Corp. Company Confidential www.mentor.com</small></p> 
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Summary

- Validated Detailed Model
 - Difficult to obtain the necessary material thermal properties
 - Time required to obtain properties makes it prohibitive to use in design
 - Computationally prohibitive to use in system level CFD analysis
- Delphi
 - Only applicable to steady state analysis (resistances)
 - Not able to predict performance for different power profiles or failure conditions
 - Computationally efficient
- Dynamic Modified 2R Compact Thermal Model
 - Validated compact model based on JESD51-14, without developing validated detailed analysis model
 - Captures transient behaviour of device
 - Computationally efficient

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