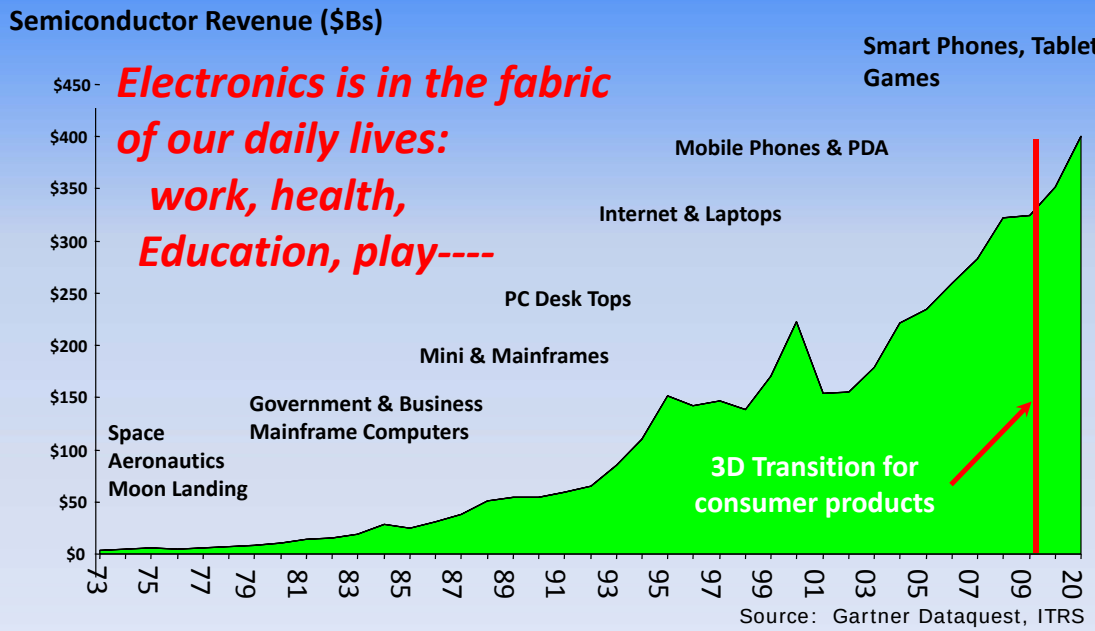
Changes in Packaging Materials and Architectures for 2012

ITRS and INEMI Roadmaps

CPMT Meeting May 9, 2012

Biltmore Hotel, Santa Clara, Ca.

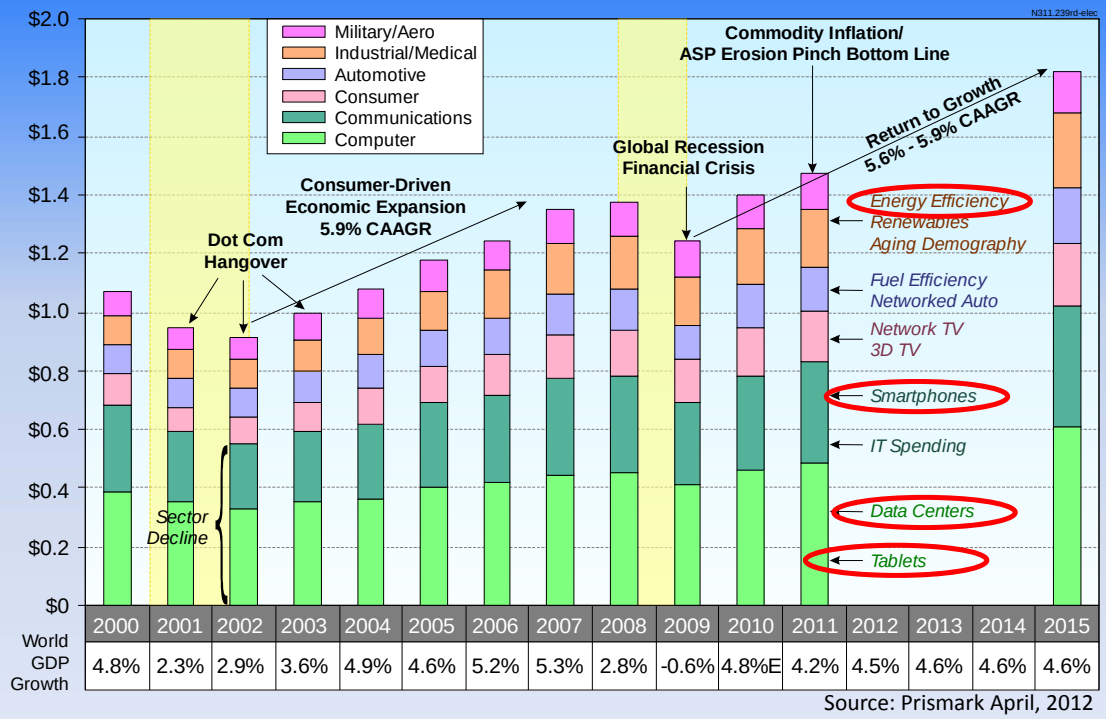
IC Industry revenue Approaching $ 300 Billion Electronics Systems (Hardware) Revenue >$1.4 Trillion



CPMT Meeting May 9, 2012

Biltmore Hotel, Santa Clara, Ca.

History and Forecast for the Electronics Industry



Source: Prismark April, 2012

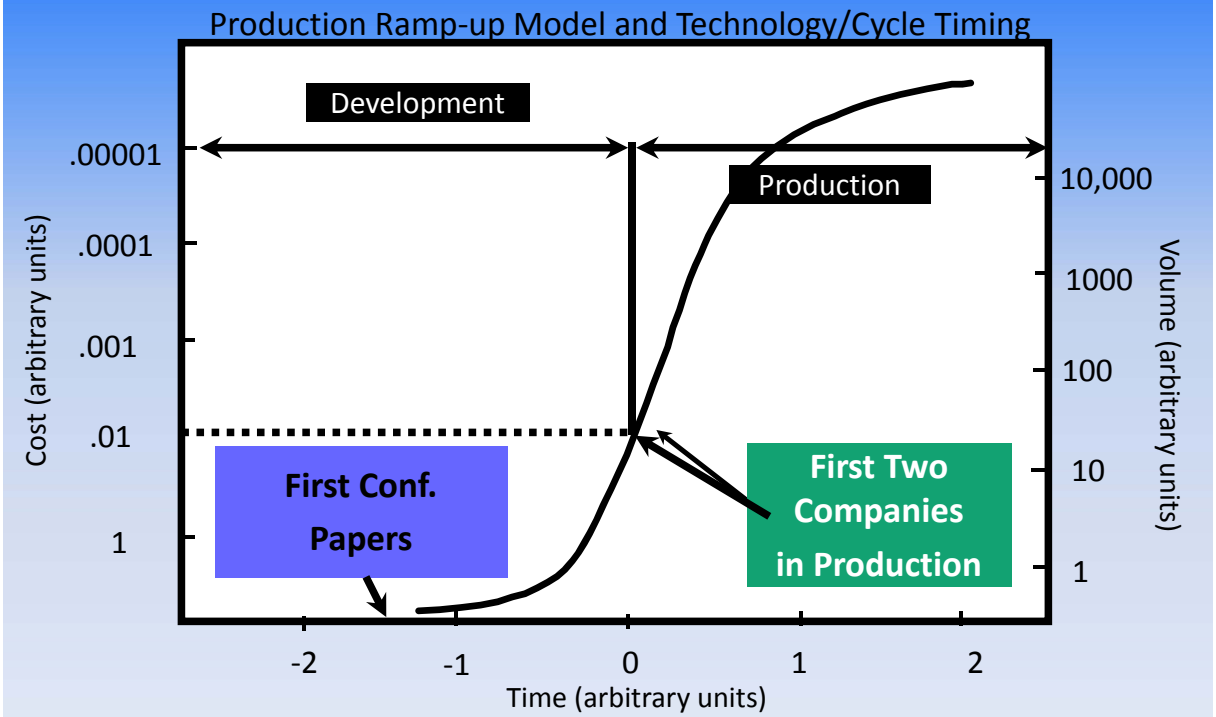
The 45 year history of knowing what comes next is over

Progress has been paced by Moore's Law and driven by:

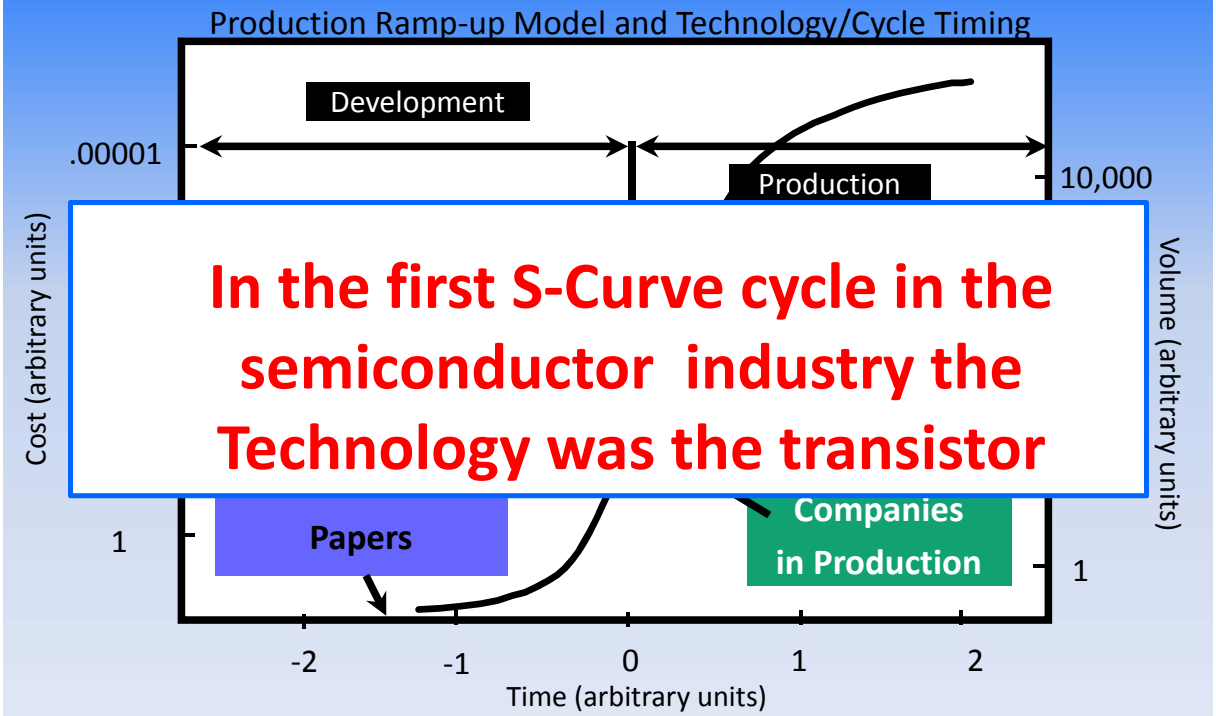
- Focus was on design and fab
  - Shrinking geometries
  - Expanding wafer size
  - Higher density designs

For digital circuits there are now limitations that can't be met by these activities alone.

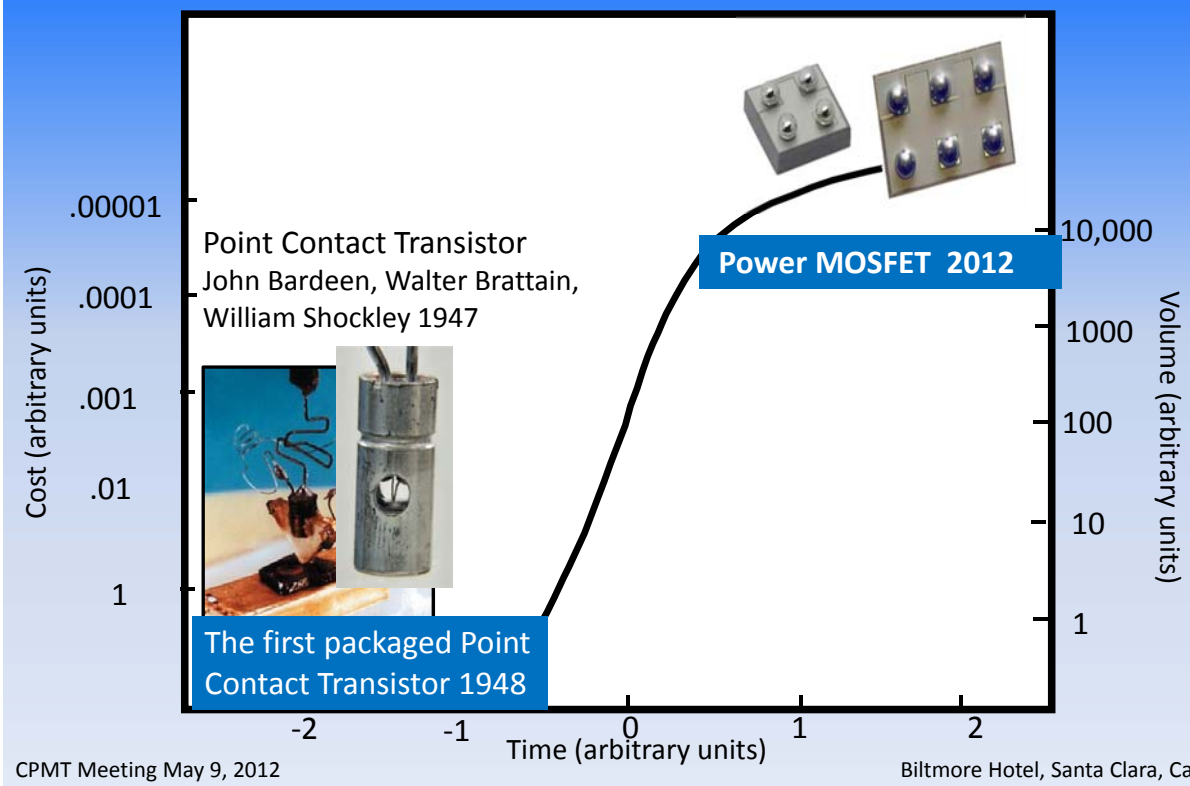
Semiconductor Electronics has been Characterized by an S-Curve



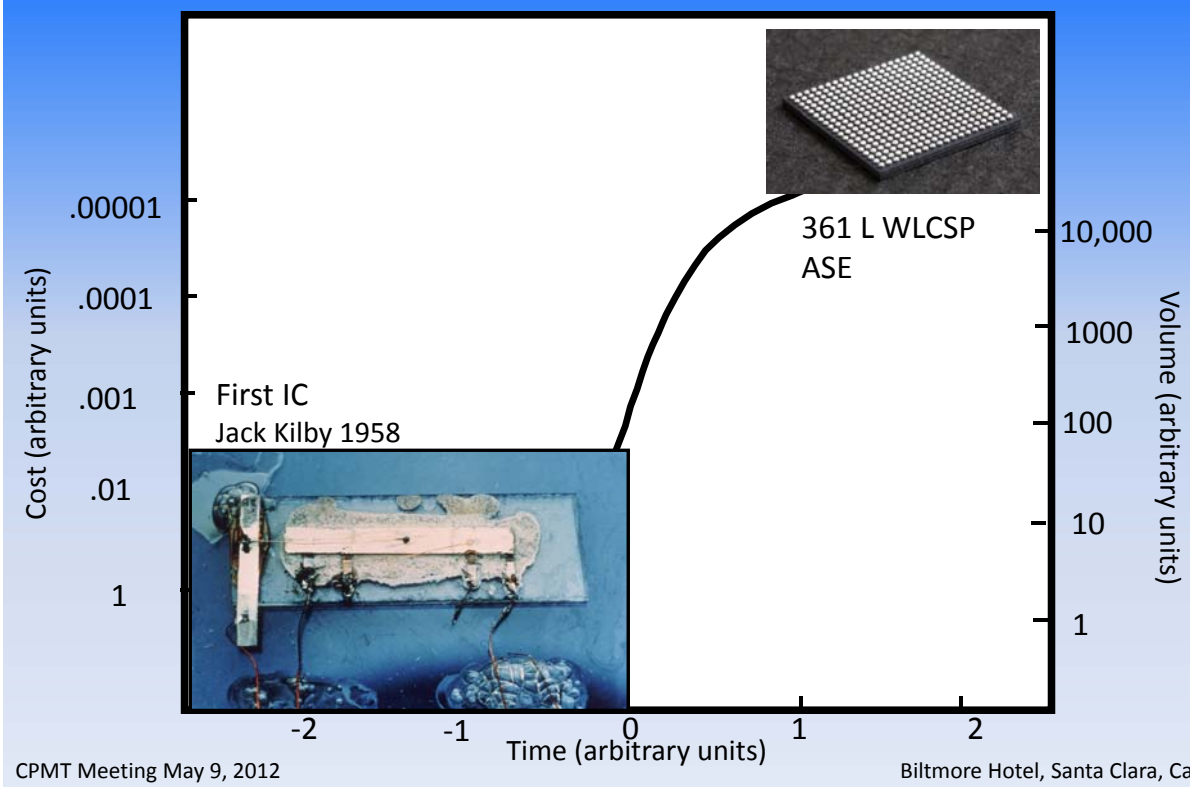
Semiconductor Electronics has been Characterized by an S-Curve



The Transistor S-Curve

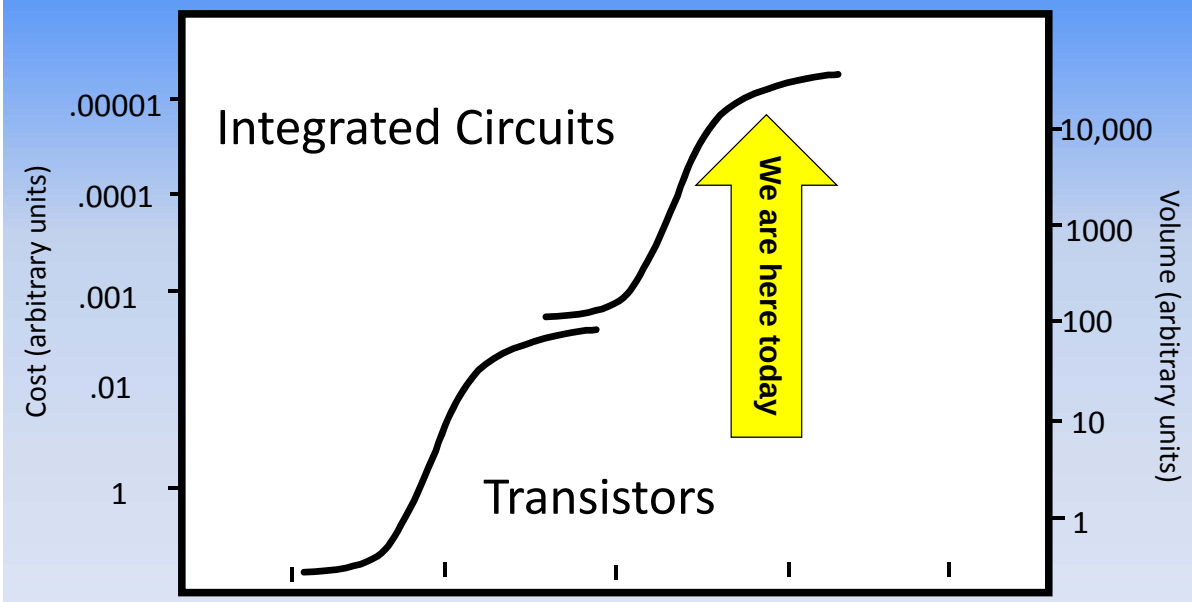


The Integrated Circuit S-Curve



Innovation maintained Progress with the second S-Curve Cycle

Production Ramp-up Model and Technology/Cycle Timing



What has Changed?

- ✓ 3D-integration is finally here
- ✓ Power efficiency is critical for all applications
  - Photovoltaics
  - LEDs
  - Consumer portable devices
  - Data centers
  - Data communication
- ✓ Physical density of Bandwidth is limiting
- ✓ Latency on the net or in the cloud
- ✓ Transistors wear out
- ✓ New transistor/IC architectures are here; more coming

What has Changed?

- ✓ 3D-integration is finally here
- ✓ Power efficiency is critical for all applications
  - – Photovoltaics
  - – LEDs
  - – Consumer portable devices
- ✓ **Packaging solutions to accommodate these changes will require new architectures, new materials and new processes**
- ✓ Latency on the net or in the cloud
- ✓ Transistors wear out
- ✓ New transistor/IC architectures are here; more coming

Focus of 2012 Packaging Roadmaps

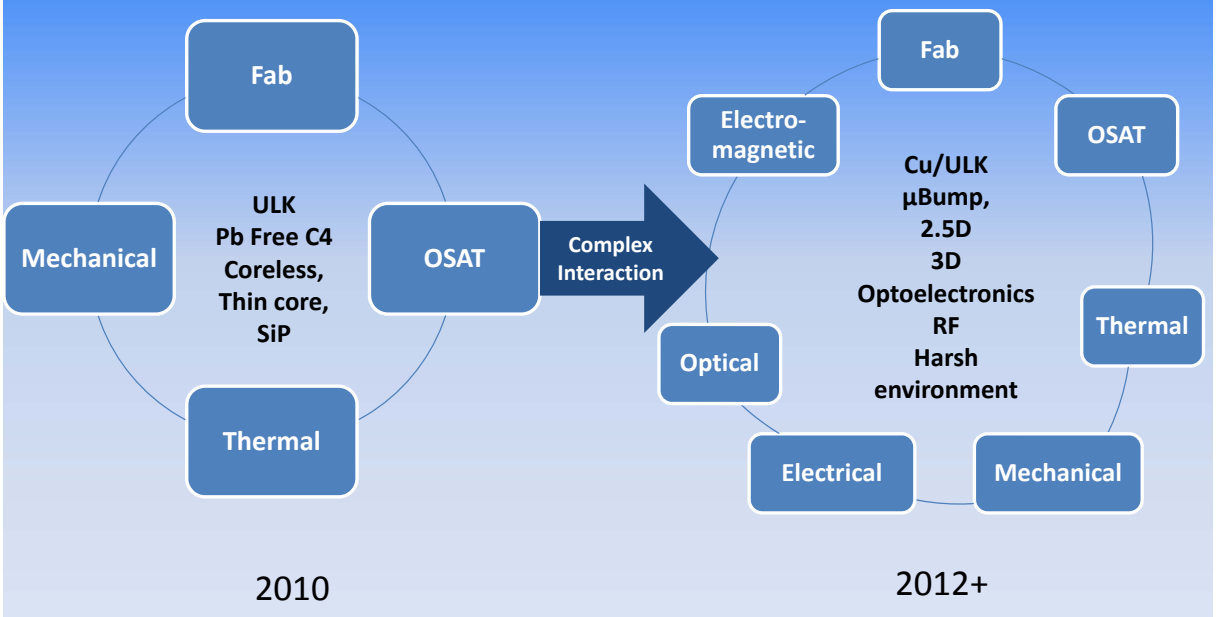
- ✓ Design
- ✓ Performance
  - – 2.5D interposers or Si package substrates
  - – 3D integration
- ✓ Functional diversification (More than Moore)
  - – System in Package (SiP)
- ✓ New materials
- ✓ Transistors will wear out

Design and Simulation Issues

Design and simulation of Chip, substrate, package, PCB interaction

- The consumer dominated market has short product life cycles
- The cost of building prototypes with subsequent revisions will be excessive as transistor count exceeds 100 billion for complex SiP packages
- Prototype designs must be built and tested in the computer to meet time-to-market and cost demands of the today's consumer dominated market

Future Interaction Challenges



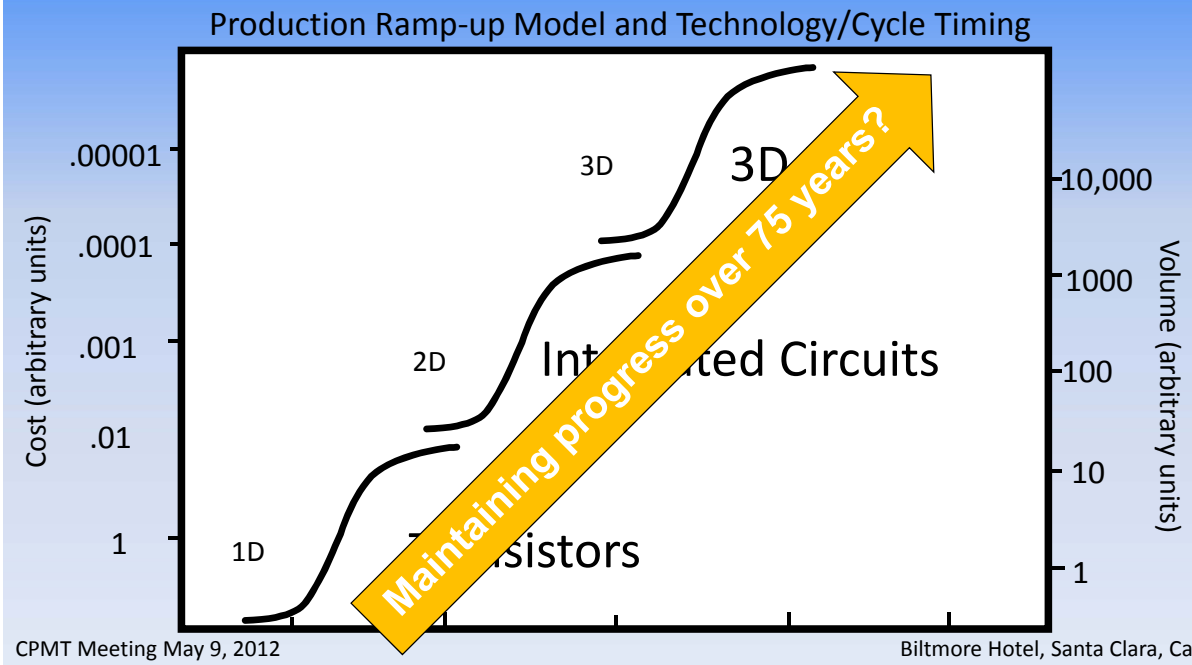
Performance Issues

Packaging limitation for logic/data devices:

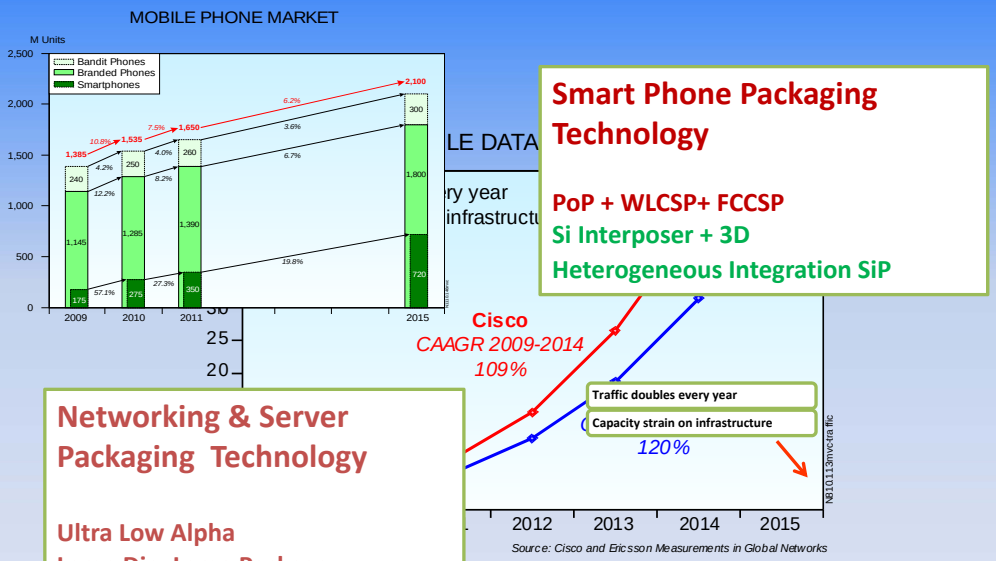
- ✓ Physical density of Bandwidth
- ✓ Latency
- ✓ Power
  - – Power delivery
  - – Power integrity
  - – Power efficiency

3D Integration is a Key to progress for each of these Performance Parameters

Can the 3D IC maintain Progress through a third S-Curve Cycle?



Changing Landscape



Smart Phone Packaging Technology

PoP + WLCSP+ FCCSP
Si Interposer + 3D
Heterogeneous Integration SiP

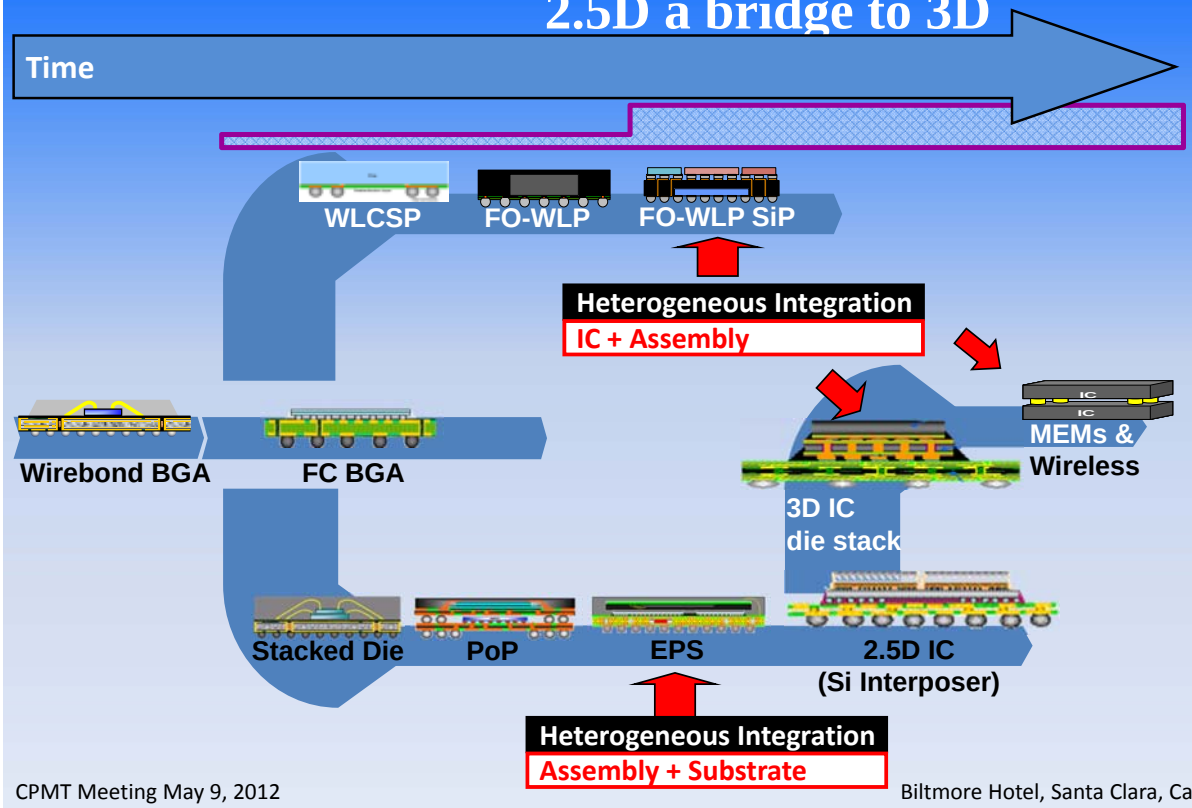
Networking & Server Packaging Technology

Ultra Low Alpha
Large Die, Large Package
Heterogeneous Integration SiP
Silicon Interposer + 3D

Where we are

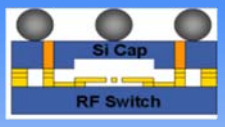
Where we are going

Evolution of Heterogeneous Integration:
2.5D a bridge to 3D

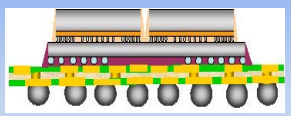


2.5D and 3DIC Productization

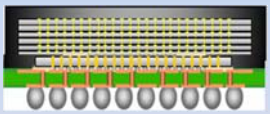
- 3D MEMs & Sensor



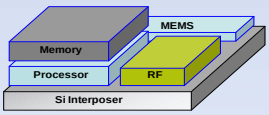
- 2.5D Silicon Interposer



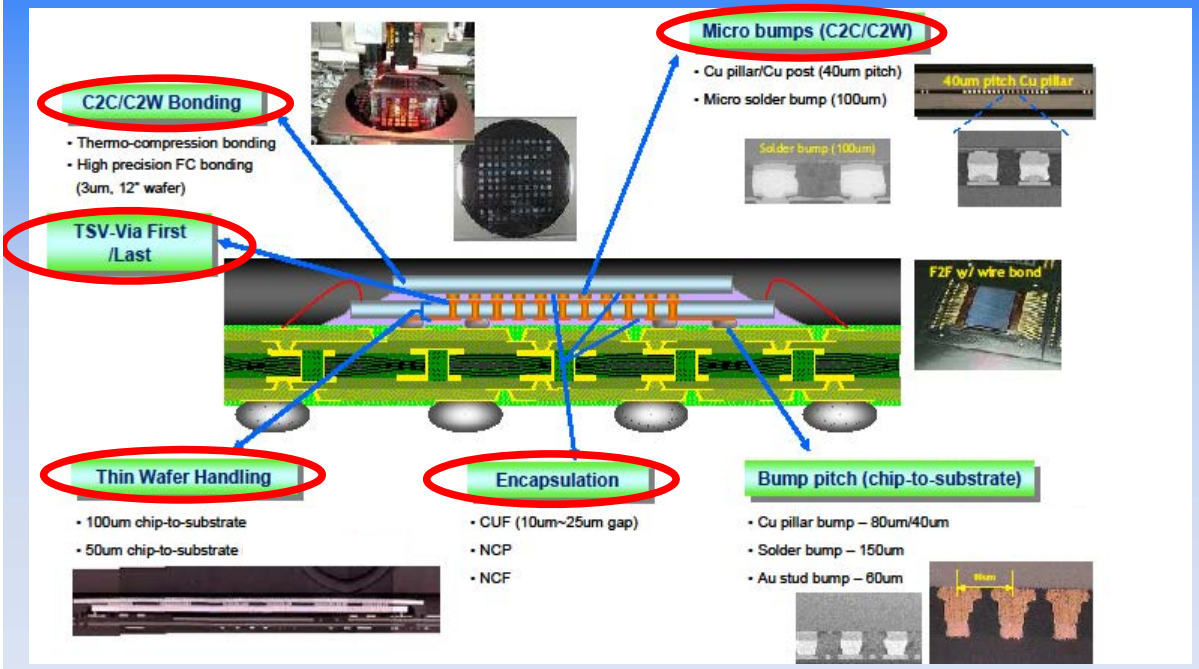
- 3D Die Stacking



- Heterogeneous SiP Integration



3D IC Packaging Requirements



Photonics is the Solution to physical density of Bandwidth for SiP

In-to and Out-of Package	Basic data taken from ITRS 2011 Roadmap					
Intended to cover Optical IO for SiP (System in a Package) for distance on-card and longer						
Year	*2012*	*2014*	*2016*	*2018*	*2020*	*2022*
Basics for both Optical and Electrical IO						
Max Package I/O Data Rate, Gb/s	2,500	4,998	9,994	19,982	39,952	79,879
Max IO Power dissipation, watts	40	40	40	40	40	40
Max power to drive off-chip/on-chip, watts	10	10	10	10	10	10
Max IO Data rate/lane; Electronic or Optical, Gb/s	10	25	25	25	40	40
# IO lanes req'd per package	250	200	400	799	999	1997
Multiplexing level for # of IO <500	1	1	1	2	2	4
Optical Specific Parameters						
# Optical waveguides when <500 optical IO.	250	200	400	400	499	499
Electrical Specific Parameters						
# lanes req'd at Max IO data rate	250	200	400	799	999	1,997

Photonics is the Solution to physical density of Bandwidth for SiP

In-to and Out-of Package	Basic data taken from ITRS 2011 Roadmap					
Intended to cover Optical IO for SiP (System in a Package) for distance on-card and longer						
Year	*2012*	*2014*	*2016*	*2018*	*2020*	*2022*
Basics for both Optical and Electrical IO						
Max Package I/O Data Rate, Gb/s	2,500	4,998	9,994	19,982	39,952	79,879
Max IO Power dissipation, watts	40	40	40	40	40	40
Max power to drive off-chip/on-chip, watts	10	10	10	10	10	10
Max IO Data rate/lane; Electronic or Optical, Gb/s	10	25	25	25	40	40

How do we resolve the size of the transistors (.02um) vs. the length of the photons (~1um)?

CPMT Meeting May 9, 2012 Biltmore Hotel, Santa Clara, Ca.

Photonics is the Solution to physical density of Bandwidth for SiP

Conclusions from the ITRS Table

- ✓ Area Required for differential electrical IO will drive IO to Optical about 2015.
- ✓ For Optical to compete, optical power must be 2 pJ/bit and decline 30%/yr

Questions remain for the Photonics Solution to physical density

Remaining Questions arising from the ITRS Table

- ✓ Is the 30 mm x 30 mm package assumed small enough ?
- ✓ Where does all of th IO power go now?
- ✓ What optical technology can achieve 2 pJ/bit ?
- ✓ Can electrical IO pitch be reduced below 1 mm BGA pitch ?
- ✓ Should Optical IO be off of the package edge rather than through bottom Ball grid array ?
- ✓ Can devices to drive 25 Gb/s and 40 Gb/s into 50 ohm differential line be built ?

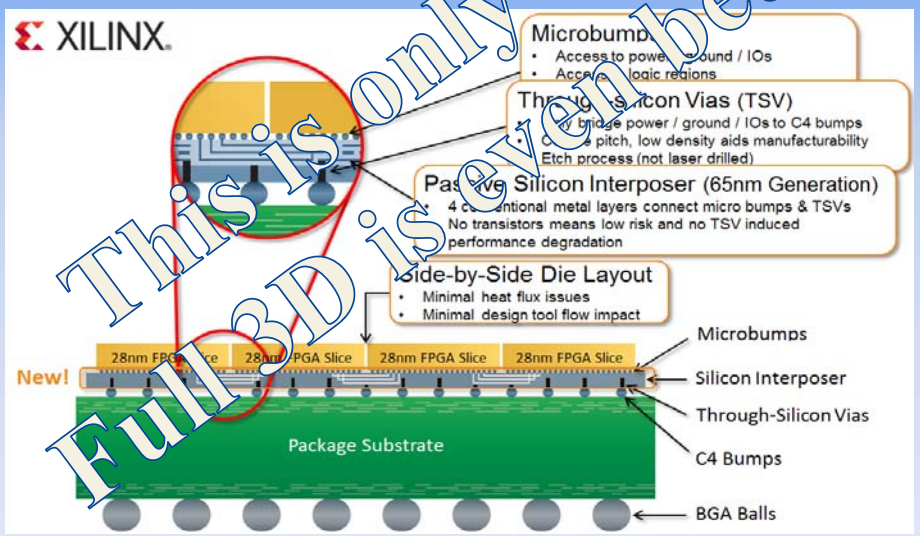
IO Structures Considered

	Basic Structure Either integral directly modulated source (A) or off chip source (B)	Electronic Substrate size mm x mm	Optical substrate size mm x mm	Chip size mm x mm	Data Density Gb/s/mm^2
1	MicroPOD Only Data Transfer	8	NA	NA	2.0
2	Conventional Processor PoP with discrete optical components	55	NA	23	3.0
3	PoP: Processor with integrated VCSEL & PIN electronics & Sub with discrete optical components	44	NA	23	12.5
4	PoP: Processor & Muxed Optical Substrate	30	30 x 30	15	?
5	Chip on Optical Substrate	NA	30 x 30	15	?
6	Chip on Optical Substrate on Electronic Substrate	25	15 x 15	15	?
7	Chip with Integrated Optical Components on Electronic Substrate	25	NA	15	?

Source: MIT CTR

Example: Xilinx Stacked Si FPGA

- ✓ Interposer substrate has more than 10,000 routing connections
- ✓ Compared with standard I/O connections it provides:
  - **> 100X die-to-die bandwidth per watt**
  - **one-fifth the latency**
  - **Uses no high-speed serial or parallel I/O resources.**



This is only 2.5D

Full 3D is even better

Consumer Market Demands now drive Power Requirements

- ✓ Power reduction initially driven by battery life and size/weight of portable electronics
  - Digital cameras, cell phones, walkman, etc.
- ✓ There has been remarkable growth in consumer driven demand for data as smart phones, digital television, 3D television and streaming video emerged
  - 3D holographic telepresence is not far behind

How can we reduce power?

Reduced Benefit from Shrinking CMOS

- ✓ Gate tunneling current increases
- ✓ Subthreshold channel leakage current increases
- ✓ Device parameter variability increases
- ✓ Source/drain resistance increases
- ✓ Copper interconnect resistivity increases

How can we reduce power?

Reduced Benefit from Shrinking CMOS

- ✓ Gate tunneling current increases
- ✓ Subthreshold channel leakage current increases
- ✓ Device parameter variability increases
- ✓ Source/drain resistance increases
- ✓ Copper interconnect resistivity increases

Power no longer scales with feature size, both static and dynamic power dissipation increase due to these barriers.

How can we reduce power?

- ✓ Reduce leakage currents **(new transistor designs)**
- ✓ Reduce on-chip Interconnect power by:
  - Improved conductor conductivity **(new material)**
  - Decrease capacitance **(new material)**
- ✓ Reduce interconnect length **(3D integration)**
- ✓ Reduce operating frequency **(increased parallelism)**
- ✓ Reduce operating voltage **(reduced Frequency)**
- ✓ Voltage regulator per core **(new IC designs)**
- ✓ Reduce *high speed* electrical signal length **(serdes with short path at the O to E converter)**

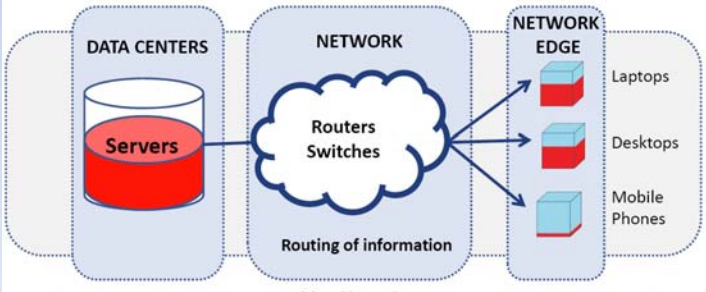
The Key to Power Optimization

Use power only where it is needed and when it is needed

In order to optimize we must identify each component of power use.

ITRS has a focus on the electrical components; INEMI has a focus on the box level network components. If the power use by each component is known, these organizations can focus their activity on identification of potential solutions to reduce power where it is needed most:

- **Memory**
- **Processors**
- **Serdes**
- **E to O to E conversion**
- **Fiber transmission losses**
- **Data Centers**
- **Other**



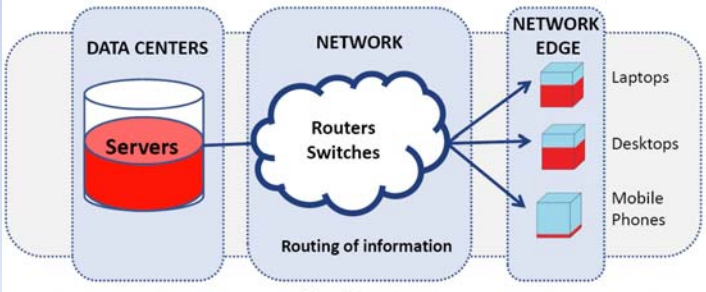
The Key to Power Optimization

Use power only where it is needed and when it is needed

ITRS and INEMI do not address Topology and Architecture of Networks but the component work enables new solutions in network architecture to reduce power.

solutions to reduce power where it is needed most:

- **Memory**
- **Processors**
- **Serdes**
- **E to O to E conversion**
- **Fiber transmission losses**
- **Data Centers**
- **Other**



CPMT Meeting May 9, 2012 Biltmore Hotel, Santa Clara, Ca.

Interconnect has become the limiting factor in power requirement

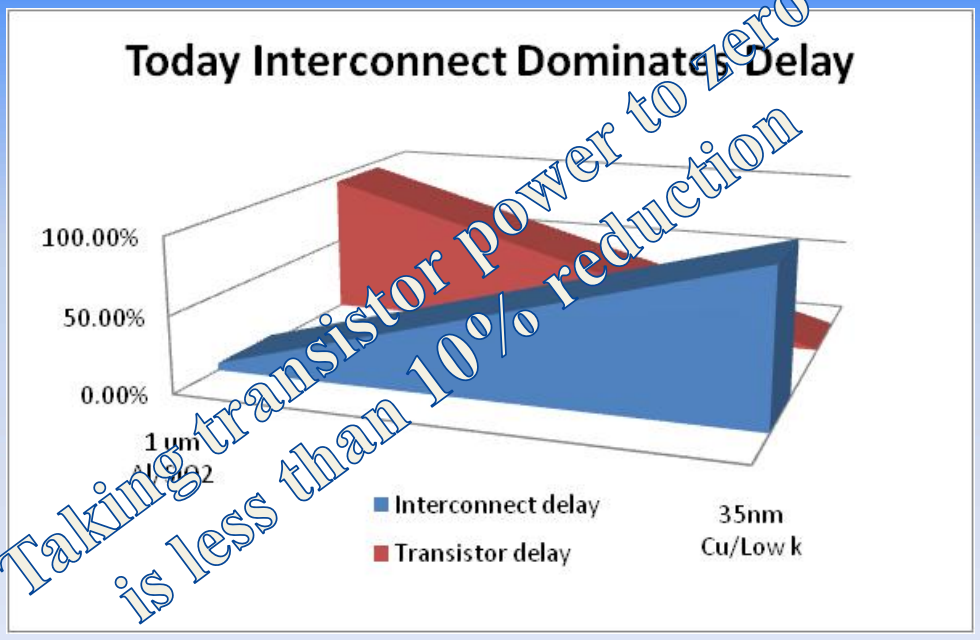
- Moore's law scaling has decreased transistor delay and power by three orders of magnitude while interconnect delay and power dissipation have been negatively impacted.

Change from Al/SiO_2 to Cu/Low k can solve the problem

For small dimensions metal resistivity increases rapidly due to sidewall and grain boundary scattering increasing RC delay

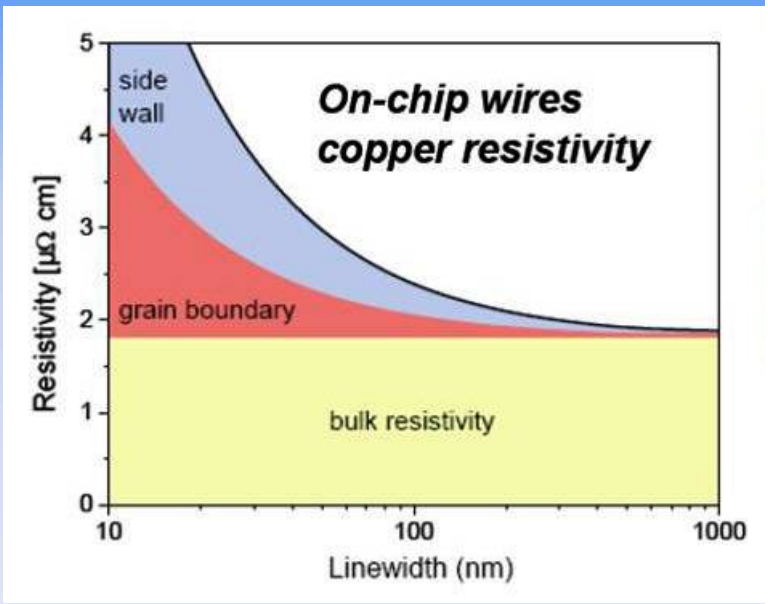
- For 1.0 um Al/SiO2 technology, transistor delay was 20 psec and RC delay for a 1 mm line was 1.0 psec
- For 32 nm Cu/low k technology, transistor delay will be 1.0 psec and RC delay for a 1 mm line is 250 psec

Interconnect will dominate delay and power dissipation



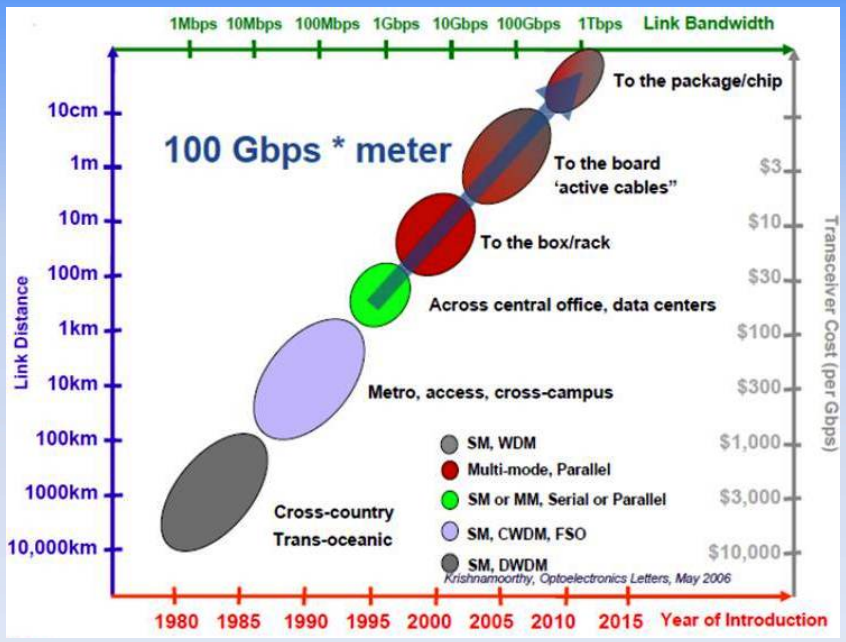
Copper Conductivity is reduced

- ✓ Grain boundary and side wall scattering increase resistivity as line width decreases



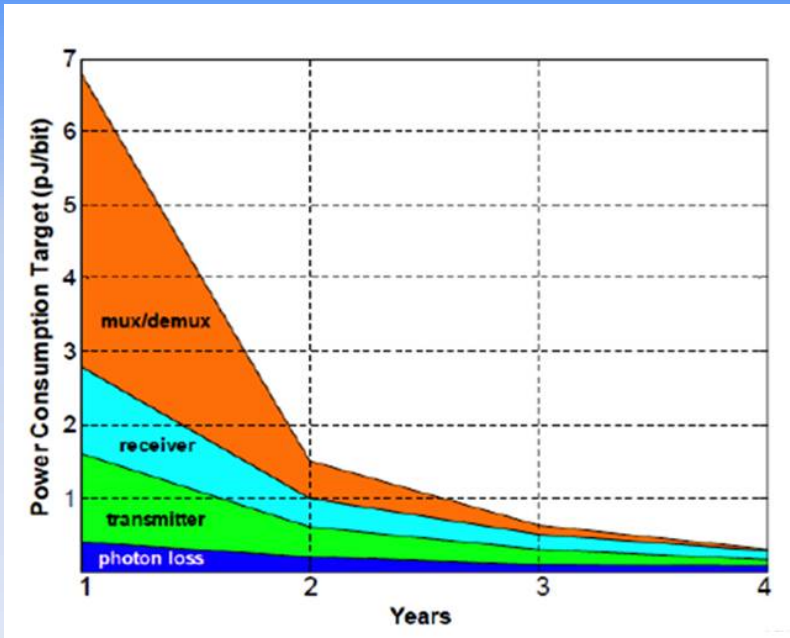
The "low handling" Fruit

- ✓ Move the photons as close to the transistors as possible



The "low handing" Fruit

- ✓ Reduce power in the serdes circuits



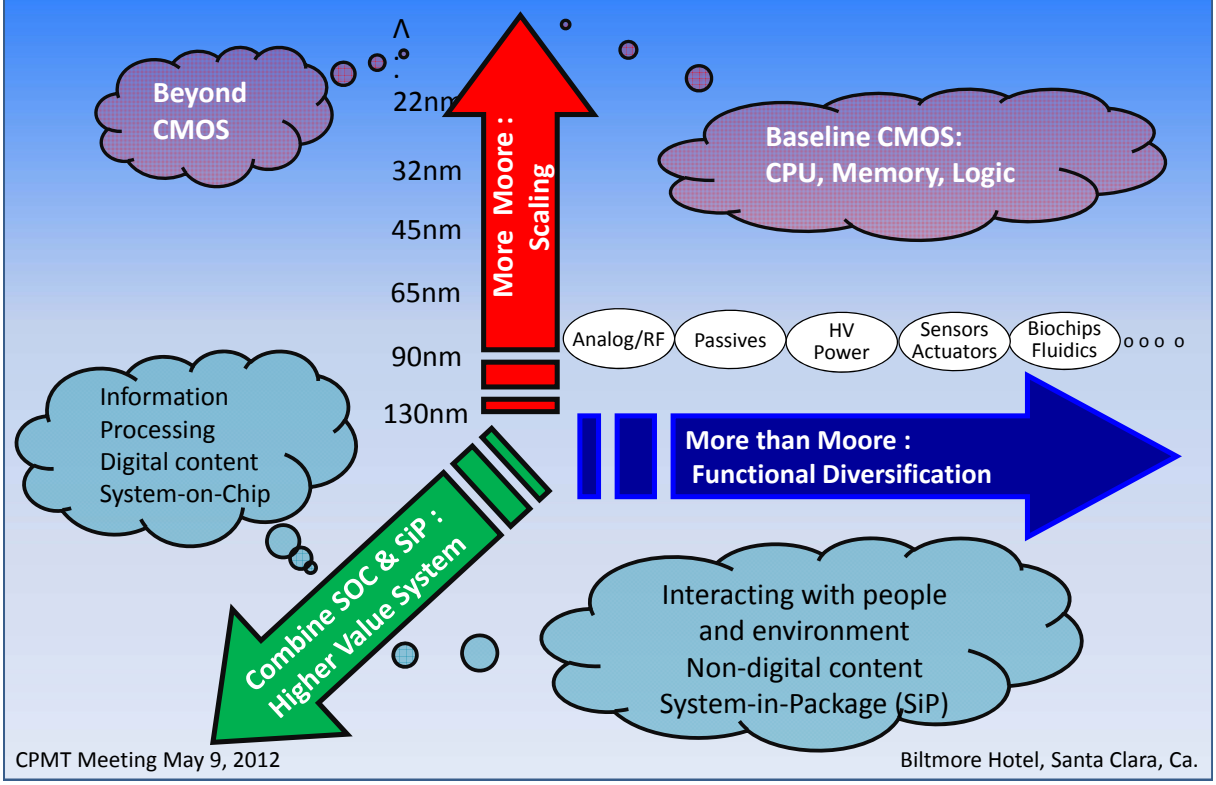
More Than Moore

Assembly and Packaging are the enablers

The use of functional diversification to deliver equivalent scaling to the Markets

- ✓ **The most cost efficient, energy efficient and highest performance is achieved when each circuit fabric type is fabricated with process and materials optimized for that component**
- ✓ **The contribution of Assembly and Packaging to MtM is System in Package (SiP) integration.**
- ✓ **The package provides:**
  - **The use of the most efficient component for each function**
  - **The delivery of the resources to the components necessary for their function**
  - **The delivery of output/removal of heat and by products from operation of the SiP**
  - **Protection of the components in the package**

Moore's Law Scaling can not maintain the Pace of Progress and Packaging enables equivalent scaling



The Role of SiP in MtM

System in Package delivers:

- ✓ Integration of diverse functions into a single package for equivalent scaling at the lowest cost
- ✓ The lowest power requirement
- ✓ The highest performance
- ✓ The lowest latency
- ✓ Reduced NRE critical to the consumer market
- ✓ Solutions to emerging market requirements through continuous integration of new components as they are developed

Materials Challenges in Packaging

Materials Challenges for discrete packages	*Issues*
Wirebond	Materials and processes for 22nm (and below) wirebond. Small diameter wires and capillaries. Pad design & metal stack for Cu Wirebond. Biased HAST compatible bonding process and molding compound. Soft 4N Cu wire and Soft Pd coated Cu wire, robust 2nd bond process and surface finish.
Underfills	Ability to support ultra low k and high Tj operations. No flow underfill material.
	Optimal Cu piller underfill and ultra fine pitch micro bump. TC bonding snap cure underfill
Thermal Interfaces Material	Increased thermal conduction, lower interface resistance, improved adhesion, higher modulus for heat sink applications, multi die applications
Materials Properties	Methodology and characterization database for frequencies above 10 GHz
Molding Compound	Molding compound for low profile multi-die package.
	Compatible with Cu Wirebond low-κ wafer structures with low moisture absorption and low ionic for high temperature lead free applications
	Molding compound for molded underffil application and hybrid wirebond and flip chip
Leadfree Solder Flip Chip Materials	Solder and UBM that supports high current density and robust for electromigration
Low Stress Die Attach Material for Tj >200C	Thin die attach material. No feasible solution known to compensate for TCE mismatch with high thermal and electrical conductivity

Materials Challenges in Packaging
continued

Materials Challenges for discrete packages	*Issues*
Low Stress Die Attach Material for Tj >200C	Thin die attach material. No feasible solution known to compensate for TCE mismatch with high thermal and electrical conductivity
Rigid Organic Substrates	Material for thin substrates and coreless substrates designed for PoP and for Embedding. Lower loss dielectric, lower TCE, and higher Tg at low cost
Embedded Passives	Small form factor. Cu terminal for Laser drill. Improved high frequency performance of dielectrics with κ above 1000; high reliability, better stability resistor materials.
	Ferromagnetics for sensor and MEMs applications
Environmental Regulatory Compliance	Cost, reliability and performance compatible materials must be identified to replace those banned
Solder Bump Replacement	Cu Pillar structure & UBM. Flexibility in joining to accommodate stress associated with TCE mismatch over the operating range
Die Attach Film	Thin wafers will suggest combination of dicing film and die attach film in a single film thin material. Lower thickness film
	Film for Wafer level processing
Through Silicon Via Materials Challenges	Low-cost, low stress via filling material and process (e.g., low-cost seeding and plating process)
	Thin wafer handling carrier material and compatible attach material
Wafer Level and Panel Fanout mateials	Robust and lower cost high UPH molding compound and Photo Imagible Dielectric for Wafer Level Fanout Process. >20 um laser via on 40 um x40 um land large format panel process with >90 % panel yield. rapid cure, fast dispense and low flow.

New Materials will be required

Many are in use today

- ✓ Cu interconnect
- ✓ Ultra Low k dielectrics
- ✓ High k dielectrics
- ✓ Organic semiconductors
- ✓ Green Materials
  - Pb free
  - Halogen free

But improvements are needed

Many are in development

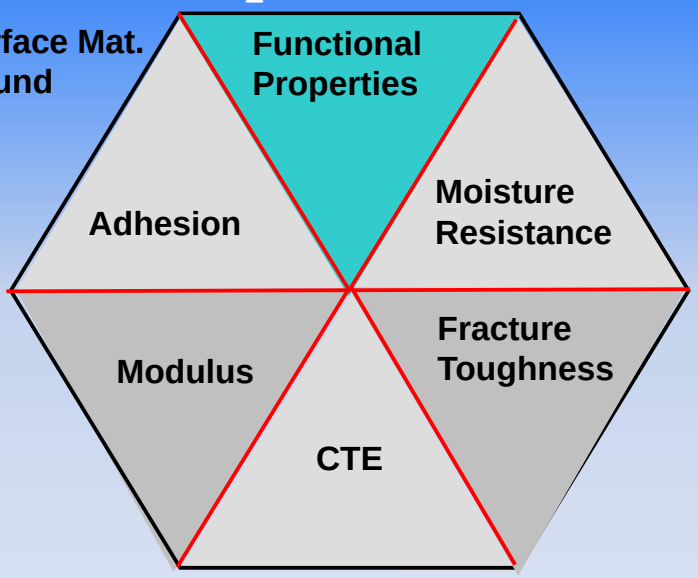
- ➢ Nanotubes
- ➢ Nano Wires
- ➢ Macromolecules
- ➢ Nano Particles
- ➢ Composite materials

100% of the packaging materials changed during the last decade

50% will change again during this decade

Hexagon of Packaging Materials Requirements

Examples
Thermal Interface Mat.
Mold Compound
Under fill
Adhesives
Epoxy



- ✓ Highly coupled Material Properties
- ✓ Apply novel materials to achieve optimal performance

Conclusions

- ✓ Everything will change over the 15 year horizon of the 2012 Roadmap
  - The basic CMOS switch
  - Device and Package architectures
    - WLP
    - SiP
    - Photons to the package (some say to the chip)
  - Emerging processes will dominate
    - Thinning
    - Stacking
    - 3D integration
    - Embedded components
    - Packaging and device materials

Conclusions

- ✓ Everything will change over the 15 year horizon of the

The development of new design tools, new materials, new equipment and novel methods of test ensuring reliability pose enormous challenges.

These Roadmaps identify the critical challenges in advance and support pre-competitive collaborations that will maintain the pace of progress

CPMT Meeting May 9, 2012 Biltmore Hotel, Santa Clara, Ca.

Thank you