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Technologies, Inc.
Advanced Organic Substrate Technologies to Enable Extreme Electronics Miniaturization
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Advanced Organic Substrate Technologies to Enable Extreme Electronics Miniaturization
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February 13, 2013
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Agenda

- Introduction
- Thin Core Substrates vs. PWBs
- Chip-Package Interaction
- Organic vs. Ceramic
- System-in-Package Building Blocks
- System-in-Package Case Studies
- Z-Interconnect
- 3D Solutions
- Extreme Miniaturization with Microflex
- New Substrate Technologies: LCP & Stretchable

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Benefits of Electronics Miniaturization

Markets: Aerospace, Defense, Industrial & Medical

MACRO ELECTRONIC ASSEMBLIES Increased Function & Integration	MICRO ELECTRONIC ASSEMBLIES Increased Function / Reduced SWaP
(Servers, Medical Systems)	(Implantables, biosensors, guidance sensors, UAVs, advanced receptors)

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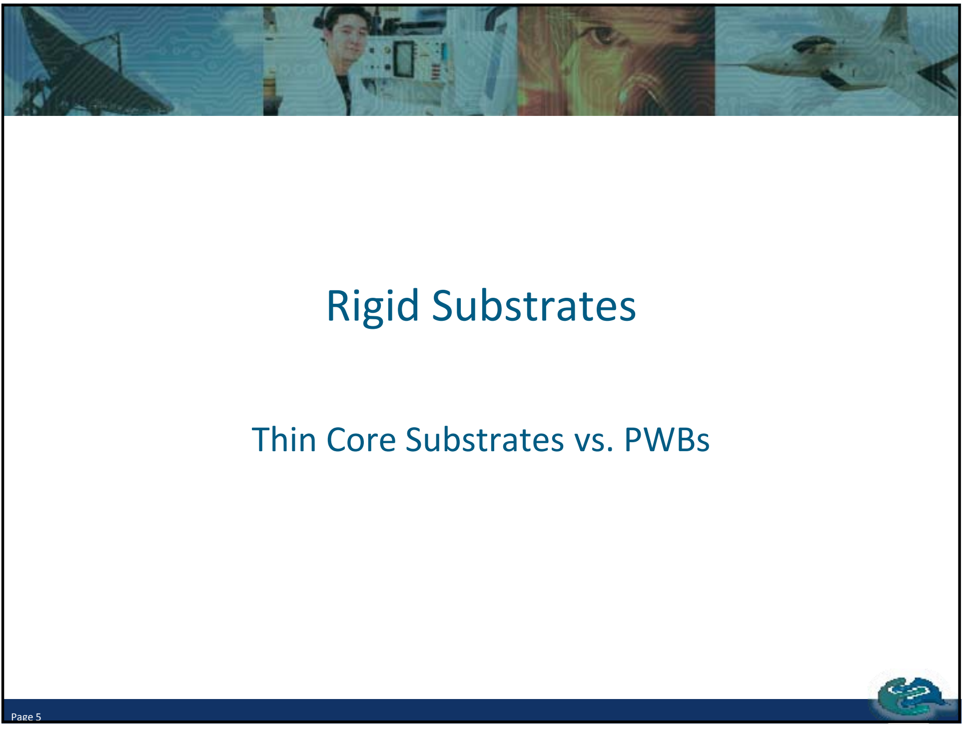
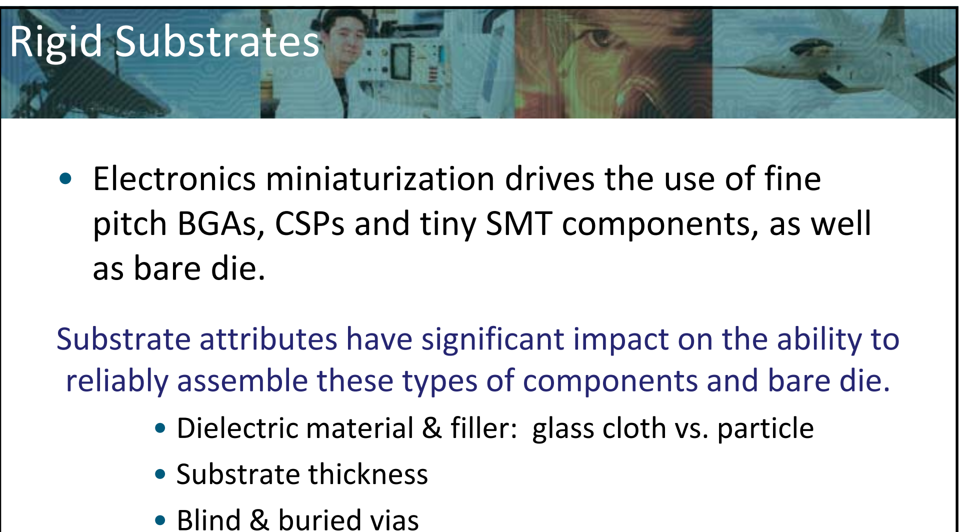
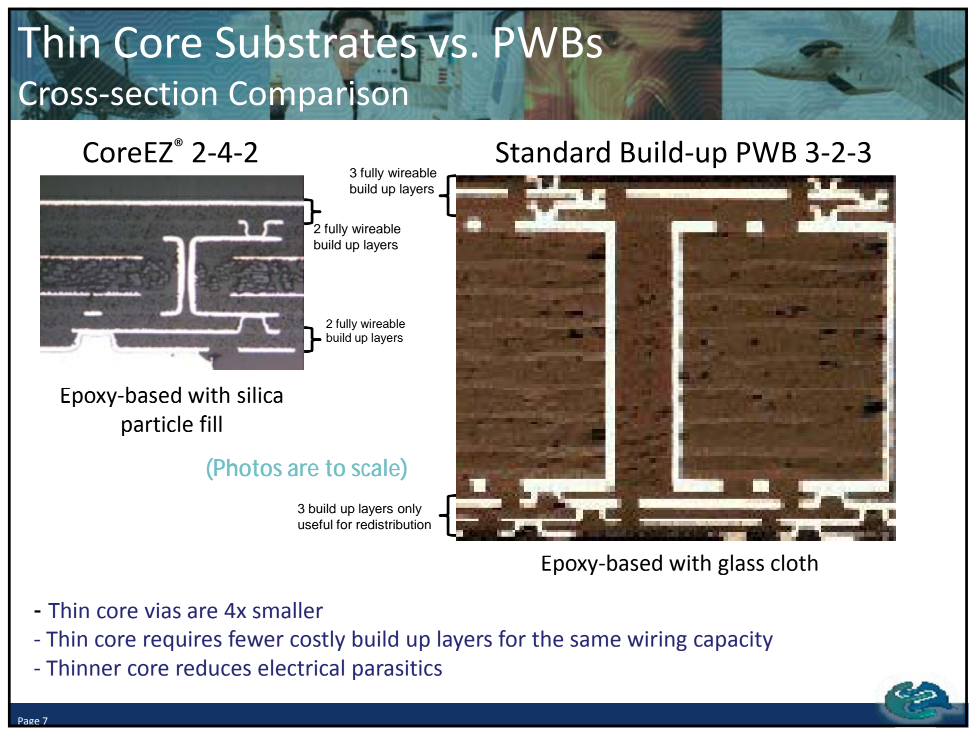

Rigid Substrates
Thin Core Substrates vs. PWBs
Page 5


Rigid Substrates
• Electronics miniaturization drives the use of fine pitch BGAs, CSPs and tiny SMT components, as well as bare die.
Substrate attributes have significant impact on the ability to reliably assemble these types of components and bare die.
• Dielectric material & filler: glass cloth vs. particle
• Substrate thickness
• Blind & buried vias
• Line width & space capability
Page 6


Thin Core Substrates vs. PWBs
Cross-section Comparison
CoreEZ® 2-4-2
Standard Build-up PWB 3-2-3
3 fully wireable build up layers
2 fully wireable build up layers
2 fully wireable build up layers
Epoxy-based with silica particle fill
(Photos are to scale)
3 build up layers only useful for redistribution
Epoxy-based with glass cloth
- Thin core vias are 4x smaller
- Thin core requires fewer costly build up layers for the same wiring capacity
- Thinner core reduces electrical parasitics
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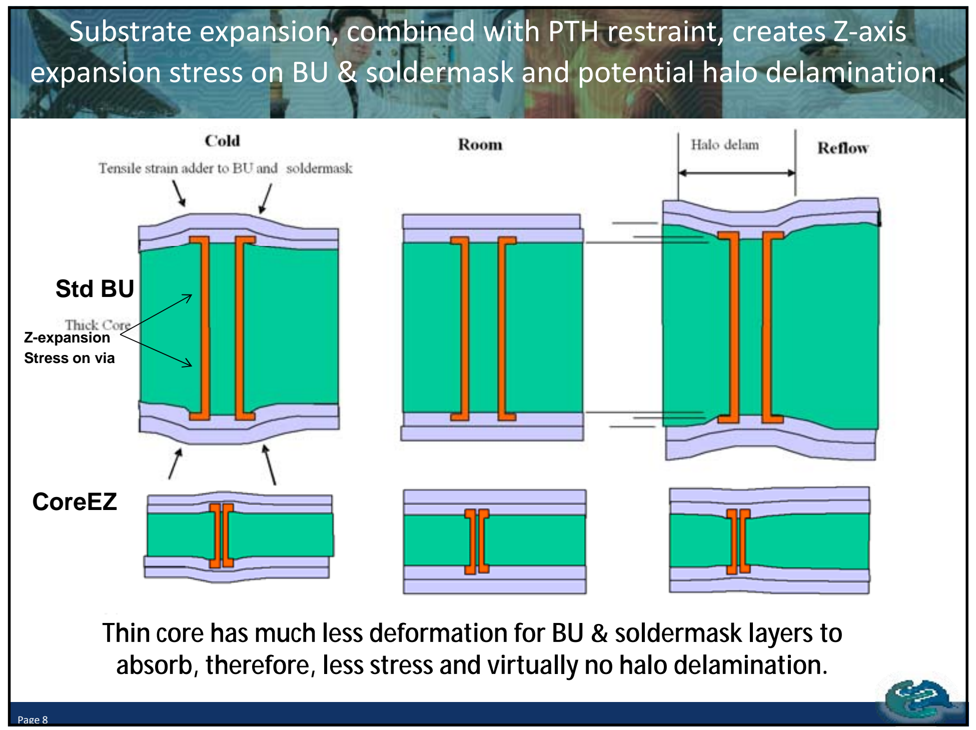
Substrate expansion, combined with PTH restraint, creates Z-axis expansion stress on BU & soldermask and potential halo delamination.
Cold
Tensile strain adder to BU and soldermask
Room
Halo delam
Reflow
Std BU
Thick Core
Z-expansion
Stress on via
CoreEZ
Thin core has much less deformation for BU & soldermask layers to absorb, therefore, less stress and virtually no halo delamination.
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Limiting Attributes of PWBs for Bare Die Assembly

- Thick Core: Z-axis Expansion
  - Limits bare die assembly primarily to wirebond or only small, low I/O flipchip die
- Glass Cloth Filler
  - Risk of CAF (conductive anodic filament) defects
  - Mechanical or CO_2 drill
  - Surface topography can impact ability to achieve conductor fine lines and spaces

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Thin Core Substrates vs. PWBs
Via Density Comparison

- Very Dense Package Interconnect
  - Ultra Dense Core Via Pitch can eliminate additional build up layers
  - When CVP is nearly die bump pitch, enables Z-escape to all wiring planes
- Dual Side Component Mounting
- Fine Line Width and Spacing
  - 18 – 25 µm

UV Laser Drilled CoreEZ® Thin Core: 100 um diameter pad (50 um via)

Standard Build-Up Mechanically drilled core: 400 micron diameter pad, 200 um diameter via

HDI Substrate has 9X Core Via Density over conventional build up PWB

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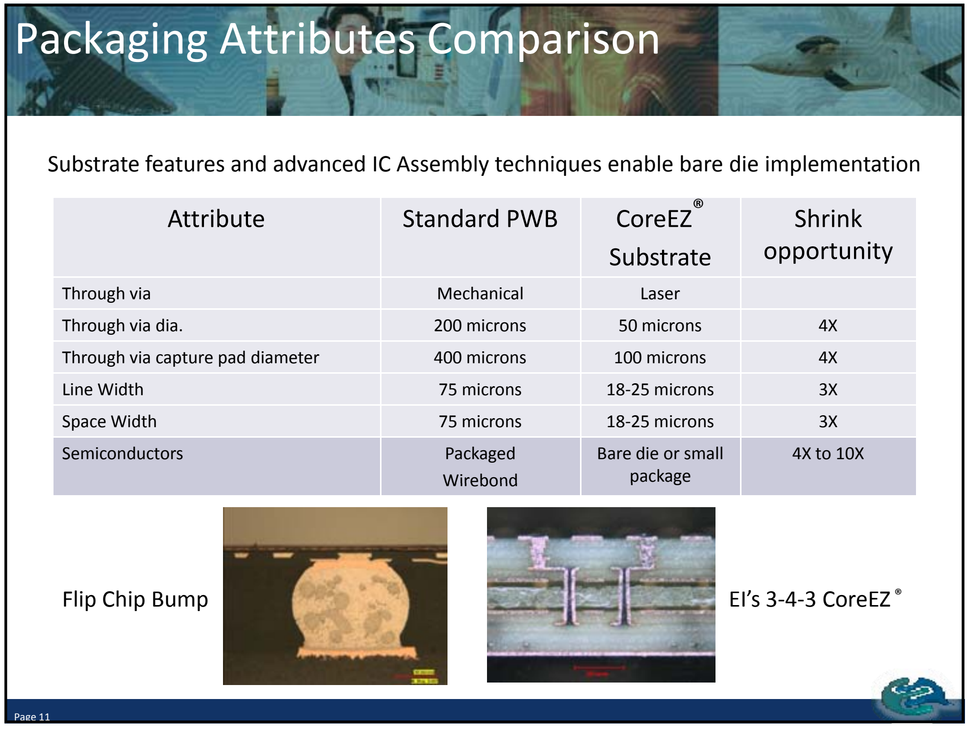
Packaging Attributes Comparison
Substrate features and advanced IC Assembly techniques enable bare die implementation
Attribute | Standard PWB | CoreEZ® Substrate | Shrink opportunity
Through via | Mechanical | Laser |
Through via dia. | 200 microns | 50 microns | 4X
Through via capture pad diameter | 400 microns | 100 microns | 4X
Line Width | 75 microns | 18-25 microns | 3X
Space Width | 75 microns | 18-25 microns | 3X
Semiconductors | Packaged Wirebond | Bare die or small package | 4X to 10X
Flip Chip Bump
EI's 3-4-3 CoreEZ®
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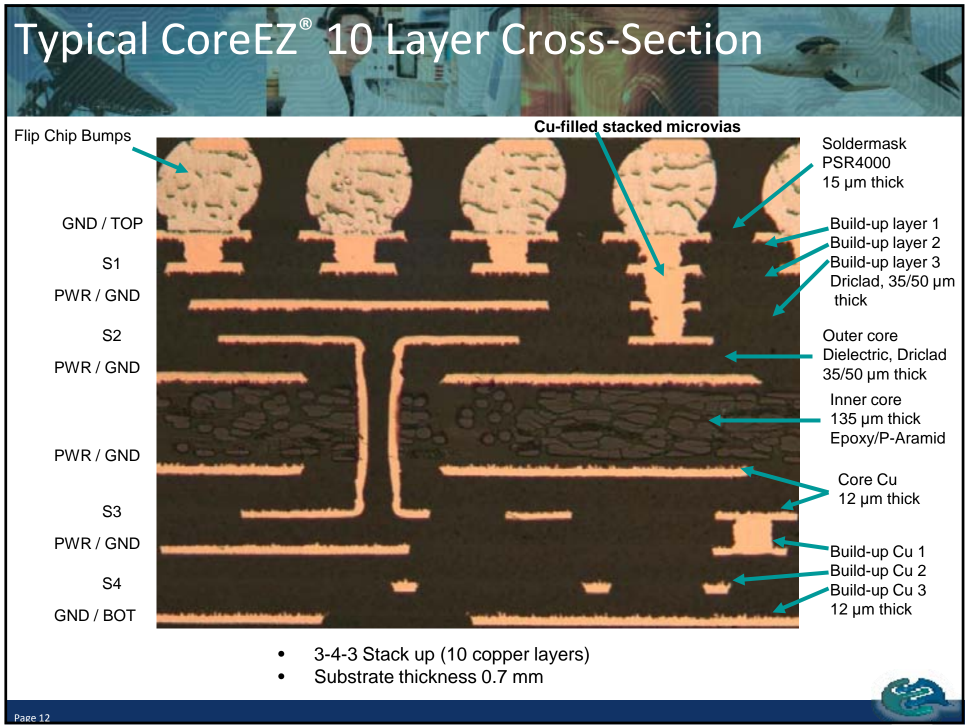
Typical CoreEZ® 10 Layer Cross-Section
Flip Chip Bumps
Cu-filled stacked microvias
Soldermask PSR4000 15 µm thick
GND / TOP
S1
PWR / GND
S2
PWR / GND
PWR / GND
S3
PWR / GND
S4
GND / BOT
Build-up layer 1
Build-up layer 2
Build-up layer 3
Driclad, 35/50 µm thick
Outer core Dielectric, Driclad 35/50 µm thick
Inner core 135 µm thick Epoxy/P-Aramid
Core Cu 12 µm thick
Build-up Cu 1
Build-up Cu 2
Build-up Cu 3
12 µm thick
• 3-4-3 Stack up (10 copper layers)
• Substrate thickness 0.7 mm
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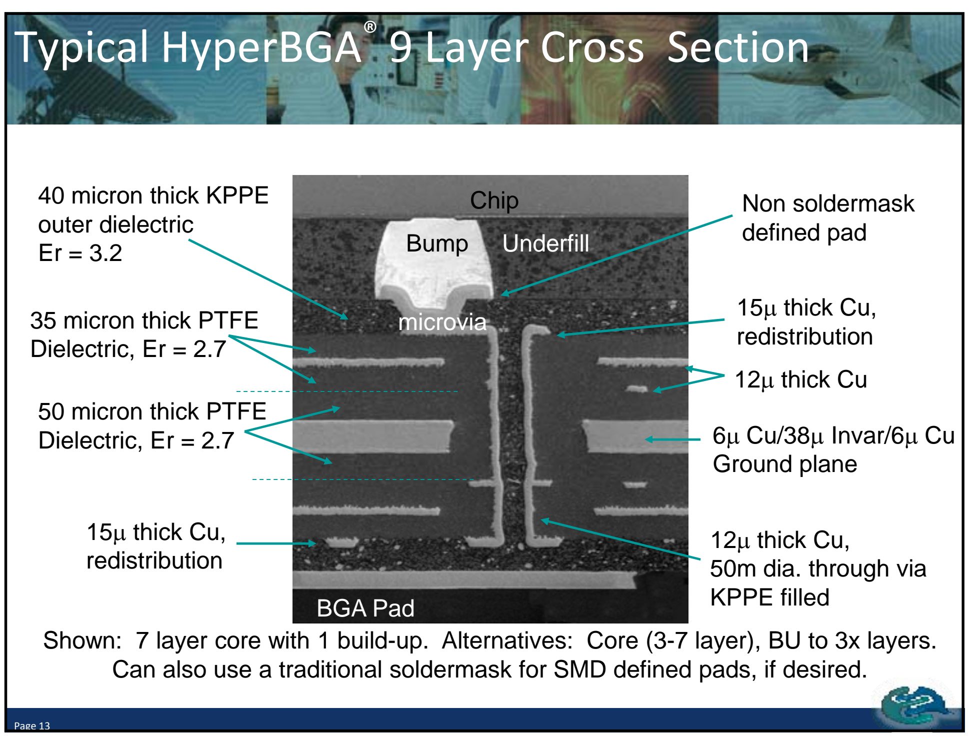
Typical HyperBGA® 9 Layer Cross Section
40 micron thick KPPE outer dielectric Er = 3.2
Chip
Bump
Underfill
Non soldermask defined pad
35 micron thick PTFE Dielectric, Er = 2.7
microvia
15µ thick Cu, redistribution
12µ thick Cu
50 micron thick PTFE Dielectric, Er = 2.7
6µ Cu/38µ Invar/6µ Cu Ground plane
15µ thick Cu, redistribution
12µ thick Cu, 50m dia. through via KPPE filled
BGA Pad
Shown: 7 layer core with 1 build-up. Alternatives: Core (3-7 layer), BU to 3x layers.
Can also use a traditional soldermask for SMD defined pads, if desired.
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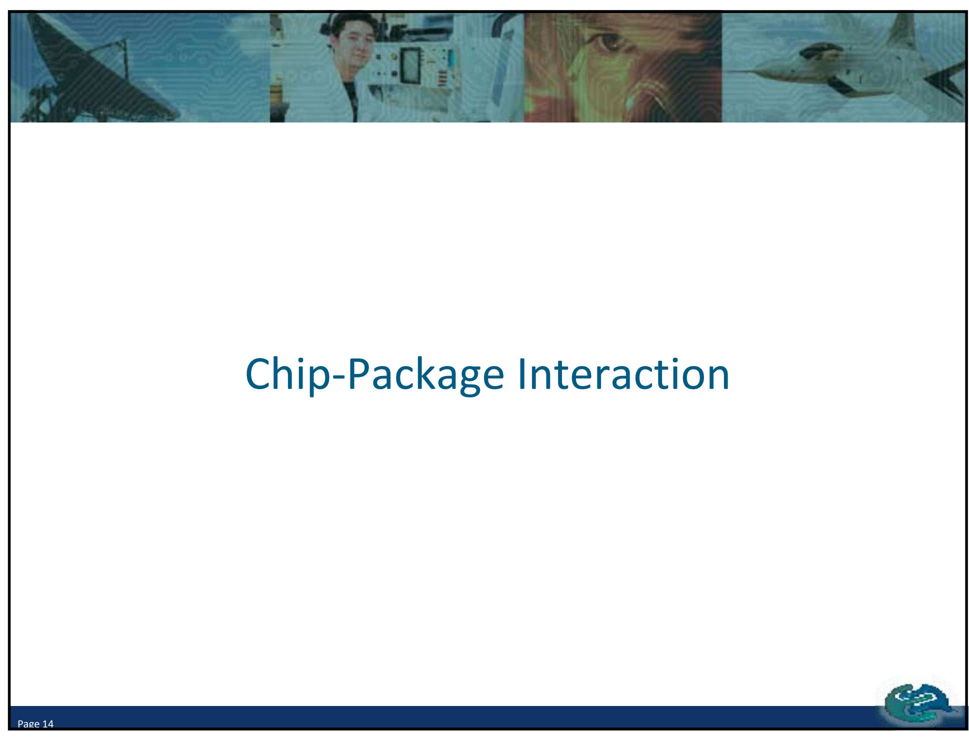
Chip-Package Interaction
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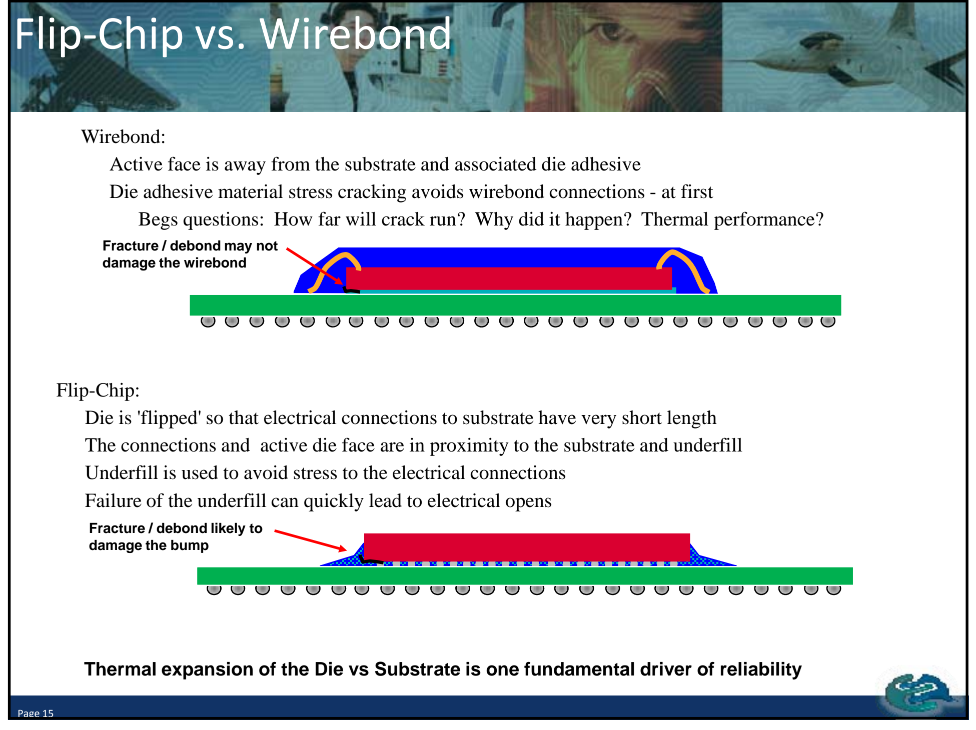
Flip-Chip vs. Wirebond
Wirebond:
Active face is away from the substrate and associated die adhesive
Die adhesive material stress cracking avoids wirebond connections - at first
Begs questions: How far will crack run? Why did it happen? Thermal performance?
Fracture / debond may not damage the wirebond
Flip-Chip:
Die is 'flipped' so that electrical connections to substrate have very short length
The connections and active die face are in proximity to the substrate and underfill
Underfill is used to avoid stress to the electrical connections
Failure of the underfill can quickly lead to electrical opens
Fracture / debond likely to damage the bump
Thermal expansion of the Die vs Substrate is one fundamental driver of reliability
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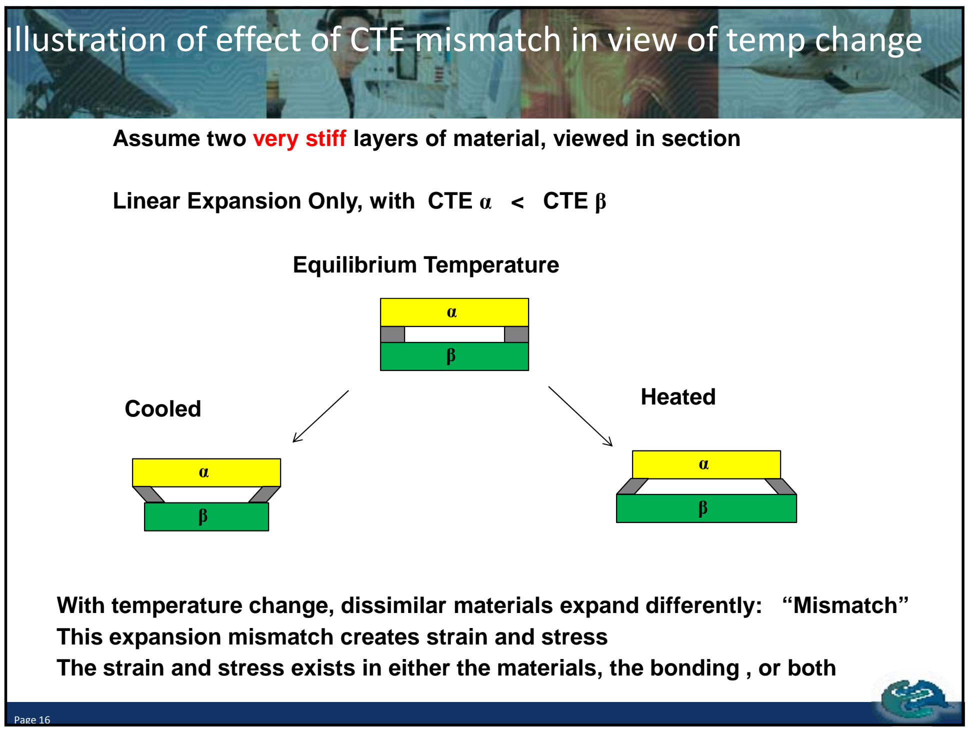
Illustration of effect of CTE mismatch in view of temp change
Assume two very stiff layers of material, viewed in section
Linear Expansion Only, with CTE α < CTE β
Equilibrium Temperature
α
β
Cooled
Heated
α
β
α
β
With temperature change, dissimilar materials expand differently: "Mismatch"
This expansion mismatch creates strain and stress
The strain and stress exists in either the materials, the bonding , or both
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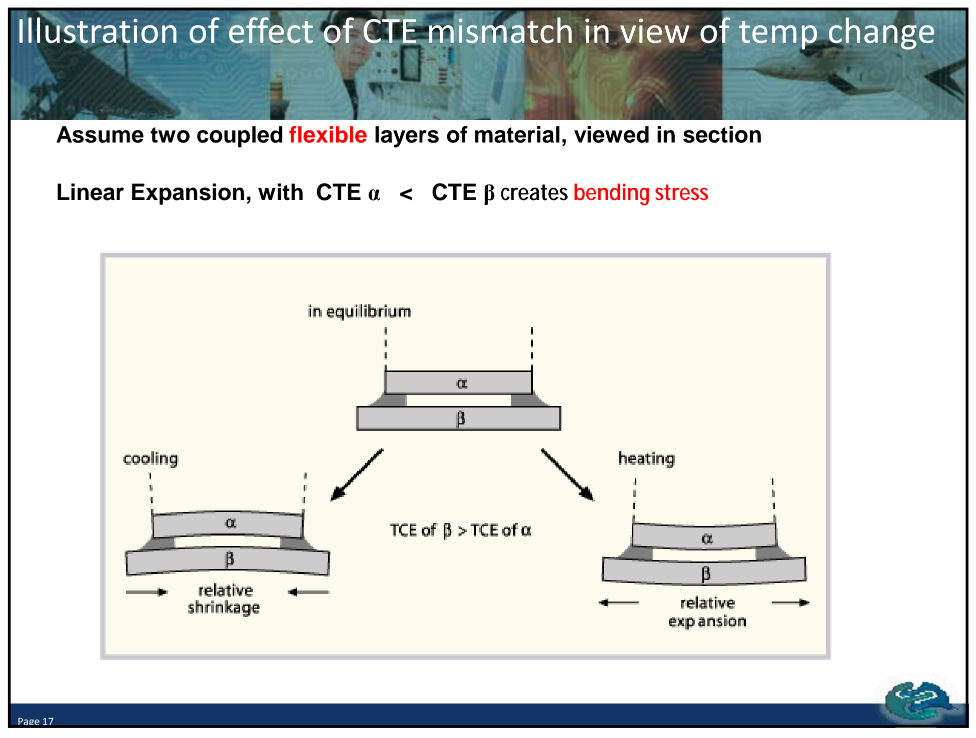
Illustration of effect of CTE mismatch in view of temp change
Assume two coupled flexible layers of material, viewed in section
Linear Expansion, with CTE α < CTE β creates bending stress
in equilibrium
α
β
cooling
heating
TCE of β > TCE of α
relative shrinkage
relative expansion
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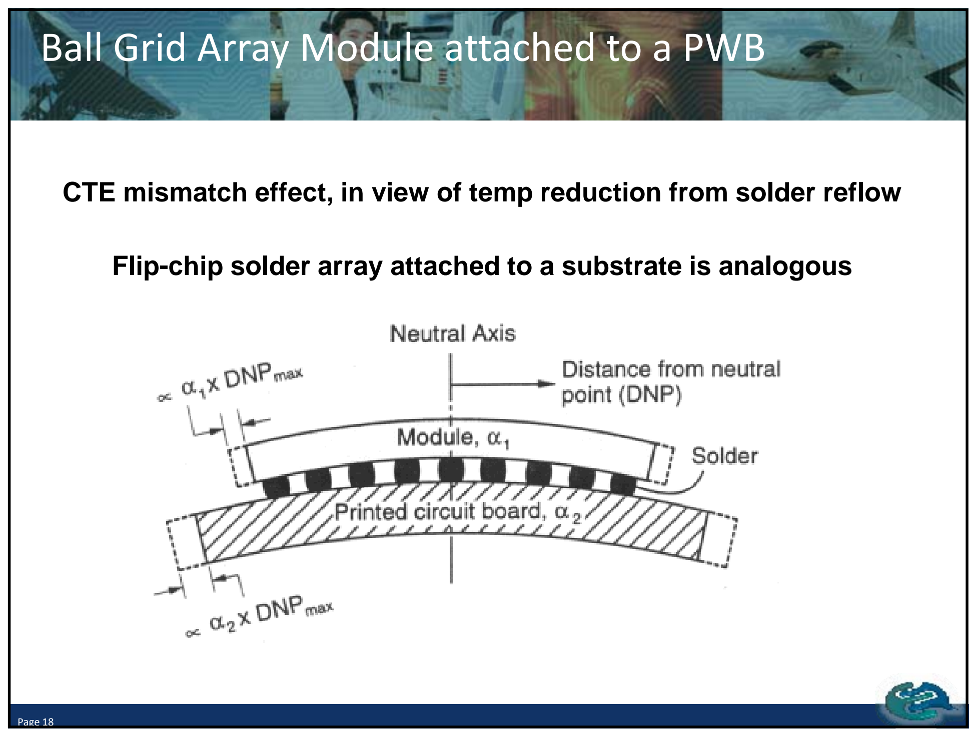
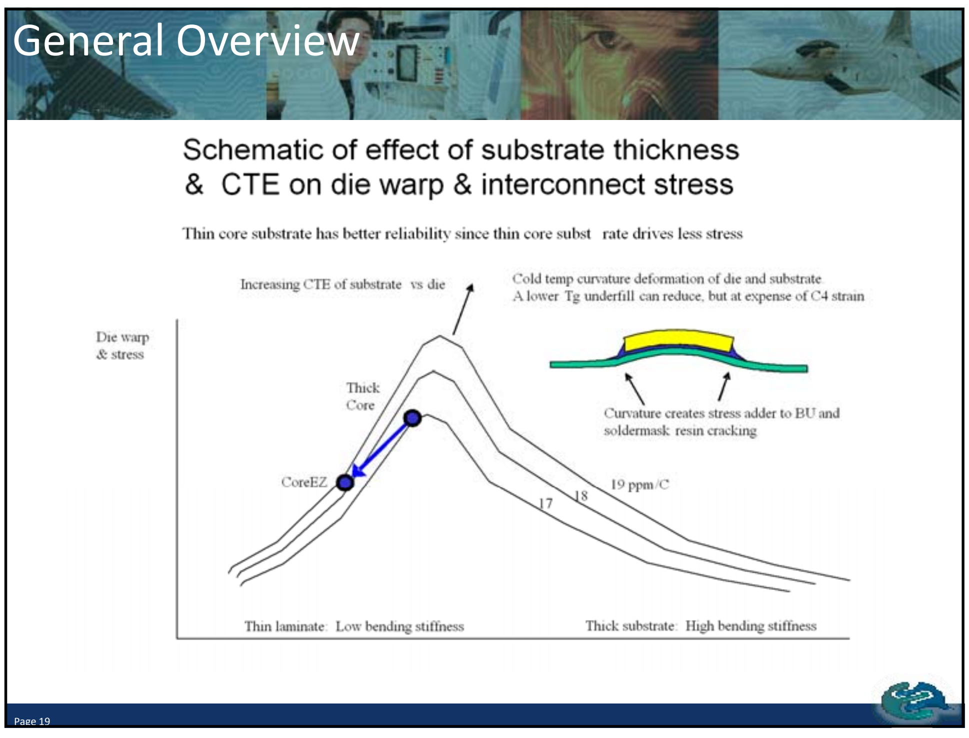

Ball Grid Array Module attached to a PWB
CTE mismatch effect, in view of temp reduction from solder reflow
Flip-chip solder array attached to a substrate is analogous
Neutral Axis
∝ α1 x DNPmax
Distance from neutral point (DNP)
Module, α1
Solder
Printed circuit board, α2
∝ α2 x DNPmax
Page 18


General Overview
Schematic of effect of substrate thickness & CTE on die warp & interconnect stress
Thin core substrate has better reliability since thin core subst rate drives less stress
Increasing CTE of substrate vs die
Cold temp curvature deformation of die and substrate
A lower Tg underfill can reduce, but at expense of C4 strain
Die warp & stress
Thick Core
CoreEZ
Curvature creates stress adder to BU and soldermask resin cracking
19 ppm/C
18
17
Thin laminate: Low bending stiffness
Thick substrate: High bending stiffness
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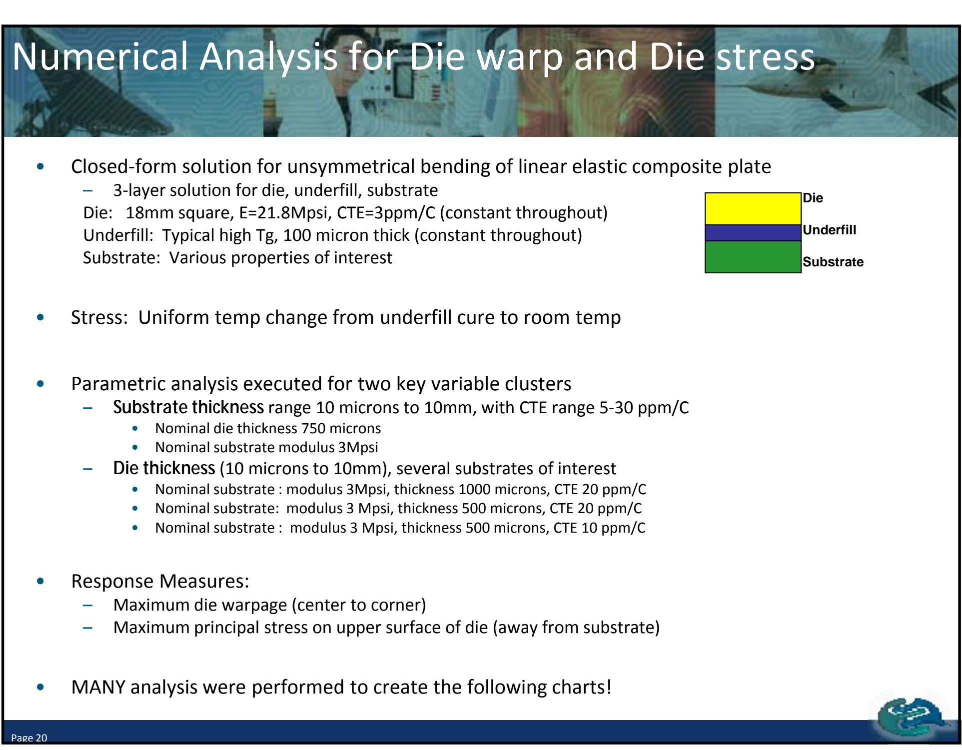
Numerical Analysis for Die warp and Die stress
Closed-form solution for unsymmetrical bending of linear elastic composite plate
3-layer solution for die, underfill, substrate
Die: 18mm square, E=21.8Mpsi, CTE=3ppm/C (constant throughout)
Underfill: Typical high Tg, 100 micron thick (constant throughout)
Substrate: Various properties of interest
Die
Underfill
Substrate
Stress: Uniform temp change from underfill cure to room temp
Parametric analysis executed for two key variable clusters
Substrate thickness range 10 microns to 10mm, with CTE range 5-30 ppm/C
Nominal die thickness 750 microns
Nominal substrate modulus 3Mpsi
Die thickness (10 microns to 10mm), several substrates of interest
Nominal substrate : modulus 3Mpsi, thickness 1000 microns, CTE 20 ppm/C
Nominal substrate: modulus 3 Mpsi, thickness 500 microns, CTE 20 ppm/C
Nominal substrate : modulus 3 Mpsi, thickness 500 microns, CTE 10 ppm/C
Response Measures:
Maximum die warpage (center to corner)
Maximum principal stress on upper surface of die (away from substrate)
MANY analysis were performed to create the following charts!
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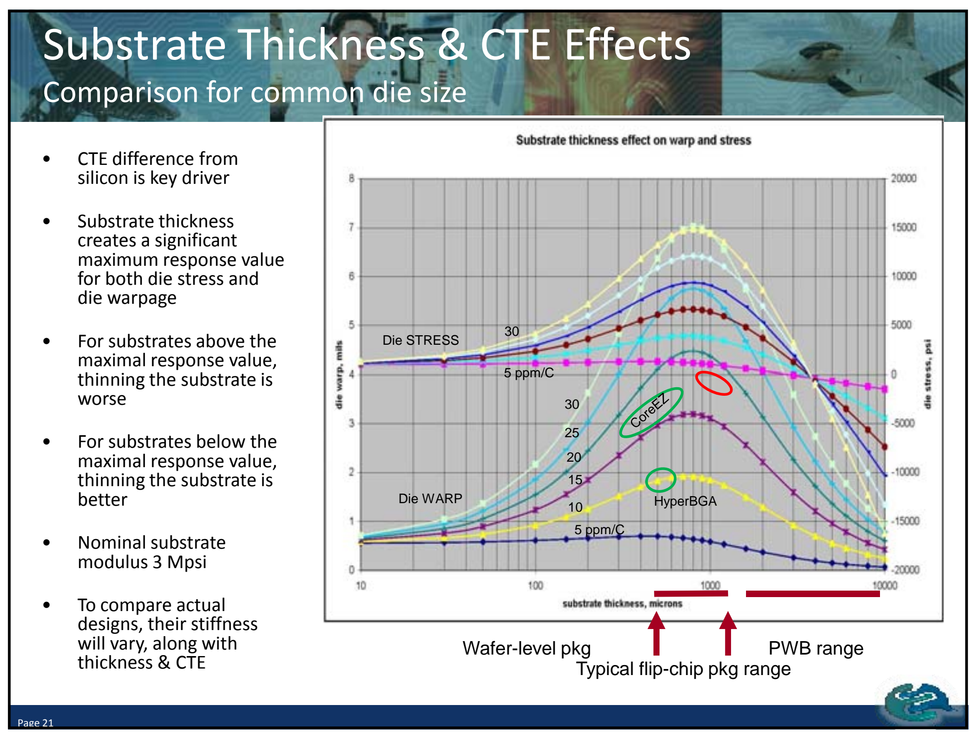
Substrate Thickness & CTE Effects
Comparison for common die size
• CTE difference from silicon is key driver
• Substrate thickness creates a significant maximum response value for both die stress and die warpage
• For substrates above the maximal response value, thinning the substrate is worse
• For substrates below the maximal response value, thinning the substrate is better
• Nominal substrate modulus 3 Mpsi
• To compare actual designs, their stiffness will vary, along with thickness & CTE
Substrate thickness effect on warp and stress
die warp, mils
die stress, psi
substrate thickness, microns
Die STRESS
30
5 ppm/C
30
25
20
15
10
5 ppm/C
Die WARP
CoreEZ
HyperBGA
Wafer-level pkg
Typical flip-chip pkg range
PWB range
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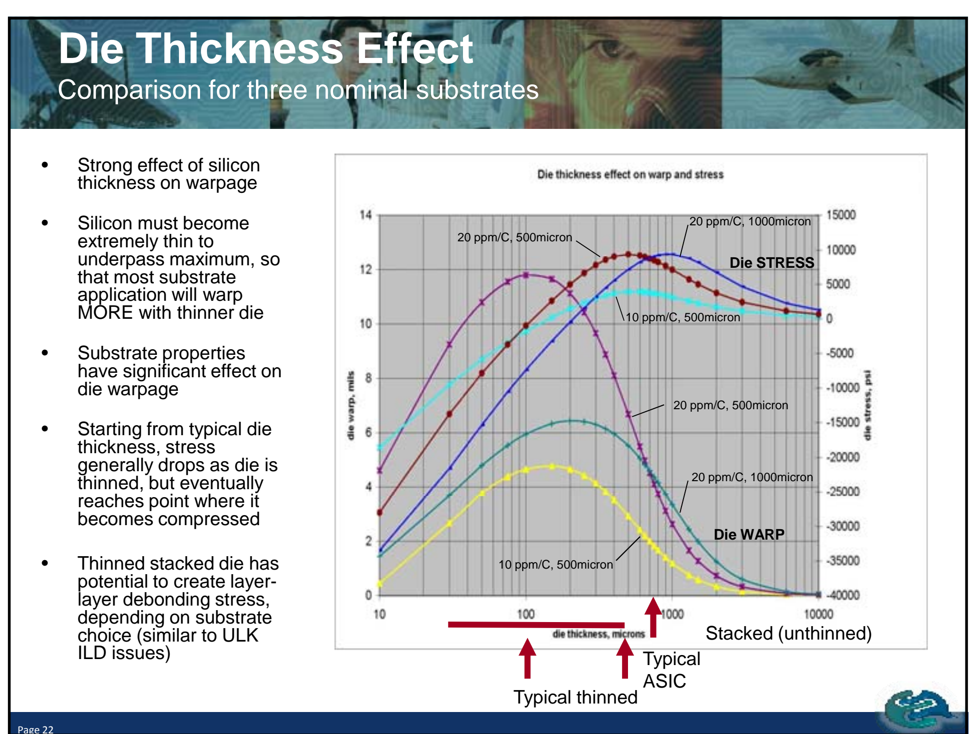
Die Thickness Effect
Comparison for three nominal substrates
• Strong effect of silicon thickness on warpage
• Silicon must become extremely thin to underpass maximum, so that most substrate application will warp MORE with thinner die
• Substrate properties have significant effect on die warpage
• Starting from typical die thickness, stress generally drops as die is thinned, but eventually reaches point where it becomes compressed
• Thinned stacked die has potential to create layer-layer debonding stress, depending on substrate choice (similar to ULK ILD issues)
Die thickness effect on warp and stress
die warp, mils
die stress, psi
die thickness, microns
20 ppm/C, 500micron
20 ppm/C, 1000micron
Die STRESS
10 ppm/C, 500micron
20 ppm/C, 500micron
20 ppm/C, 1000micron
Die WARP
10 ppm/C, 500micron
Stacked (unthinned)
Typical ASIC
Typical thinned
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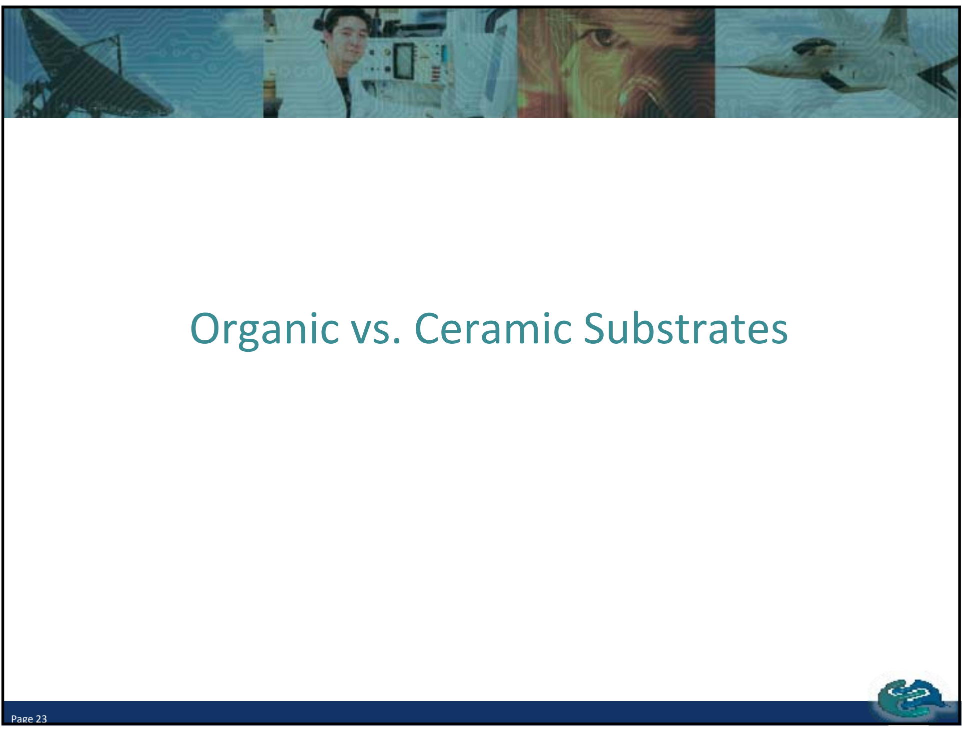
Organic vs. Ceramic Substrates
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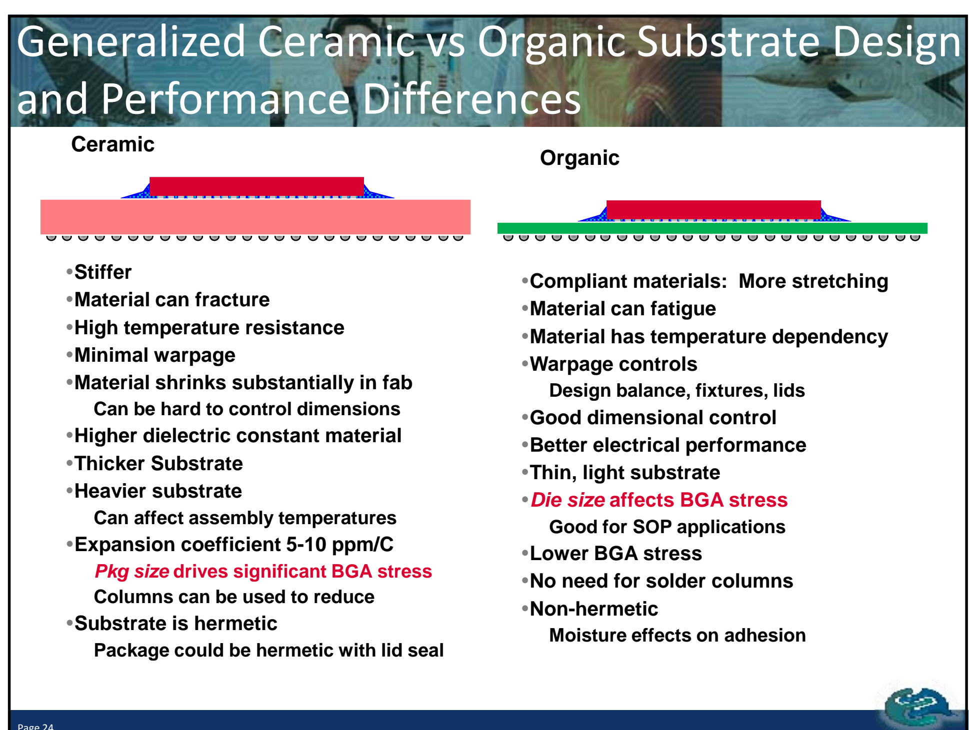
Generalized Ceramic vs Organic Substrate Design and Performance Differences
Ceramic
•Stiffer
•Material can fracture
•High temperature resistance
•Minimal warpage
•Material shrinks substantially in fab
Can be hard to control dimensions
•Higher dielectric constant material
•Thicker Substrate
•Heavier substrate
Can affect assembly temperatures
•Expansion coefficient 5-10 ppm/C
Pkg size drives significant BGA stress
Columns can be used to reduce
•Substrate is hermetic
Package could be hermetic with lid seal
Organic
•Compliant materials: More stretching
•Material can fatigue
•Material has temperature dependency
•Warpage controls
Design balance, fixtures, lids
•Good dimensional control
•Better electrical performance
•Thin, light substrate
•Die size affects BGA stress
Good for SOP applications
•Lower BGA stress
•No need for solder columns
•Non-hermetic
Moisture effects on adhesion
Page 24

Weight Comparisons

40 mm body size substrate	Approximate substrate weight (gm)
Ceramic (30 layer, alumina, 10mil/layer)	48
Ceramic (15 layer, alumina, 10 mil/layer)	24
PTFE BGA 9 layer substrate	2.3
Thin core build up 10 layer substrate	2.9
Thin core build up 6 layer substrate	2.0

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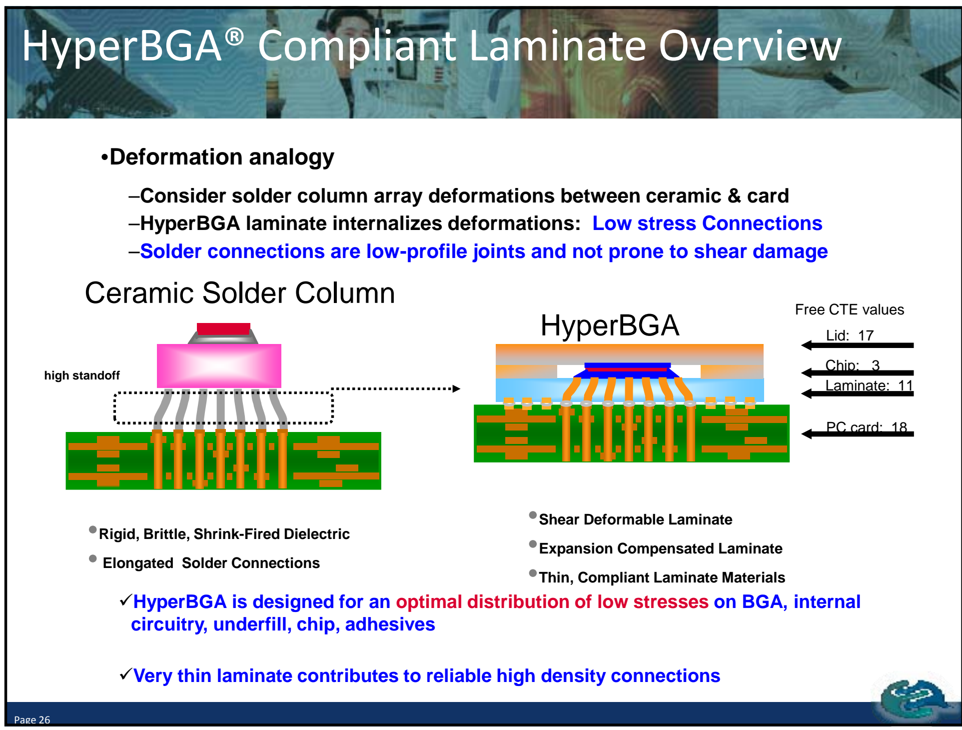

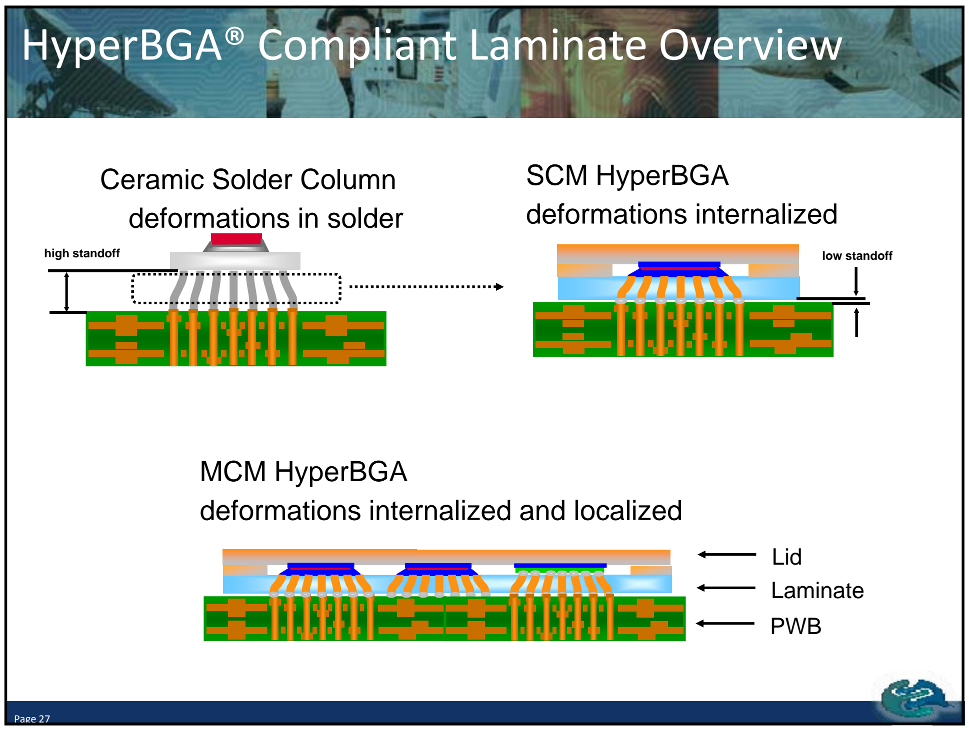
HyperBGA® Compliant Laminate Overview
Ceramic Solder Column
deformations in solder
high standoff
SCM HyperBGA
deformations internalized
low standoff
MCM HyperBGA
deformations internalized and localized
Lid
Laminate
PWB
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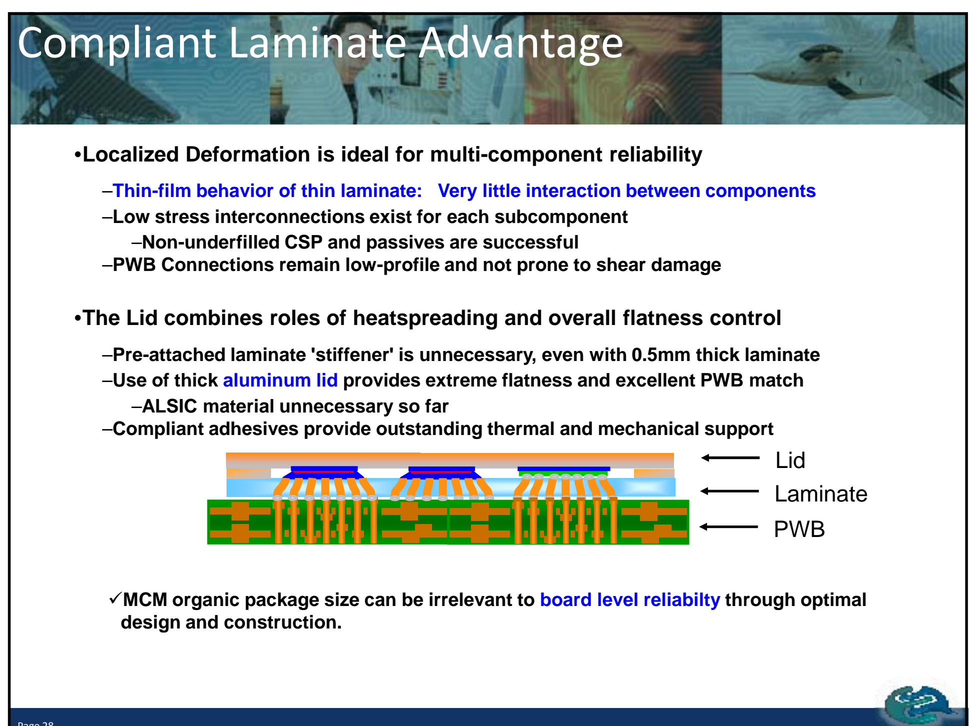
Compliant Laminate Advantage
•Localized Deformation is ideal for multi-component reliability
–Thin-film behavior of thin laminate: Very little interaction between components
–Low stress interconnections exist for each subcomponent
–Non-underfilled CSP and passives are successful
–PWB Connections remain low-profile and not prone to shear damage
•The Lid combines roles of heatspreading and overall flatness control
–Pre-attached laminate 'stiffener' is unnecessary, even with 0.5mm thick laminate
–Use of thick aluminum lid provides extreme flatness and excellent PWB match
–ALSIC material unnecessary so far
–Compliant adhesives provide outstanding thermal and mechanical support
Lid
Laminate
PWB
✓MCM organic package size can be irrelevant to board level reliabilty through optimal design and construction.
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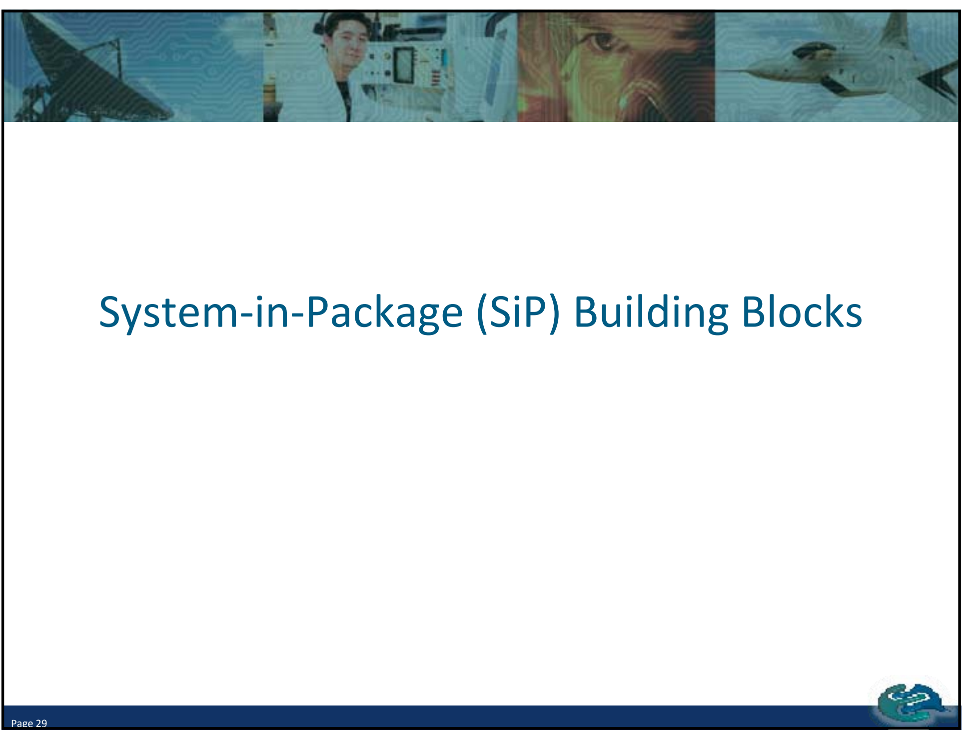
System-in-Package (SiP) Building Blocks
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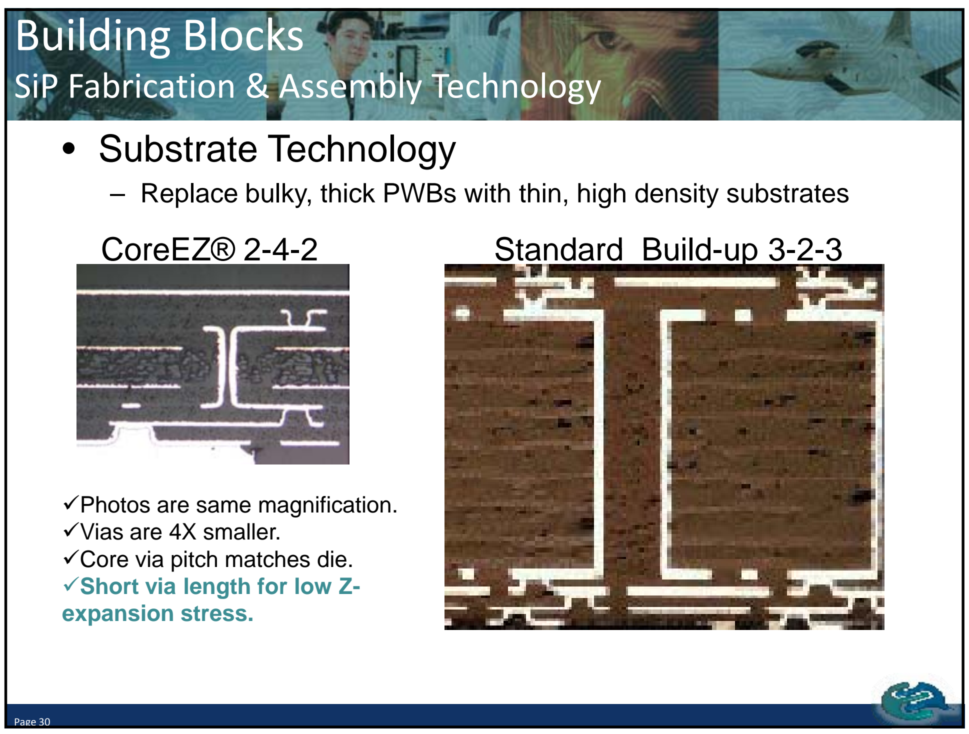
Building Blocks
SiP Fabrication & Assembly Technology
• Substrate Technology
– Replace bulky, thick PWBs with thin, high density substrates
CoreEZ® 2-4-2
Standard Build-up 3-2-3
✓Photos are same magnification.
✓Vias are 4X smaller.
✓Core via pitch matches die.
✓Short via length for low Z-expansion stress.
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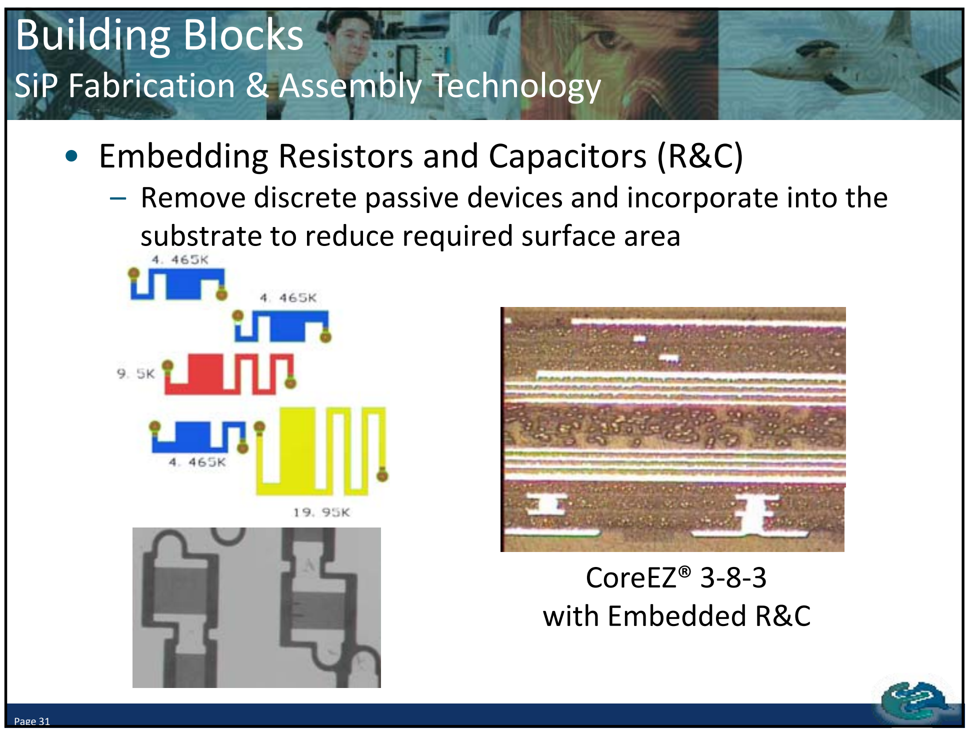
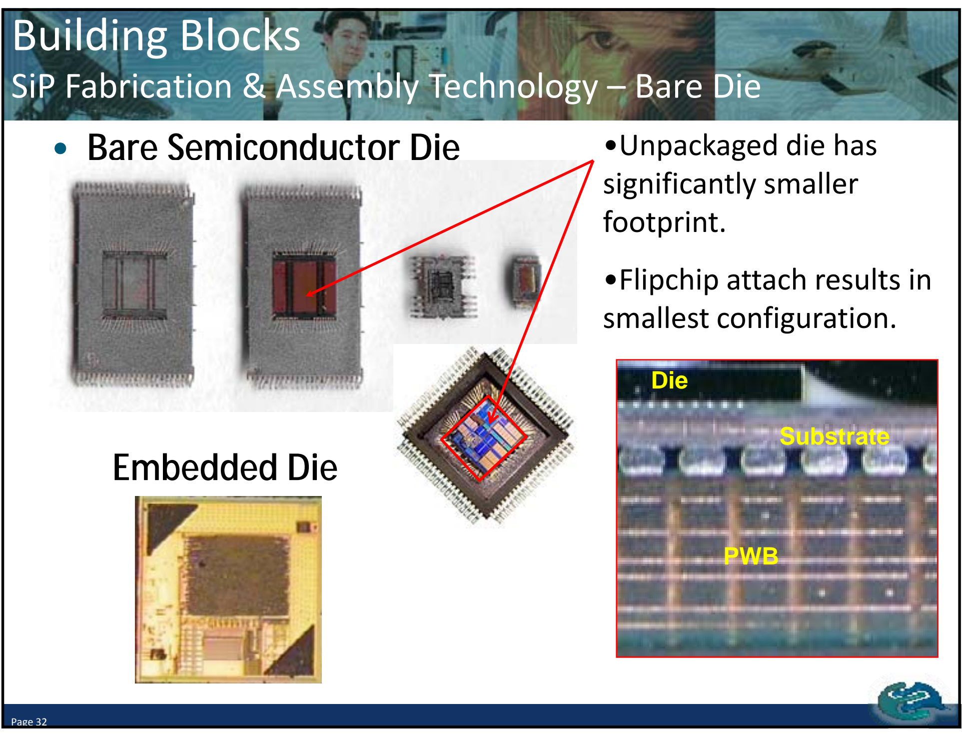
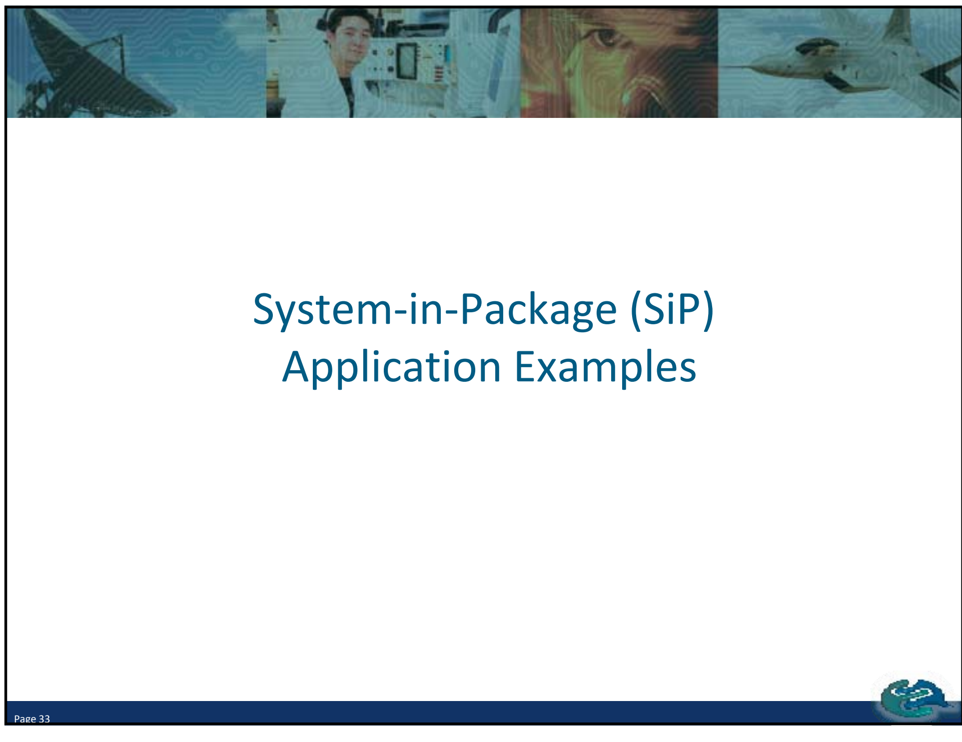

Building Blocks
SiP Fabrication & Assembly Technology
• Embedding Resistors and Capacitors (R&C)
– Remove discrete passive devices and incorporate into the substrate to reduce required surface area
4. 465K
4. 465K
9. 5K
4. 465K
19. 95K
CoreEZ® 3-8-3
with Embedded R&C
Page 31


Building Blocks
SiP Fabrication & Assembly Technology – Bare Die
• Bare Semiconductor Die
•Unpackaged die has significantly smaller footprint.
•Flipchip attach results in smallest configuration.
Die
Substrate
PWB
Embedded Die
Page 32


System-in-Package (SiP)
Application Examples
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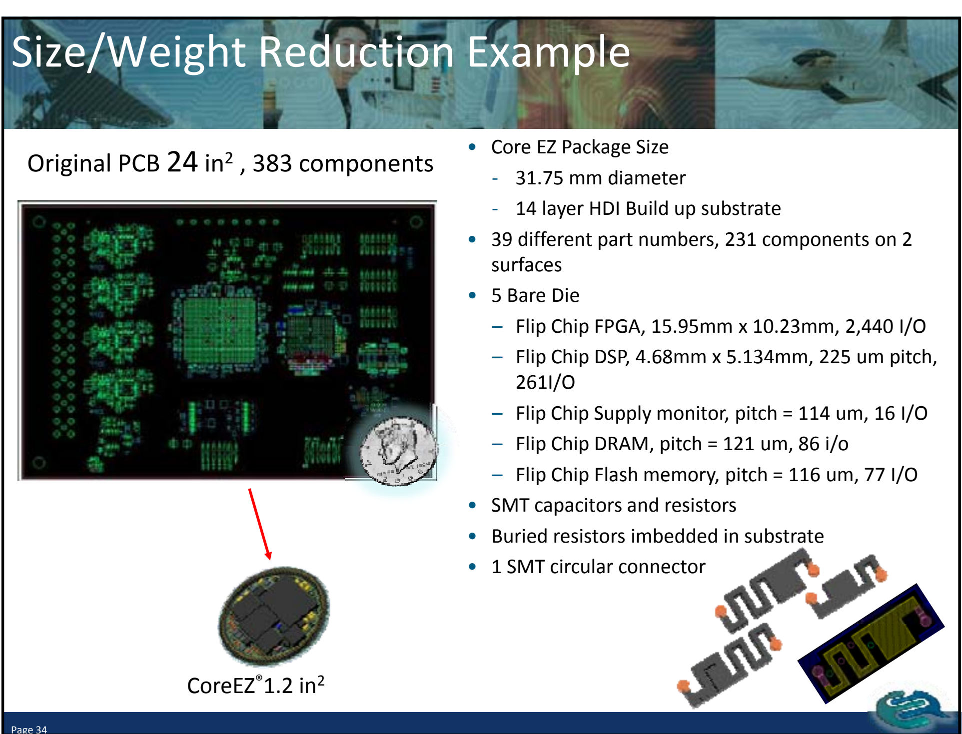
Size/Weight Reduction Example
Original PCB 24 in², 383 components
CoreEZ® 1.2 in²
• Core EZ Package Size
- 31.75 mm diameter
- 14 layer HDI Build up substrate
• 39 different part numbers, 231 components on 2 surfaces
• 5 Bare Die
– Flip Chip FPGA, 15.95mm x 10.23mm, 2,440 I/O
– Flip Chip DSP, 4.68mm x 5.134mm, 225 um pitch, 261I/O
– Flip Chip Supply monitor, pitch = 114 um, 16 I/O
– Flip Chip DRAM, pitch = 121 um, 86 i/o
– Flip Chip Flash memory, pitch = 116 um, 77 I/O
• SMT capacitors and resistors
• Buried resistors imbedded in substrate
• 1 SMT circular connector
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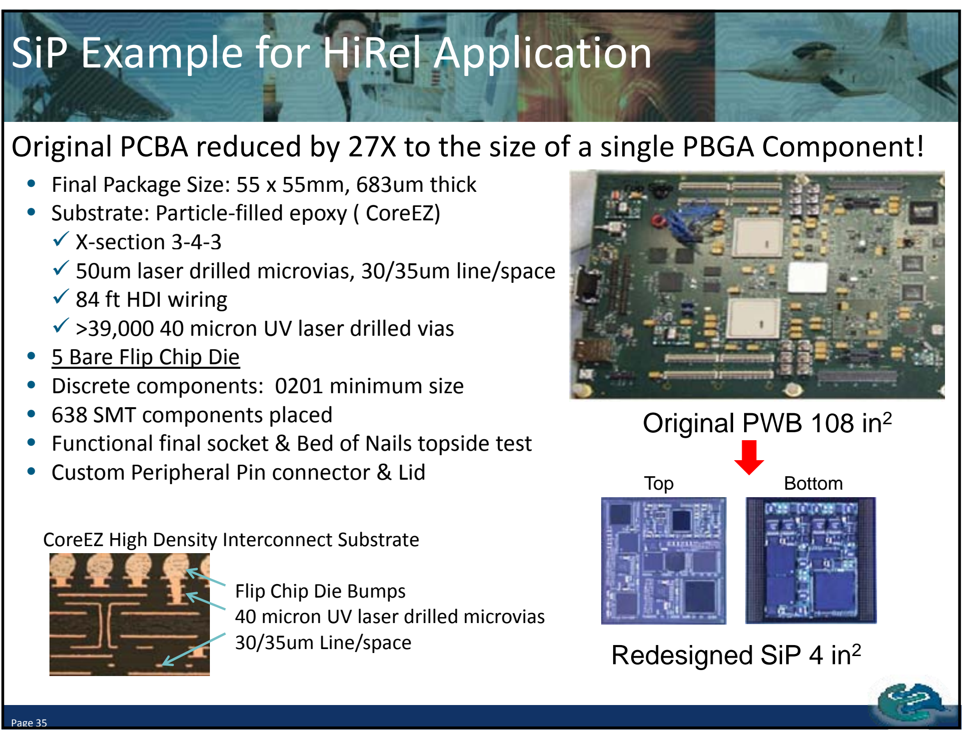
SiP Example for HiRel Application
Original PCBA reduced by 27X to the size of a single PBGA Component!
• Final Package Size: 55 x 55mm, 683um thick
• Substrate: Particle-filled epoxy (CoreEZ)
✓ X-section 3-4-3
✓ 50um laser drilled microvias, 30/35um line/space
✓ 84 ft HDI wiring
✓ >39,000 40 micron UV laser drilled vias
• 5 Bare Flip Chip Die
• Discrete components: 0201 minimum size
• 638 SMT components placed
• Functional final socket & Bed of Nails topside test
• Custom Peripheral Pin connector & Lid
CoreEZ High Density Interconnect Substrate
Flip Chip Die Bumps
40 micron UV laser drilled microvias
30/35um Line/space
Original PWB 108 in²
Top
Bottom
Redesigned SiP 4 in²
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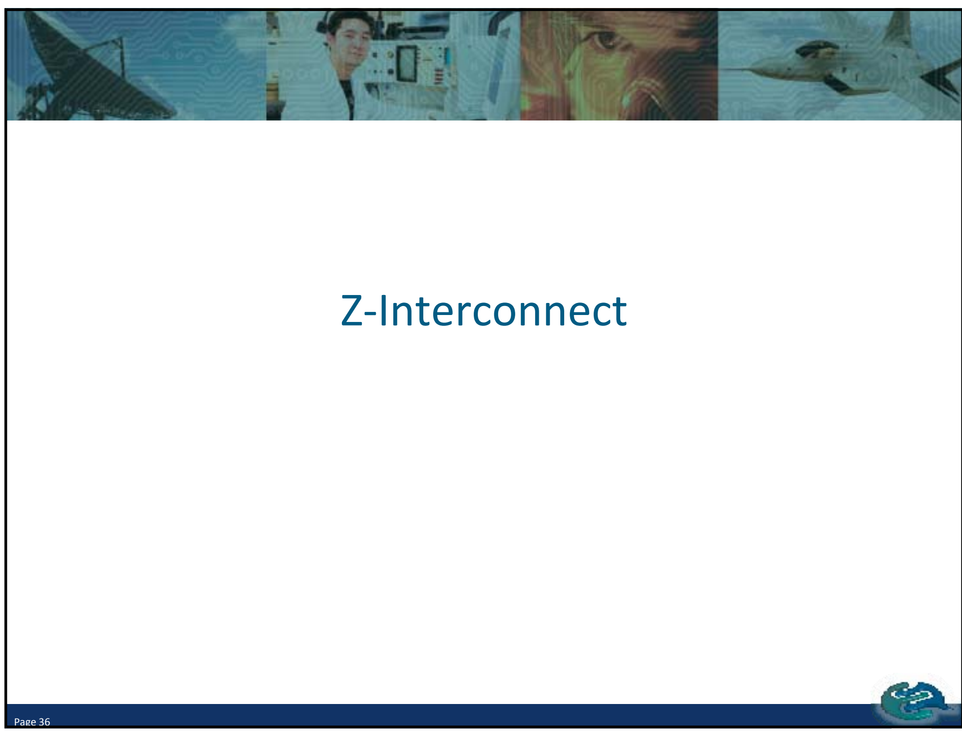
Z-Interconnect
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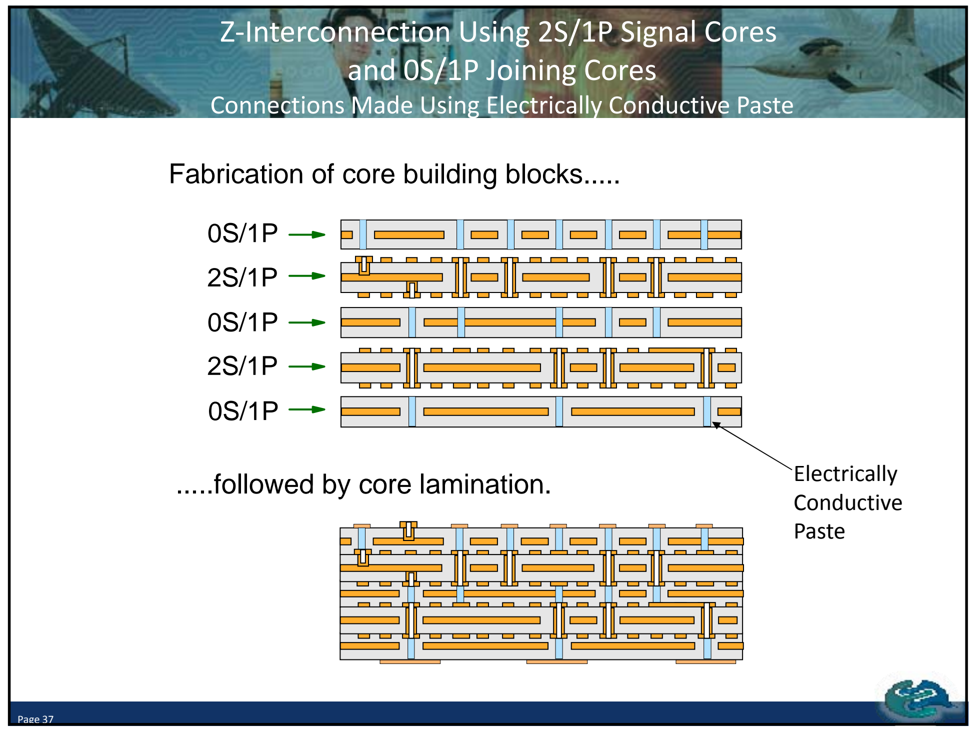
Z-Interconnection Using 2S/1P Signal Cores and 0S/1P Joining Cores
Connections Made Using Electrically Conductive Paste
Fabrication of core building blocks.....
0S/1P
2S/1P
0S/1P
2S/1P
0S/1P
.....followed by core lamination.
Electrically Conductive Paste
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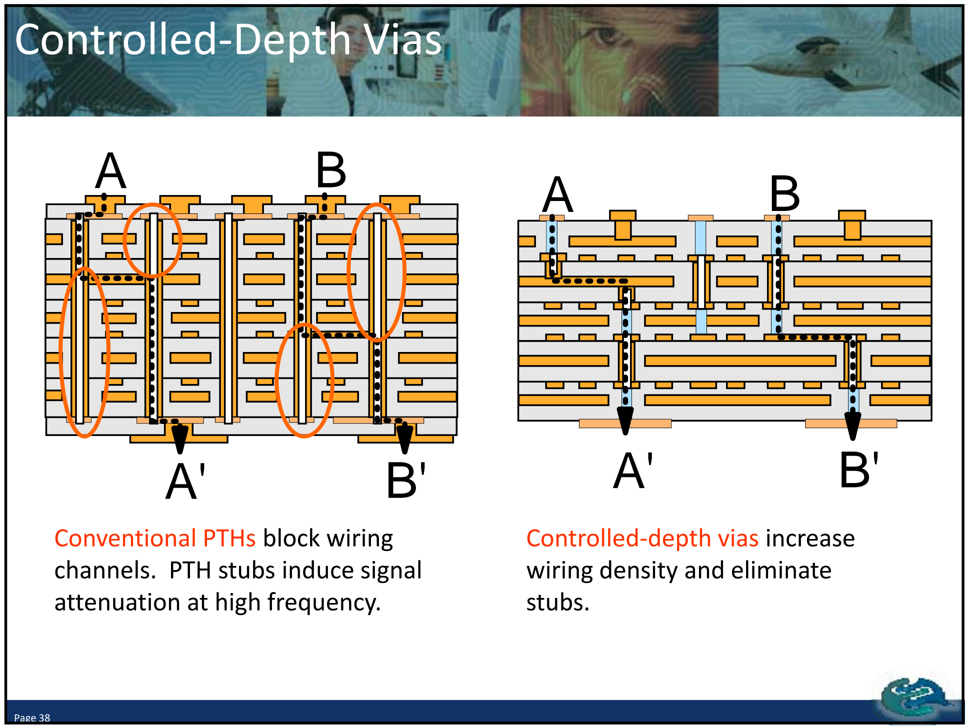
Controlled-Depth Vias
A
B
A'
B'
A
B
A'
B'
Conventional PTHs block wiring channels. PTH stubs induce signal attenuation at high frequency.
Controlled-depth vias increase wiring density and eliminate stubs.
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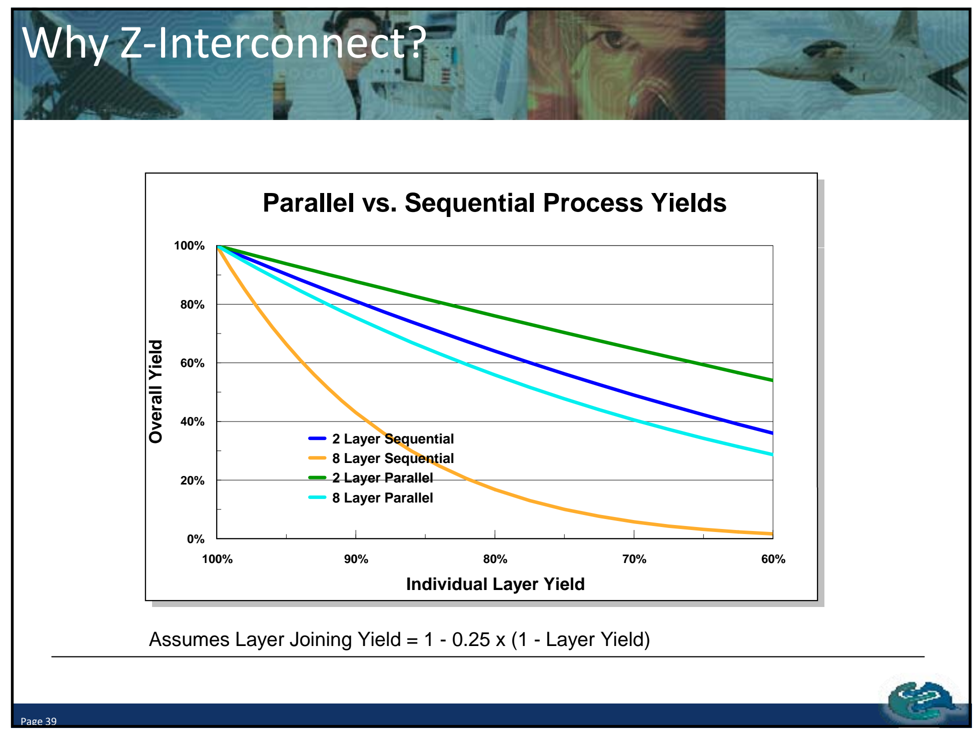
Why Z-Interconnect?
Parallel vs. Sequential Process Yields
Overall Yield
100%
80%
60%
40%
20%
0%
2 Layer Sequential
8 Layer Sequential
2 Layer Parallel
8 Layer Parallel
100%
90%
80%
70%
60%
Individual Layer Yield
Assumes Layer Joining Yield = 1 - 0.25 x (1 - Layer Yield)
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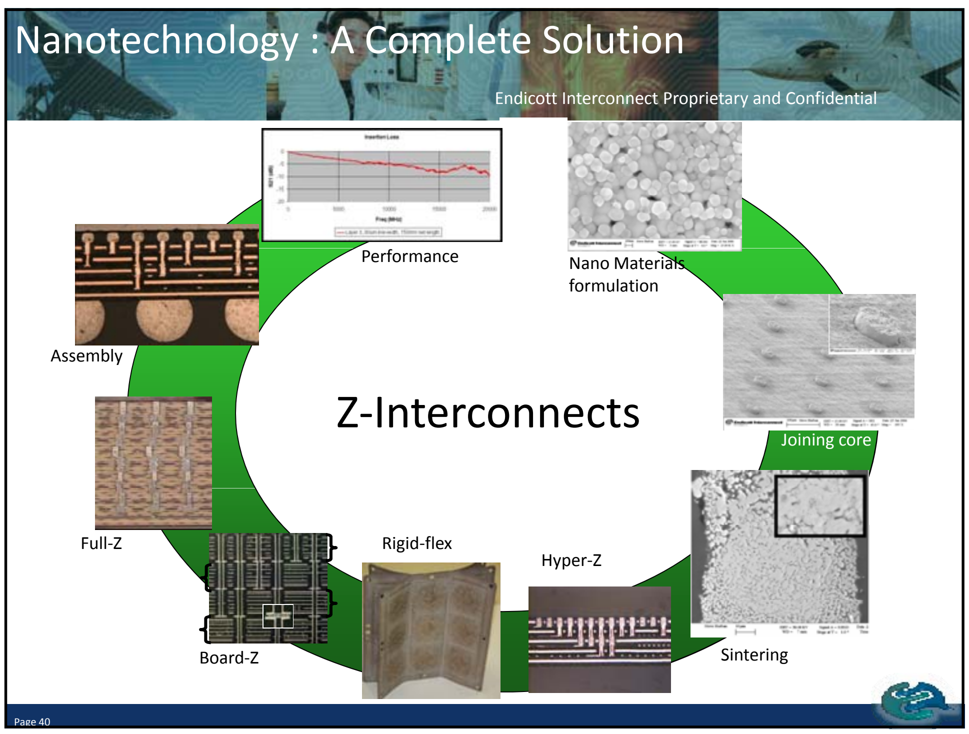
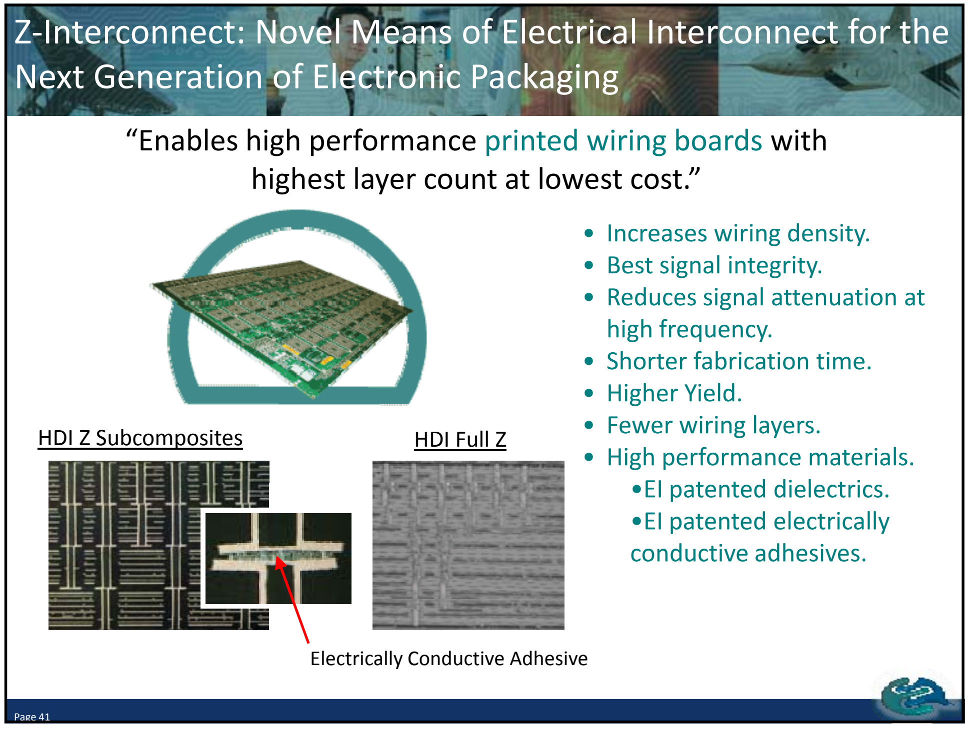
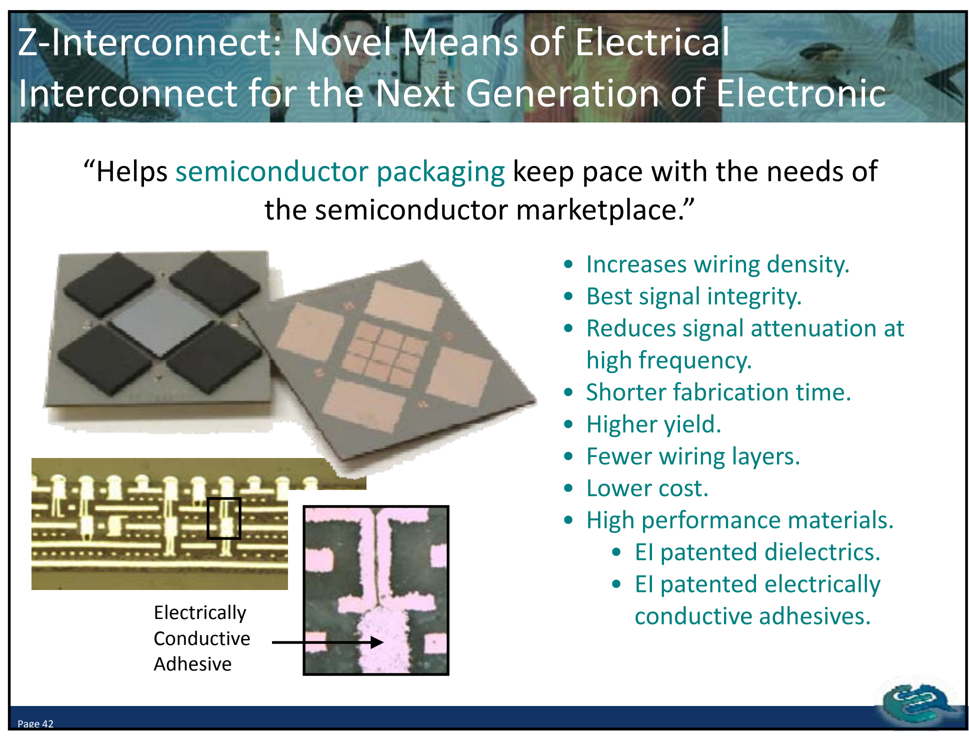
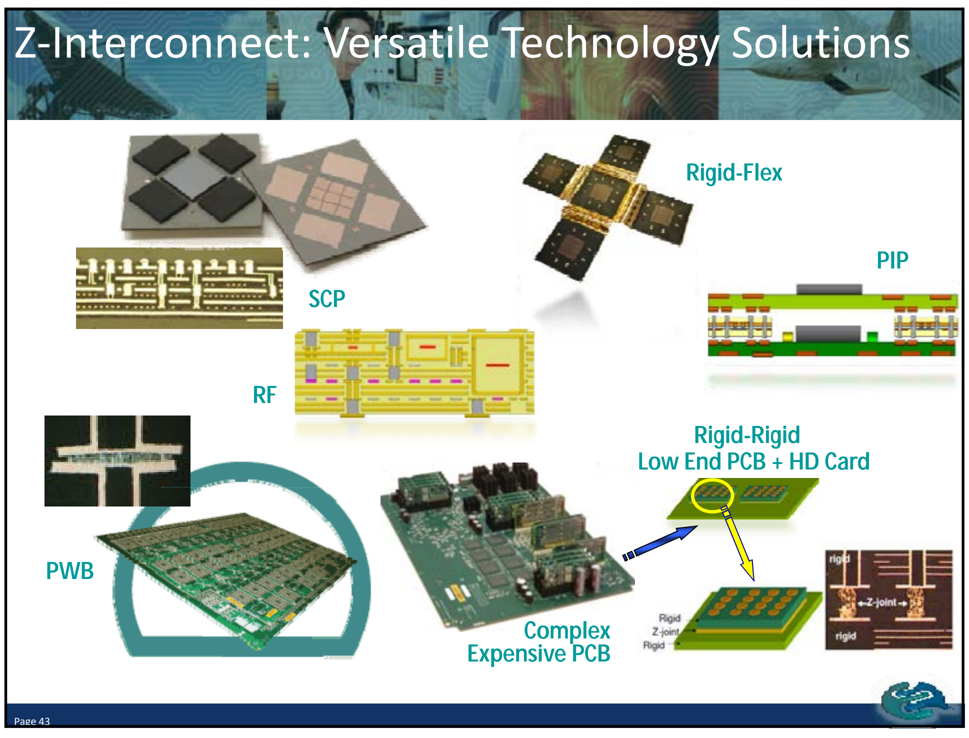
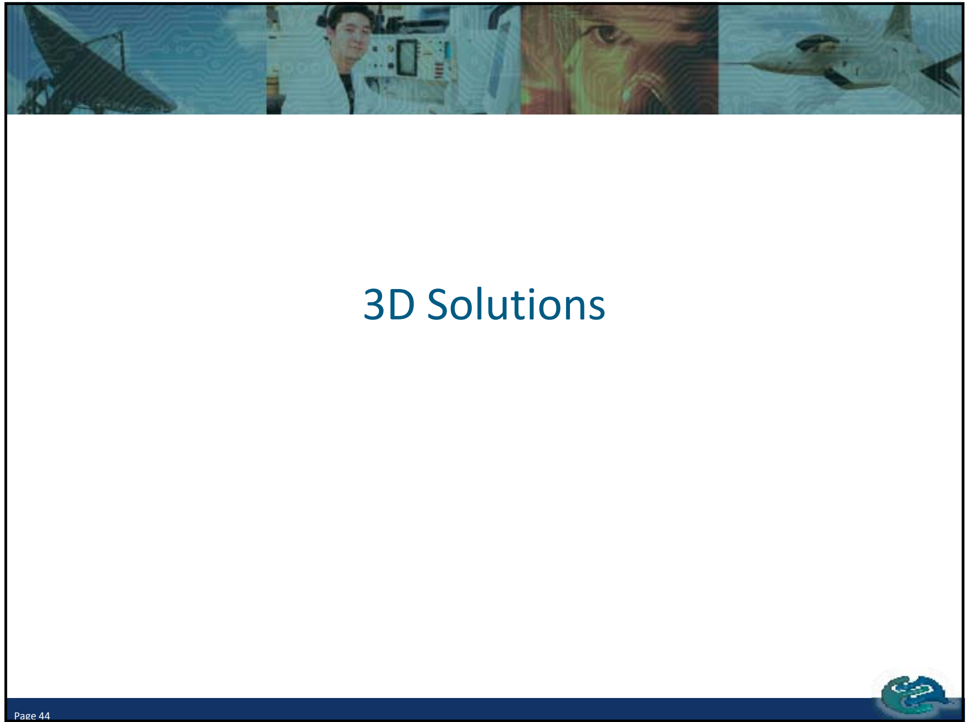
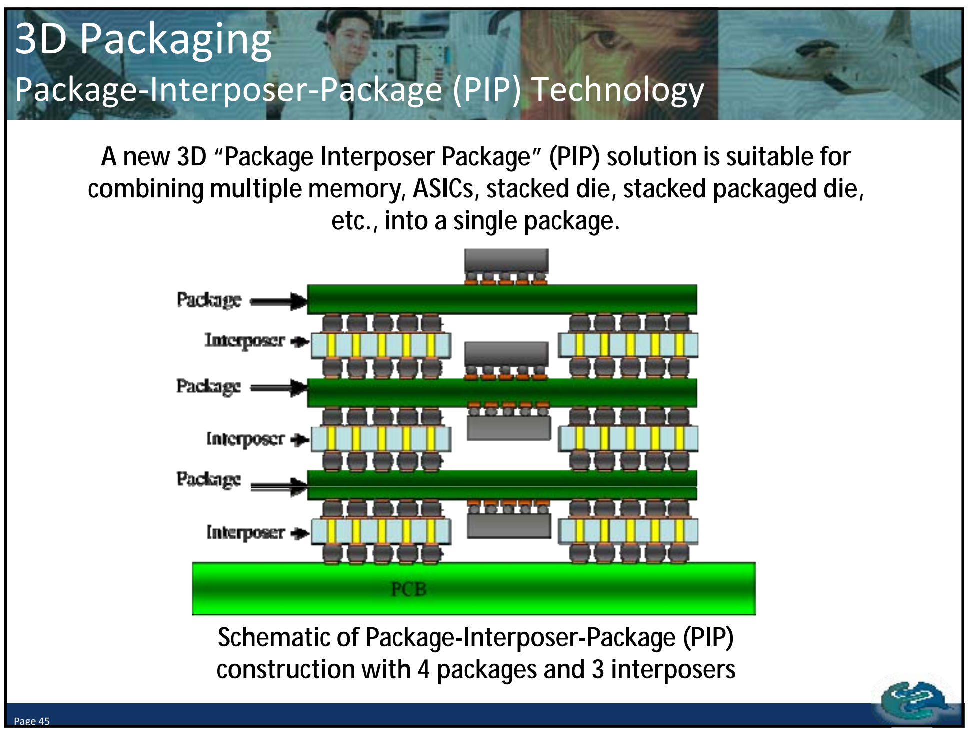

Nanotechnology : A Complete Solution
Endicott Interconnect Proprietary and Confidential
Performance
Nano Materials formulation
Assembly
Z-Interconnects
Joining core
Full-Z
Rigid-flex
Hyper-Z
Board-Z
Sintering
Page 40


Z-Interconnect: Novel Means of Electrical Interconnect for the Next Generation of Electronic Packaging
"Enables high performance printed wiring boards with highest layer count at lowest cost."
HDI Z Subcomposites
HDI Full Z
Electrically Conductive Adhesive
• Increases wiring density.
• Best signal integrity.
• Reduces signal attenuation at high frequency.
• Shorter fabrication time.
• Higher Yield.
• Fewer wiring layers.
• High performance materials.
•EI patented dielectrics.
•EI patented electrically conductive adhesives.
Page 41

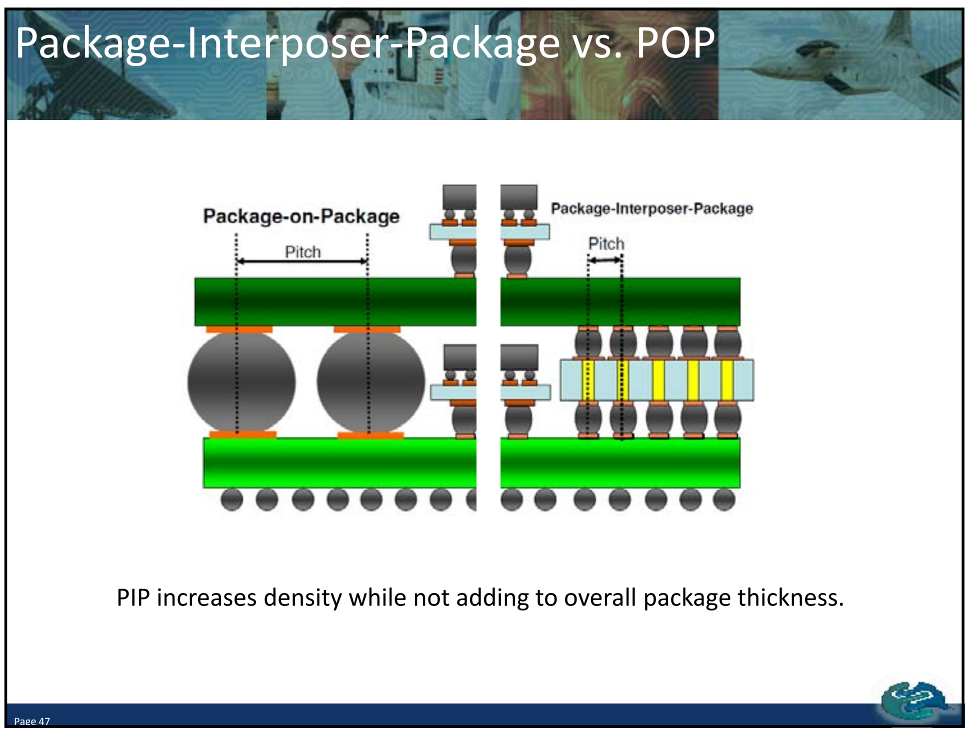

Z-Interconnect: Novel Means of Electrical Interconnect for the Next Generation of Electronic
"Helps semiconductor packaging keep pace with the needs of the semiconductor marketplace."
Electrically Conductive Adhesive
• Increases wiring density.
• Best signal integrity.
• Reduces signal attenuation at high frequency.
• Shorter fabrication time.
• Higher yield.
• Fewer wiring layers.
• Lower cost.
• High performance materials.
• EI patented dielectrics.
• EI patented electrically conductive adhesives.
Page 42

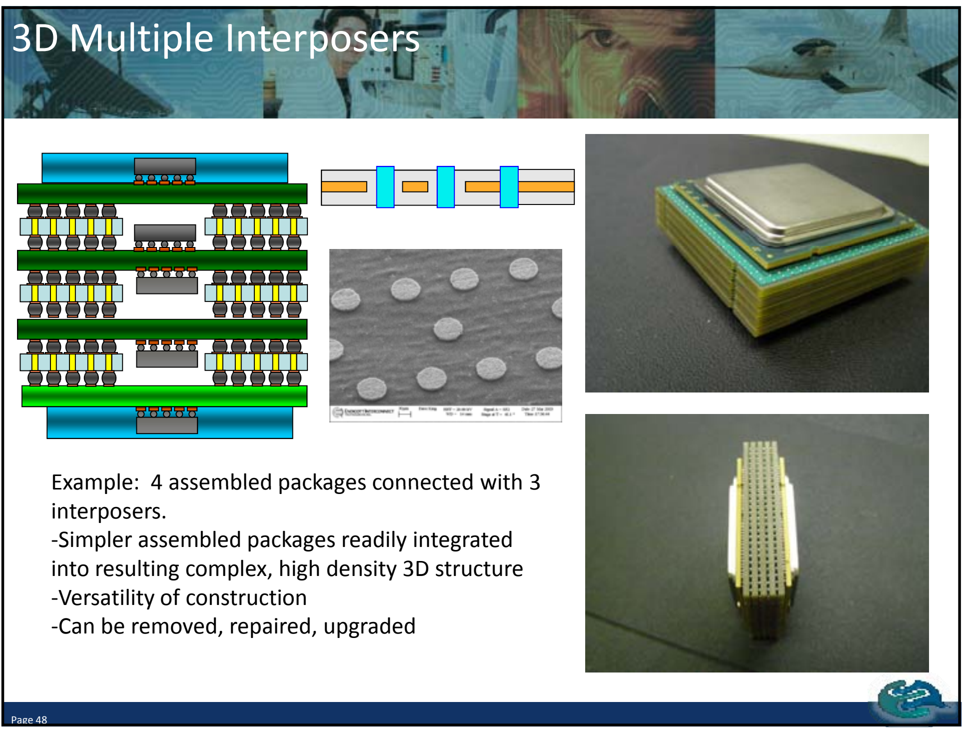

Z-Interconnect: Versatile Technology Solutions
Rigid-Flex
PIP
SCP
RF
Rigid-Rigid
Low End PCB + HD Card
PWB
Complex
Expensive PCB
Page 43

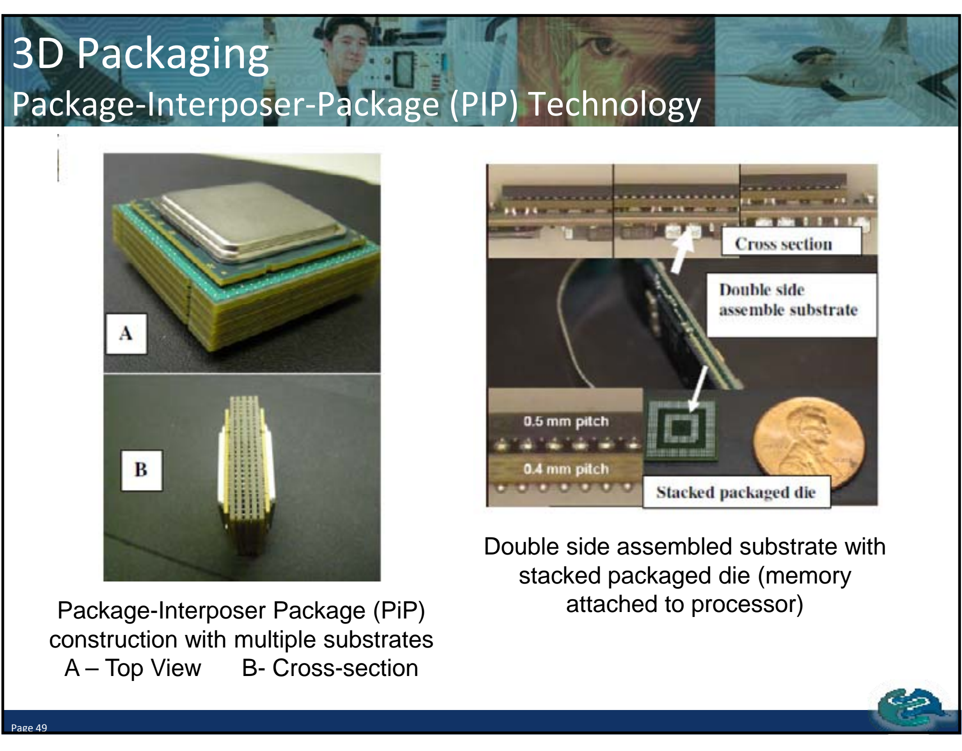

3D Solutions
Page 44

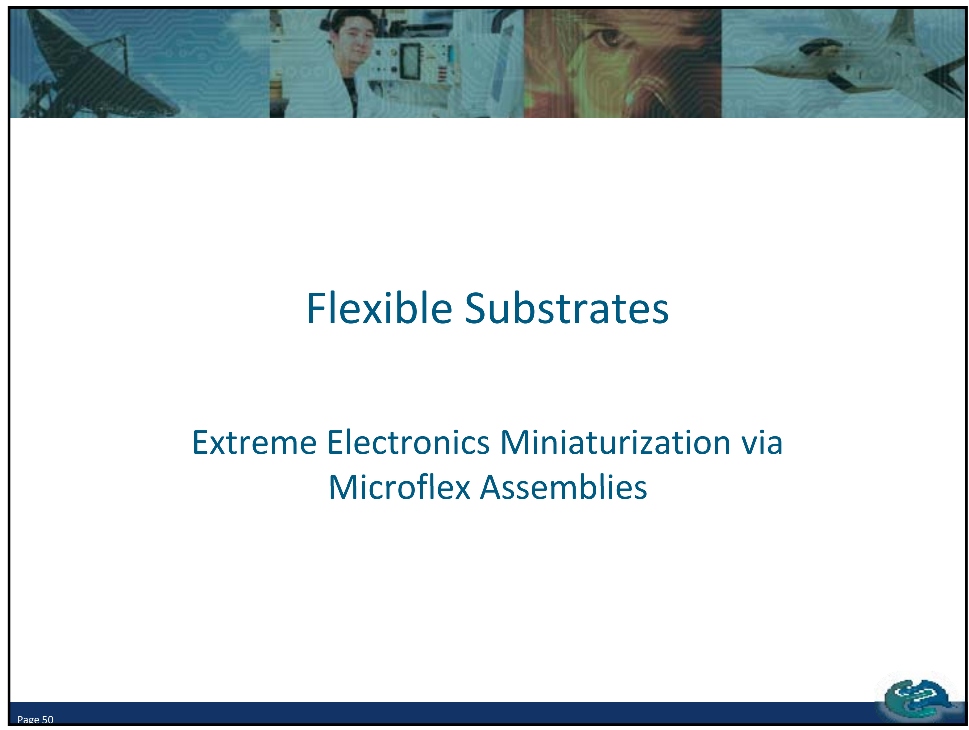

3D Packaging
Package-Interposer-Package (PIP) Technology
A new 3D "Package Interposer Package" (PIP) solution is suitable for combining multiple memory, ASICs, stacked die, stacked packaged die, etc., into a single package.
Package
Interposer
Package
Interposer
Package
Interposer
PCB
Schematic of Package-Interposer-Package (PIP) construction with 4 packages and 3 interposers
Page 45

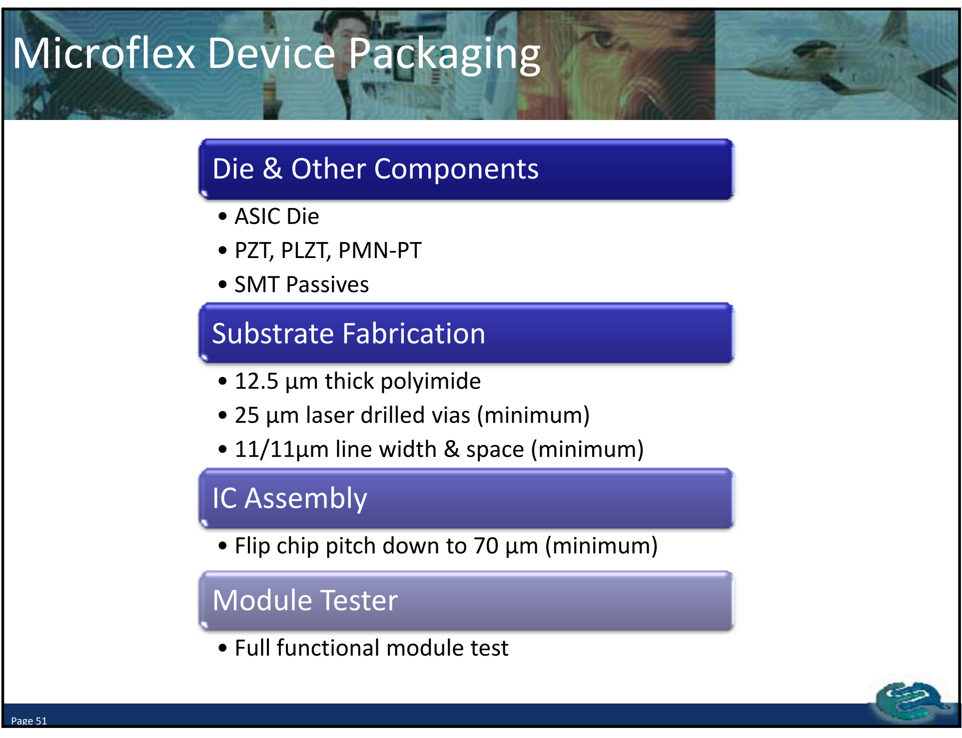
3D Packaging
Package-Interposer-Package (PIP) Technology
Benefits of Package-Interposer-Package
High density, small pitch
Re-workable and replaceable
Polymer or ceramic interposer provides additional support for improving stability and reliability
PIP will experience less warpage and thermal stress
Mitigates problems with coplanarity between packages
Interposer Options:
Dielectric material
Embedded passives
Embedded actives
Page 46


Package-Interposer-Package vs. POP
Package-on-Package
Pitch
Package-Interposer-Package
Pitch
PIP increases density while not adding to overall package thickness.
Page 47

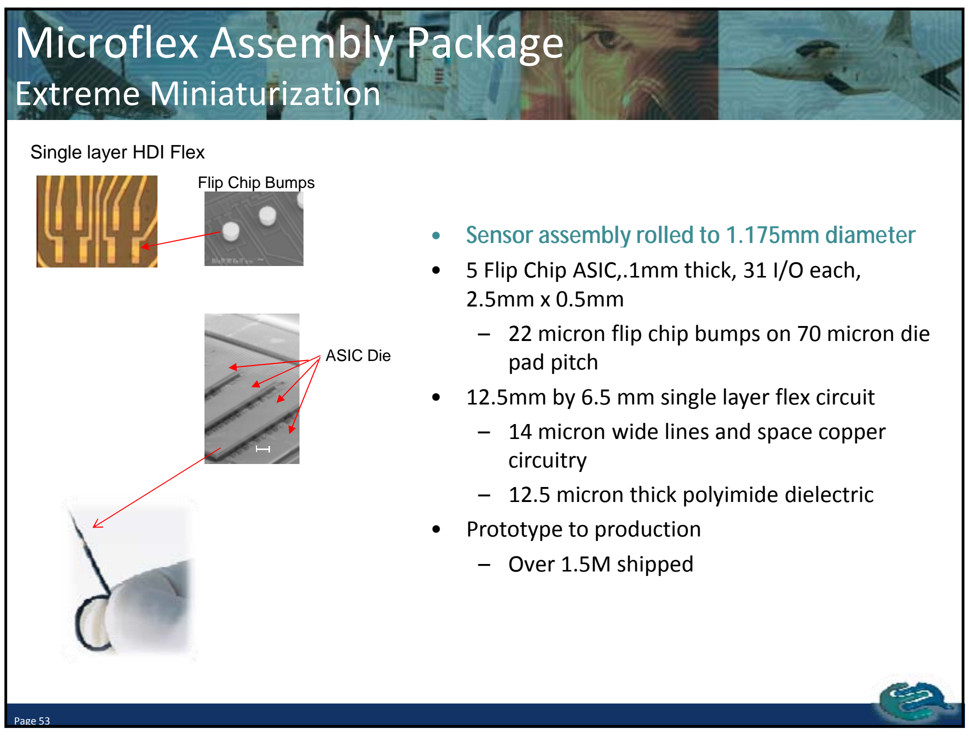

3D Multiple Interposers
Example: 4 assembled packages connected with 3 interposers.
-Simpler assembled packages readily integrated into resulting complex, high density 3D structure
-Versatility of construction
-Can be removed, repaired, upgraded
Page 48

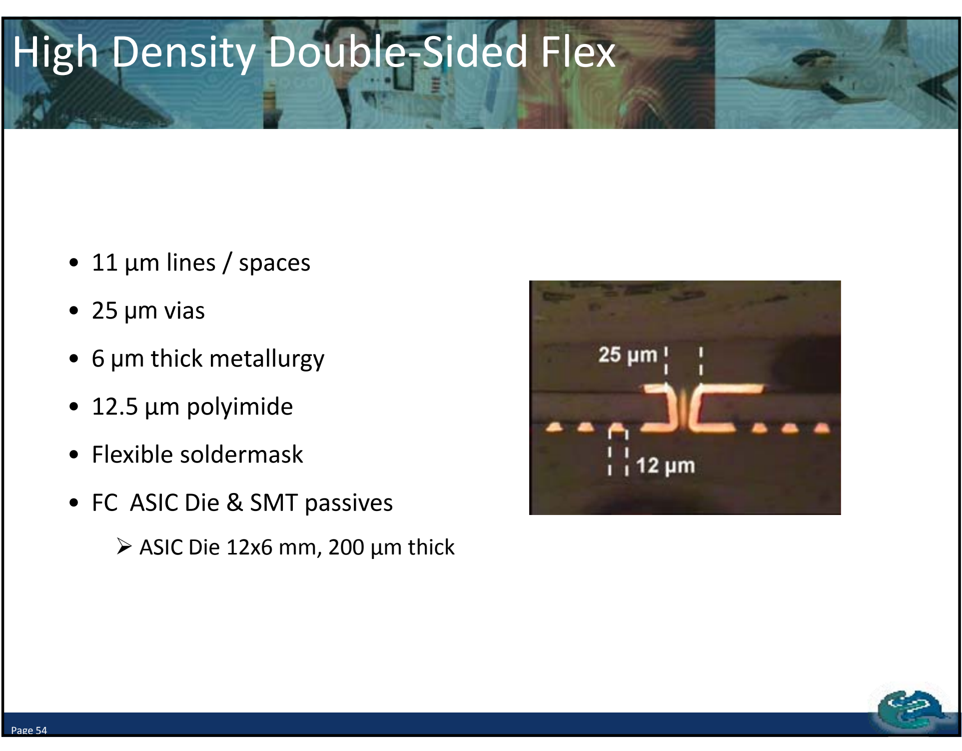

3D Packaging
Package-Interposer-Package (PIP) Technology
A
B
Cross section
Double side assemble substrate
0.5 mm pitch
0.4 mm pitch
Stacked packaged die
Package-Interposer Package (PiP) construction with multiple substrates
A – Top View B- Cross-section
Double side assembled substrate with stacked packaged die (memory attached to processor)
Page 49

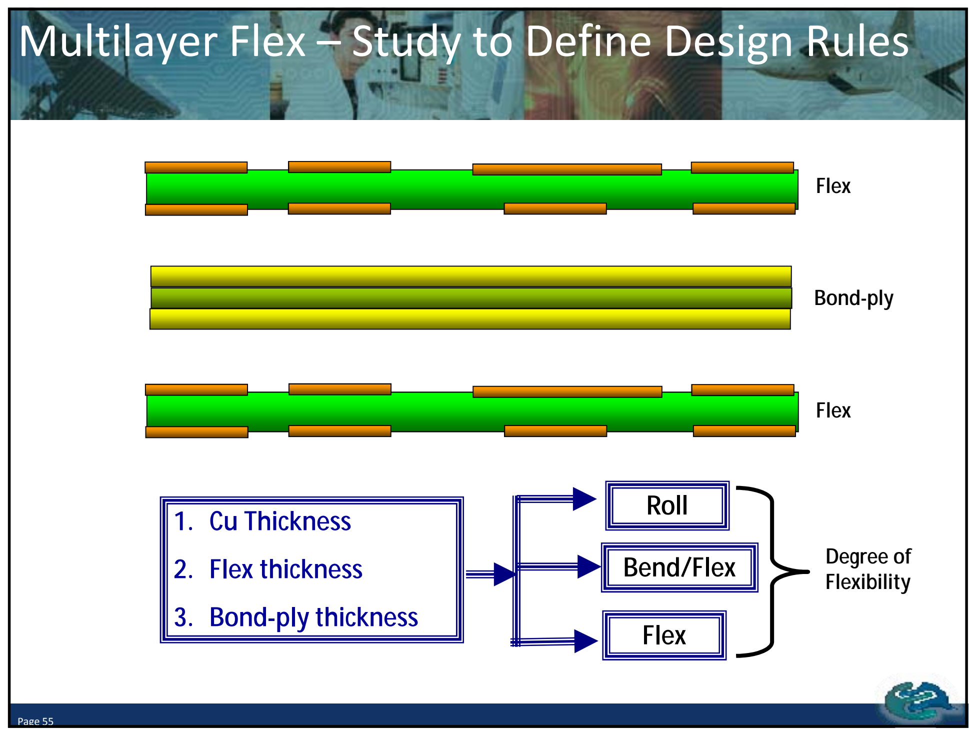

Flexible Substrates
Extreme Electronics Miniaturization via Microflex Assemblies
Page 50

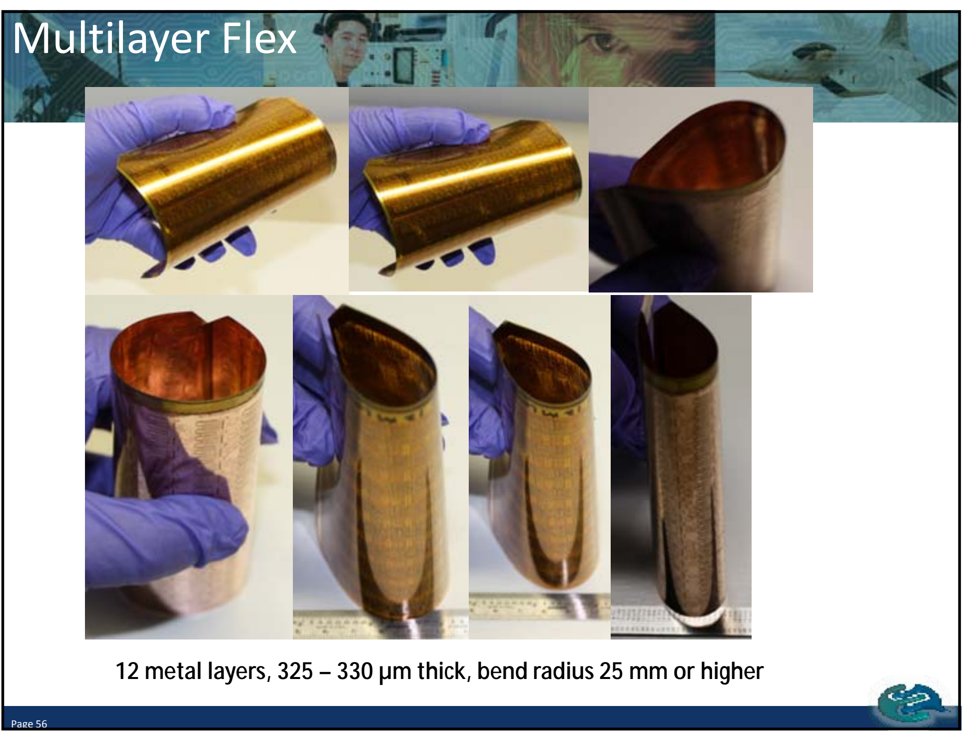

Microflex Device Packaging
Die & Other Components
• ASIC Die
• PZT, PLZT, PMN-PT
• SMT Passives
Substrate Fabrication
• 12.5 µm thick polyimide
• 25 µm laser drilled vias (minimum)
• 11/11µm line width & space (minimum)
IC Assembly
• Flip chip pitch down to 70 µm (minimum)
Module Tester
• Full functional module test
Page 51

Micro Pillar Technology for Finer Pitch Applications
Acc.V Spot Magn Det WD 20 µm
25.00 kV 6.0 750x NONE 7.5 0.4 Torr
ASIC die with 70 µm bonding pad pitch, 22 µm diameter pillar
Page 52

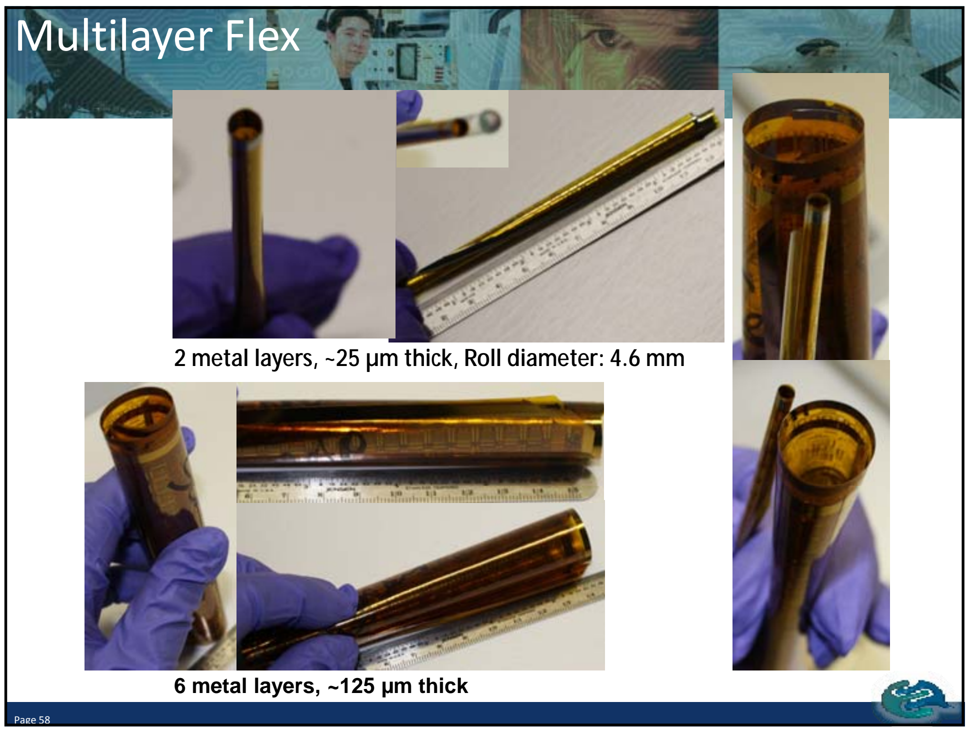

Microflex Assembly Package
Extreme Miniaturization
Single layer HDI Flex
Flip Chip Bumps
ASIC Die
Sensor assembly rolled to 1.175mm diameter
5 Flip Chip ASIC,.1mm thick, 31 I/O each, 2.5mm x 0.5mm
22 micron flip chip bumps on 70 micron die pad pitch
12.5mm by 6.5 mm single layer flex circuit
14 micron wide lines and space copper circuitry
12.5 micron thick polyimide dielectric
Prototype to production
Over 1.5M shipped
Page 53

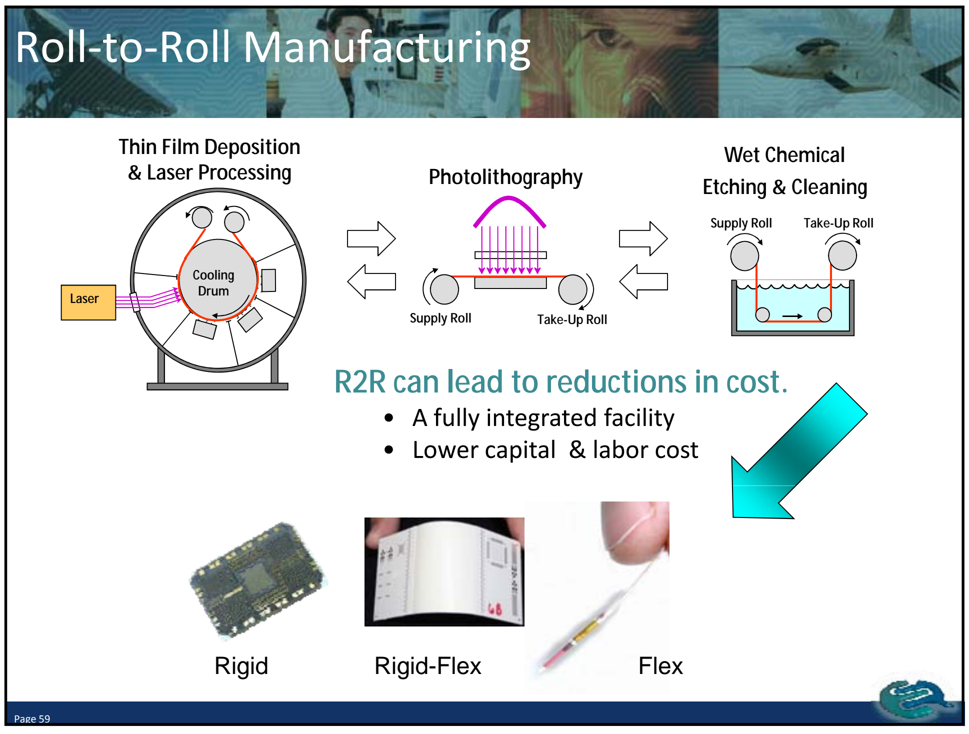

High Density Double-Sided Flex
11 µm lines / spaces
25 µm vias
6 µm thick metallurgy
12.5 µm polyimide
Flexible soldermask
FC ASIC Die & SMT passives
ASIC Die 12x6 mm, 200 µm thick
25 µm
12 µm
Page 54


Multilayer Flex – Study to Define Design Rules
Flex
Bond-ply
Flex
1. Cu Thickness
2. Flex thickness
3. Bond-ply thickness
Roll
Bend/Flex
Flex
Degree of Flexibility
Page 55

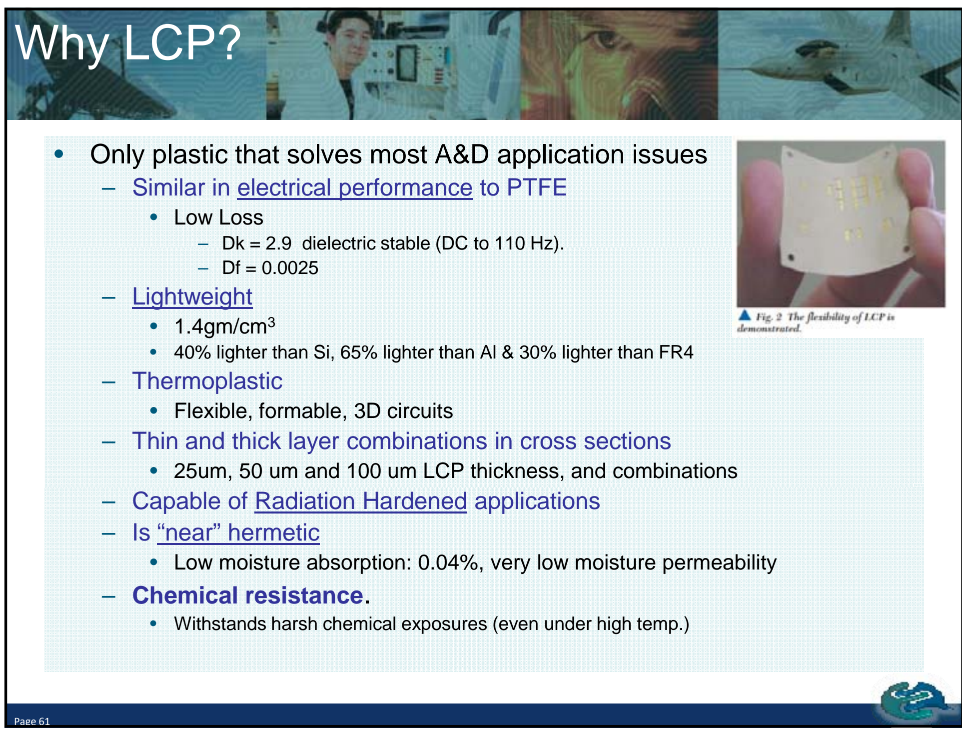

Multilayer Flex
12 metal layers, 325 – 330 µm thick, bend radius 25 mm or higher
Page 56

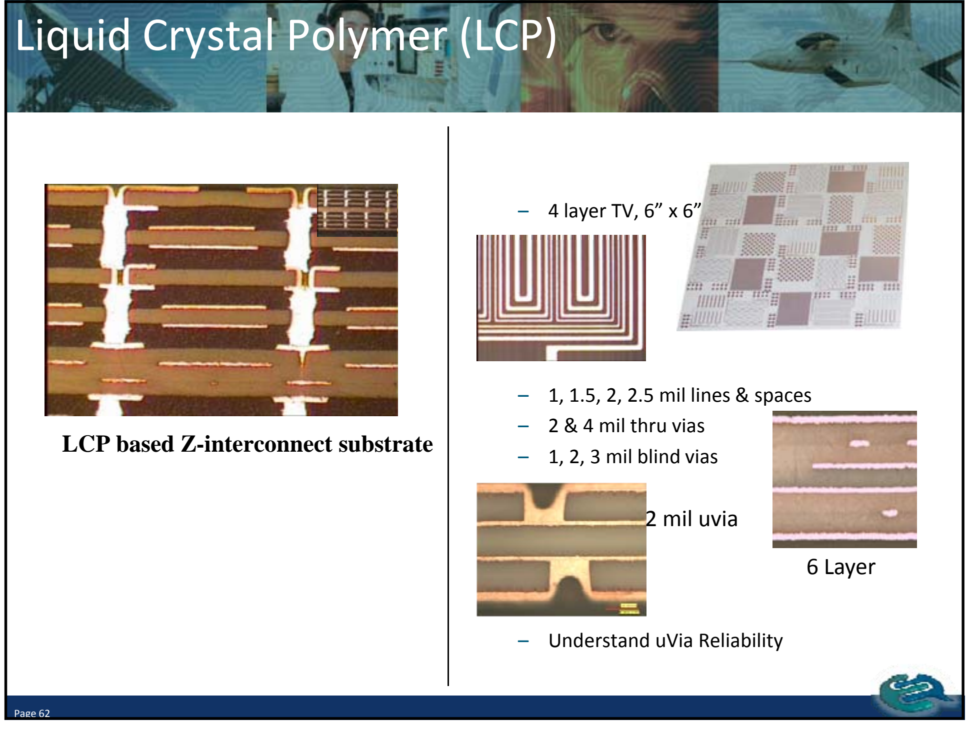
Multilayer Flex
12 metal layers, 190 μm thick, bend radius 25 mm or less
Page 57

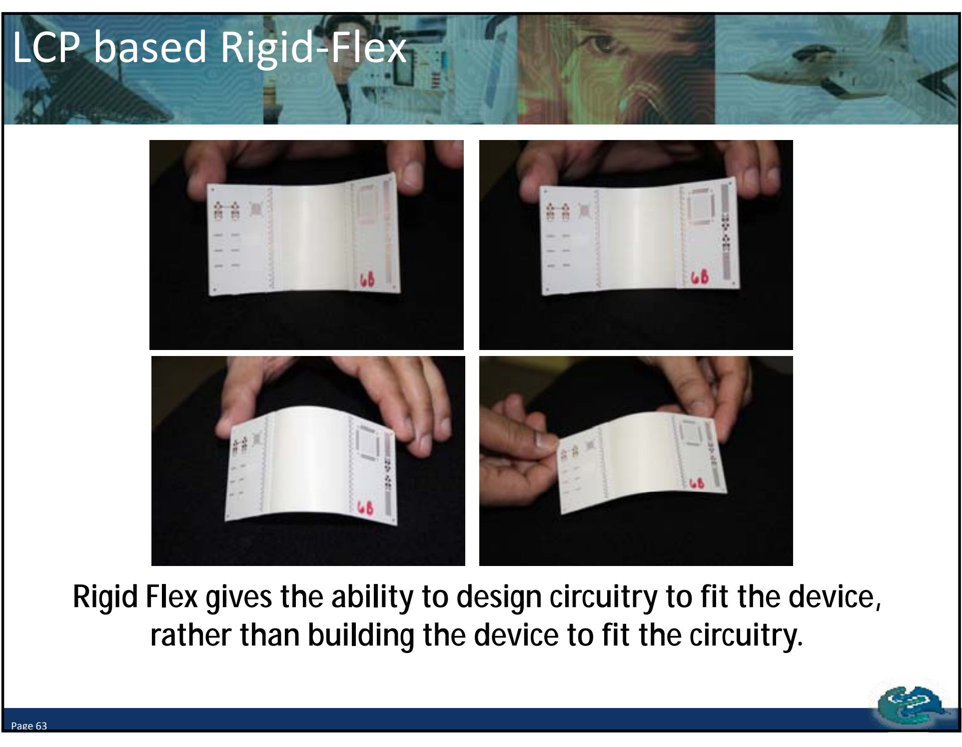

Multilayer Flex
2 metal layers, ~25 μm thick, Roll diameter: 4.6 mm
6 metal layers, ~125 μm thick
Page 58


Roll-to-Roll Manufacturing
Thin Film Deposition
& Laser Processing
Cooling Drum
Laser
Photolithography
Supply Roll
Take-Up Roll
Wet Chemical
Etching & Cleaning
Supply Roll
Take-Up Roll
R2R can lead to reductions in cost.
• A fully integrated facility
• Lower capital & labor cost
Rigid
Rigid-Flex
Flex
Page 59

New Substrate Technologies
Liquid Crystal Polymer (LCP)
Page 60

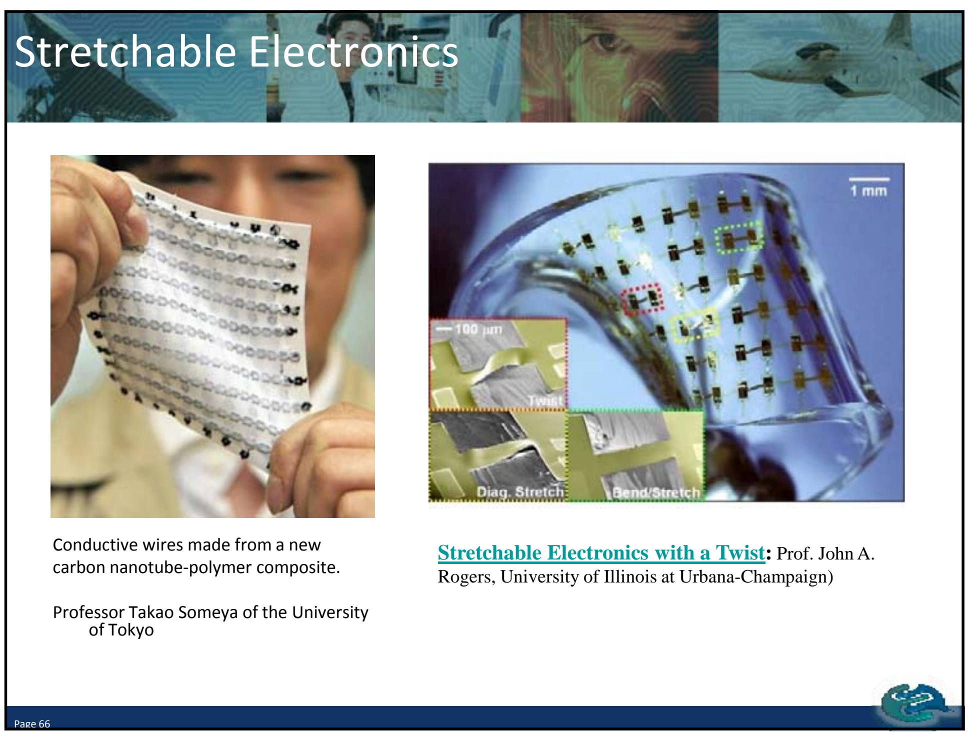

Why LCP?
• Only plastic that solves most A&D application issues
– Similar in electrical performance to PTFE
• Low Loss
– Dk = 2.9 dielectric stable (DC to 110 Hz).
– Df = 0.0025
– Lightweight
• 1.4gm/cm3
• 40% lighter than Si, 65% lighter than Al & 30% lighter than FR4
– Thermoplastic
• Flexible, formable, 3D circuits
– Thin and thick layer combinations in cross sections
• 25um, 50 um and 100 um LCP thickness, and combinations
– Capable of Radiation Hardened applications
– Is "near" hermetic
• Low moisture absorption: 0.04%, very low moisture permeability
– Chemical resistance.
• Withstands harsh chemical exposures (even under high temp.)
Fig. 2 The flexibility of LCP is demonstrated.
Page 61

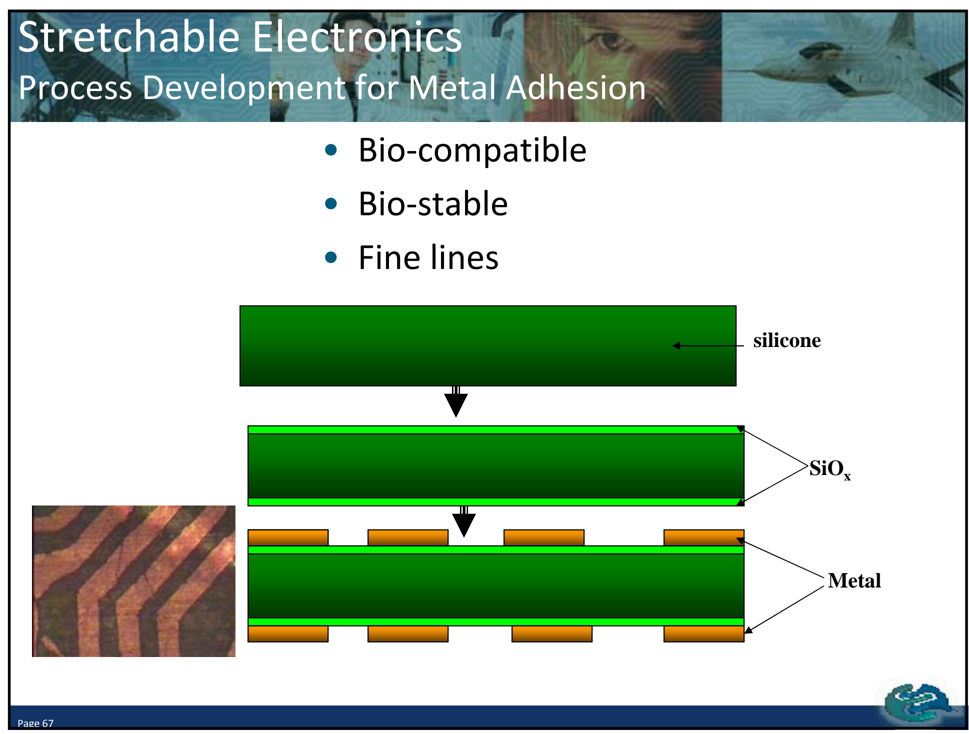

Liquid Crystal Polymer (LCP)
LCP based Z-interconnect substrate
– 4 layer TV, 6" x 6"
– 1, 1.5, 2, 2.5 mil lines & spaces
– 2 & 4 mil thru vias
– 1, 2, 3 mil blind vias
2 mil uvia
6 Layer
– Understand uVia Reliability
Page 62

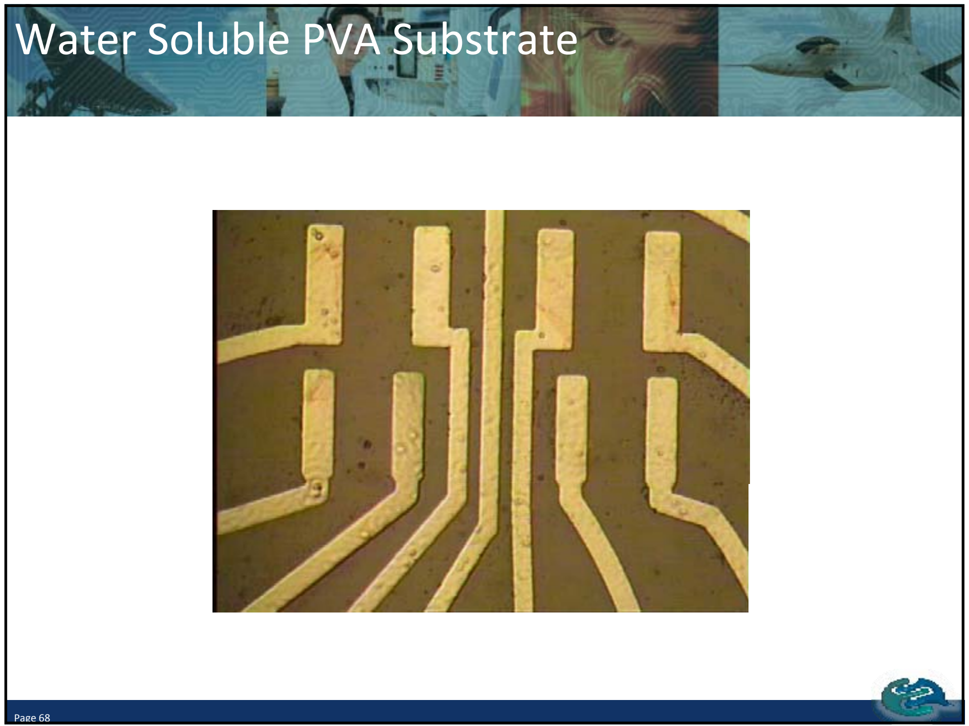

LCP based Rigid-Flex
Rigid Flex gives the ability to design circuitry to fit the device, rather than building the device to fit the circuitry.
Page 63

Stretchable Substrates
Conformable Electronics
Page 64

Silicones
Polydimethylsiloxane (PDMS)
Medicals
Nano composites
Random lasers
Electromechanical actuators
Silicones
Microfluidics
Microbe-resistant household products
Thermal interface materials
Marine coatings
Magnetic
Page 65


Stretchable Electronics
1 mm
100 μm
Twist
Diag. Stretch
Bend/Stretch
Conductive wires made from a new carbon nanotube-polymer composite.
Professor Takao Someya of the University of Tokyo
Stretchable Electronics with a Twist: Prof. John A. Rogers, University of Illinois at Urbana-Champaign)
Page 66


Stretchable Electronics
Process Development for Metal Adhesion
Bio-compatible
Bio-stable
Fine lines
silicone
SiOx
Metal
Page 67


Water Soluble PVA Substrate
Page 68

Advanced Electronics Packaging for A&D, industrial and medical applications is driving the need for novel substrate materials, ultra high density assemblies and unique form factors.

Substrate materials and construction are key to overall package performance and reliability.

Thank you for your attention!

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