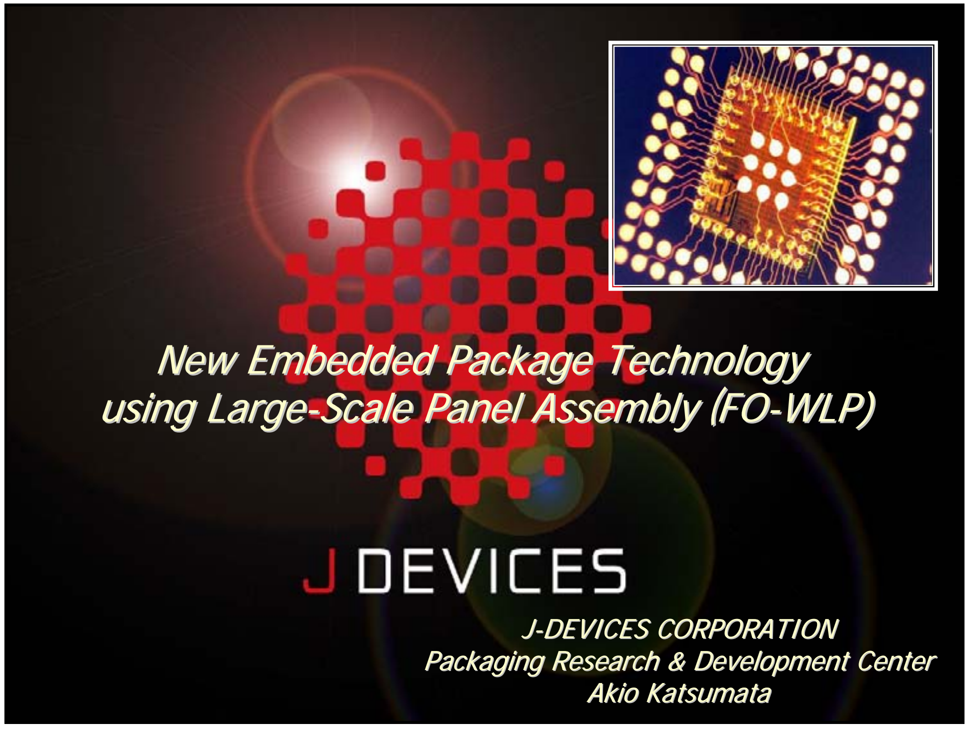
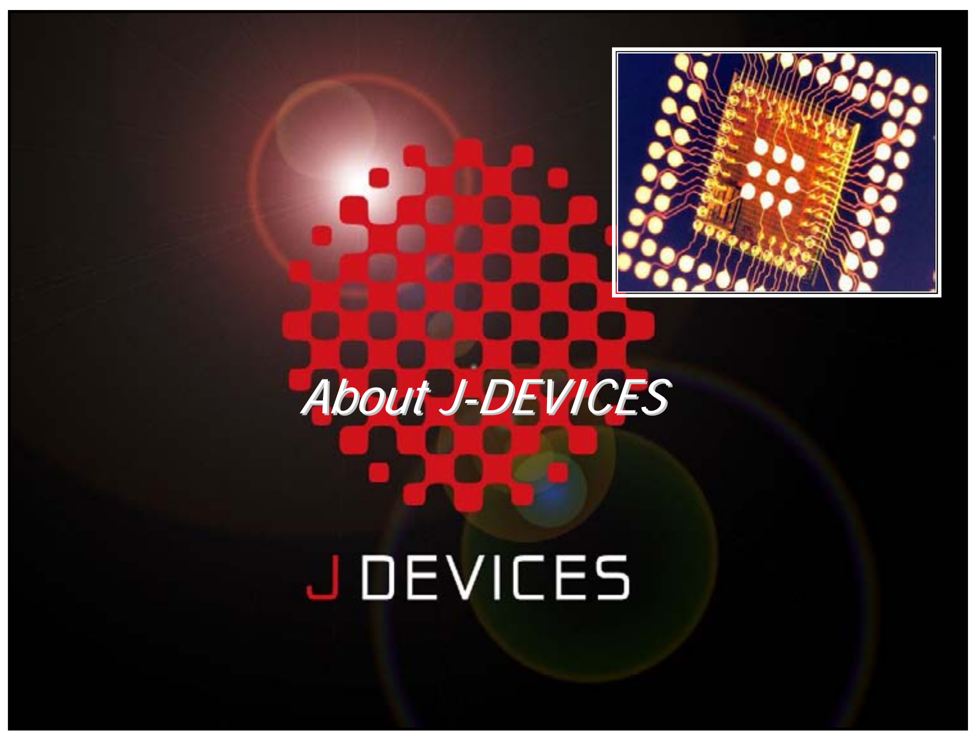

New Embedded Package Technology
using Large-Scale Panel Assembly (FO-WLP)
J DEVICES
J-DEVICES CORPORATION
Packaging Research & Development Center
Akio Katsumata


About J-DEVICES
J DEVICES

About J-DEVICES

Foundation
- Established with capital from NAKAYA Micro Devices, Amkor and Toshiba in 2009.
- Merged Fujitsu Semiconductor's assembly and test division (FIM) in 2012.
- Will merge Renesas three assembly and test factories in 2013.

Goal
- To become one of the leading global companies in the semiconductor backend business.

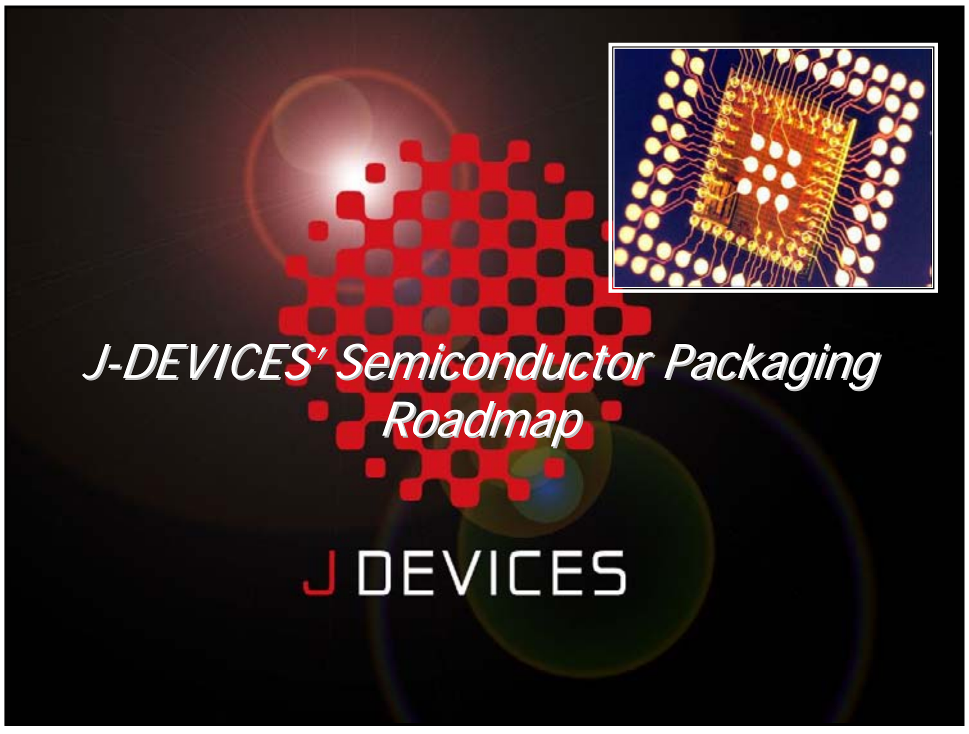
Focus
- R&D is focused on developing new connecting technologies and has the experience to manufacture using new connecting technologies.
  ex. Three years experience with 40um bump pitch CoC manufacturing.
- Automotive product experience

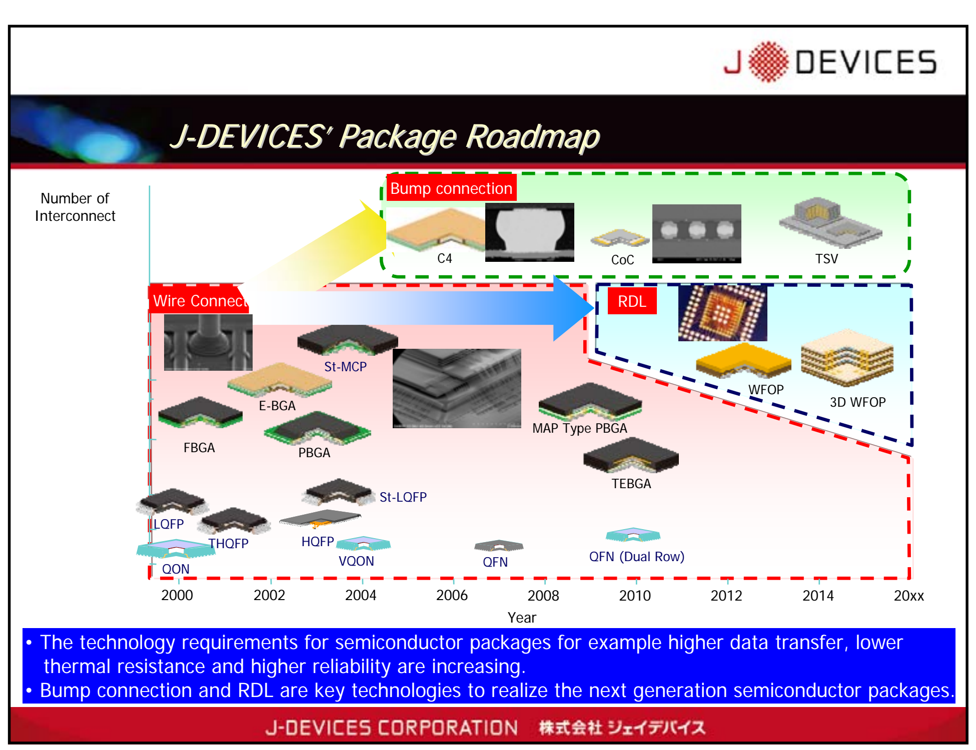
J-DEVICES CORPORATION 株式会社 ジェイデバイス

Contents

1. J-DEVICES' Semiconductor Packaging Roadmap
2. FO-WLP Market Trend & J-DEVICES' Development Concept
3. WFOP Characteristics & Reliability
4. Design Rule
5. Target Applications & Roadmap
6. Conclusion

J DEVICES


J-DEVICES' Semiconductor Packaging Roadmap
J DEVICES


J DEVICES
J-DEVICES' Package Roadmap
Number of Interconnect
Bump connection
C4
CoC
TSV
Wire Connect
RDL
WFOP
3D WFOP
St-MCP
E-BGA
FBGA
PBGA
MAP Type PBGA
TEBGA
St-LQFP
LQFP
THQFP
HQFP
QON
VQON
QFN
QFN (Dual Row)
2000
2002
2004
2006
2008
2010
2012
2014
20xx
Year
• The technology requirements for semiconductor packages for example higher data transfer, lower thermal resistance and higher reliability are increasing.
• Bump connection and RDL are key technologies to realize the next generation semiconductor packages.
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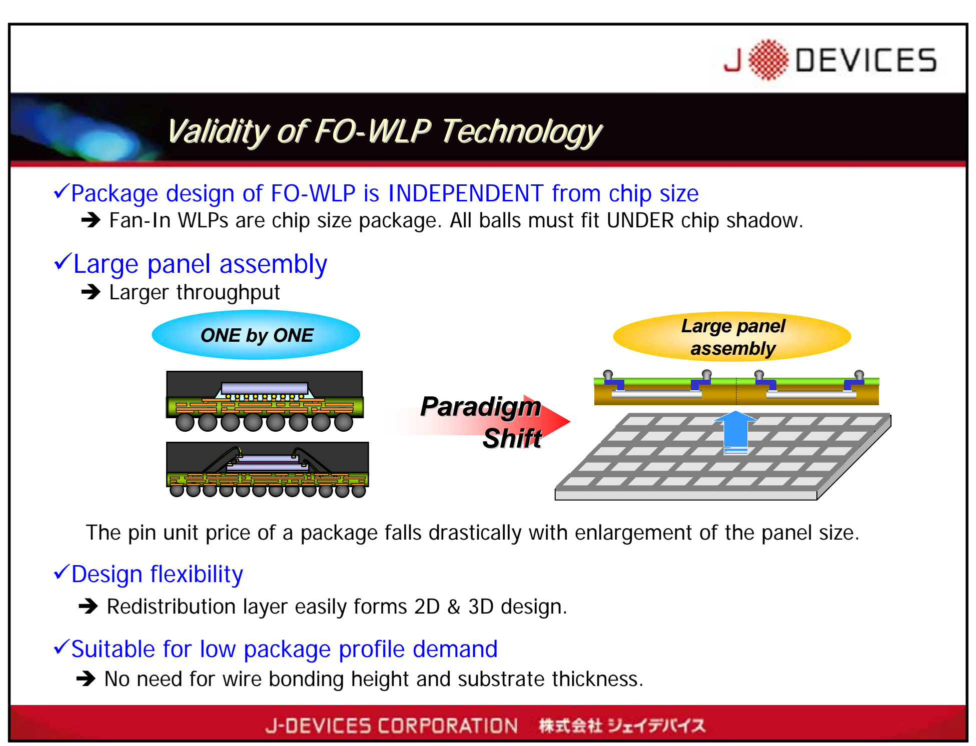
FO-WLP Market Trend & J-DEVICES'
Development Concept
J DEVICES


J DEVICES
Validity of FO-WLP Technology
✓Package design of FO-WLP is INDEPENDENT from chip size
➔ Fan-In WLPs are chip size package. All balls must fit UNDER chip shadow.
✓Large panel assembly
➔ Larger throughput
ONE by ONE
Paradigm Shift
Large panel assembly
The pin unit price of a package falls drastically with enlargement of the panel size.
✓Design flexibility
➔ Redistribution layer easily forms 2D & 3D design.
✓Suitable for low package profile demand
➔ No need for wire bonding height and substrate thickness.
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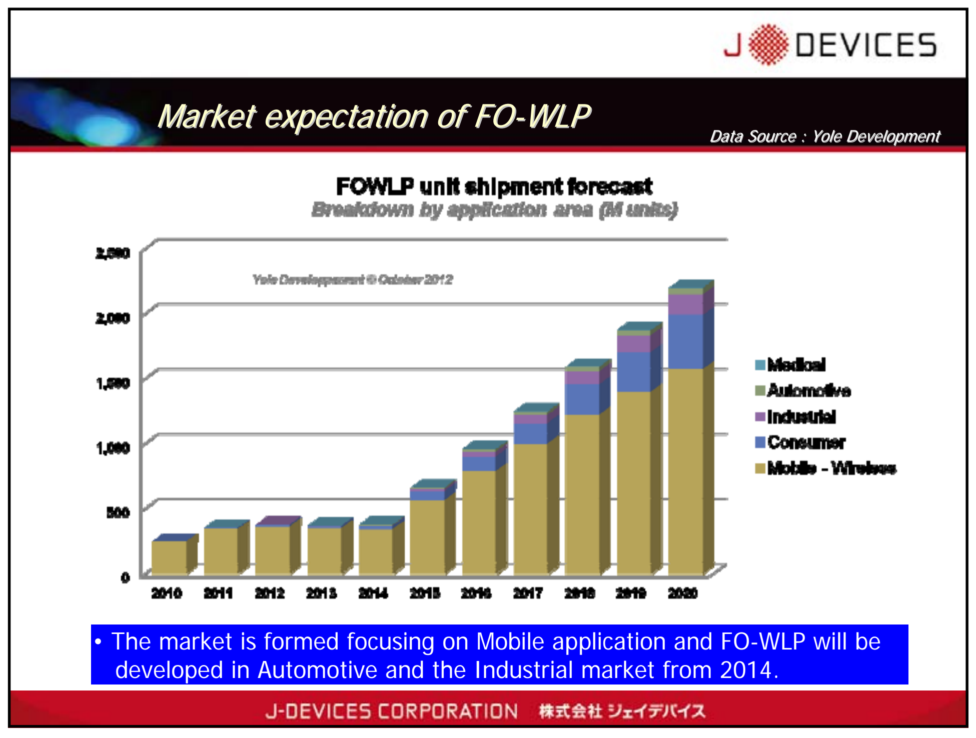
J DEVICES
Market expectation of FO-WLP
Data Source : Yole Development
FOWLP unit shipment forecast
Breakdown by application area (M units)
Medical
Automotive
Industrial
Consumer
Mobile - Wireless
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
• The market is formed focusing on Mobile application and FO-WLP will be developed in Automotive and the Industrial market from 2014.
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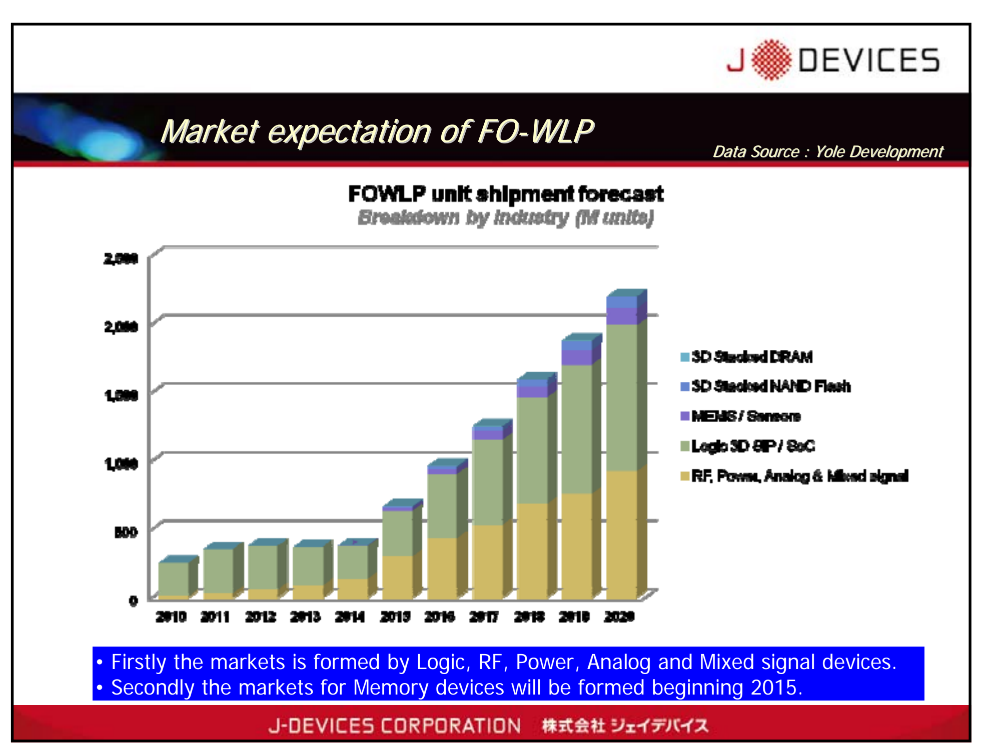
J DEVICES
Market expectation of FO-WLP
Data Source : Yole Development
FOWLP unit shipment forecast
Breakdown by industry (M units)
3D Stacked DRAM
3D Stacked NAND Flash
MEMS / Sensors
Logic 3D SIP / SoC
RF, Power, Analog & Mixed signal
• Firstly the markets is formed by Logic, RF, Power, Analog and Mixed signal devices.
• Secondly the markets for Memory devices will be formed beginning 2015.
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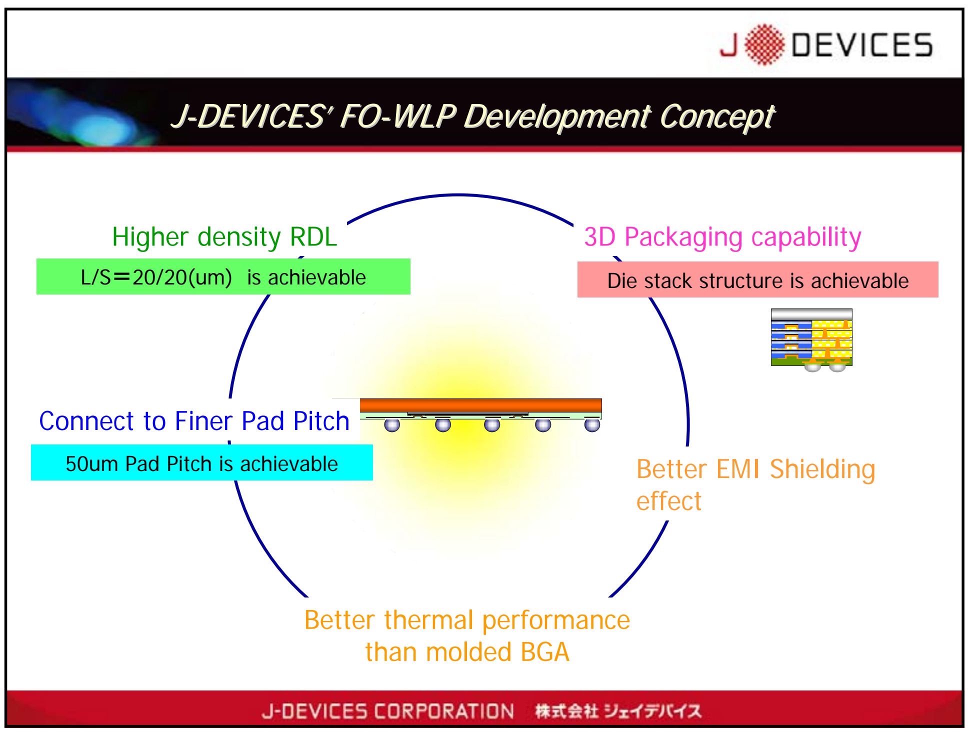
J DEVICES
J-DEVICES' FO-WLP Development Concept
Higher density RDL
L/S=20/20(um) is achievable
3D Packaging capability
Die stack structure is achievable
Connect to Finer Pad Pitch
50um Pad Pitch is achievable
Better EMI Shielding effect
Better thermal performance than molded BGA
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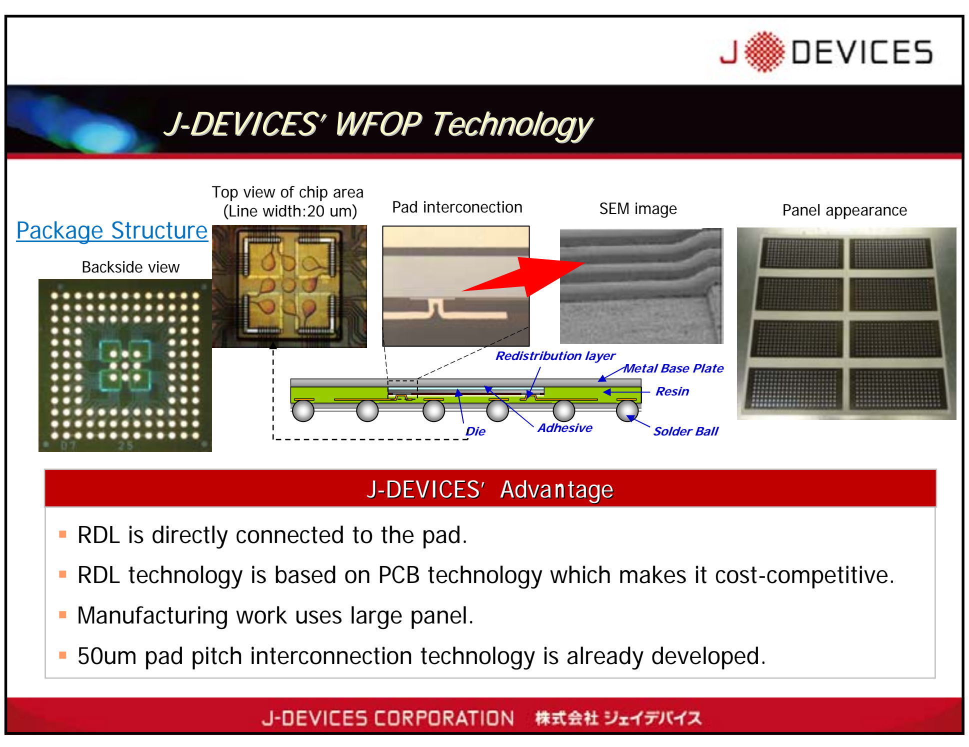
J DEVICES
J-DEVICES' WFOP Technology
Package Structure
Backside view
Top view of chip area (Line width:20 um)
Pad interconnection
SEM image
Panel appearance
Redistribution layer
Metal Base Plate
Resin
Die
Adhesive
Solder Ball
J-DEVICES' Advantage
RDL is directly connected to the pad.
RDL technology is based on PCB technology which makes it cost-competitive.
Manufacturing work uses large panel.
50um pad pitch interconnection technology is already developed.
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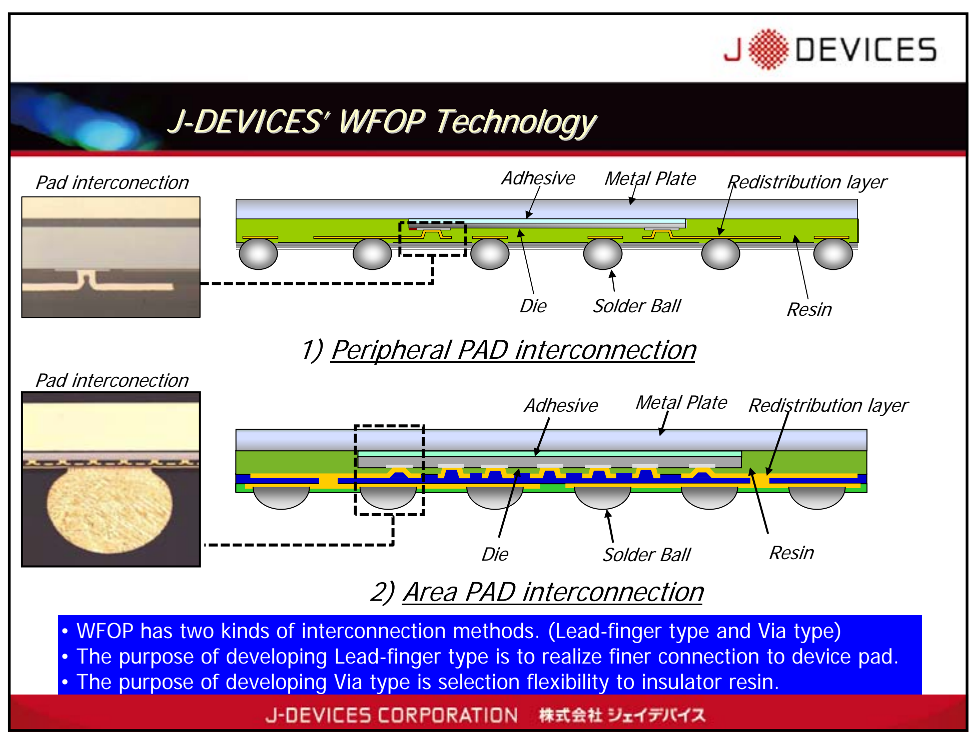
J DEVICES
J-DEVICES' WFOP Technology
J-DEVICES CORPORATION 株式会社 ジェイデバイス


J DEVICES
J-DEVICES' WFOP Technology
Pad interconnection
Adhesive
Metal Plate
Redistribution layer
Die
Solder Ball
Resin
1) Peripheral PAD interconnection
Pad interconnection
Adhesive
Metal Plate
Redistribution layer
Die
Solder Ball
Resin
2) Area PAD interconnection
• WFOP has two kinds of interconnection methods. (Lead-finger type and Via type)
• The purpose of developing Lead-finger type is to realize finer connection to device pad.
• The purpose of developing Via type is selection flexibility to insulator resin.
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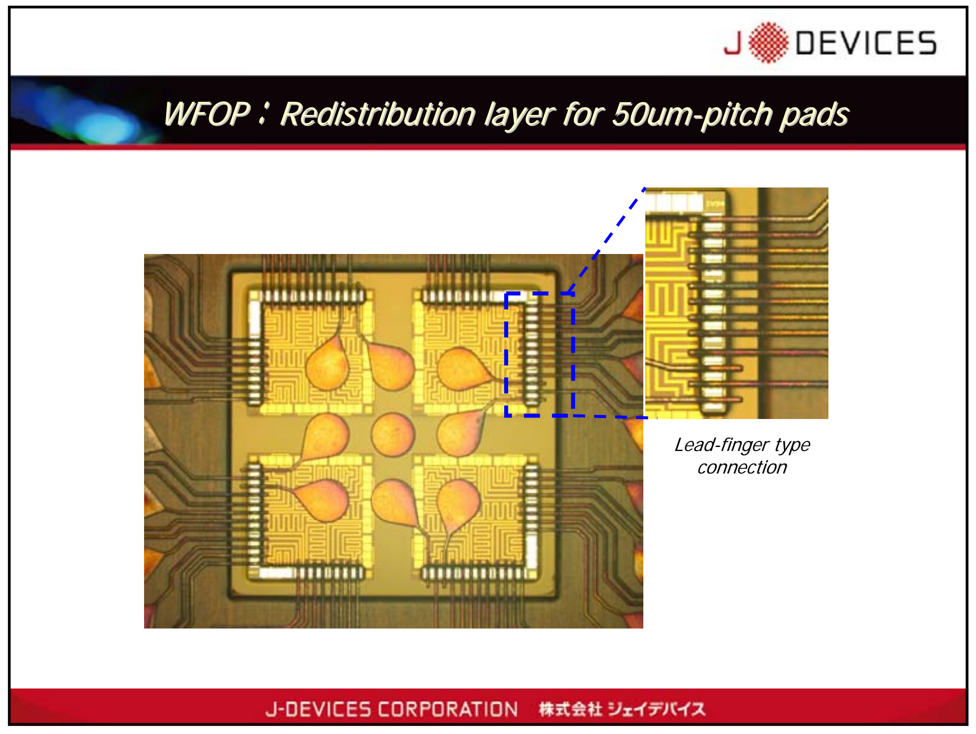
J DEVICES
WFOP : Redistribution layer for 50um-pitch pads
Lead-finger type
connection
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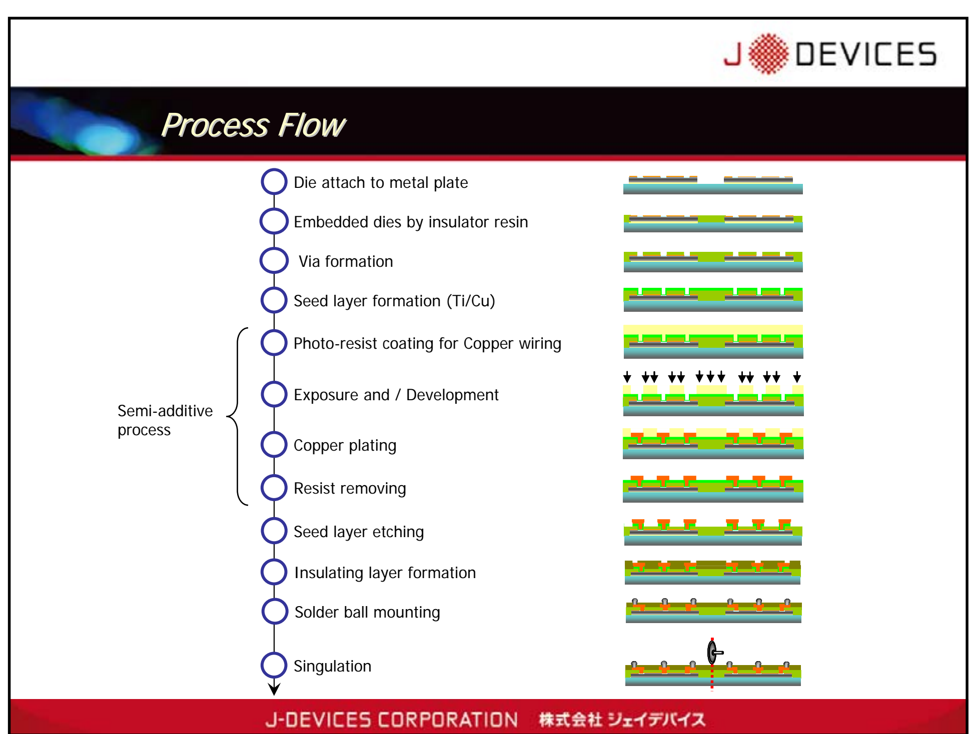
J DEVICES
Process Flow
Die attach to metal plate
Embedded dies by insulator resin
Via formation
Seed layer formation (Ti/Cu)
Semi-additive
process
Photo-resist coating for Copper wiring
Exposure and / Development
Copper plating
Resist removing
Seed layer etching
Insulating layer formation
Solder ball mounting
Singulation
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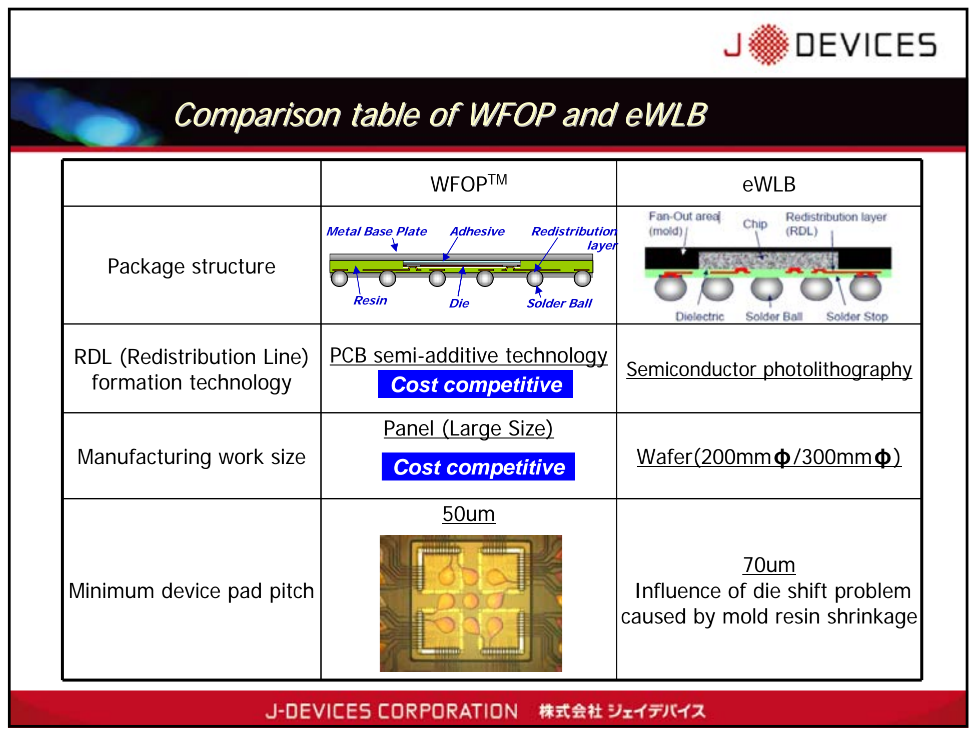
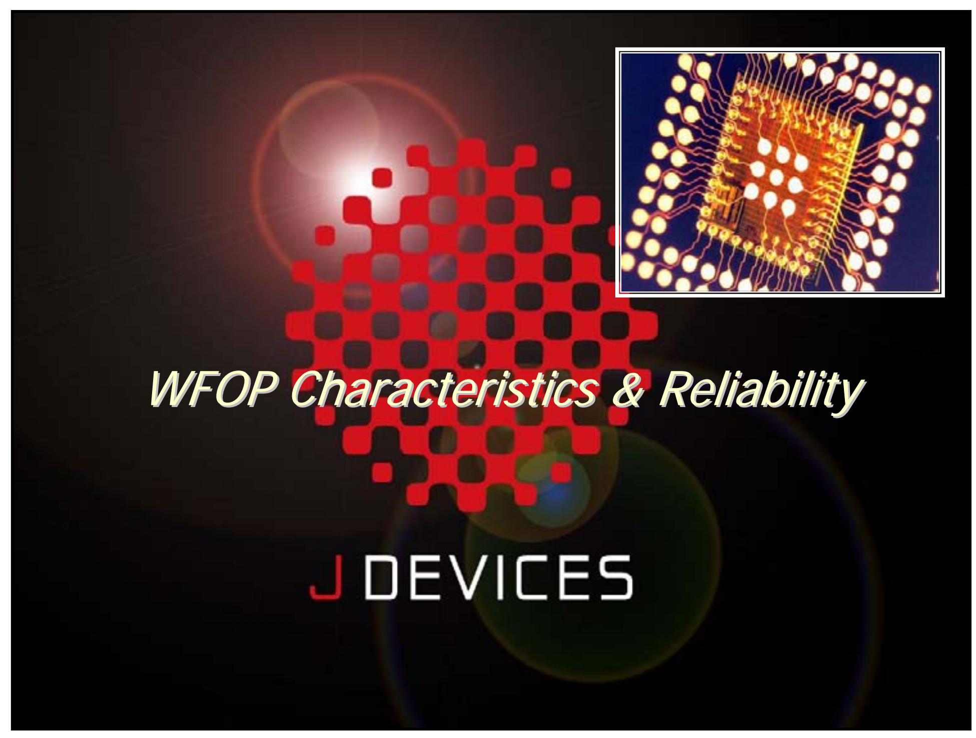
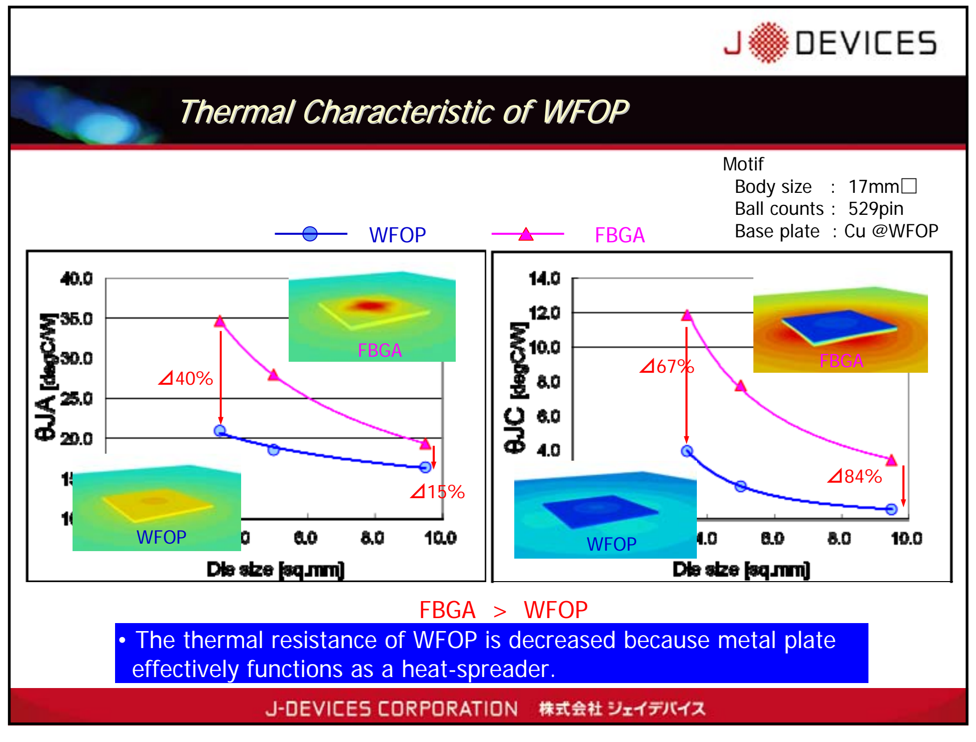


	WFOP™	eWLB
Package structure		
RDL (Redistribution Line) formation technology	PCB semi-additive technology **Cost competitive**	Semiconductor photolithography
Manufacturing work size	Panel (Large Size) **Cost competitive**	Wafer(200mmΦ/300mmΦ)
Minimum device pad pitch	50um	70um Influence of die shift problem caused by mold resin shrinkage




J DEVICES
Thermal Characteristic of WFOP
Motif
Body size : 17mm□
Ball counts : 529pin
Base plate : Cu @WFOP
WFOP
FBGA
θJA [degC/W]
θJC [degC/W]
Die size [sq.mm]
⊿40%
⊿15%
⊿67%
⊿84%
FBGA > WFOP
• The thermal resistance of WFOP is decreased because metal plate effectively functions as a heat-spreader.
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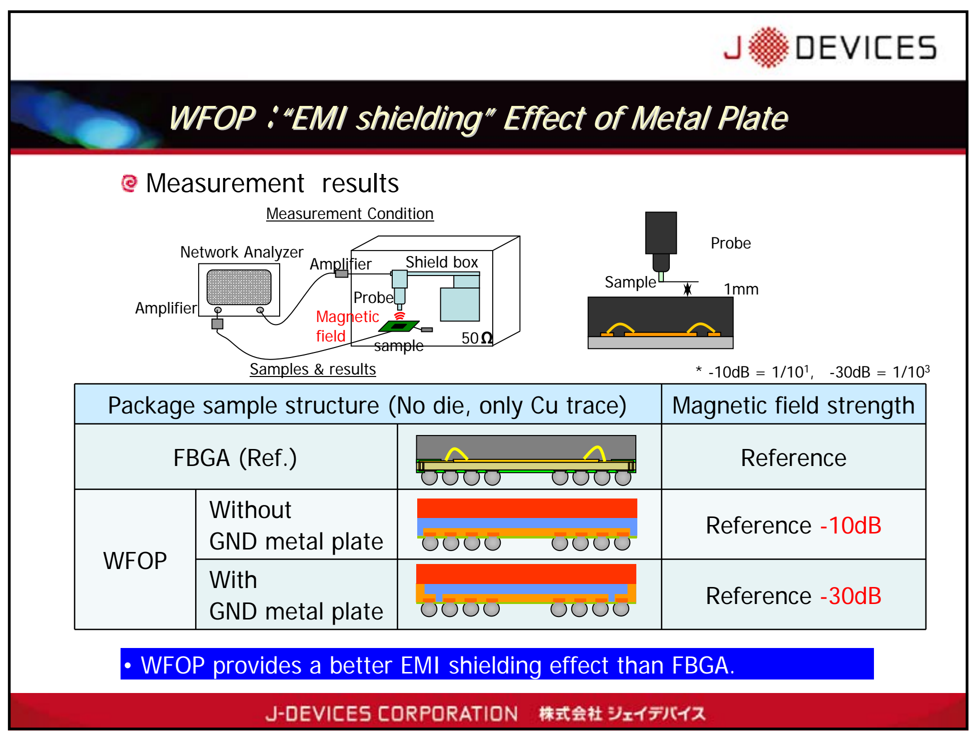
J DEVICES
WFOP :"EMI shielding" Effect of Metal Plate
Measurement results
Measurement Condition
Network Analyzer
Amplifier
Shield box
Probe
Magnetic field
sample
50Ω
Sample
1mm
Samples & results
* -10dB = 1/10¹, -30dB = 1/10³
Package sample structure (No die, only Cu trace)
Magnetic field strength
FBGA (Ref.)
Reference
WFOP
Without GND metal plate
Reference -10dB
With GND metal plate
Reference -30dB
• WFOP provides a better EMI shielding effect than FBGA.
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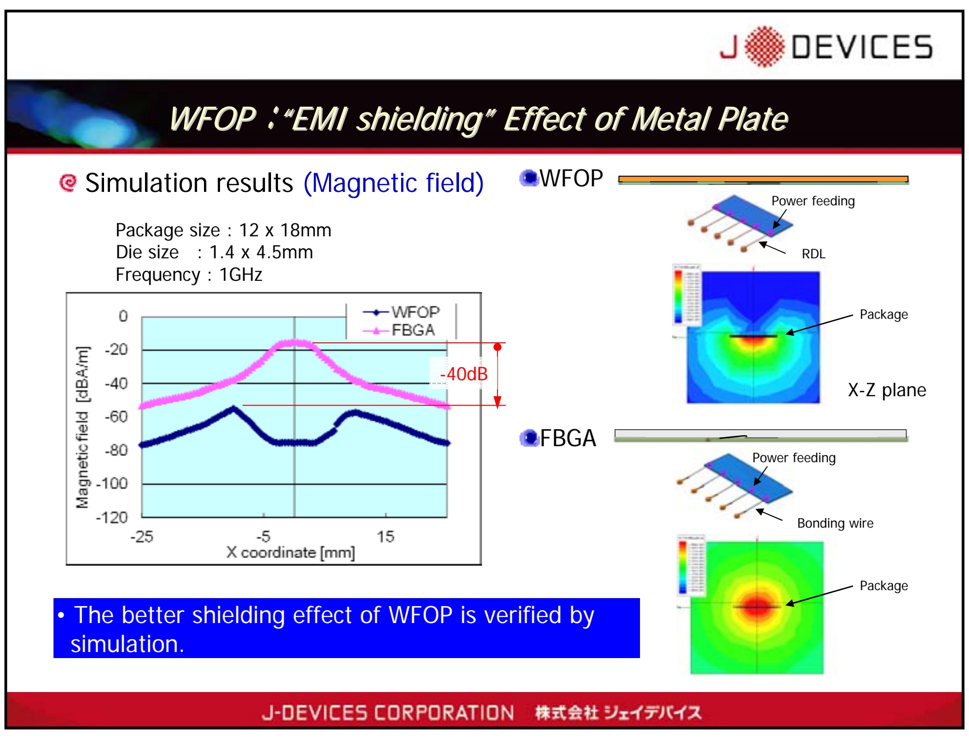
J DEVICES
WFOP :"EMI shielding" Effect of Metal Plate
Simulation results (Magnetic field)
Package size : 12 x 18mm
Die size : 1.4 x 4.5mm
Frequency : 1GHz
WFOP
FBGA
-40dB
Magnetic field [dBA/m]
X coordinate [mm]
WFOP
Power feeding
RDL
Package
X-Z plane
FBGA
Power feeding
Bonding wire
Package
• The better shielding effect of WFOP is verified by simulation.
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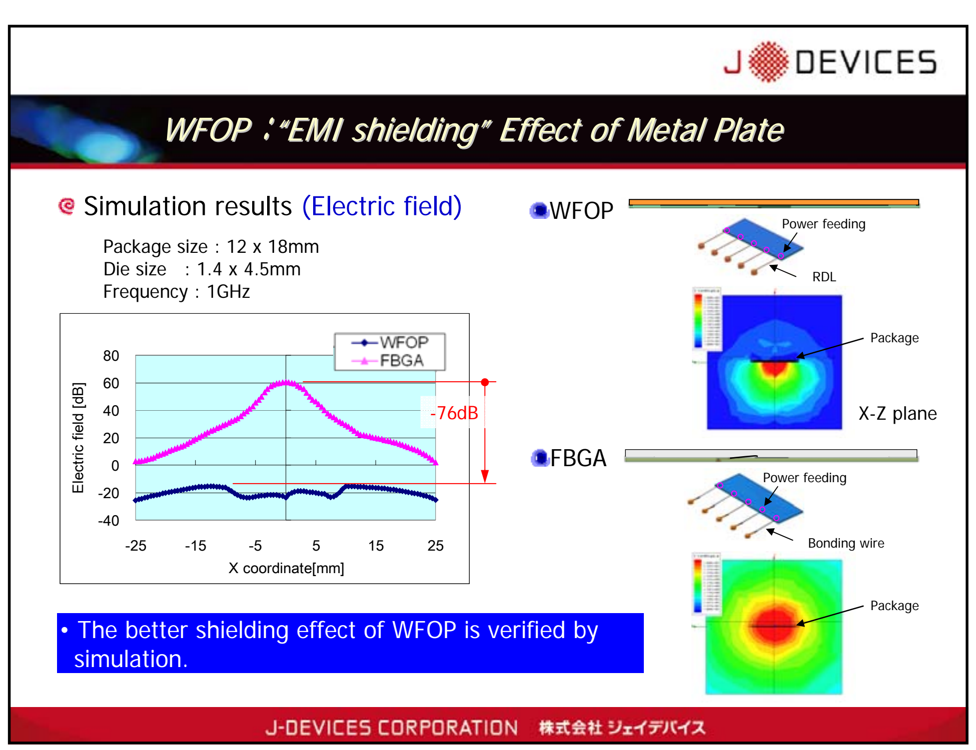
J DEVICES
WFOP :"EMI shielding" Effect of Metal Plate
Simulation results (Electric field)
Package size : 12 x 18mm
Die size : 1.4 x 4.5mm
Frequency : 1GHz
WFOP
FBGA
-76dB
Electric field [dB]
X coordinate[mm]
WFOP
Power feeding
RDL
Package
X-Z plane
FBGA
Power feeding
Bonding wire
Package
• The better shielding effect of WFOP is verified by simulation.
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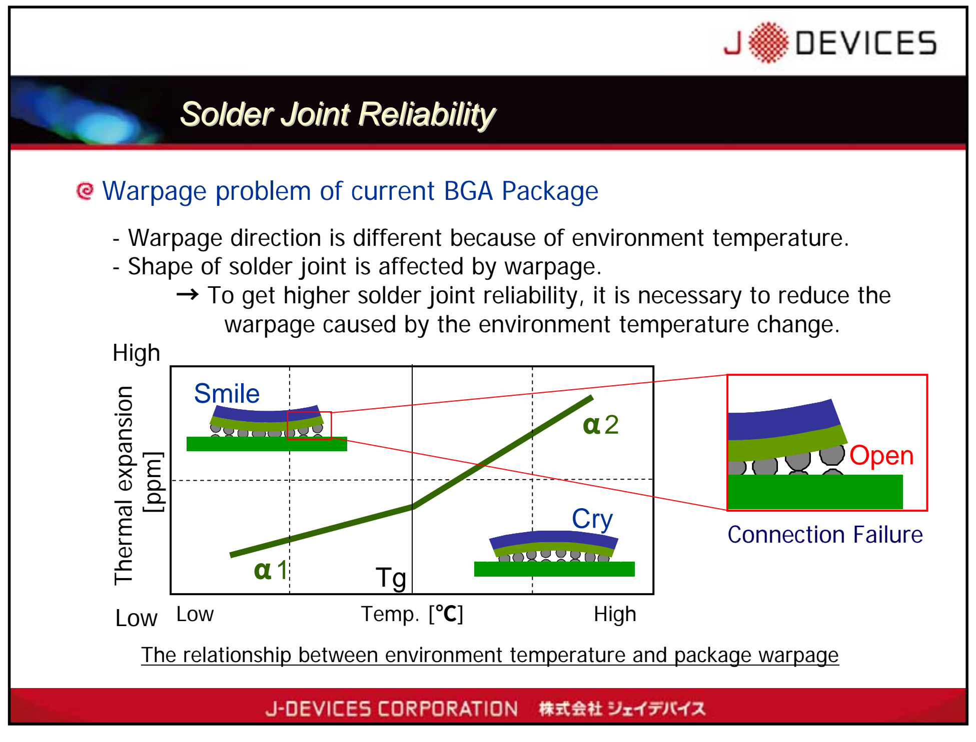
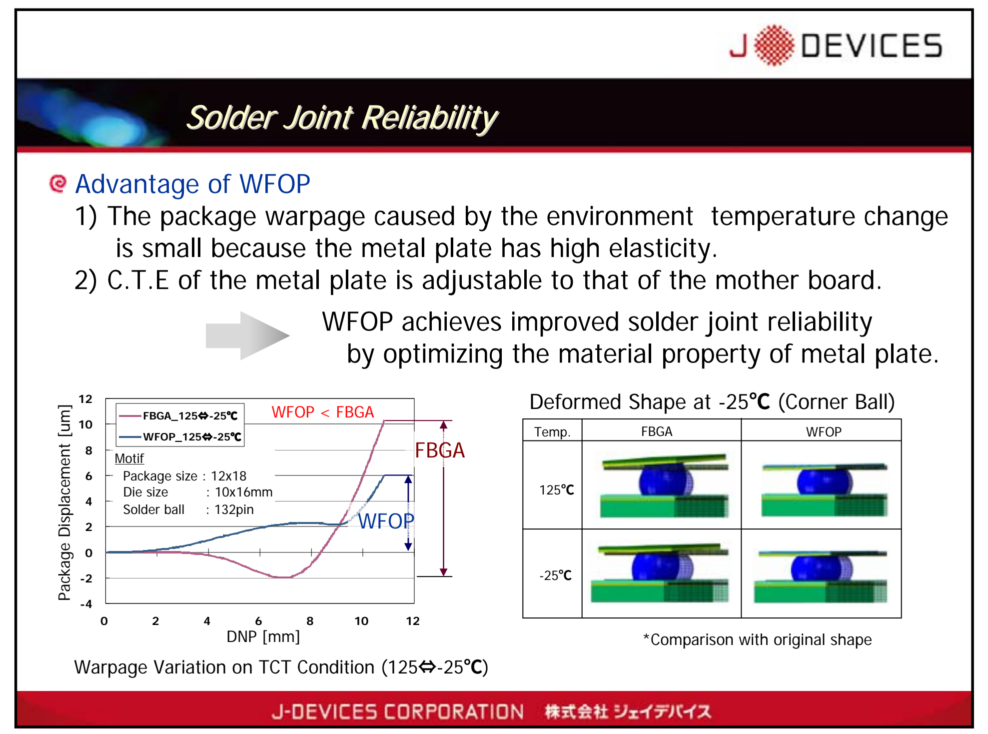

J DEVICES
Solder Joint Reliability
Warpage problem of current BGA Package
- Warpage direction is different because of environment temperature.
- Shape of solder joint is affected by warpage.
→ To get higher solder joint reliability, it is necessary to reduce the warpage caused by the environment temperature change.
High
Thermal expansion [ppm]
Low
Smile
α2
Open
Cry
Connection Failure
α1
Tg
Low
Temp. [℃]
High
The relationship between environment temperature and package warpage
J-DEVICES CORPORATION 株式会社ジェイデバイス


J DEVICES
Solder Joint Reliability
Advantage of WFOP
1) The package warpage caused by the environment temperature change is small because the metal plate has high elasticity.
2) C.T.E of the metal plate is adjustable to that of the mother board.
WFOP achieves improved solder joint reliability by optimizing the material property of metal plate.
FBGA_125⇔-25℃
WFOP_125⇔-25℃
WFOP < FBGA
FBGA
WFOP
Motif
Package size : 12x18
Die size : 10x16mm
Solder ball : 132pin
Package Displacement [um]
DNP [mm]
Warpage Variation on TCT Condition (125⇔-25℃)
Deformed Shape at -25℃ (Corner Ball)
Temp.
FBGA
WFOP
125℃
-25℃
*Comparison with original shape
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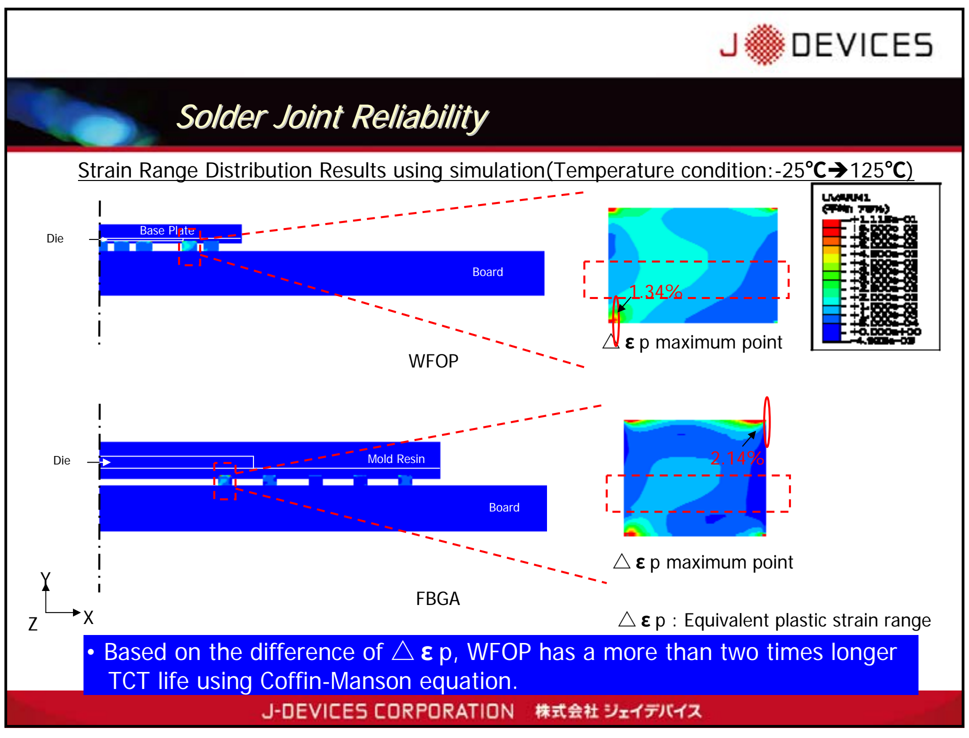


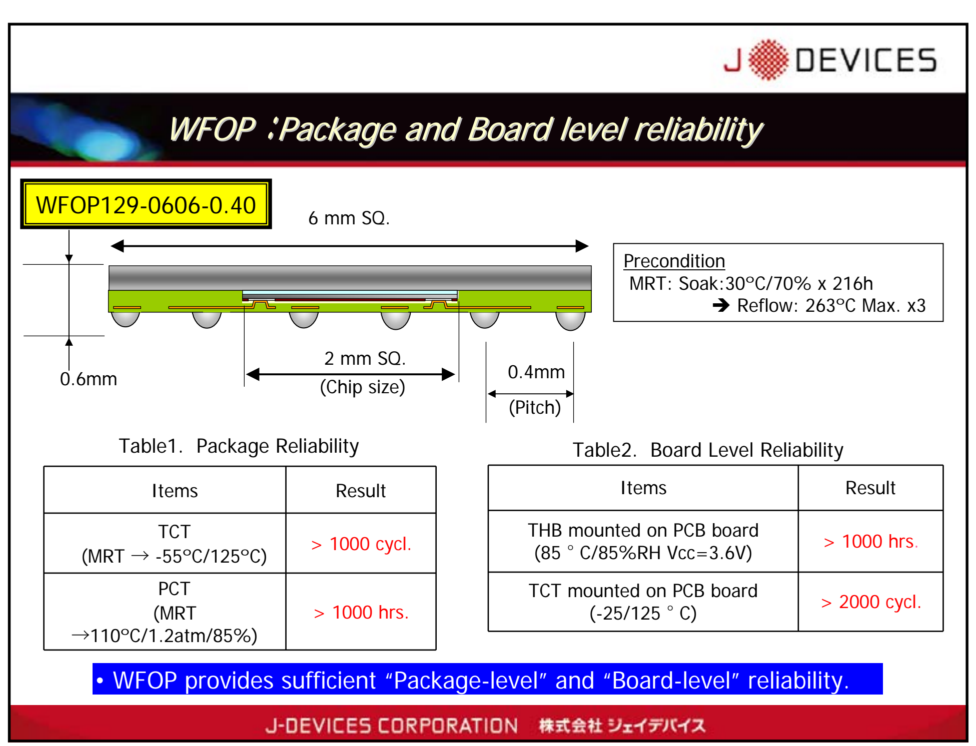
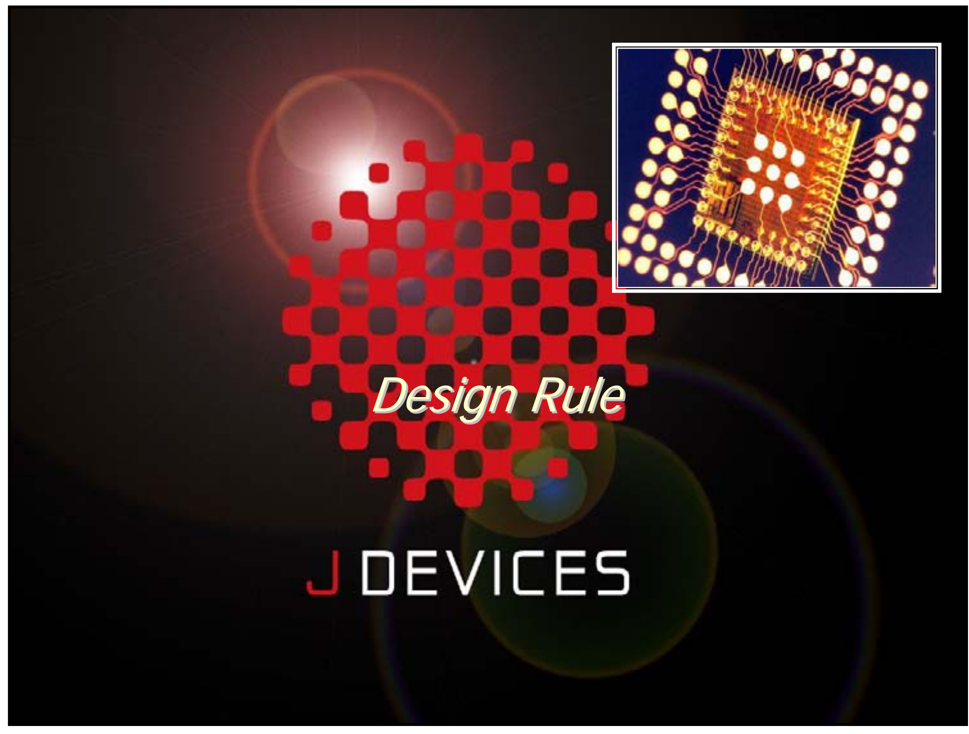


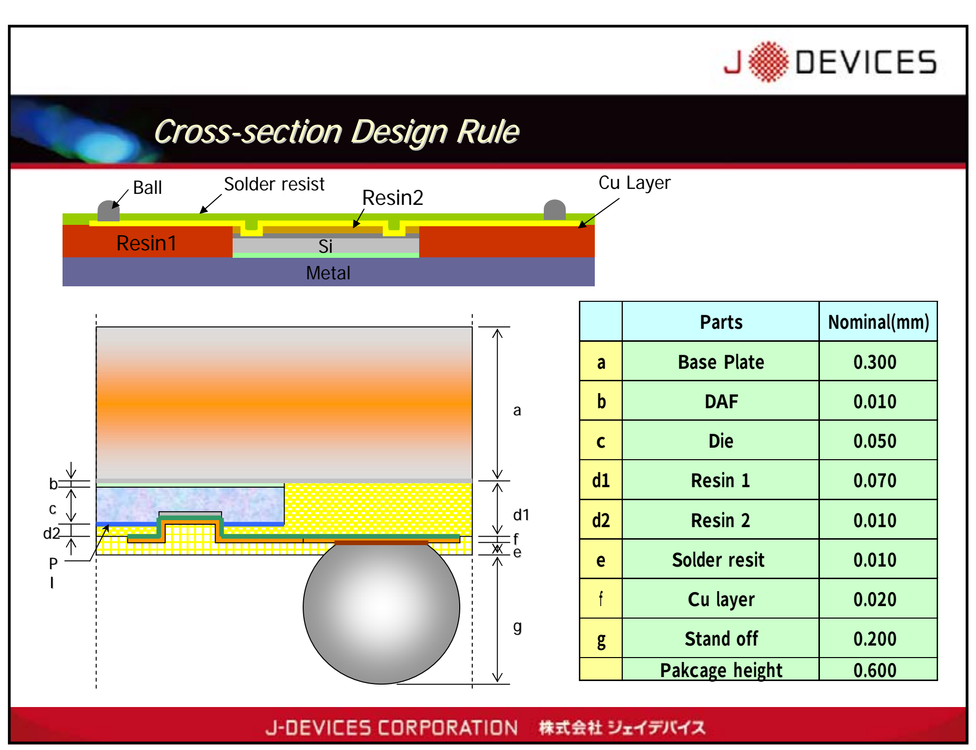
Table1. Package Reliability

Items	Result
TCT (MRT → -55°C/125°C)	＞ 1000 cycl.
PCT (MRT →110°C/1.2atm/85%)	＞ 1000 hrs.

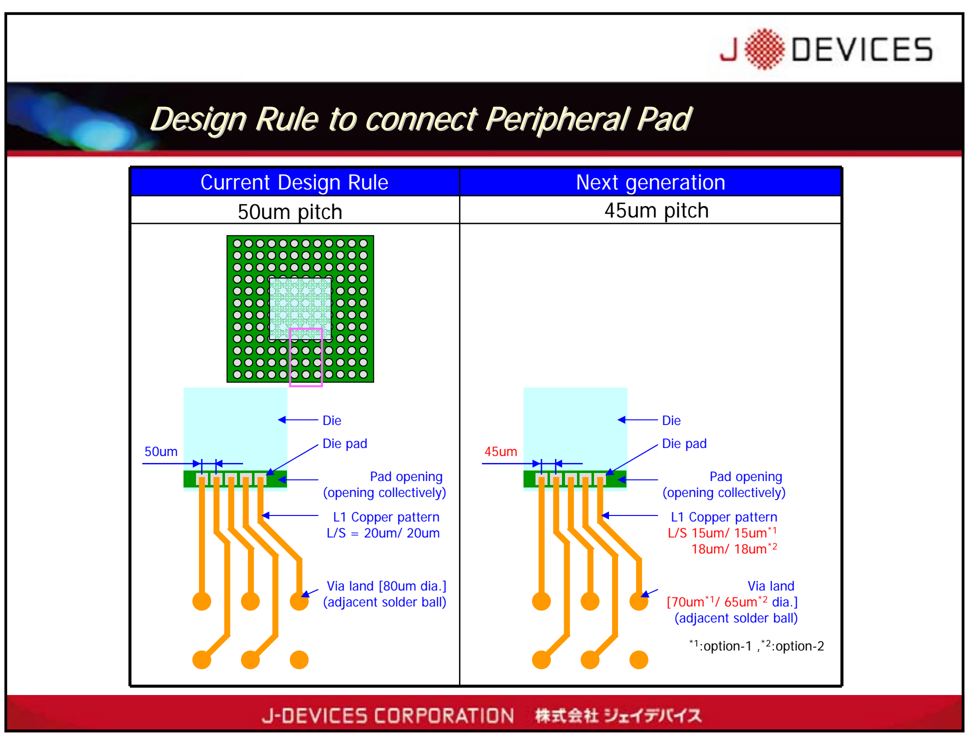
Table2. Board Level Reliability

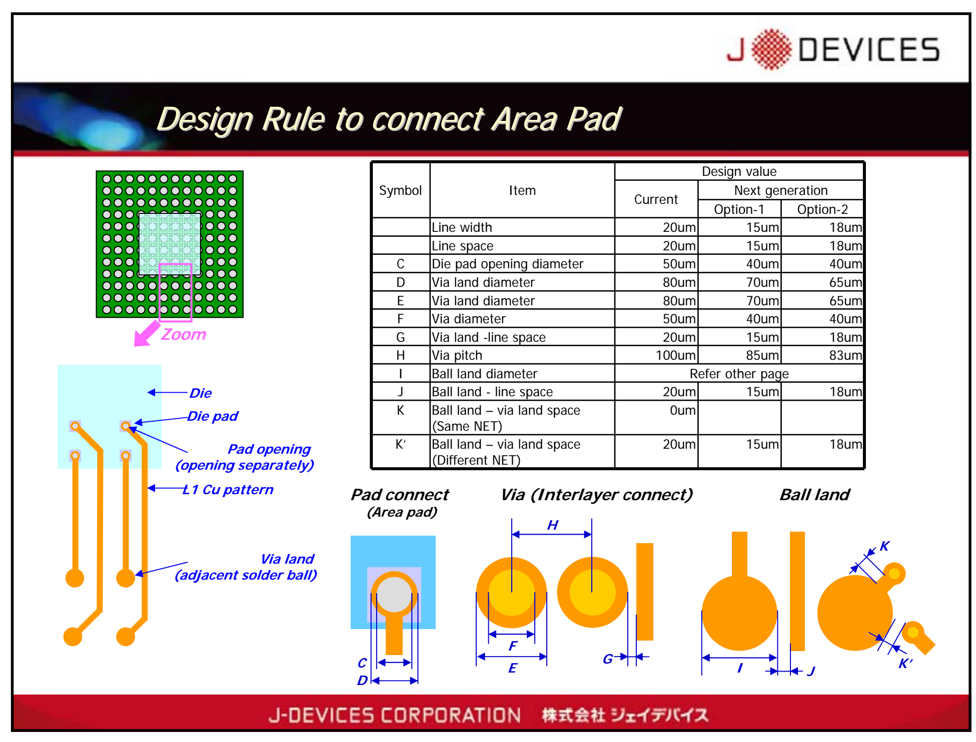
Items	Result
THB mounted on PCB board (85 ° C/85%RH Vcc=3.6V)	＞ 1000 hrs.
TCT mounted on PCB board (-25/125 ° C)	＞ 2000 cycl.



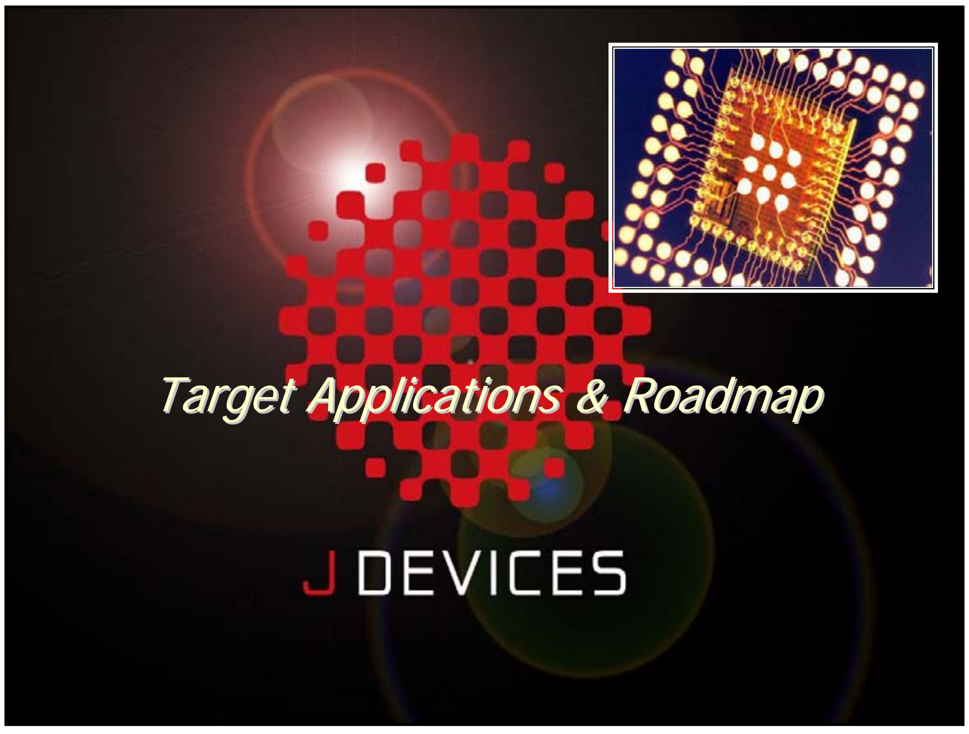


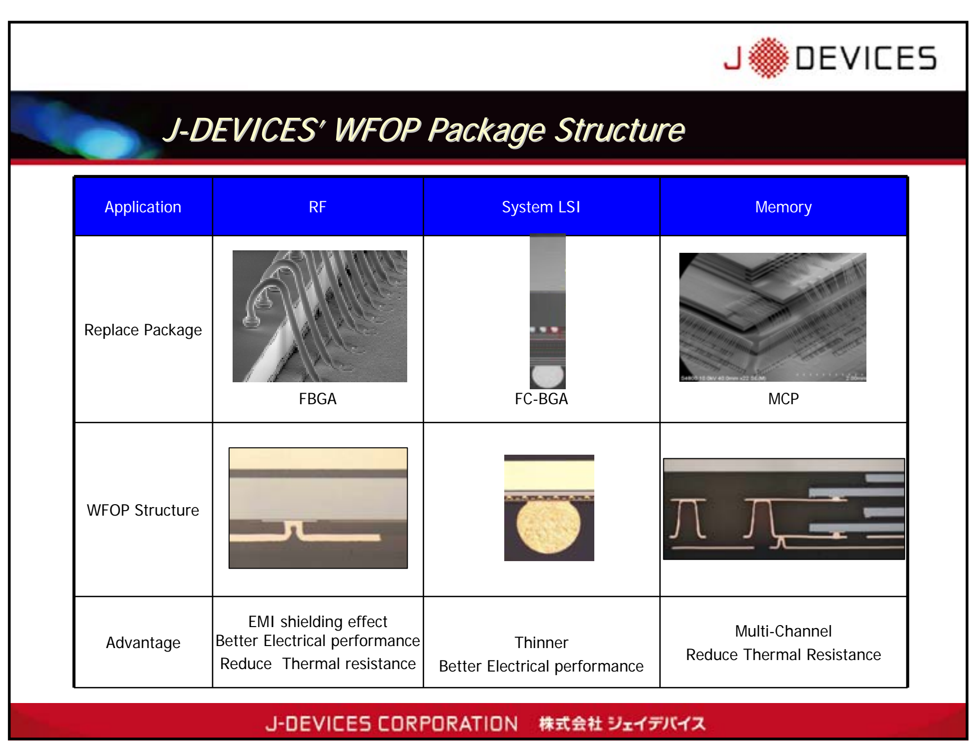
	Parts	Nominal(mm)
a	Base Plate	0.300
b	DAF	0.010
c	Die	0.050
d1	Resin 1	0.070
d2	Resin 2	0.010
e	Solder resit	0.010
f	Cu layer	0.020
g	Stand off	0.200
	Pakcage height	0.600



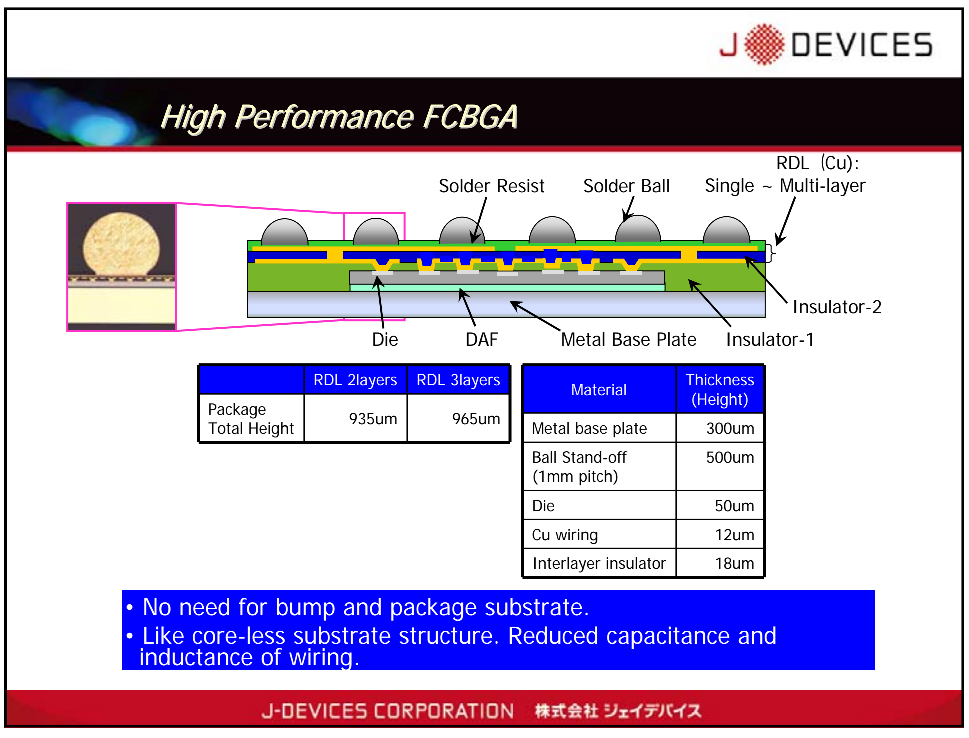


Symbol	Item	Design value		
		Current	Next generation	
			Option-1	Option-2
	Line width	20um	15um	18um
	Line space	20um	15um	18um
C	Die pad opening diameter	50um	40um	40um
D	Via land diameter	80um	70um	65um
E	Via land diameter	80um	70um	65um
F	Via diameter	50um	40um	40um
G	Via land -line space	20um	15um	18um
H	Via pitch	100um	85um	83um
I	Ball land diameter	Refer other page		
J	Ball land - line space	20um	15um	18um
K	Ball land – via land space (Same NET)	0um		
K'	Ball land – via land space (Different NET)	20um	15um	18um





Application	RF	System LSI	Memory
Replace Package	FBGA	FC-BGA	MCP
WFOP Structure			
Advantage	EMI shielding effect Better Electrical performance Reduce Thermal resistance	Thinner Better Electrical performance	Multi-Channel Reduce Thermal Resistance


J DEVICES
High Performance FCBGA
Solder Resist
Solder Ball
RDL (Cu): Single ~ Multi-layer
Insulator-2
Die
DAF
Metal Base Plate
Insulator-1

	RDL 2layers	RDL 3layers
Package Total Height	935um	965um

Material	Thickness (Height)
Metal base plate	300um
Ball Stand-off (1mm pitch)	500um
Die	50um
Cu wiring	12um
Interlayer insulator	18um

• No need for bump and package substrate.
• Like core-less substrate structure. Reduced capacitance and inductance of wiring.
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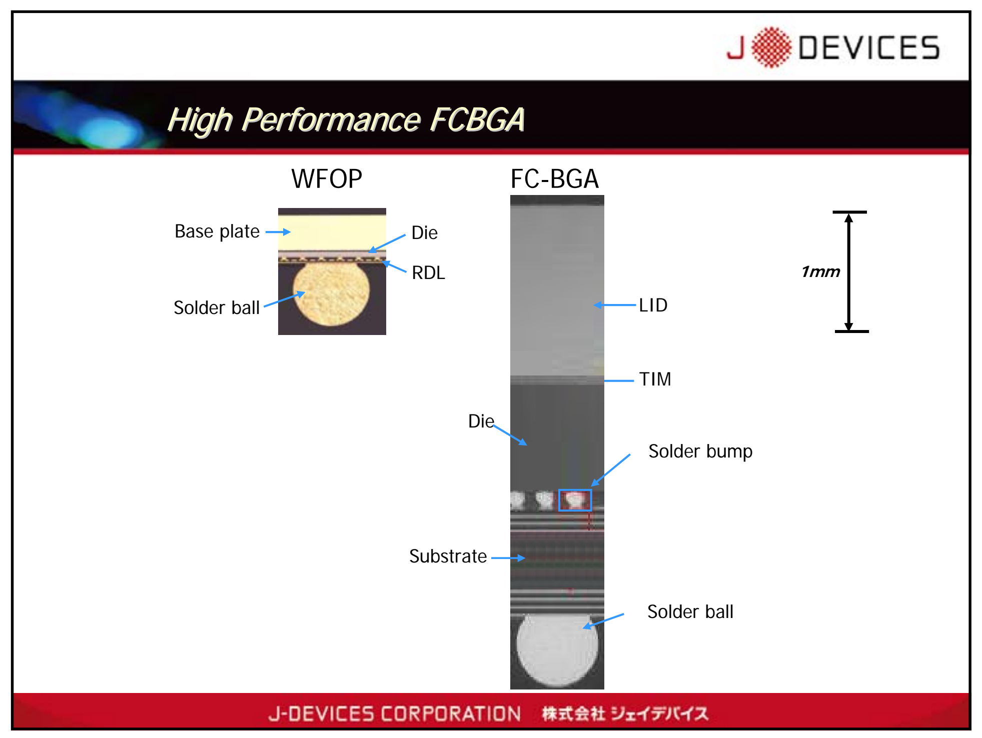
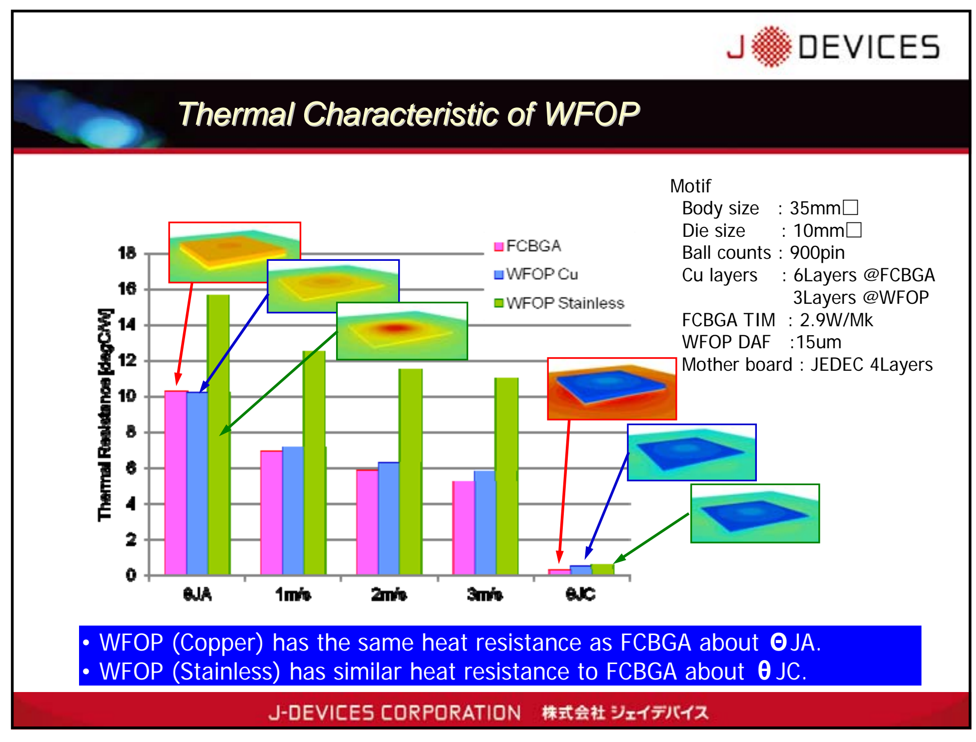

J DEVICES
High Performance FCBGA
WFOP
FC-BGA
Base plate
Die
RDL
Solder ball
LID
TIM
Die
Solder bump
Substrate
Solder ball
1mm
J-DEVICES CORPORATION 株式会社 ジェイデバイス


J DEVICES
Thermal Characteristic of WFOP
Motif
Body size : 35mm□
Die size : 10mm□
Ball counts : 900pin
Cu layers : 6Layers @FCBGA
3Layers @WFOP
FCBGA TIM : 2.9W/Mk
WFOP DAF :15um
Mother board : JEDEC 4Layers
FCBGA
WFOP Cu
WFOP Stainless
Thermal Resistance [degC/W]
0
2
4
6
8
10
12
14
16
18
θJA
1m/s
2m/s
3m/s
θJC
• WFOP (Copper) has the same heat resistance as FCBGA about ΘJA.
• WFOP (Stainless) has similar heat resistance to FCBGA about θJC.
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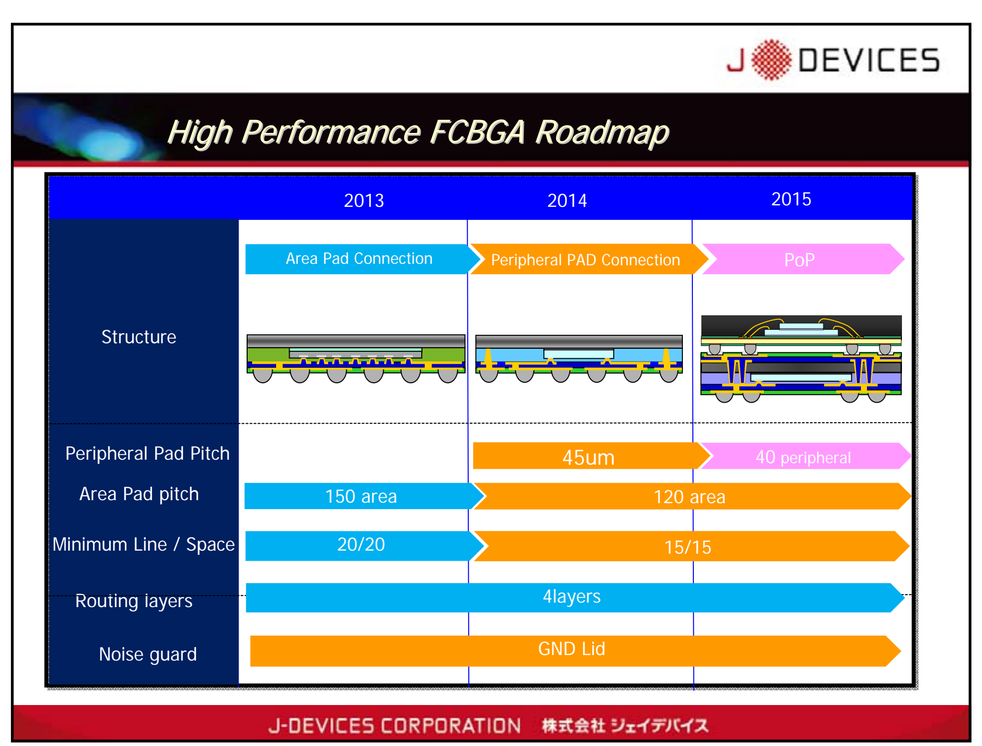
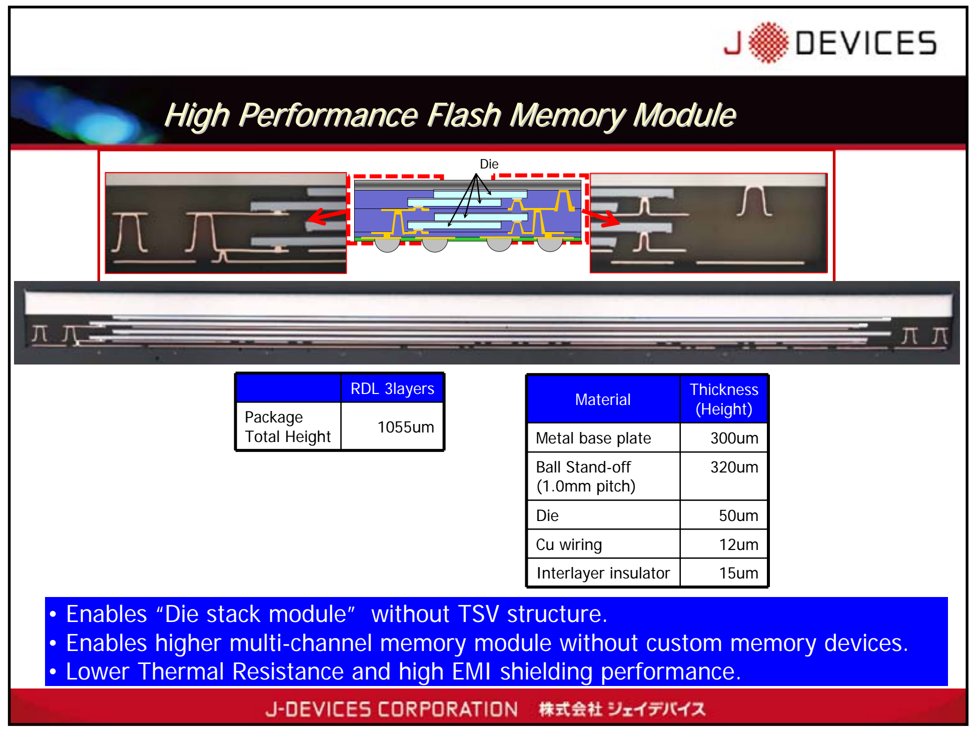

J DEVICES
High Performance FCBGA Roadmap
2013
2014
2015
Structure
Area Pad Connection
Peripheral PAD Connection
PoP
Peripheral Pad Pitch
45um
40 peripheral
Area Pad pitch
150 area
120 area
Minimum Line / Space
20/20
15/15
Routing layers
4layers
Noise guard
GND Lid
J-DEVICES CORPORATION 株式会社ジェイデバイス


J DEVICES
High Performance Flash Memory Module
Die
	RDL 3layers
Package Total Height	1055um

Material	Thickness (Height)
Metal base plate	300um
Ball Stand-off (1.0mm pitch)	320um
Die	50um
Cu wiring	12um
Interlayer insulator	15um

• Enables "Die stack module" without TSV structure.
• Enables higher multi-channel memory module without custom memory devices.
• Lower Thermal Resistance and high EMI shielding performance.
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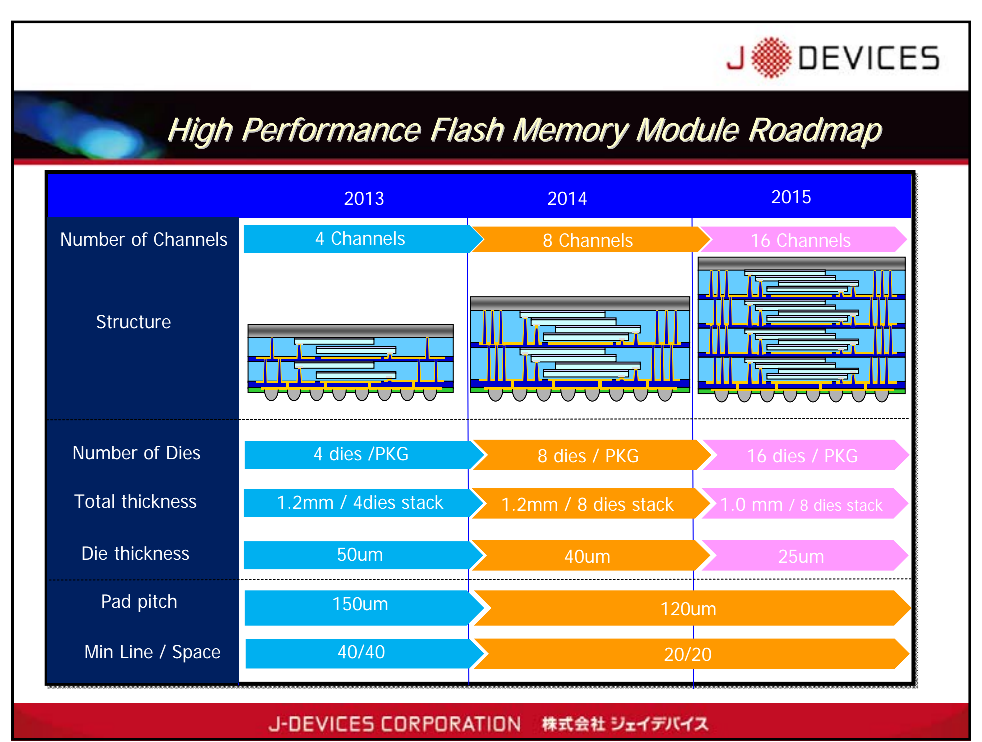
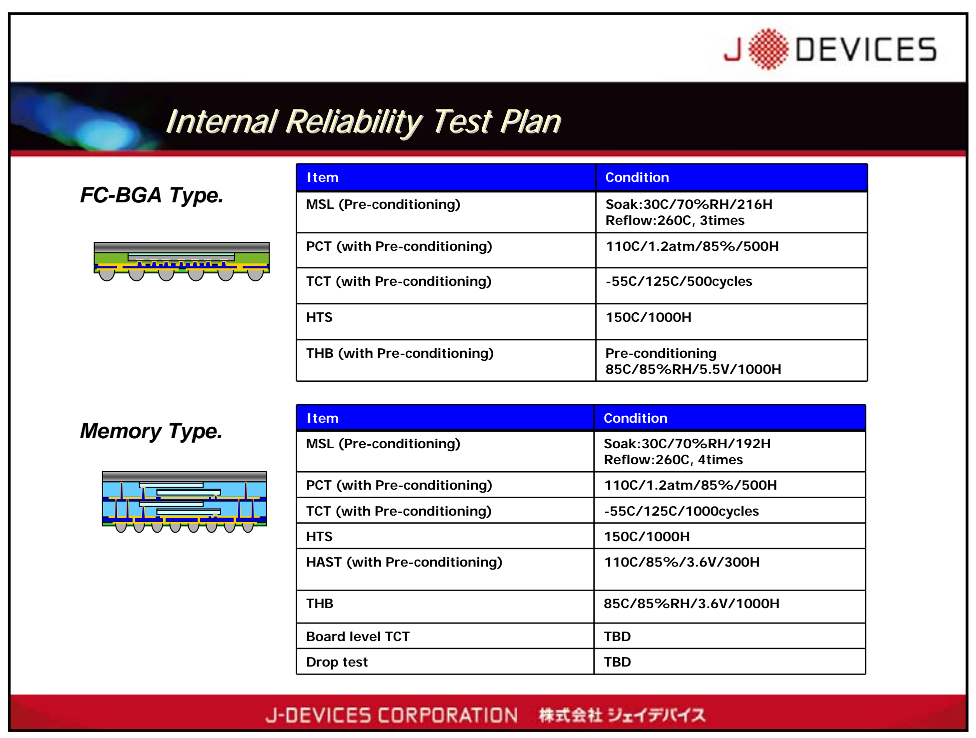
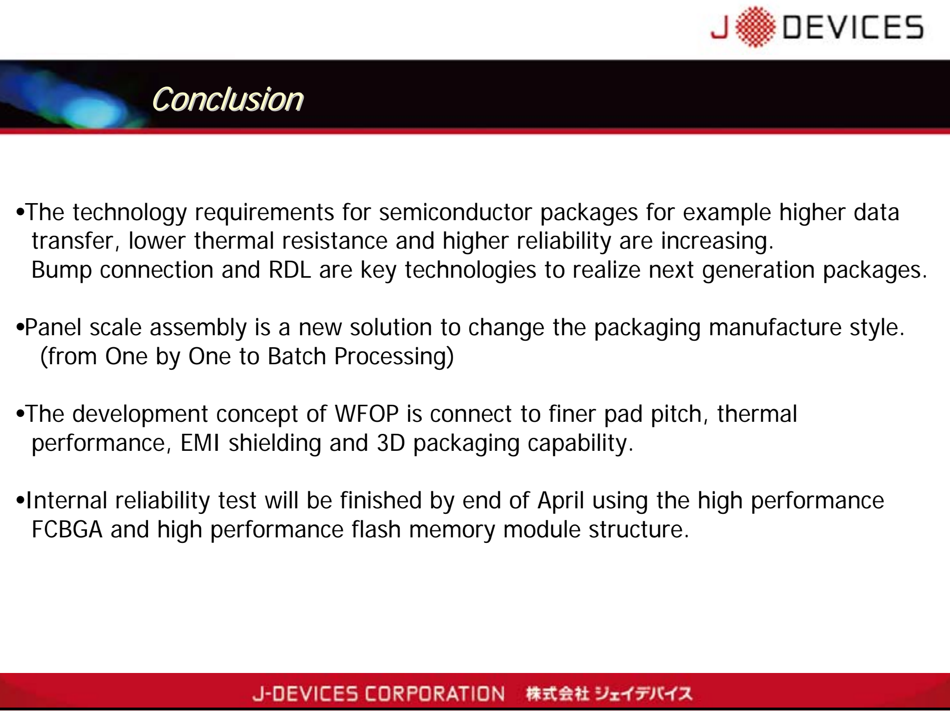

J DEVICES
High Performance Flash Memory Module Roadmap
	2013	2014	2015
Number of Channels	4 Channels	8 Channels	16 Channels
Structure			
Number of Dies	4 dies /PKG	8 dies / PKG	16 dies / PKG
Total thickness	1.2mm / 4dies stack	1.2mm / 8 dies stack	1.0 mm / 8 dies stack
Die thickness	50um	40um	25um
Pad pitch	150um	120um	
Min Line / Space	40/40	20/20	

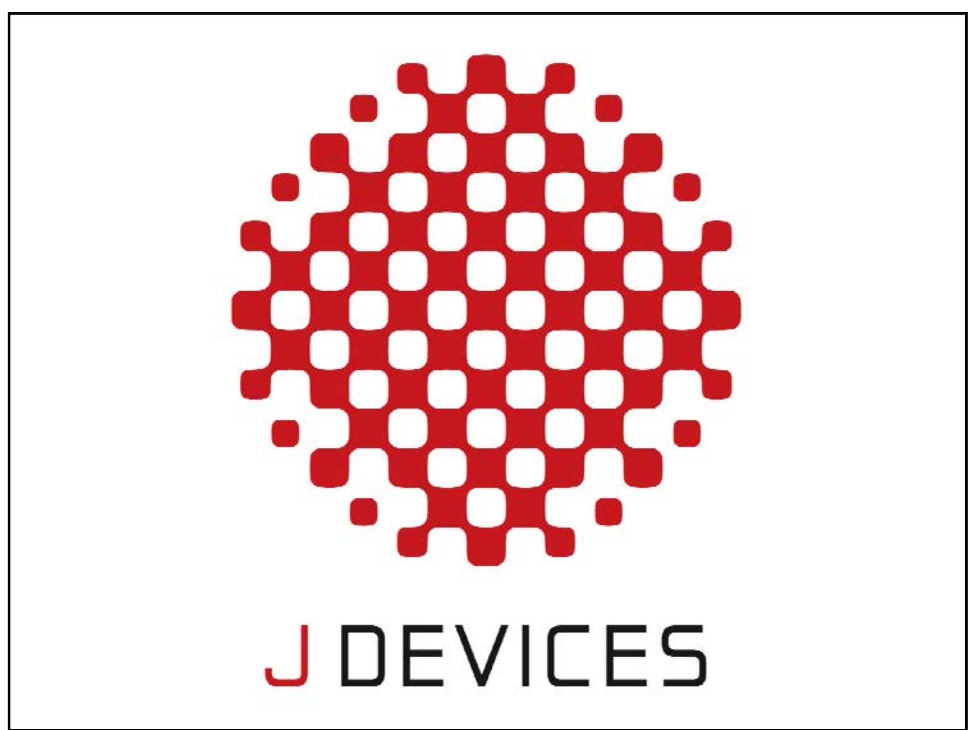
J-DEVICES CORPORATION 株式会社 ジェイデバイス



Item	Condition
MSL (Pre-conditioning)	Soak:30C/70%RH/216H Reflow:260C, 3times
PCT (with Pre-conditioning)	110C/1.2atm/85%/500H
TCT (with Pre-conditioning)	-55C/125C/500cycles
HTS	150C/1000H
THB (with Pre-conditioning)	Pre-conditioning 85C/85%RH/5.5V/1000H

Item	Condition
MSL (Pre-conditioning)	Soak:30C/70%RH/192H Reflow:260C, 4times
PCT (with Pre-conditioning)	110C/1.2atm/85%/500H
TCT (with Pre-conditioning)	-55C/125C/1000cycles
HTS	150C/1000H
HAST (with Pre-conditioning)	110C/85%/3.6V/300H
THB	85C/85%RH/3.6V/1000H
Board level TCT	TBD
Drop test	TBD




J DEVICES