Advanced Package Migration to System Level Integration

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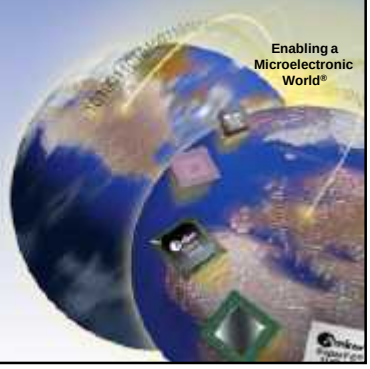


Topics

- **Advanced Substrate Technologies**
- **Interposers & Role**
- **Embedded Die Solutions**
- **Package-on-Package**
- **Migration to System Level Integration**

Advanced Substrates

Advanced Substrate Roadmap : CSP

	HVM	Available	2013	2014	2015
Line & space(um) • Prepreg • Build-up film	≥20/20 ≥20/20	18/18 20/20	14/14 15/15	12/12 12/12	10/10 10/10
Laser via pad (um) • Blind via (prepreg) • Blind via (build-up film) • Inner layer via	≥120/65 ≥100/60 ≥175/75	110/65 100/60 175/75	100/60 95/60 155/75	100/60 90/55 150/75	95/55 85/50 143/75
W/B pad pitch (um)	≥65	65	60	70	←
F/C pitch (um) • Full array • Peripheral array	≥150 ≥40/60	150 40/60	140 40/60	← 30/60	← ←
SRO/SRR (um) • Solder resist open • Solder resist registration	≥80 ≥12.5	70 12.5	65 10	60 ←	← 8
Prepreg thickness (um)	≥35	30	25	←	←

Advanced Substrate Roadmap : BGA

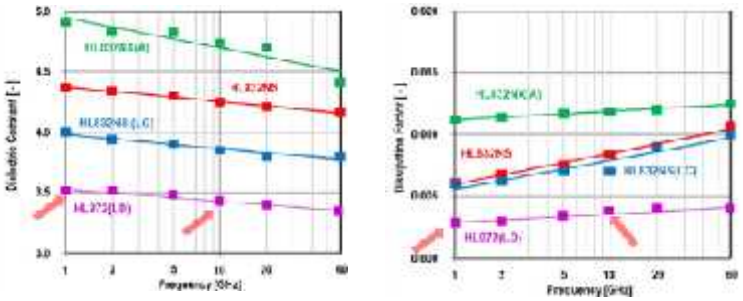
	HVM	Available	2013	2014	2015
Line & space (um)	≥15/15	14/14	9/12	←	8/8
Via / via pad (um)					
• Blind via	≥100/65	100/65	90/65	90/65	90/60
• Inner layer via	≥250/100	180/80	155/75	150/75	145/75
SRO/SRR (um)					
• Solder resist opening	≥85	80	75	70	65
• Solder resist registration	≥15	15	12.5	10	8
• SOP pitch	≥150	150	140	130	125
• fpfc pitch			40/80	30/60	←

Advanced Substrate Roadmap : BGA, cont.

	HVM	Available	2013	2014	2015
Core thickness	800, 400 Cored	800, 400 Coreless	250 Coreless	200 Coreless	<200 Coreless
Core material	E679FGR E700GR	E705G R1515A R1515W	E705GLH HL832NSF-LCA	←	1~2 ppm Core
Build-up material	GX-13	GX-92 GX-T31 GZ-41	GX-A01 GY-11 NX-04H NQ-05	←	←
Solder mask material (* film type SR)	AUS 703	SR7200G AUS 410*	SR7300G AUS SR-1*	AUS G-2 SR7400	←
Surface finish					
• FCBGA	ENIG (w/ SOP) IT (w/SOP) OSP (w/SOP)	←	←	←	←
• fpfcBGA			ENEPIG, EPIG, OSP	←	←

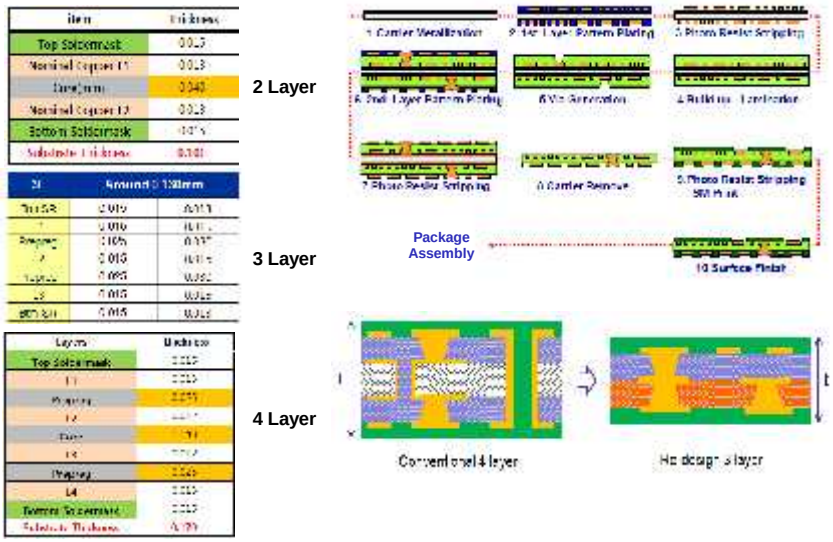
Low Dk / Df Dielectric Materials

- **Dielectric material needs for future high frequency devices**
  - Need for materials with Dk < 4.0 (dielectric constant)
  - Need for materials with Df < 0.01 ~ preferably 0.005 (dissipation factor)
  - CTE will play a larger role for the embedded die products



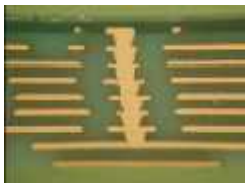
Substrate Technology Advancements

- **Ultra Thin Substrates**



Advanced Substrates

- **Coreless**
  - Today = Coreless
    - Qualified 45mm body and 15 x 20mm die
    - Provides better electrical performance

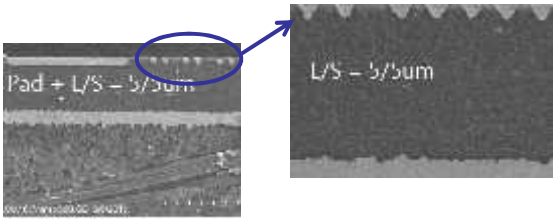


- **Future Generation Design Rules**
  - Lab level
    - 5/5 line-space ; 18/30 via-pad
    - proprietary processing ; new materials
  - Lab level +
    - 3/3 line-space ; 10/22 via-pad
    - wafer based equipment for panels ; thin film materials

Next Generation Substrates

- **Laser Embedded Signals & Pads**
  - Is it time?
  - Proven on multiple formats
  - Proven with multiple materials
  - Advanced substrate manufacturer has capability / capacity today

Line=5/5um, Pad=120um



Interposers & Role

Interposers & Role: Overview

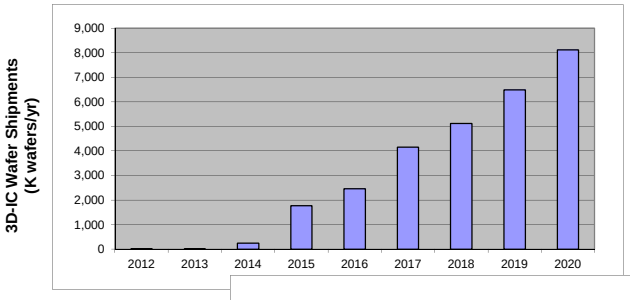
- **Advanced MCM SiP Packages**
  - Need method to integrate advanced node die on same package platform
  - Die must be integrated in close proximity; need high bandwidth and low power
  - Deconstructed advanced node logic & high end memory driving integration
- **Markets**
  - High End FPGA, ASIC, SERDES
  - Mid End CPU, GPU, APU, High end Memory
  - Low End Mobile
- **Interposer Options**
  - Silicon interposer
    - high end, mid end, low end
  - Glass interposer
    - unavailable today ; could be solution for all markets in the future
  - Organic interposer
    - mid end, low end

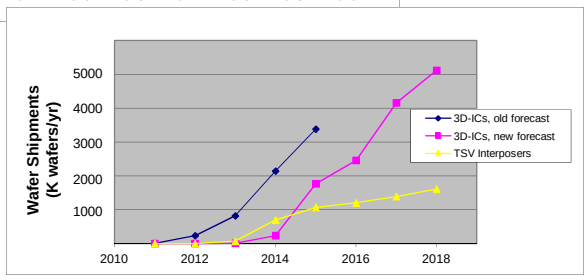
MCM Integrated Interposer Market

- **Product Applications**
  - Gaming, HD-TV, mobile, tablets, computing, servers – very broad
  - High end graphics cards will be initial focus with HBM memory integration
  - Mobile space will follow based upon availability of lower cost interposer solutions
- **Market Longevity**
  - Expect very long life cycle ; production already started
  - Long term continued use through deconstruction of very high end node logic to address system level cost and power
- **Demand Forecast**
  - Continued low volumes with FPGAs and ASICS
  - Moderate volumes for high end graphics cards ; HBM cost / availability driven
  - High volumes for mobile ; interposer cost driven at $0.01 per sq.mm

Package Migration to MCM Integrated Interposers

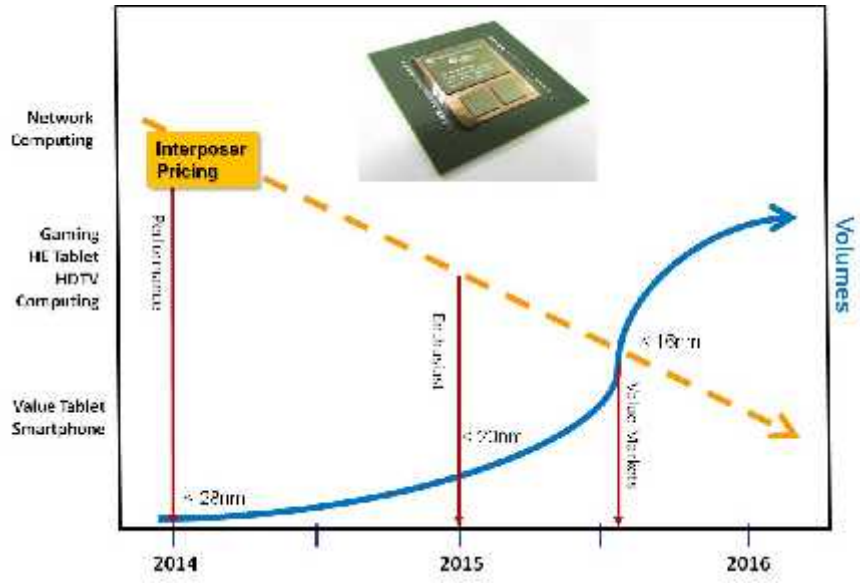
- **TSV Product Demand (300mm equiv. wafers)**





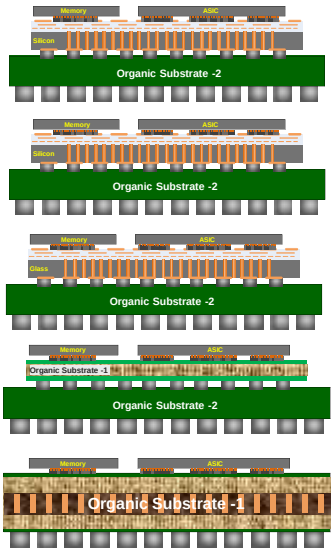
Courtesy of TechSearch International, Inc. 2012

Package Growth Dependence on Interposers



MCM Interposer Integrated Solutions

- **Five Primary Methods**
  - **Silicon on Organic Substrate**
  - **Low Cost Silicon on Organic Substrate**
  - **Glass on Organic Substrate**
  - **Adv. Dual Organic Substrate**
  - **Adv. Hybrid Organic Substrate**

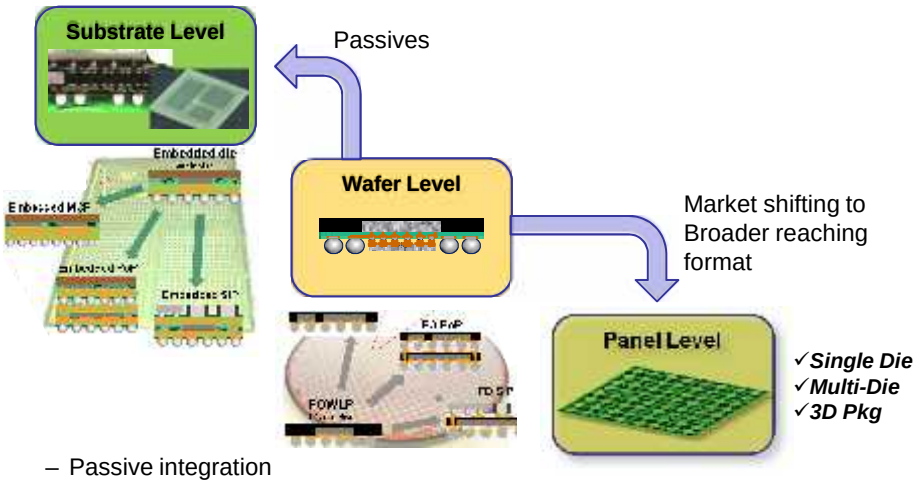


Integrated Interposer Summary

- **General Market Looking Forward**
  - Expect very long life cycle ; production already started at high end
  - Long term continued use through deconstruction of very high end node SoC logic to address system level cost and power
- **Interposer Options / Sources**
  - High End silicon will dominate
  - Mid End silicon to be prominent ; organic may play role
  - Low End organic?? ; need technology and large sourcing supply
- **Other Factors**
  - Pricing pressure ; will continue to stress Tier-1 foundries
    - ✓ Need Tier-2 silicon supply chain without ties to bundling
  - Silicon ; industry growth will necessitate more worldwide capacity than currently available
  - Organic may be ultimate long term answer

Embedded Die Solutions

Advanced Platform : Embedded Die Methods



- Passive integration
- Internal EMI shielding possibilities
- Multi-die capability – more than one die may be embedded
- Two-sided construction – top side components may be mounted

Embedded Die as Package Solution

- **Future package technology requires higher levels of integration, thinness, and cost effective solutions**
  - Planar scaling has ended
  - 3D packaging necessary as integration tool
  - Embedded die is a key enabling package technology that addresses key product roadmap requirements
- **Embedded die in substrate already supported**
  - Passive integration is in high volumes already
  - Active integration is restarting in the industry again
- **Industry now focused on a 'Panel Level Embedded Die' platform to address cost, integration, and scalability**
  - The need for 3D access to the die is increasing

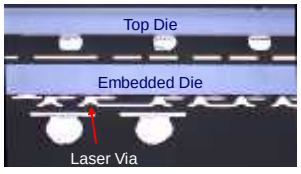
Embedded Passives in Substrate
"EPS"

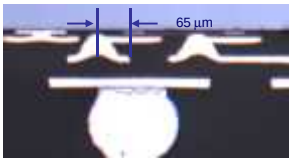
- **Embedding Passive Component (MLCC)**
  - 100nF, 1.0 x 0.5mm
  - High volume production

- **Embedding an Integrated Passives Device (IPD)**
  - 100nF, 1.0 x 1.0mm
  - Production capable ~ no usage today
    - ✓ Issue arises in additional cost to create contact ready pads
    - ✓ + 2 wk delay in cycle time to create pads at bumping house

Embedded Active Die in Substrate
"EDS"

- **Lower Volume Activity Today**
  - Passes all package level tests
  - Small die only with very low I/O
    - ✓ Limited substrate supply base supporting today



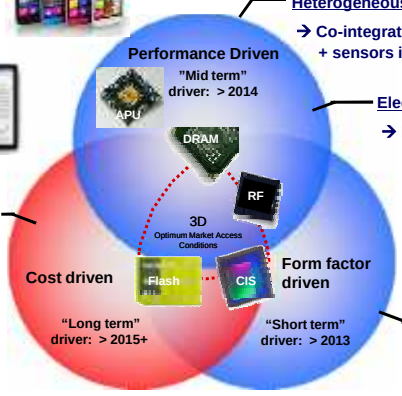


Embedded Die in Substrate Roadmap

	2013	2014	2015	2016	2017
Embedded Die					
• Active	Low Volume / Sample		Production		
• Passive MLCC	Production				
• Passive Silicon (IPD)	Sample Only		Production?		
Key Design Rules					
• Die Size	~ 2 mm		< 4 mm		< 9 mm
• # Die per Cavity					
✓ Silicon	1		2		4
✓ MLCC	1		2		4
• Blind Via / Blind Pad / Via Pitch					
✓ Silicon	65 /150 /180		50 / 120 / 135		50 / 100 / 115
✓ MLCC	65 /250/ NA		50 / 200 / NA		50 / 150 / NA
• Die Thickness					
✓ Silicon	110 um		90-70 um		60 um
✓ MLCC (100nF ; 220nF Future)	150 um		110 um		80 um

Embedded Die Market Drivers

- **The 3D integration of technologies will enable performance, form factor and cost requirements for the next generation of electronic devices**



Heterogeneous integration

→ Co-integration of RF + logic + memory + sensors in a reduced space

Electrical performances

→ Interconnect speed and reduced parasitics ; precision circuitry

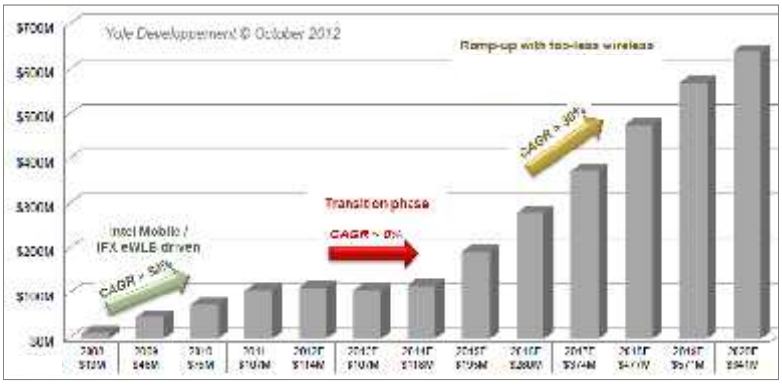
The Ultimate Driver

→ Which version provides the lowest cost option? Cost as the ultimate driver will dictate the optimal / primary direction

Density

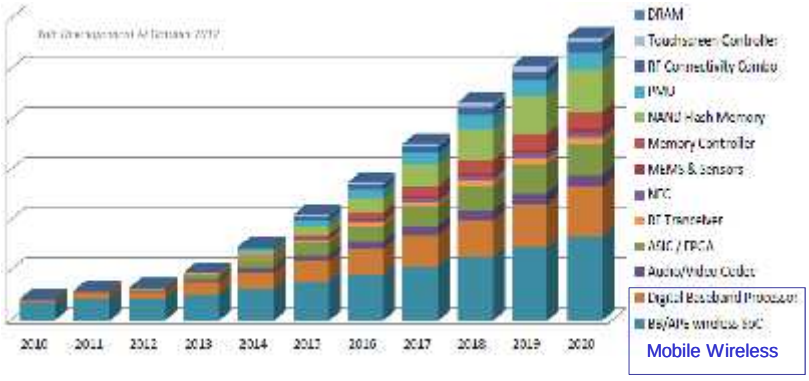
→ Achieving the highest capacity / volume ratio

Embedded Die in Wafer/Panel Projected Growth
(by revenue)



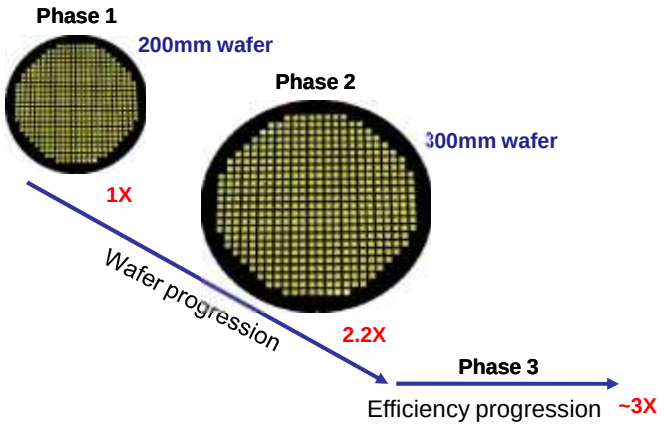
- **Product Need begins to escalate in 2015 for 3D formats**
  - 30% CAGR from 2015 to 2020 time frame
  - Revenue will be $641M /year by 2020

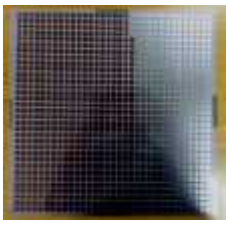
Embedded Die in Wafer/Panel Projections
(by IC type)



- **~ $1 billion market in 2020 if infrastructure can support the growth**
- **Nearly half of all wafers will be consumed by the <u>Mobile Wireless market</u>**

Embedded Die Solutions Strategy



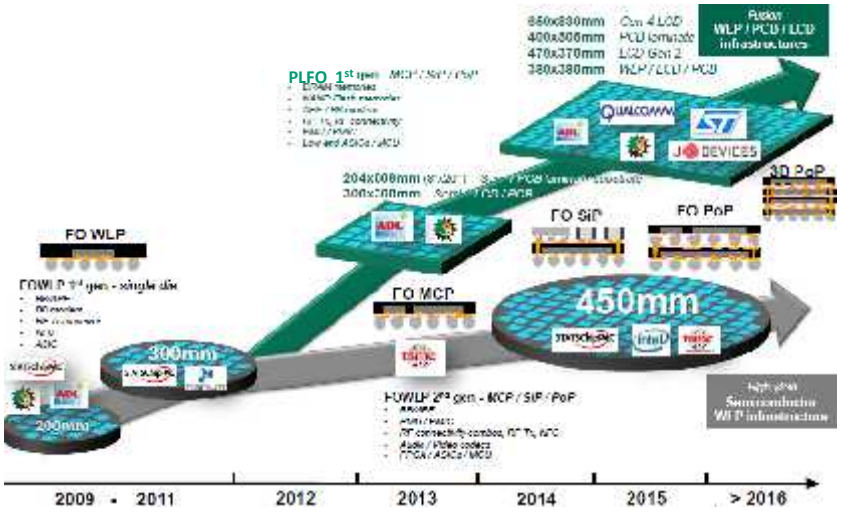


300x300mm panel

- Integration levels increasing
- 3D access required
- Modularization is a focus

… SiP / advanced MCM

Embedded Die Landscape ; Diverging Paths

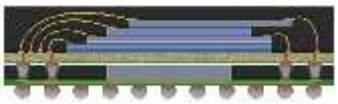


Source: Yole Development

Package-on-Packaging
"Industry Love Affair"

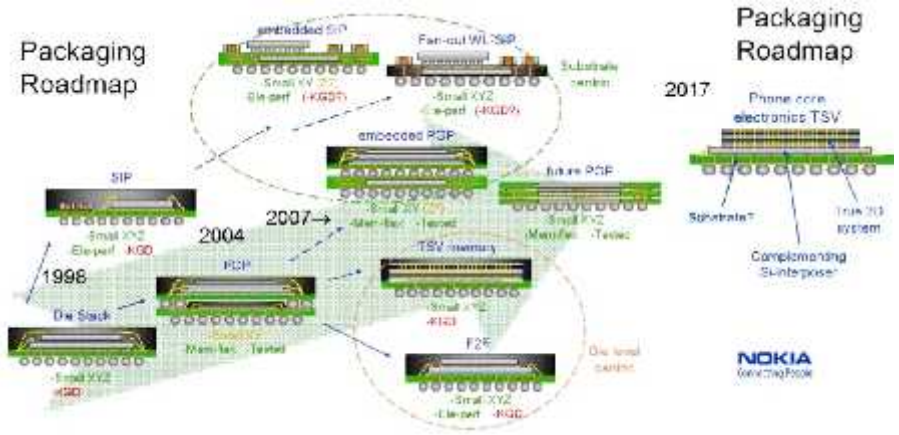
PoP Packaging Advantages

- **Each device is packaged separately**
  - Mature technology and infrastructure
- **Each component is tested and burned-in separately at the package level**
  - Mature technology and infrastructure
- **No margin stacking**
  - Each component is sourced separately by OEM or EMS provider
- **Joining technology widely available**
  - Utilizes standard SMT process and existing manufacturing platform
- **Joining process is very high yielding**
- **Relatively clear ownership of defect liability**
  - Failure analysis methods are mature



PoP Package Roadmap – Nokia

- **IDMs' and OSATs' technical relationship with Cell Phone providers has helped shape their packaging roadmaps**



Source: http://www.imicronews.com/upload/Micronews/images/Nokia_3DIC_TSV_Packaging_Roadmap.jpg

3D Package Roadmap : TMV® (Through Mold Via)

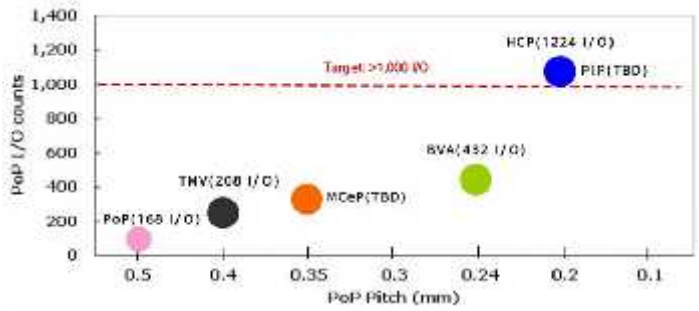
Available	2014	2015	2016
WB TMV 0.5mm memory pitch	Exposed die TMV <0.4mm memory pitch	3D WLFO TMV	TSV TMV
FC TMV 0.5 – 0.4mm memory pitch	Fan-in TMV	F2F TMV	
Possum TMV 0.5 - 0.4mm memory pitch			
Exposed die TMV 0.4mm memory pitch			

3D Package Roadmap : TMV®

	Available	2013	2014	2015
Body size (mm)	8~17	←	←	←
Bottom BGA pitch (mm)	0.40	<0.40	←	←
Stand off height (mm)	0.18	0.13	0.10	0.08
Memory pitch (mm)	0.40	<0.40	←	←
Min. mold cap thickness* (mm)	0.15	0.10	←	←
Substrate thickness (mm) (4-layer)	0.30	0.25	0.23	0.21
Package height(nom., mm)	0.63	0.48	0.43	0.39
Max. stacked-up height** (mm)	1.24	1.09	1.04	1.00

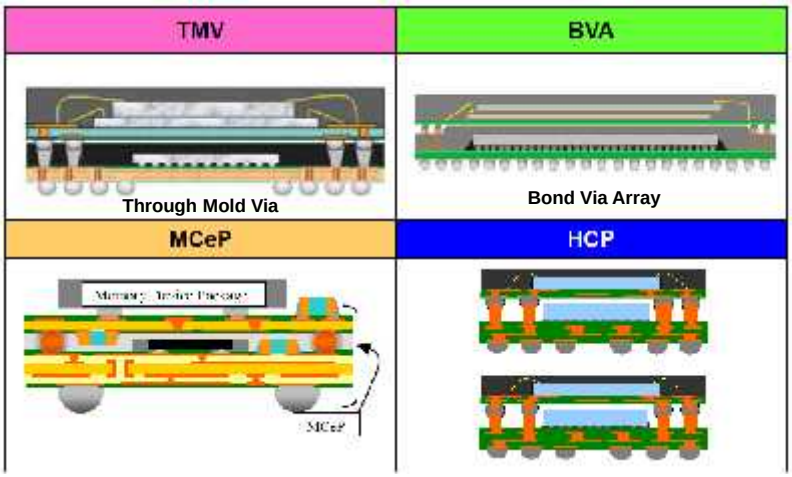
* Single die FC
** Assumed nominal 0.7mm memory (with 0.35mm thick mold)

Advanced PoP Technologies



- TMV® : Through Mold Via — Amkor
- MCeP : Molded Core Embedded Package — Shinko
- BVA : Bond Via Array — Invensas
- PIP : Package Interposer Package — IBM
- HCP : High Copper Pillar — Unimicron

Advanced PoP Technology Comparison



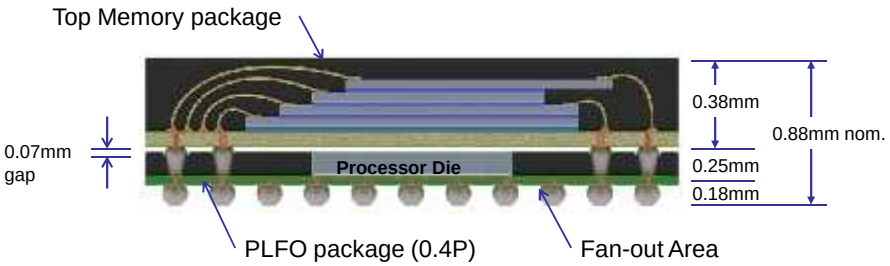
Advanced PoP Technology Comparison, cont.

- **Fan-In Technologies**

PoP Approach	TMV	BVA	PIP	MCeP	HCP
Developer	Amkor	Invensas	Endicott Interconnect	Shinko	Unimicron
Structure					
Key Feature	Through mold via	Cu wire + mold	Interposer	Cu solder ball	High Cu Pillar
Min. pitch demonstration	0.4 mm	0.24 mm	-	0.35 mm	0.2 mm

✓ Package height, pitch, and cost will determine winner

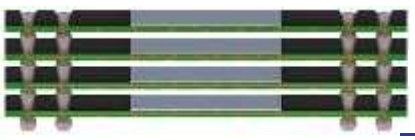
3D PoP Panel Level Fan-Out



- Standard Fan-Out technology can be expanded in the vertical (Z) direction when connecting it as a 3D PoP structure
- This is enabled through the use of advanced laser and via fill processes
- Opportunity for improved electrical performance due to low impedance interconnects and dielectric stack-up

3D Fan-Out Memory Packages

3D PoP Fan Out **vs.** **Laminate-based Technology**

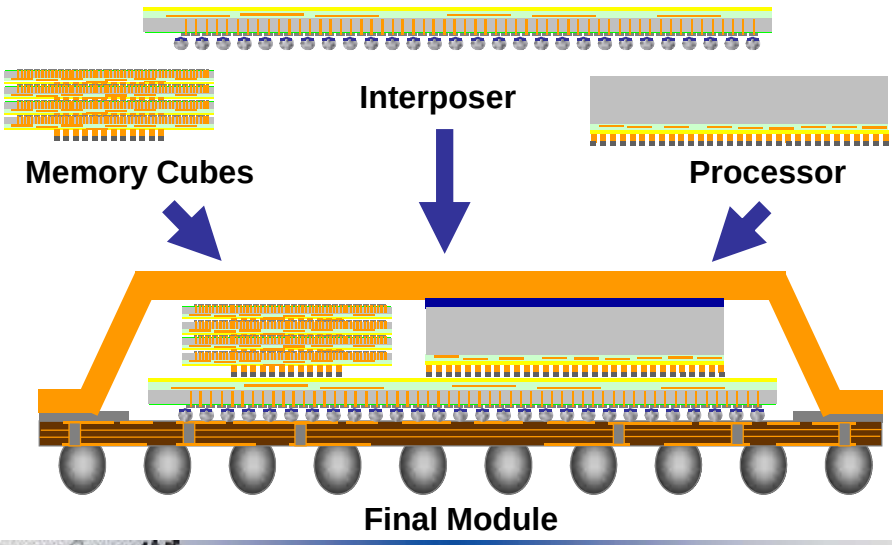


3D PoP Memory Package Stack-up

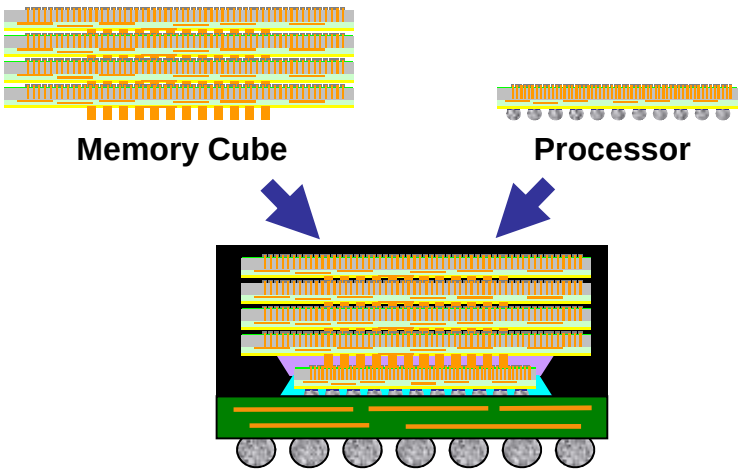
Item	3D PoP PLFO
Encapsulate	0.10mm
Substrate (2L) (PLFO: 2 layer RDL)	0.05mm
BGA (0.4mm pitch)	0.10mm
Total thickness (nom)	0.25mm

- 3D PoP Fan-Out provides the opportunity to achieve very low profile package stacks due to the elimination of the traditional laminate substrate

SiP Packages – TSV

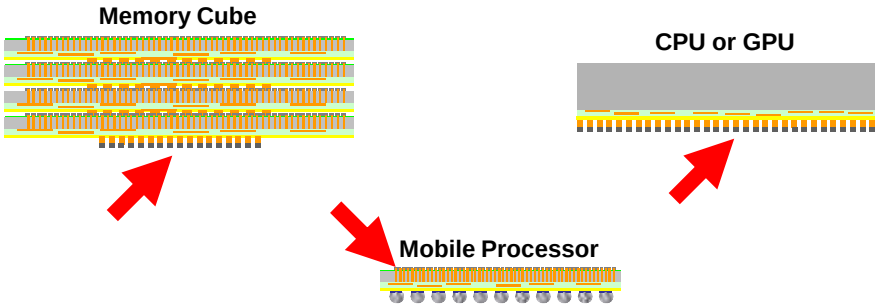


SiP Packages – TSV



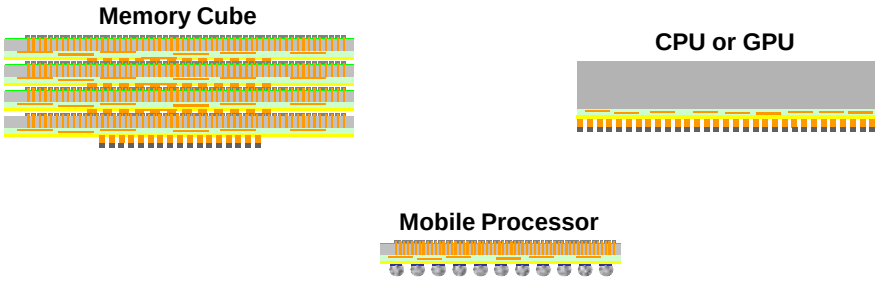
Probe Contact Challenges

- Probe contacting infrastructure is not mature for fine pitch area array contacts
- 100s to 1000s of contacts per die at 40um pitch
- Difficult to probe thin wafers, 2-sided wafers



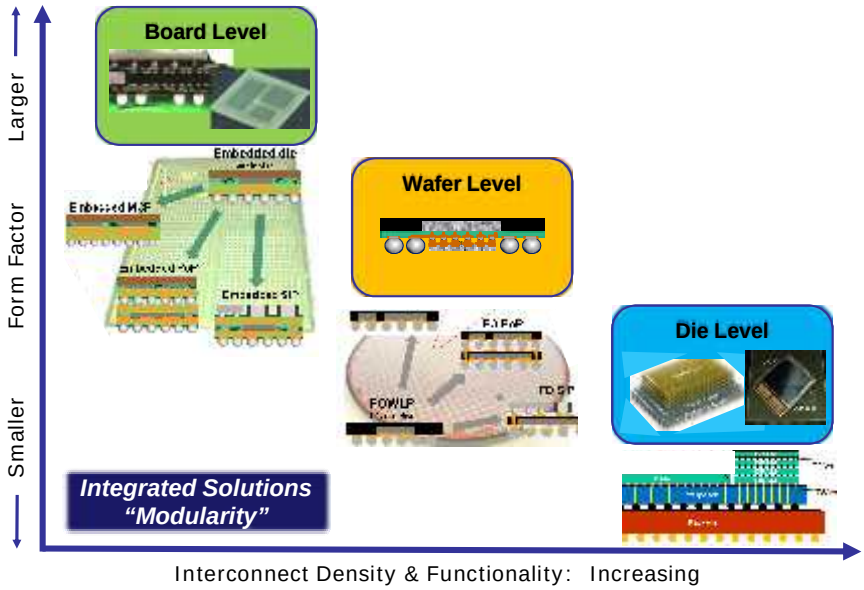
Burn-in Challenges

- Infrastructure to burn-in bare die or wafers with fine pitch area array connections is not mature
- Difficult to properly heat sink high power devices in bare die or wafer format
- Stresses during burn-in of bare die are not likely equivalent to stresses during burn-in of packaged die

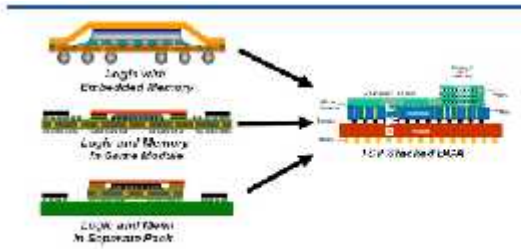


Package Migration to System Level Integration

Advanced Package Integration

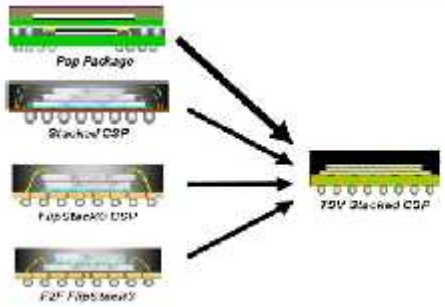


Package Migration to SiP – MCM Integration



2.5D MCM - GPU, GPU, Networking

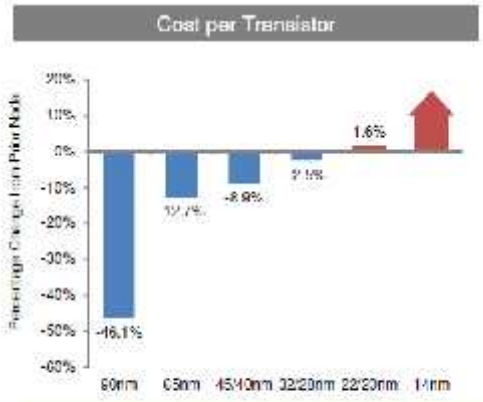
- 100X Improvement in Inter-Die Bandwidth / Watt
- 50% Power Savings
- 6X Latency Reduction
- 20X denser Wire Pitch



3D - Smartphones, Tablets, Memory

- 8X Performance in Bandwidth
- 50% Power Savings
- Profile Improvement

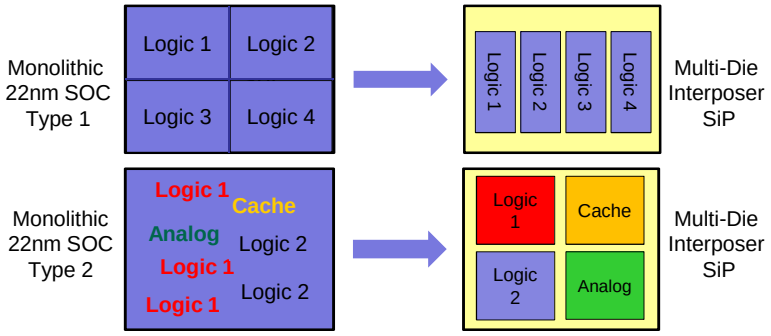
Advanced Silicon Nodes Driving Higher Costs



- For the First Time Ever, Wafer Price Increases Eliminating Scaling Benefits at 22/20nm
- Substantial Process R&D
- Increased Equipment Costs
- Lithography Now 50% of Wafer Costs

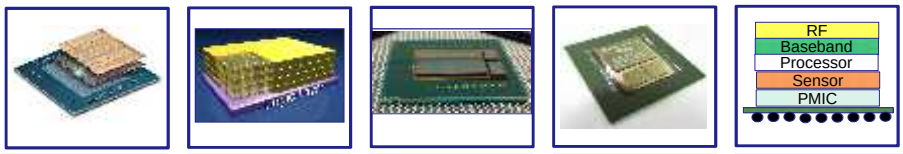
Use Advanced Packaging to Minimize or Reduce the Number of Layers of Circuitry that Need to Be Created on the Wafer

SOC to 2.5D TSV MCM SiP Drivers



- **Focus Process Node Development on Specific Application Functionalities**
  - ✓ Reduces complexity and mask layer count of process node
  - ✓ Improves wafer yield
  - ✓ Reduces wafer start cost
  - ✓ Improves performance, power, and area of each application

Long Term Advanced Packaging Roadmap



2.5D TSV 20nm Partitioning Cu Pillar C-o-C	Memory Cube Package Stacking C-o-C	2.5D GPU + HBM TSV Embedded Die	2.5D TSV 14nm Partitioning APU SoC Deconstruct	3D TSV Heterogeneous Die Stacking Si Photonics
Market: FPGA	Market: Mobile Network	Market: Processors Network Tablet	Market: Processors Network Mobile, Tablet	Market: Processors Network Mobile, Tablet
2013	2014	2015	2016	2017

Time

Advanced Package Integration Roadmap