Stacking Untested Wafers to Improve Yield

or

3D: Where the Timid Go to Die

The 3D Enigma

The Promise

- High Performance
- Low Power
- Improved Density

More than Moore
or at least
as much as Moore

The Reality

- A decade of "next year"
- High costs
- Low yields
- Non-existent ecosystem
- Loss of credibility

Tezzaron

Historic Precedent
Tezzaron

Poor Science
Tezzaron

Excessive Complexity

Tezzaron

Fear

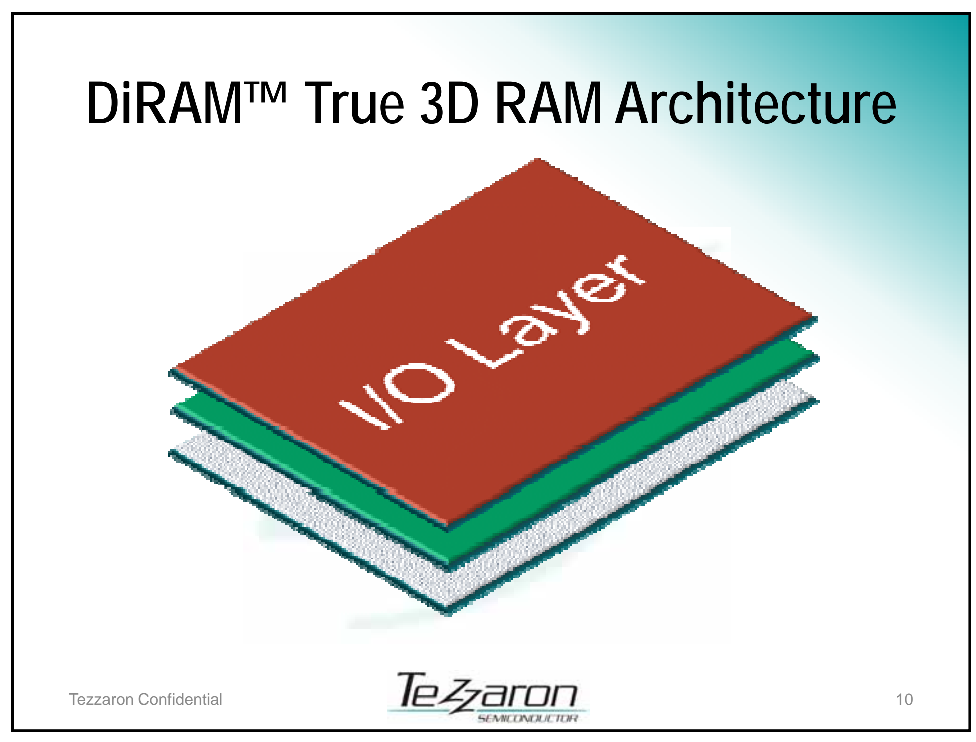
Tezzaron

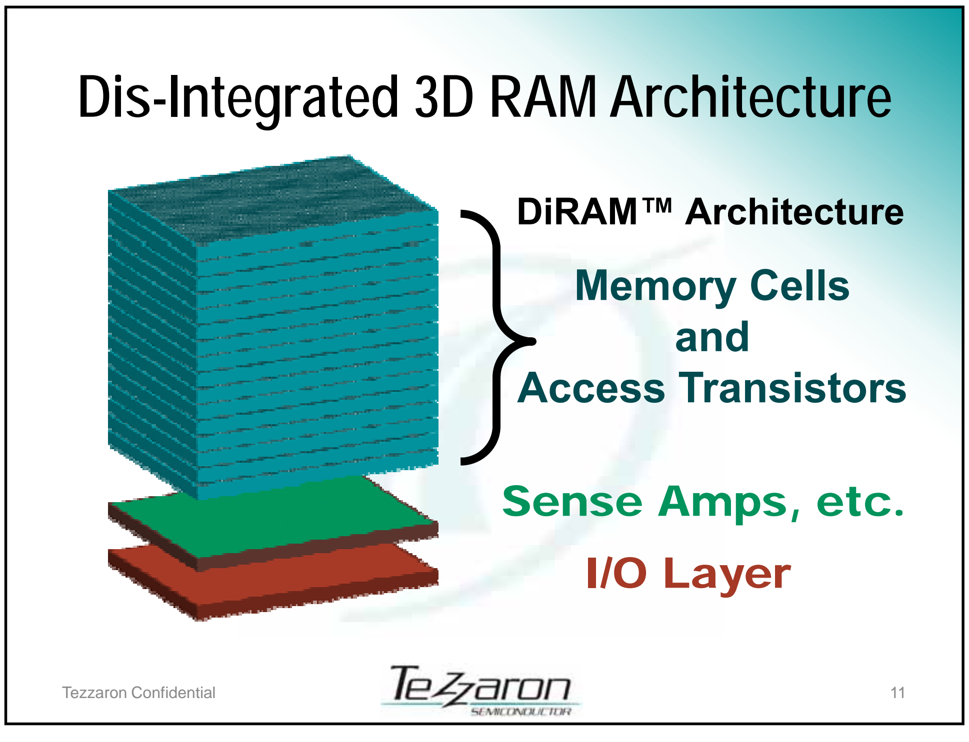
Heroes focus on Landing

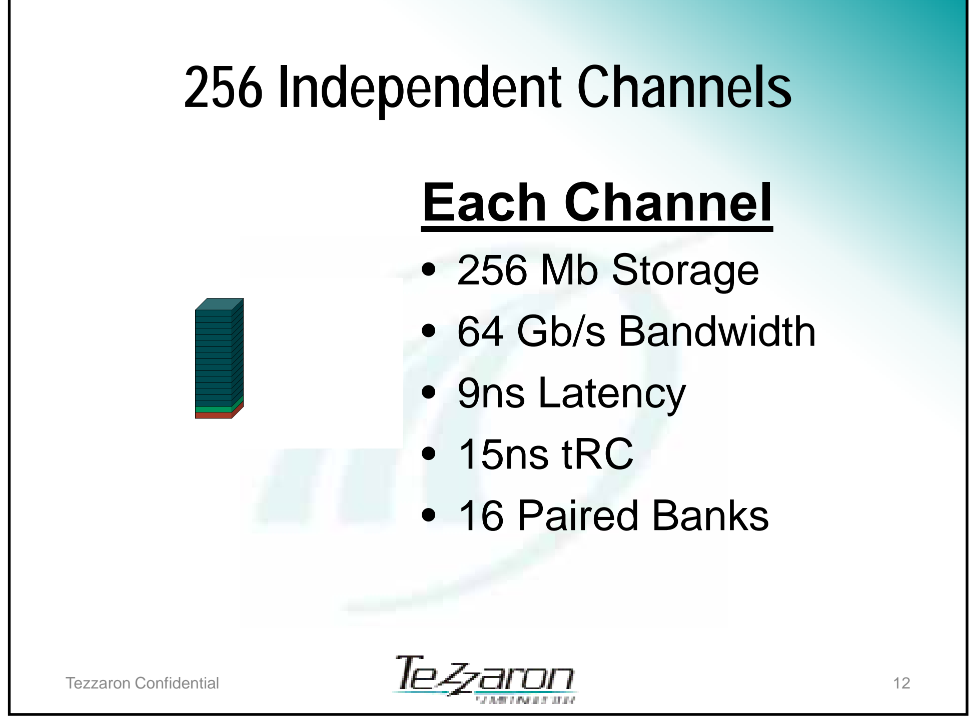
US Airways Flight 1549 in the Hudson River
– Capt. Chesley Sullenberger in command.

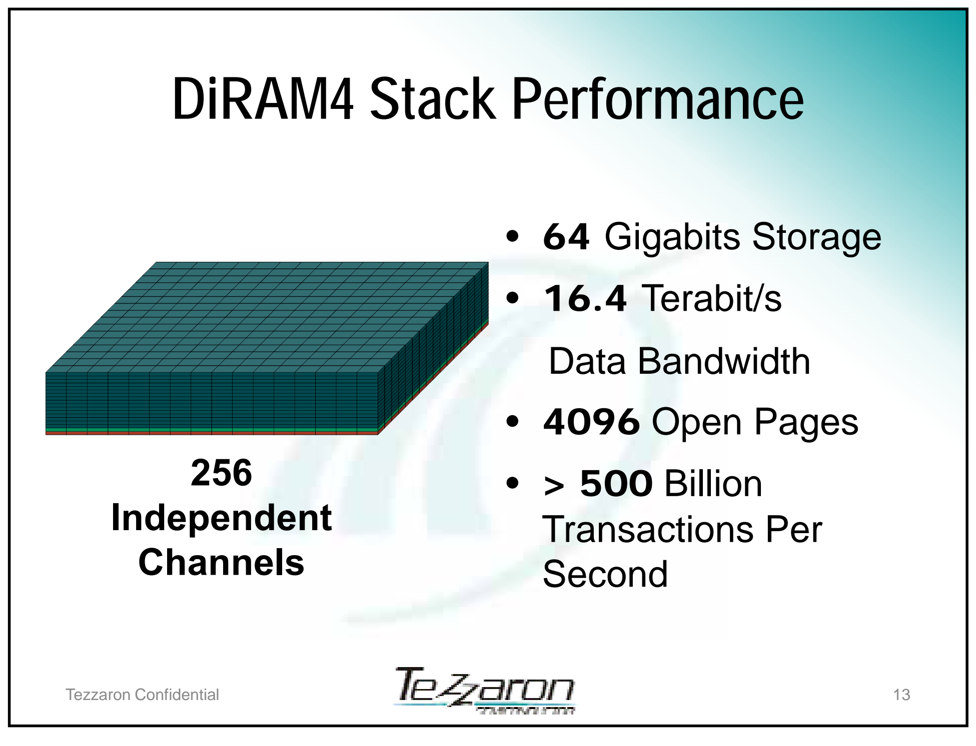
Tezzaron

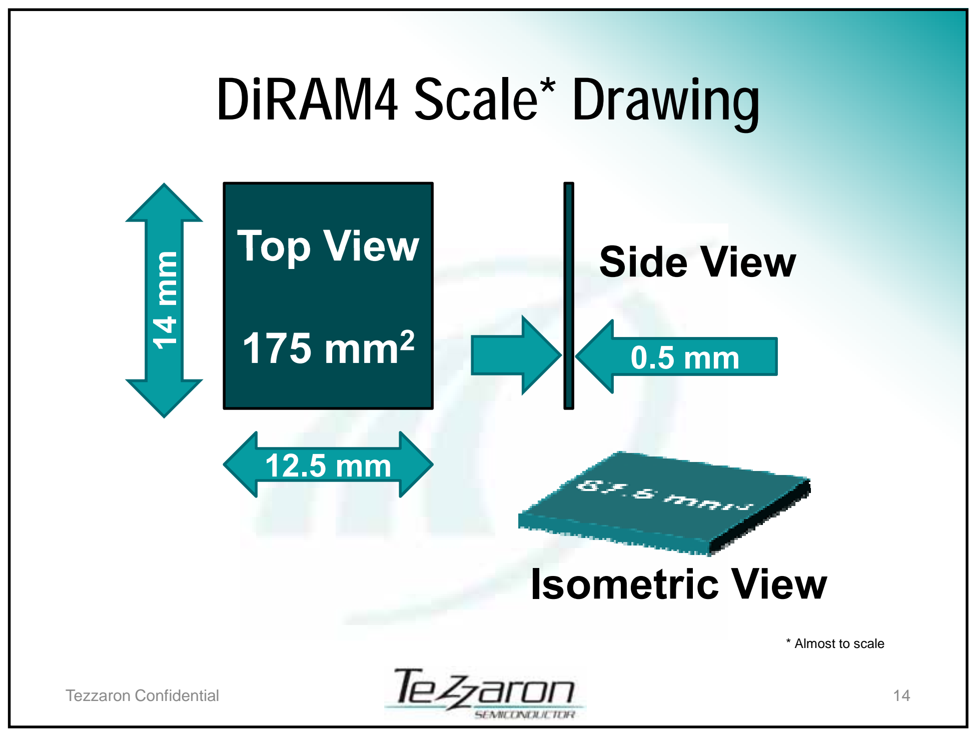
Step 1: Commit to 3D
Tezzaron

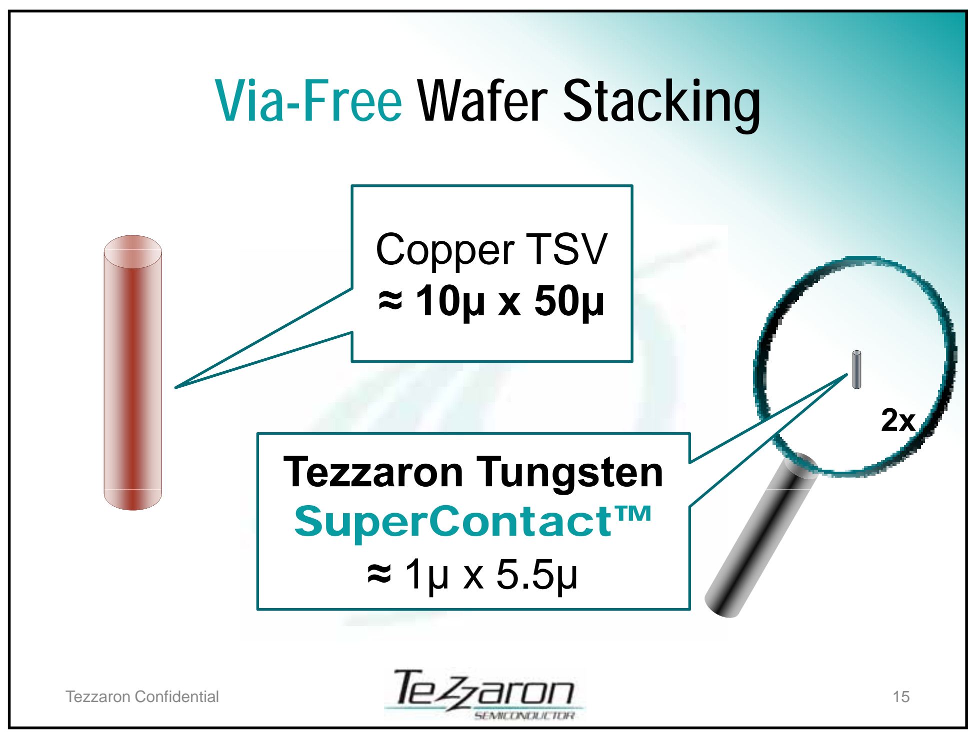

DiRAM™ True 3D RAM Architecture
I/O Layer
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
10

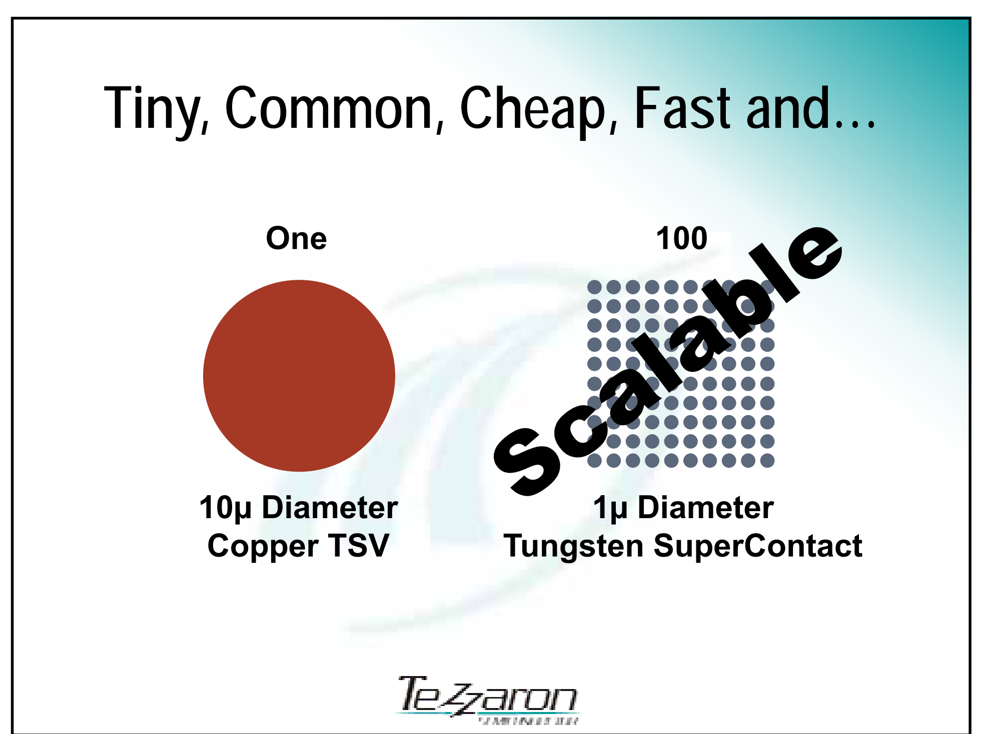

Dis-Integrated 3D RAM Architecture
DiRAM™ Architecture
Memory Cells
and
Access Transistors
Sense Amps, etc.
I/O Layer
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
11


256 Independent Channels
Each Channel
• 256 Mb Storage
• 64 Gb/s Bandwidth
• 9ns Latency
• 15ns tRC
• 16 Paired Banks
Tezzaron Confidential
Tezzaron
12


DiRAM4 Stack Performance
256 Independent Channels
• 64 Gigabits Storage
• 16.4 Terabit/s Data Bandwidth
• 4096 Open Pages
• > 500 Billion Transactions Per Second
Tezzaron Confidential
Tezzaron
13


DiRAM4 Scale* Drawing
14 mm
Top View
175 mm²
12.5 mm
Side View
0.5 mm
Isometric View
* Almost to scale
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
14


Via-Free Wafer Stacking
Copper TSV
≈ 10μ x 50μ
Tezzaron Tungsten
SuperContact™
≈ 1μ x 5.5μ
2x
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
15


Tiny, Common, Cheap, Fast and…
One
100
Scalable
10μ Diameter
Copper TSV
1μ Diameter
Tungsten SuperContact
Tezzaron

Radically Different Manufacturing

Conventional Flow

- Fabricate Wafer
- Probe Test Die
- Thin Wafer
- Singulate Die
- Stack Good Die
- Package Stack
- Burn-In & Test Stack

Tezzaron Flow

- Fabricate Wafer
- **Stack Wafers**
- **Thin Top Wafer**
- ***Repeat***
- **Probe Test Stacks**
- **Singulate Stacks**
- Package Stacks
- Burn-In & Test Stack

Tezzaron Confidential

17

Never Handle A Thin Wafer

The Tezzaron Mantra

Bond Two…Grind One

…to make the world's thinnest RAM wafers

Tezzaron Confidential

18

"That can't work..."

"...bonding un-tested die will produce **near zero yields**, **poor reliability** and **high costs**."

Translation

You Tezzaron people are crazy!

Tezzaron Confidential 19

Novati Technologies - Austin

- Tezzaron subsidiary
  - Manufacturing volume
  - Services available
- 3D Assembly Options
  - Cu-Cu
  - DBI®,
  - Oxide Bonding
  - Intermetallic
  - Gold-Indium, Gold-Gold
- Silicon Interposers
  - Passive
  - Passive Plus
  - Active

Tezzaron Confidential 20

Super dense interconnect allows…

Bi-STAR™

Built-**i**n **S**elf **T**est **A**nd **R**epair

- Controlled by **embedded ARM processor**
- Enabled by **per-cell** control interconnect
- Super-fine grained test and repair
- Continuous, in-the-system hard and soft error repair

Tezzaron Confidential

21

Bi-STAR™ Does More, Works Better

Bi-STAR Repairs

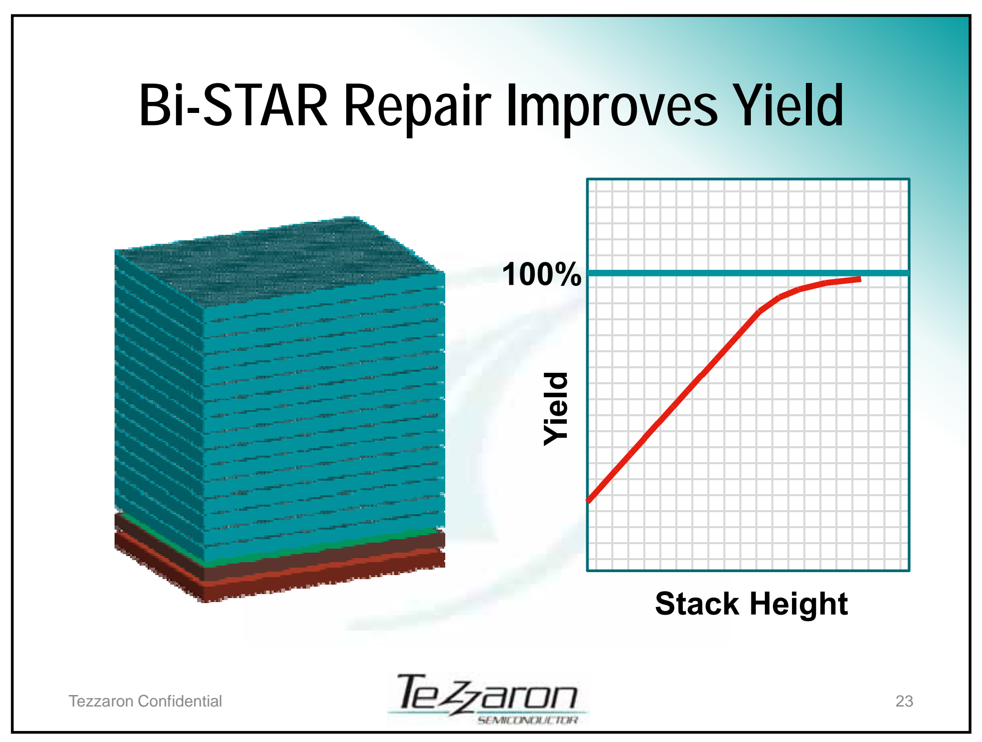
- Bad memory cells
- Bad line drivers
- Bad sense amps
- Shorted word lines
- Shorted bit-lines
- Leaky bits
- Bad secondary bus drivers

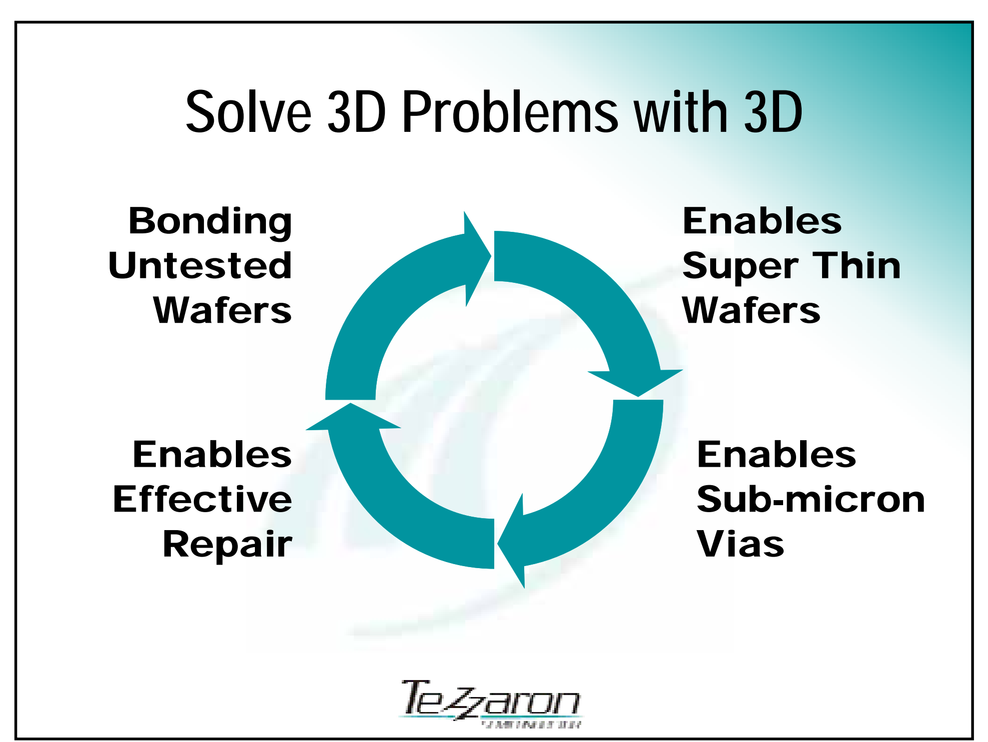
Bi-STAR Tests

- Tests > 300,000 nodes per clock cycle
- Tests > 1,000x faster than external memory tester
- Via SPI port, works with Host to allow continuous scrub / repair

Tezzaron Confidential

22


Bi-STAR Repair Improves Yield
100%
Yield
Stack Height
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
23


Solve 3D Problems with 3D
Bonding Untested Wafers
Enables Super Thin Wafers
Enables Sub-micron Vias
Enables Effective Repair
Tezzaron

DiRAM: Efficiency for the Future

- **Less aggressive wafers**
- **Higher array efficiency**
- **Much lower test cost**
- **Higher yield**
- **Longer product life cycles**

Tezzaron Confidential

25

DiRAM: Efficiency for the Future

- **Less aggressive wafers**
- **Higher array efficiency**
- **Much lower test cost**
- **Higher yield**
- **Longer product life cycles**

Tezzaron Confidential

26

High End Routing

Tasks

- **Packet Buffer**
  (Burst Read/Write)
- **Tables**
  (Read Dominated)
- **Stats**
  (Read-Mod-Write)

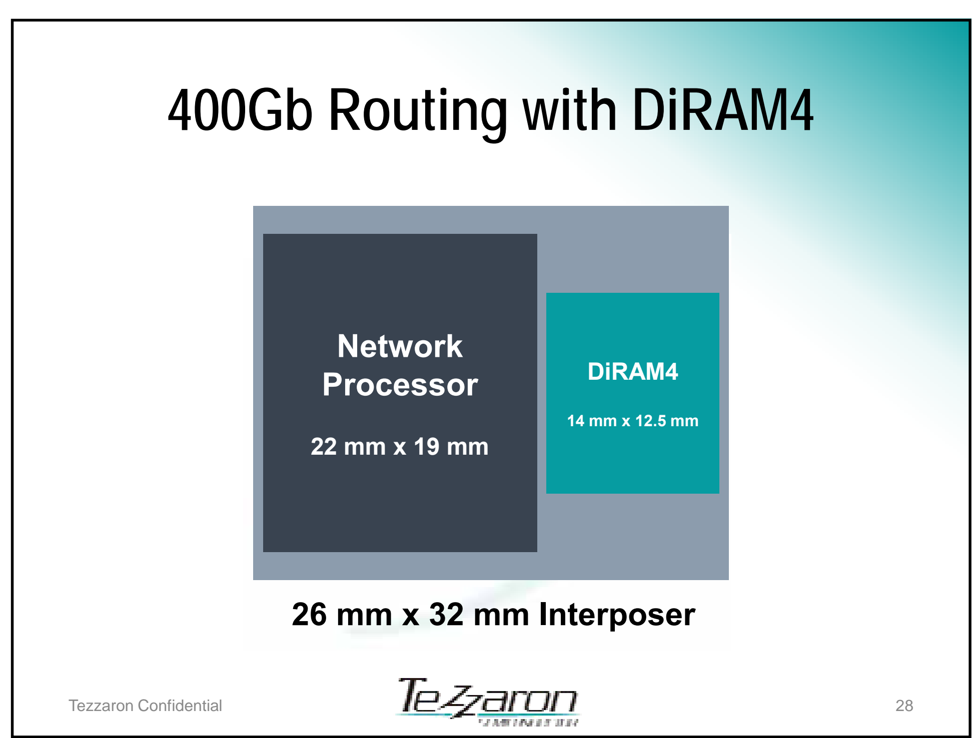
Performance Metrics

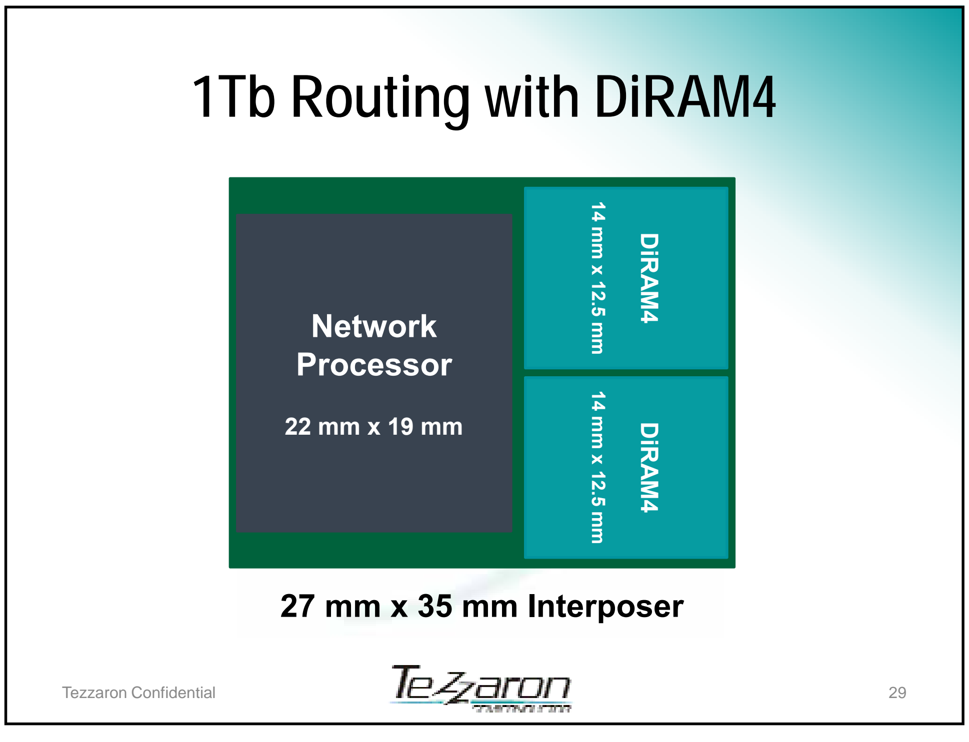
- **Density**
  – Line Rate / Seconds
- **Bandwidth**
  – Line Rate x 2.5
- **Transaction Rate**
  – Transactions x Line Rate / Min Packet Size

Tezzaron Confidential

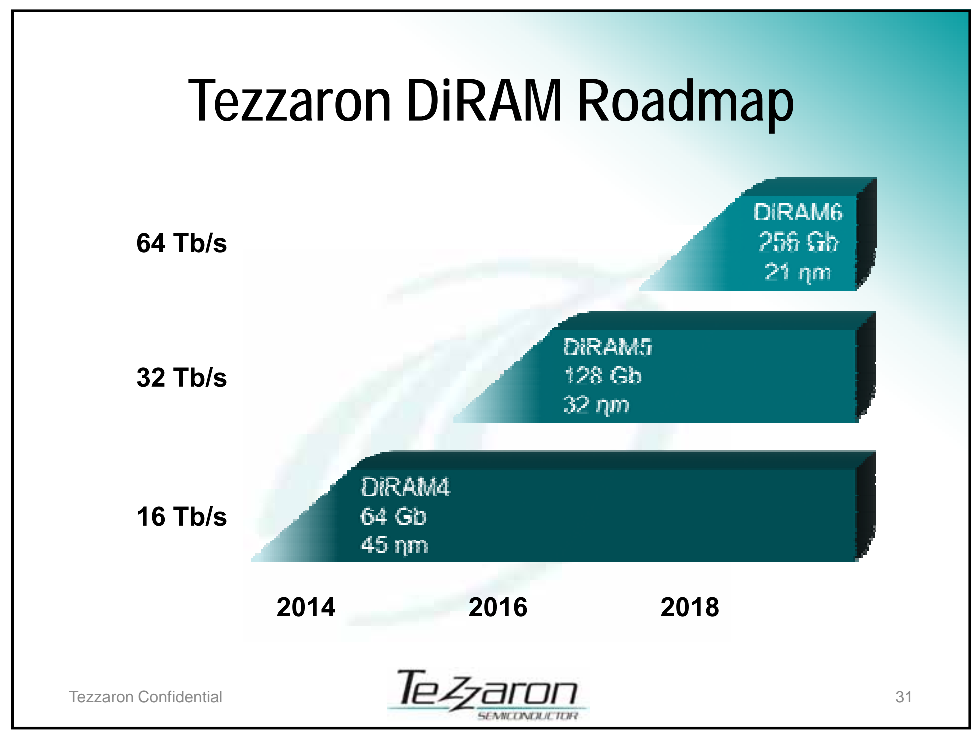
27

400Gb Routing with DiRAM4




1Tb Routing with DiRAM4
Network Processor
22 mm x 19 mm
DiRAM4
14 mm x 12.5 mm
DiRAM4
14 mm x 12.5 mm
27 mm x 35 mm Interposer
Tezzaron Confidential
Tezzaron
29

The Right I/O for Each Market
DiRAM4
Launches
with
0.7 V CMOS I/O
2.5D Si or Organic
• Low Power
• High Performance
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
30


Tezzaron DiRAM Roadmap
64 Tb/s
32 Tb/s
16 Tb/s
DiRAM6
256 Gb
21 nm
DiRAM5
128 Gb
32 nm
DiRAM4
64 Gb
45 nm
2014
2016
2018
Tezzaron Confidential
Tezzaron
SEMICONDUCTOR
31

Tezzaron
SEMICONDUCTOR
David Chapman
VP Marketing &
Technical Sales
512-356-2534
dchapman@tezzaron.com
Tezzaron Confidential
Tezzaron
32