High performance datacenter platform: Using InP for Silicon Photonics?

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Maybe this is topic is suitable for the 'next generation' IC?

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Abstract of the talk

- Overview
  - Is a high-performance datacenter platform using InP a silicon photonics play? This issue will be addressed.
  - Designing and packaging InP-based PICs (Photonic Integrated Circuits) & OEICs (Optoelectronic Integrated Circuits) will be discussed.
  - ***A review of packaging technologies for datacom products will be made.***
  - Particular attention will be a focus on a highly reliable and robust platform with Photonic Integrated Circuits (PICs) that have included lasers, modulators, detectors, waveguides, Mux/Demux, and large spot converters by OneChip Photonics.
  - Current products are focused on both client-side and line-side applications in data and tele-communications networks. Initial performance levels indicate suitability for 100Gb/s datacenter and 50Gb/s metro opportunities using OneChip's InP-based OEIC platform.

Common denominator is packaging…

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Agenda

- What drives a next generation IC?
  - Photonics packaging
    - History of and evolution over 50yrs
    - Silicon for photonics packaging
    - Non-hermetic packaging
    - One example of 'generic' PIC packaging today
  - Drivers for photonics integration…
    - Next generation IC → Photonic Integrated Circuit (PIC)
    - Optoelectronic Integrated Circuit (OEIC)
    - Silicon photonics (and the need for InP lasers)
    - Photonics integration drivers:
      - Miniaturization (and higher traffic capacity)
      - Fast growing markets
      - The very essence of 'green photonics'
      - OIDA's movement to accelerate the segment in 2013
- Takeaways…

(Packaging: first four sub-items; PIC/OEIC chips: second group)

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Part 1: Packaging (it's actually critical): a quick history…

5

Where have we come from?

Progress over the past 50+ years for photonics packaging to reach a maturity level to address PICs/OEICs and the next generation IC…

~1962

In the beginning, the humble crystal triode (later known as transistor)

~1965

And the germanium photo transistor OCP71

(just remove the black paint guys)

Packaging: critical for next generation IC…

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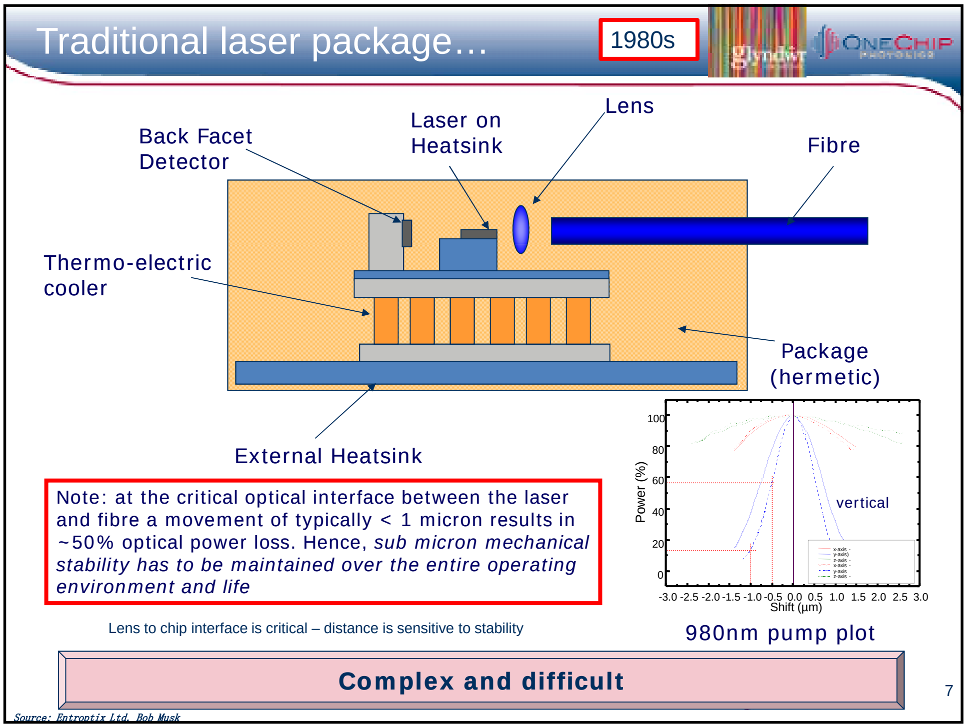
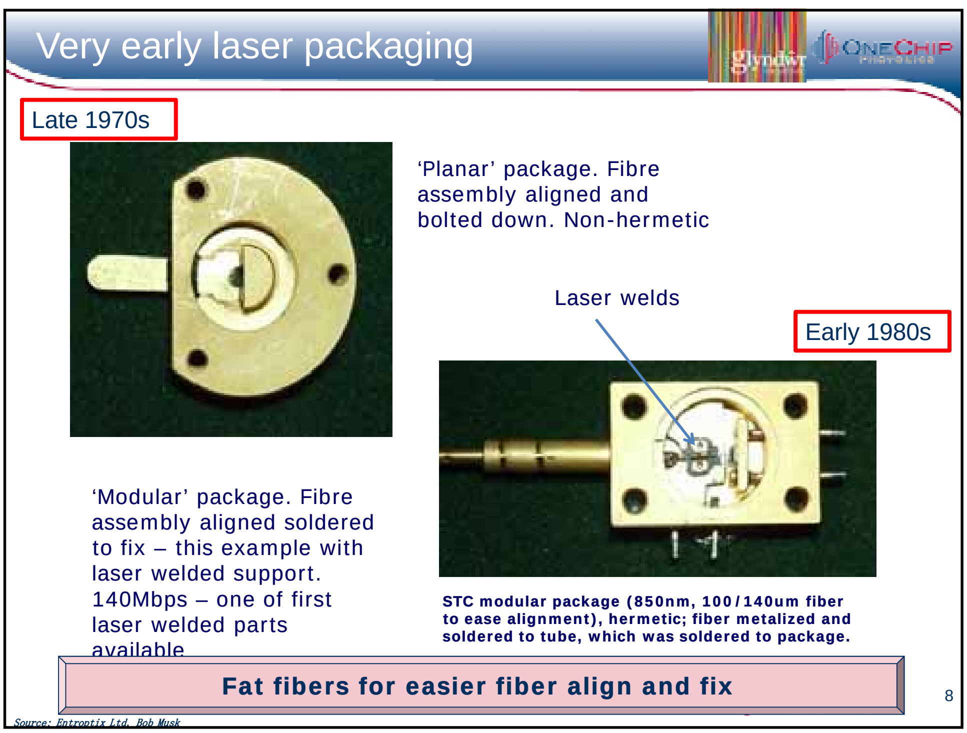
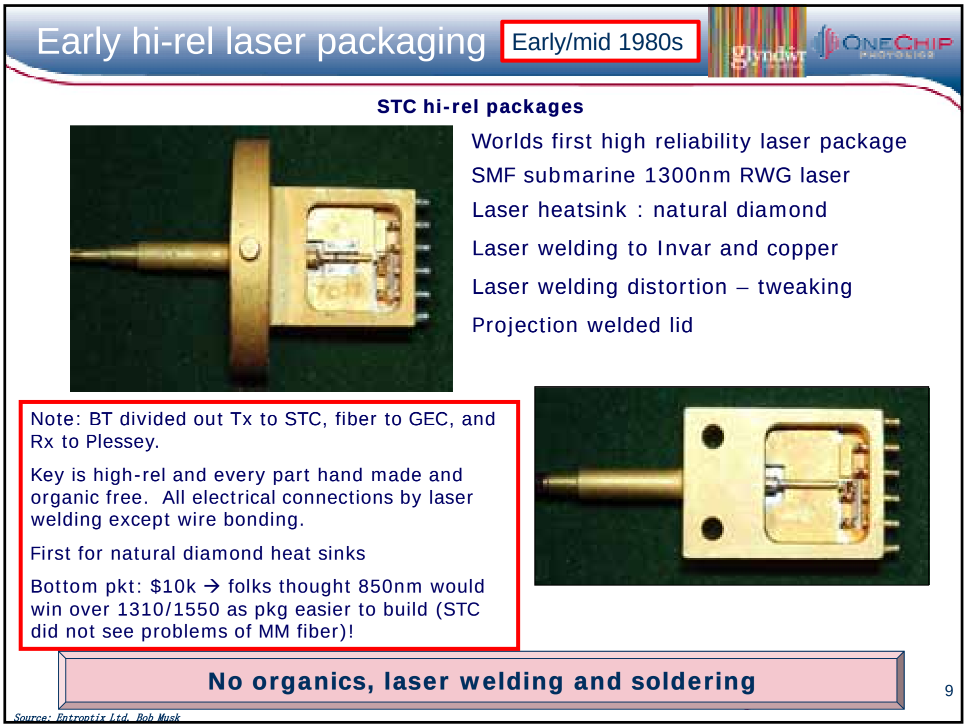
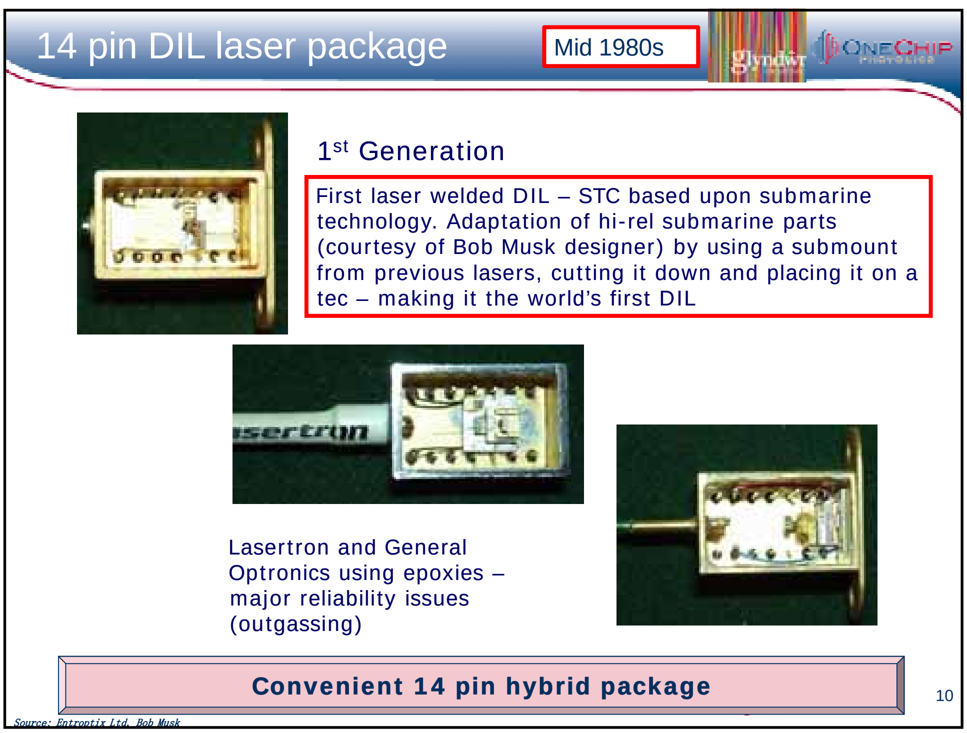
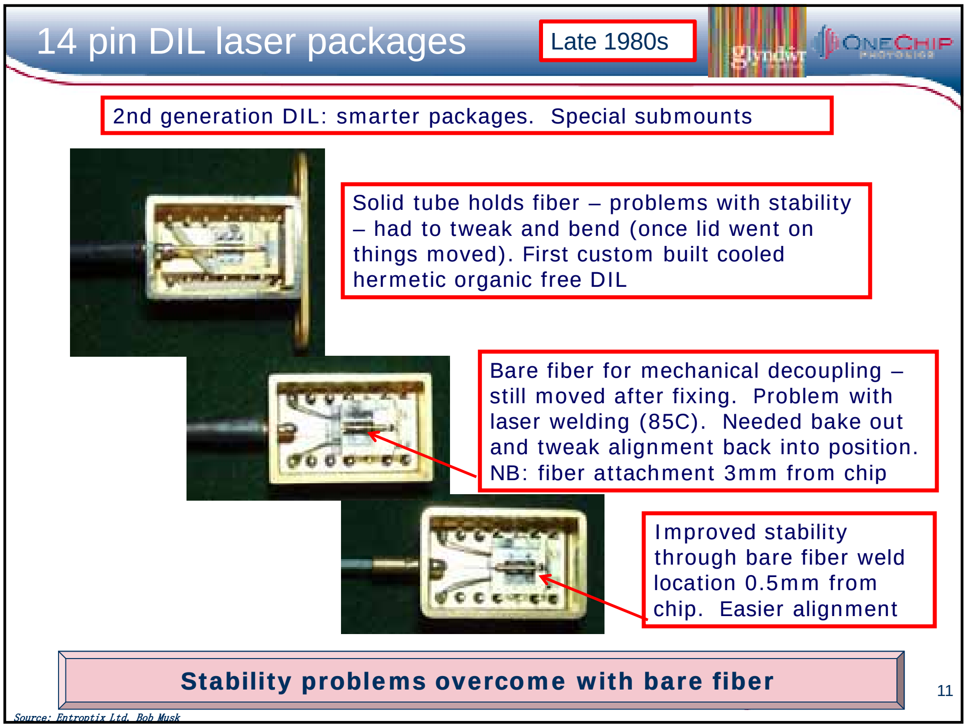
Source: Entroptix Ltd, Bob Musk


Traditional laser package…
1980s
Back Facet
Detector
Laser on
Heatsink
Lens
Fibre
Thermo-electric
cooler
Package
(hermetic)
External Heatsink
Power (%)
Shift (µm)
vertical
980nm pump plot
Note: at the critical optical interface between the laser and fibre a movement of typically < 1 micron results in ~50% optical power loss. Hence, sub micron mechanical stability has to be maintained over the entire operating environment and life
Lens to chip interface is critical – distance is sensitive to stability
Complex and difficult
7
Source: Entroptix Ltd, Bob Musk


Very early laser packaging
Late 1970s
'Planar' package. Fibre assembly aligned and bolted down. Non-hermetic
Laser welds
Early 1980s
'Modular' package. Fibre assembly aligned soldered to fix – this example with laser welded support. 140Mbps – one of first laser welded parts available
STC modular package (850nm, 100/140um fiber to ease alignment), hermetic; fiber metalized and soldered to tube, which was soldered to package.
Fat fibers for easier fiber align and fix
8
Source: Entroptix Ltd, Bob Musk


Early hi-rel laser packaging
Early/mid 1980s
STC hi-rel packages
Worlds first high reliability laser package
SMF submarine 1300nm RWG laser
Laser heatsink : natural diamond
Laser welding to Invar and copper
Laser welding distortion – tweaking
Projection welded lid
Note: BT divided out Tx to STC, fiber to GEC, and Rx to Plessey.
Key is high-rel and every part hand made and organic free. All electrical connections by laser welding except wire bonding.
First for natural diamond heat sinks
Bottom pkt: $10k → folks thought 850nm would win over 1310/1550 as pkg easier to build (STC did not see problems of MM fiber)!
No organics, laser welding and soldering
9
Source: Entroptix Ltd, Bob Musk


14 pin DIL laser package
Mid 1980s
1st Generation
First laser welded DIL – STC based upon submarine technology. Adaptation of hi-rel submarine parts (courtesy of Bob Musk designer) by using a submount from previous lasers, cutting it down and placing it on a tec – making it the world's first DIL
Lasertron and General Optronics using epoxies – major reliability issues (outgassing)
Convenient 14 pin hybrid package
10
Source: Entroptix Ltd, Bob Musk


14 pin DIL laser packages
Late 1980s
2nd generation DIL: smarter packages. Special submounts
Solid tube holds fiber – problems with stability – had to tweak and bend (once lid went on things moved). First custom built cooled hermetic organic free DIL
Bare fiber for mechanical decoupling – still moved after fixing. Problem with laser welding (85C). Needed bake out and tweak alignment back into position. NB: fiber attachment 3mm from chip
Improved stability through bare fiber weld location 0.5mm from chip. Easier alignment
Stability problems overcome with bare fiber
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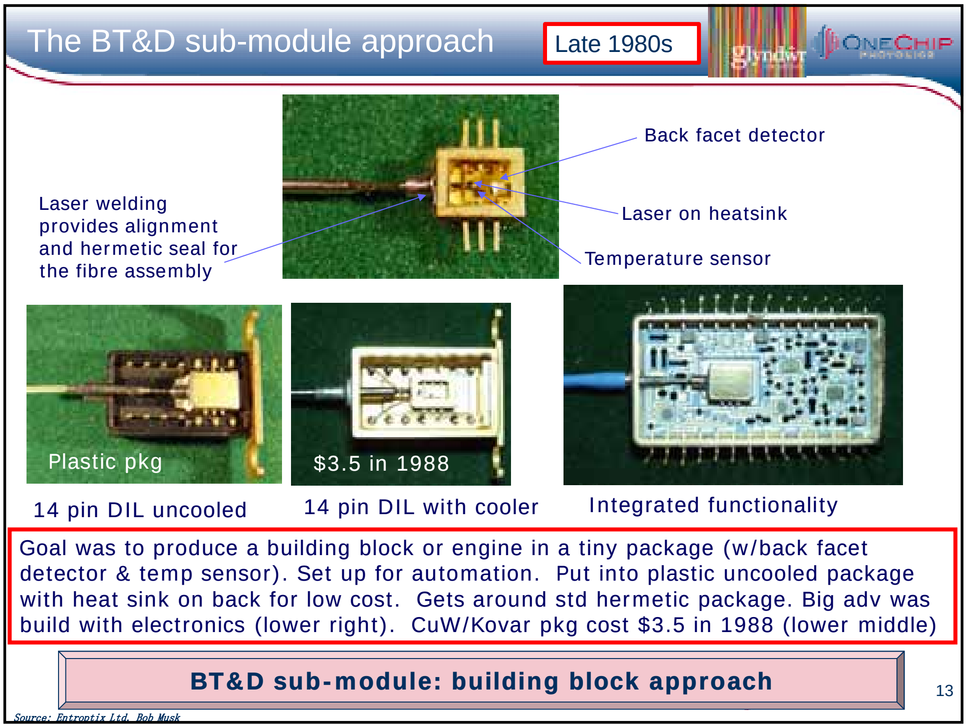
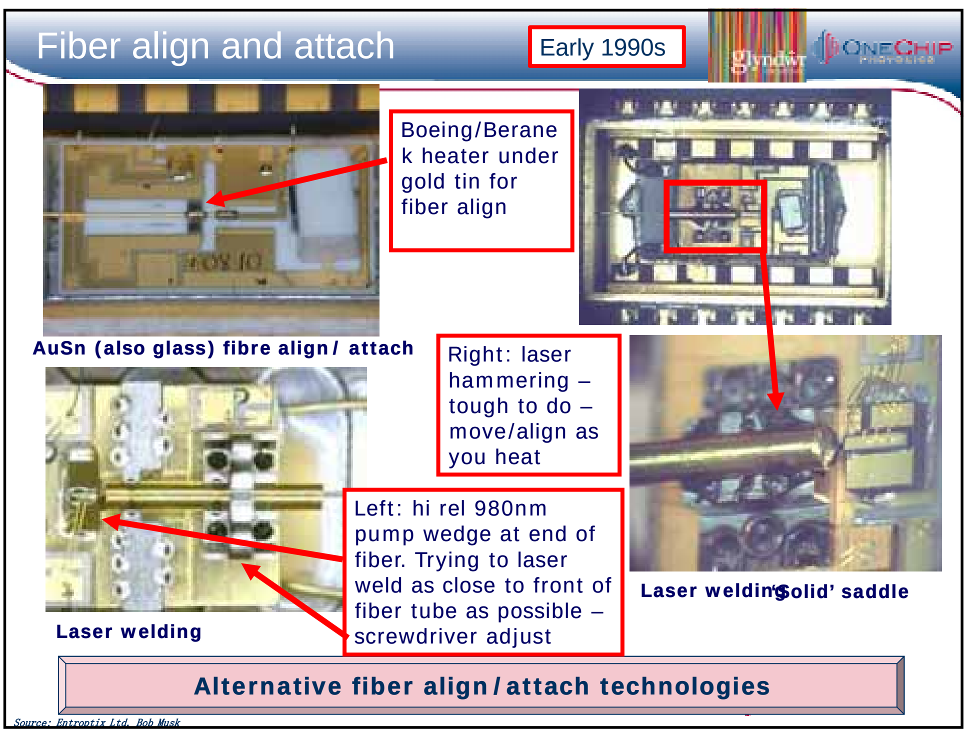
Source: Entroptix Ltd. Bob Musk

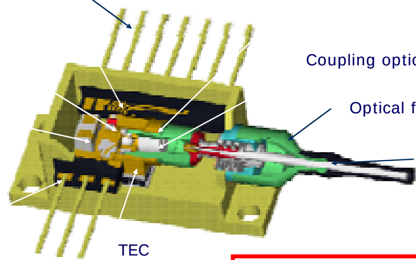

DIL laser packages
Late 1980s (3rd gen)
1st Generation
2nd generation
3rd generation
1st and 2nd generation use RWG lasers with a TEC cooler. 3rd gen do not need TEC and use BH laser 1310nm. Pin configuration is same as cooled DIL. First surface mount – fiber could only withstand 85C max. Detachable allows easier manf/ & SM. First non-hermetic and std IC plastic encapsulation lead techniques
3rd generation mini DIL and plastic
12
Source: Entroptix Ltd. Bob Musk


The BT&D sub-module approach
Late 1980s
Laser welding provides alignment and hermetic seal for the fibre assembly
Back facet detector
Laser on heatsink
Temperature sensor
Plastic pkg
$3.5 in 1988
14 pin DIL uncooled
14 pin DIL with cooler
Integrated functionality
Goal was to produce a building block or engine in a tiny package (w/back facet detector & temp sensor). Set up for automation. Put into plastic uncooled package with heat sink on back for low cost. Gets around std hermetic package. Big adv was build with electronics (lower right). CuW/Kovar pkg cost $3.5 in 1988 (lower middle)
BT&D sub-module: building block approach
13
Source: Entroptix Ltd. Bob Musk


Fiber align and attach
Early 1990s
Boeing/Berane k heater under gold tin for fiber align
AuSn (also glass) fibre align / attach
Right: laser hammering – tough to do – move/align as you heat
Left: hi rel 980nm pump wedge at end of fiber. Trying to laser weld as close to front of fiber tube as possible – screwdriver adjust
Laser welding
Laser welding
'Solid' saddle
Alternative fiber align / attach technologies
Source: Entroptix Ltd. Bob Musk

14 pin butterfly package

~2000s



Extremely complex structure

High piece part count (>20)

Not designed for automation

EXPENSIVE

Metal bellows around fiber to decouple from package. Collimated lens system with isolator.

Alternative approaches - expensive

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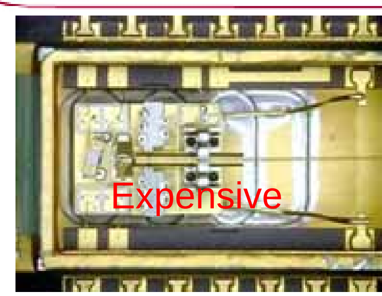
Source: Entroptix Ltd. Bob Musk. JDSU (Philips)

Hermetic packaging implementations

Early 2000s

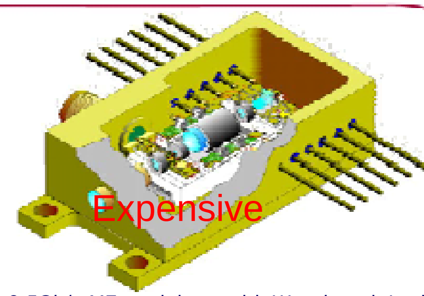


JDSU/Bookham 980nm Pump

High piecepart count

Complex manufacturing process

Limited capability for automation



Nortel 2.5Gb/s MZ modulator with Wavelength Locker

Highly complex structure

Multiple interactive alignments

Not designed for automation

Left: Hi rel 980nm JDSU/IBM chip big market for 980nm pumps with limited capability for automation – traditional gold box – hand built, hand aligned

Right: 1st approach at integration of bulk optics packaging. Clever design as did not use lithium niobate. Complex, and lots of interactive alignments. Virtually impossible to automate

Quite complex and expensive!!!

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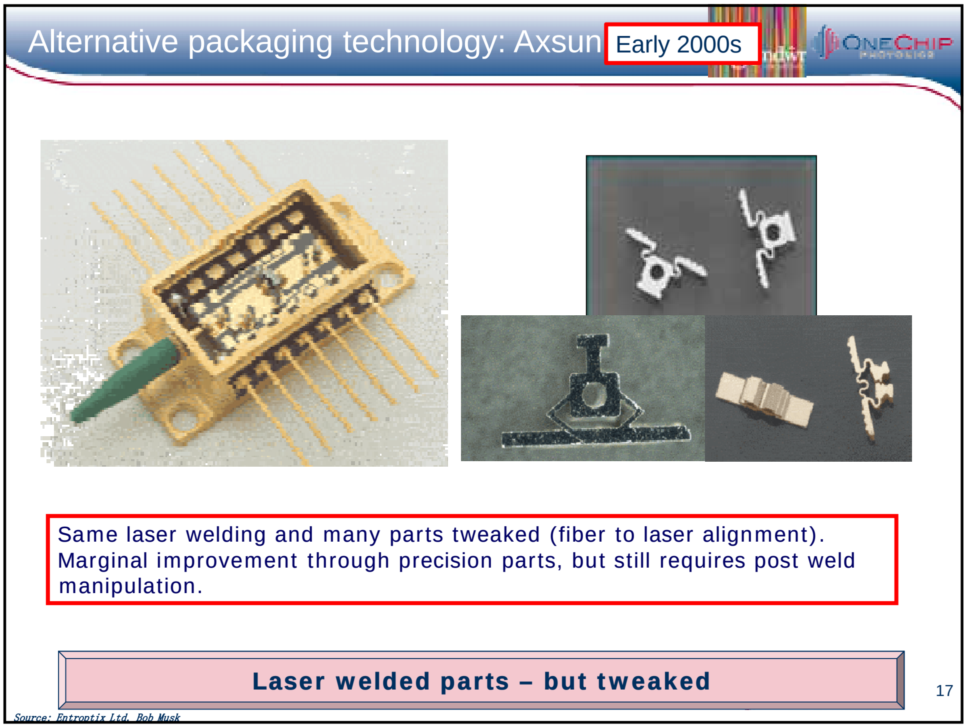
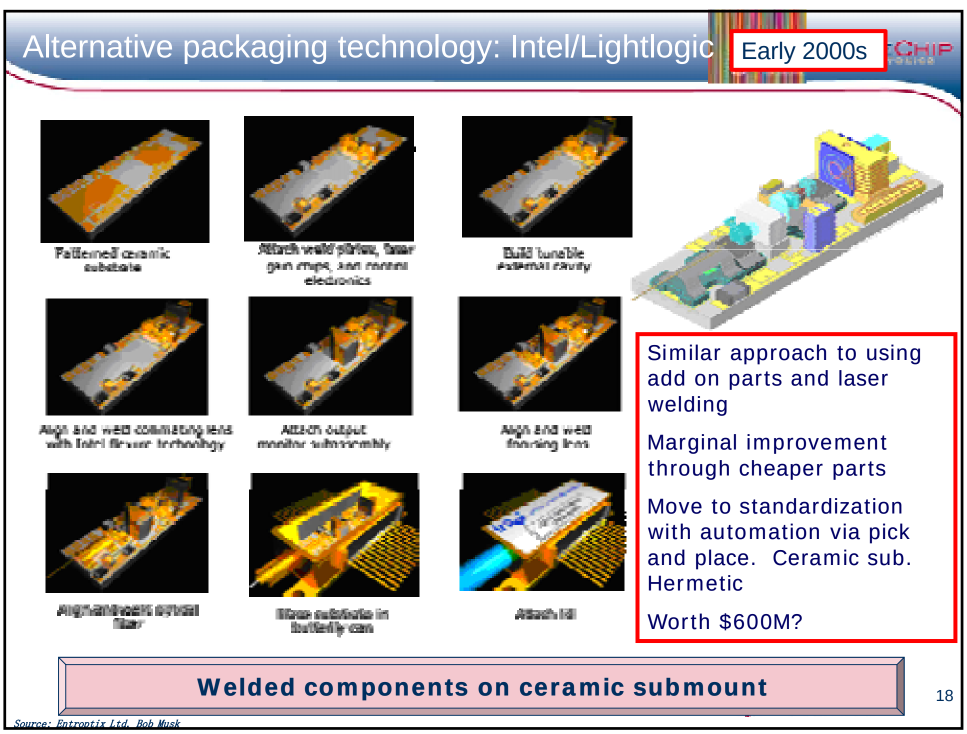
Source: Entroptix Ltd. Bob Musk. JDSU. Nortel


Alternative packaging technology: Axsun
Early 2000s
Same laser welding and many parts tweaked (fiber to laser alignment). Marginal improvement through precision parts, but still requires post weld manipulation.
Laser welded parts – but tweaked
17
Source: Entroptix Ltd, Bob Musk


Alternative packaging technology: Intel/Lightlogic
Early 2000s
Patterned ceramic substrate
Build tunable external cavity
Attach output monitor subassembly
Align and weld focusing lens
Attach lid
Similar approach to using add on parts and laser welding
Marginal improvement through cheaper parts
Move to standardization with automation via pick and place. Ceramic sub. Hermetic
Worth $600M?
Welded components on ceramic submount
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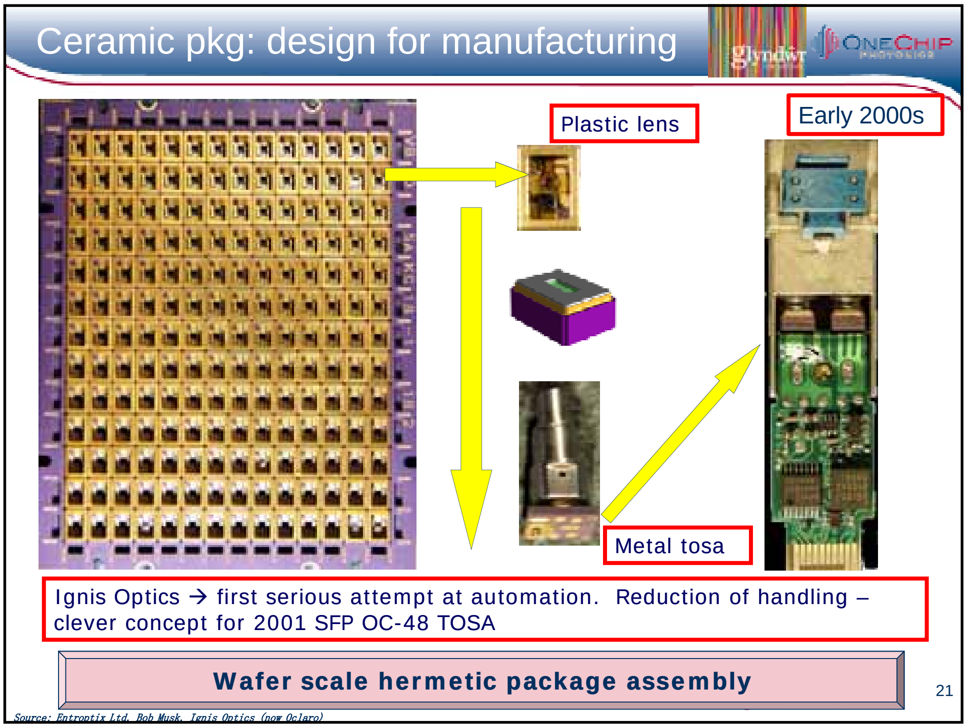
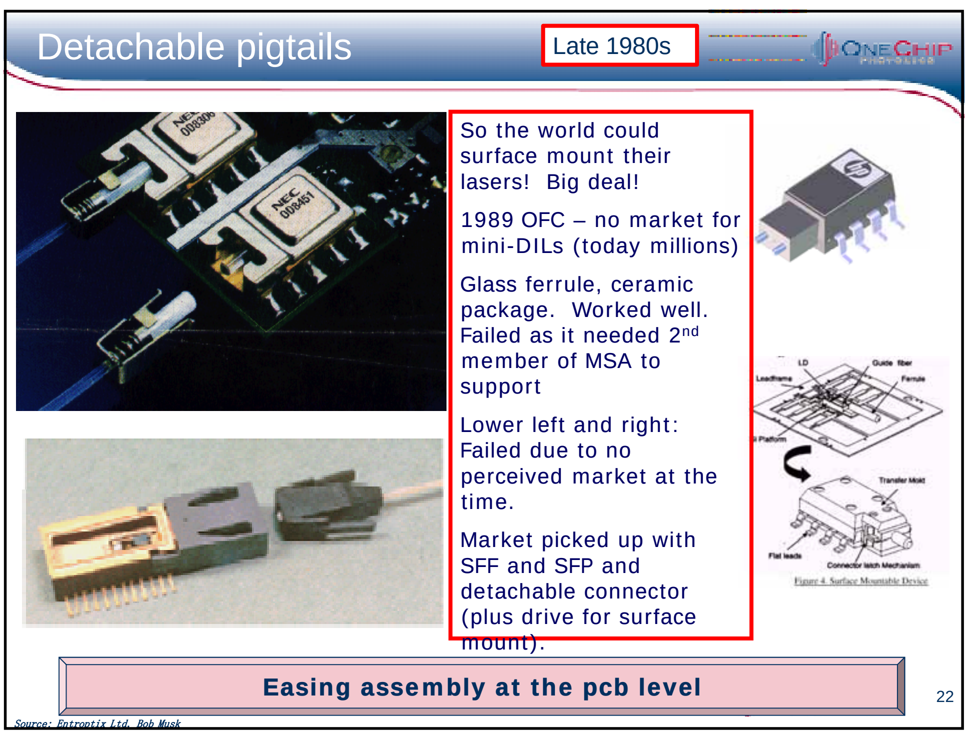
Source: Entroptix Ltd, Bob Musk


Hermetic metal packaging styles
Late 1990s and Early 2000s
Fiber feed-through main differentiator. Although 14 pin DIL and butterfly std, package itself was custom to each manufacturer.
Many options and variants – standards?
19
Source: Entroptix Ltd, Bob Musk


Ceramic packages for photonics
Early 2000s
Several High Speed over 10G Lines
Scalable O/E Integration
← Integrated submount – electronics on the inside. Problem was use of high temp for the fiber
Robust Al2O3 Ceramic / Hermetic
solder ball for signal I/O
Surface Mount O/E integrated package for High speed data link
No standards → precursors to todays multi layer ceramic pkgs
Photodiode submount location
Electrical interconnection
Laser submount location
← LTCC – elegant solution using thermal vias but expensive
From LTCC to ceramic pkgs → lots of styles and $$$
20
Source: Entroptix Ltd, Bob Musk


Ceramic pkg: design for manufacturing
Plastic lens
Early 2000s
Metal tosa
Ignis Optics → first serious attempt at automation. Reduction of handling – clever concept for 2001 SFP OC-48 TOSA
Wafer scale hermetic package assembly
21
Source: Entroptix Ltd, Bob Musk, Ignis Optics (now Oclaro)


Detachable pigtails
Late 1980s
So the world could surface mount their lasers! Big deal!
1989 OFC – no market for mini-DILs (today millions)
Glass ferrule, ceramic package. Worked well. Failed as it needed 2nd member of MSA to support
Lower left and right: Failed due to no perceived market at the time.
Market picked up with SFF and SFP and detachable connector (plus drive for surface mount).
Easing assembly at the pcb level
22
Source: Entroptix Ltd, Bob Musk

The rise of the transistor outline…

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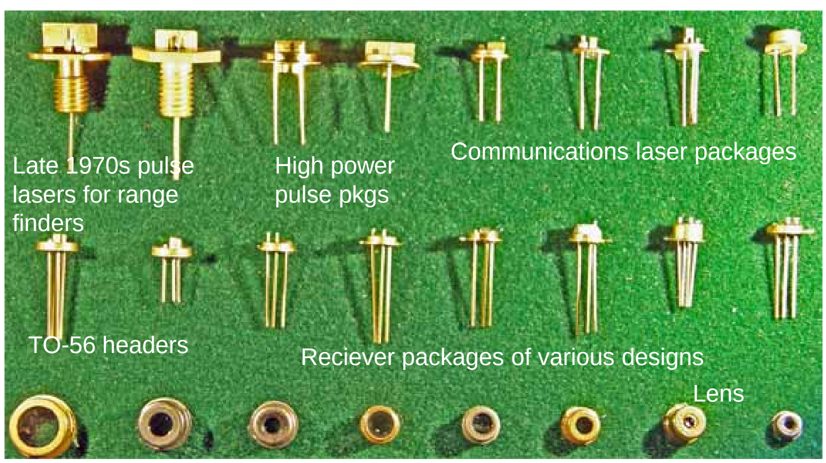
TO headers

Late 1970s, 1980s, 1990s



Always been there. Low cost hermetic package with plane or lens windows suitable for automation. Limited in speed and thermal perf. Up to 10Gbps.

Simple, high volume, low cost

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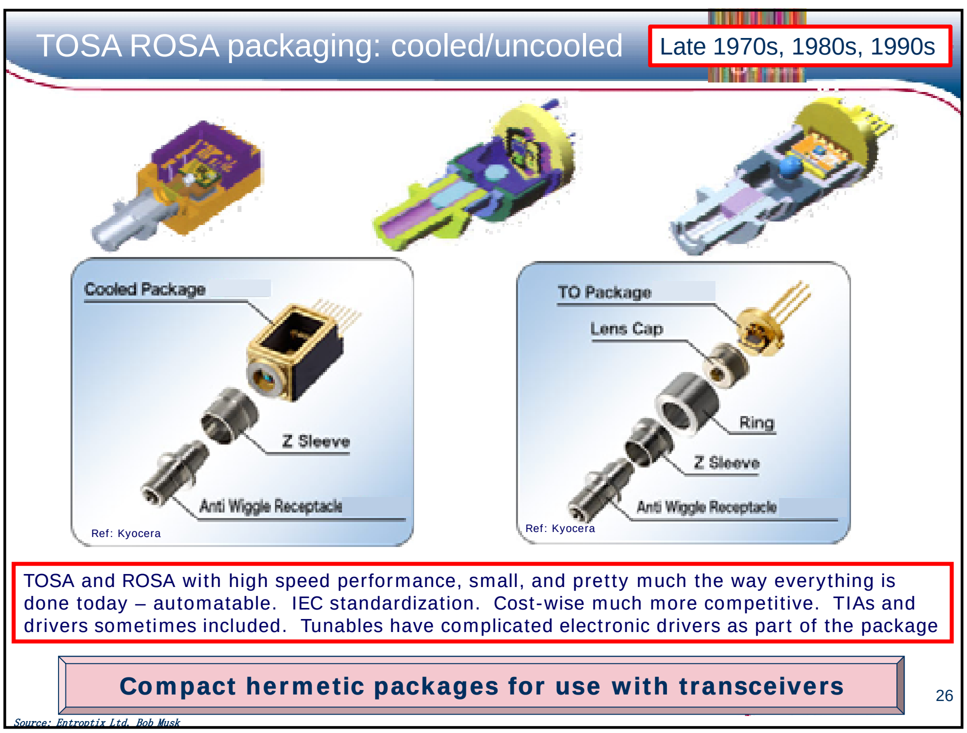
Source: Entroptix Ltd, Bob Musk


TO based products
1980s, 1990s
Move towards connector receptacles – 1 piece – low cost automatable
First basis to making TxRx – left are ST screw panel mount, rest into modules
Easily pig-tailed TOSA and ROSA
Simple, high volume, easy to use products
25
Source: Entroptix Ltd. Bob Musk


TOSA ROSA packaging: cooled/uncooled
Late 1970s, 1980s, 1990s
Cooled Package
Z Sleeve
Anti Wiggle Receptacle
Ref: Kyocera
TO Package
Lens Cap
Ring
Z Sleeve
Anti Wiggle Receptacle
Ref: Kyocera
TOSA and ROSA with high speed performance, small, and pretty much the way everything is done today – automatable. IEC standardization. Cost-wise much more competitive. TIAs and drivers sometimes included. Tunables have complicated electronic drivers as part of the package
Compact hermetic packages for use with transceivers
26
Source: Entroptix Ltd. Bob Musk

Use of silicon for photonics packaging

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Materials choice for an optical packaging platform

	Kovar	Copper-tungsten	Alumina	Aluminium nitride	Silicon	Gallium arsenide	Indium phosphide
Expansion coefficent	5.8 ✓	~7 ✓	4.9 ✓	4.5 ✓	2.6 ✓	5.8 ✓	4.5 ✓
Thermal conductivity	17 ✖	~180 ✓	32 ✖	~170 ✓	150 ✓	40 ✖	60 ✖
Mechanical stability	✓	✓	✓	✓	✓	?	?
Reliability	✓	✓	✓	✓	✓	?	?
Scales to micro-packaging	✖	✖	✖	✖	✓	✓	✓
High-speed electrical	✖	✖	✓	✓	✓	✓	✓
Bonding of chips, passives, IC's	✖	✖	✓	✓	✓	?	?
Precision location features	✖	✖	✖	✖	✓	?	?
Batch manufacture	✖	✖	✓	✓	✓	✓	✓
Batch population	✓	✓	✓	✓	✓	✓	✓
Waveguides	✖	✖	✖	✖	✓	✓	✓
Maturity	✓	✓	✓	✓	✓	✖	✖

Silicon becomes the obvious choice for packaging

Source: Entroptix Ltd, Bob Musk

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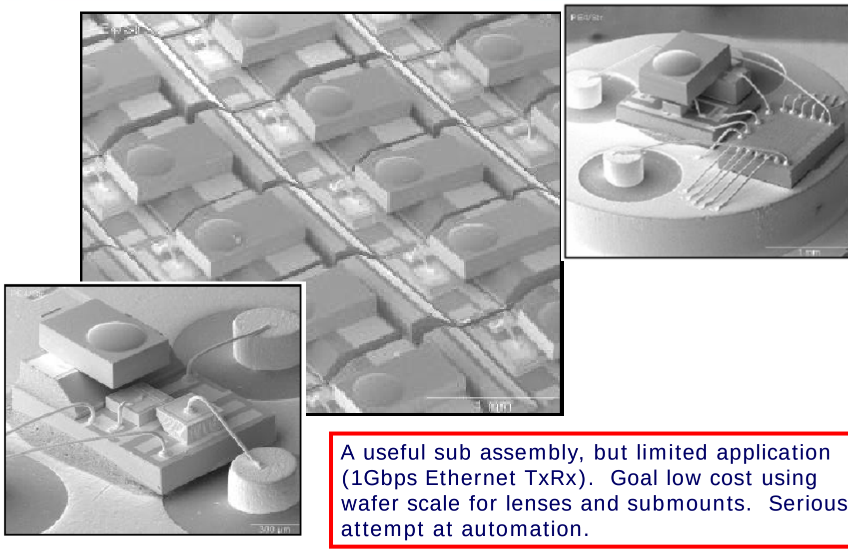
Silicon micro-bench

Late 1990s



A useful sub assembly, but limited application (1Gbps Ethernet TxRx). Goal low cost using wafer scale for lenses and submounts. Serious attempt at automation.

Wafer scale potential – TO applications

Source: Entroptix Ltd. Bob Musk, Infineon

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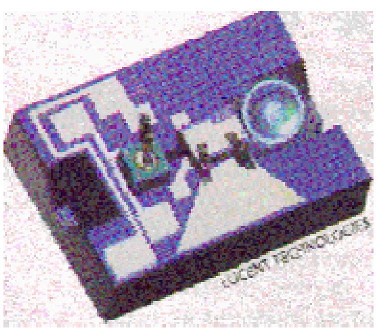
Silicon micro-bench

Early 2000s



Optical subassemblies – a good approach, but only the first step…serious attempt at automation. Was successful and worked well.

Wafer scale tested sub assemblies

Source: Entroptix Ltd. Bob Musk, Agere (formally Lucent/Bell Labs)

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Non-hermetic packaging approaches

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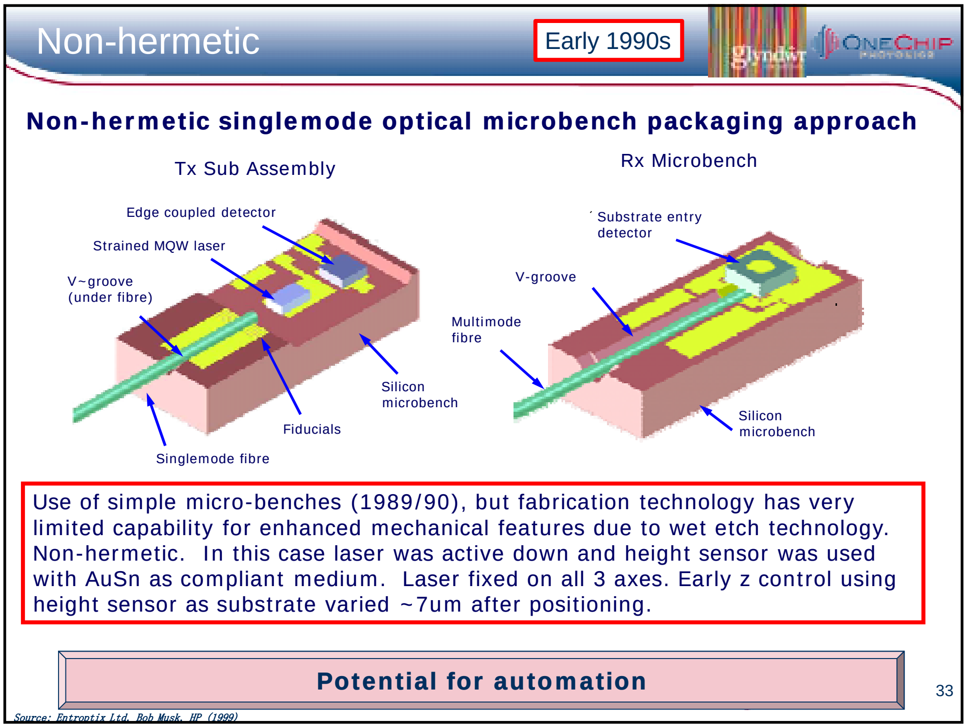
Non-hermetic
Early 1990s
Non-hermetic singlemode optical microbench packaging approach
Tx Sub Assembly
Rx Microbench
Edge coupled detector
Strained MQW laser
V~groove (under fibre)
Silicon microbench
Fiducials
Singlemode fibre
Substrate entry detector
V-groove
Multimode fibre
Silicon microbench
Use of simple micro-benches (1989/90), but fabrication technology has very limited capability for enhanced mechanical features due to wet etch technology. Non-hermetic. In this case laser was active down and height sensor was used with AuSn as compliant medium. Laser fixed on all 3 axes. Early z control using height sensor as substrate varied ~7um after positioning.
Potential for automation
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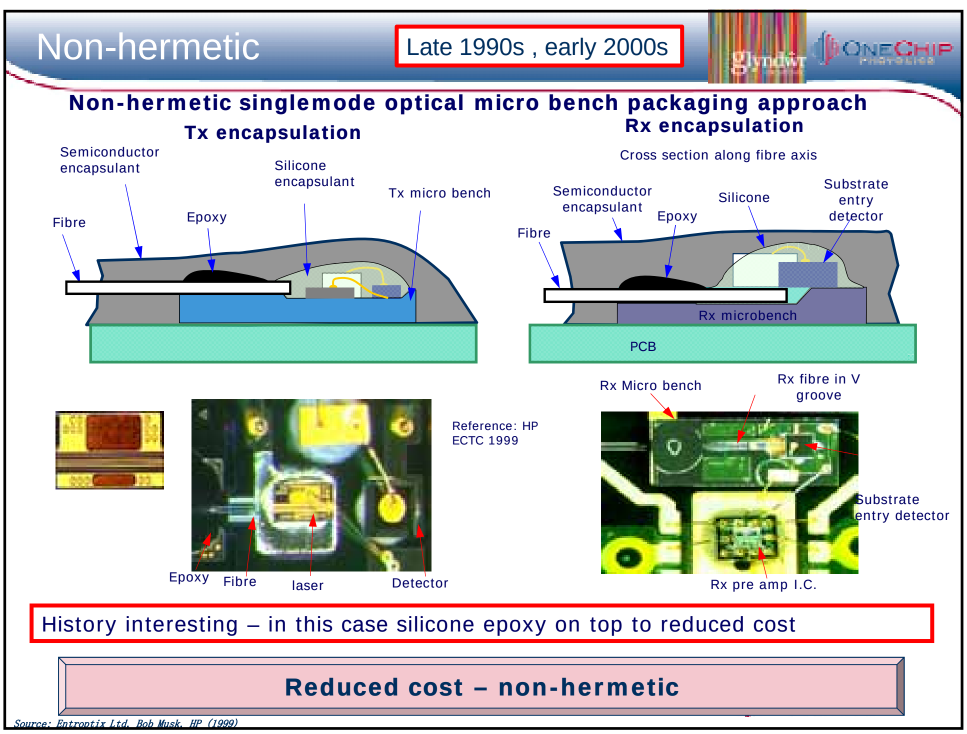
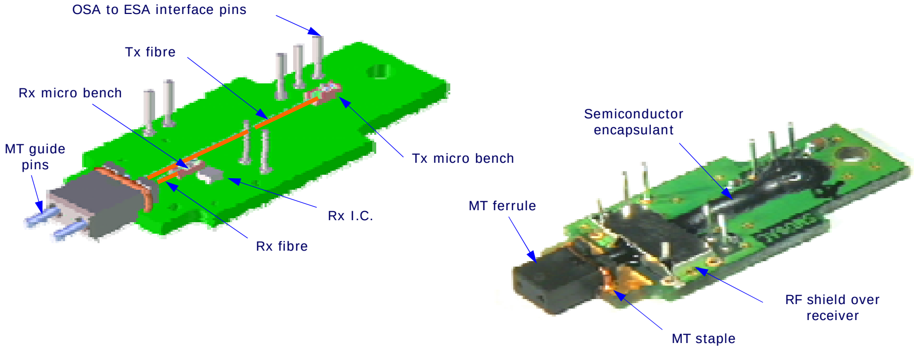
Source: Entroptix Ltd. Bob Musk, HP (1999)


Non-hermetic
Late 1990s , early 2000s
Non-hermetic singlemode optical micro bench packaging approach
Tx encapsulation
Rx encapsulation
Cross section along fibre axis
Semiconductor encapsulant
Silicone encapsulant
Tx micro bench
Fibre
Epoxy
Semiconductor encapsulant
Silicone
Substrate entry detector
Epoxy
Fibre
Rx microbench
PCB
Reference: HP ECTC 1999
Rx Micro bench
Rx fibre in V groove
Substrate entry detector
Rx pre amp I.C.
Epoxy
Fibre
laser
Detector
History interesting – in this case silicone epoxy on top to reduced cost
Reduced cost – non-hermetic
Source: Entroptix Ltd. Bob Musk, HP (1999)

Non-hermetic OSA

Late 1990s

Singlemode SFF transceiver :
Non-hermetic optical sub assembly arrangement



Only first level optical subassemblies used, higher levels of integration will be required in the future for better performance i.e. integrated modulators and isolators. In this case MT ferrule used, but lost competitive advantage due to LC costs dropping when MT entered market. Simple assembly technology.

Simple assembly methodology

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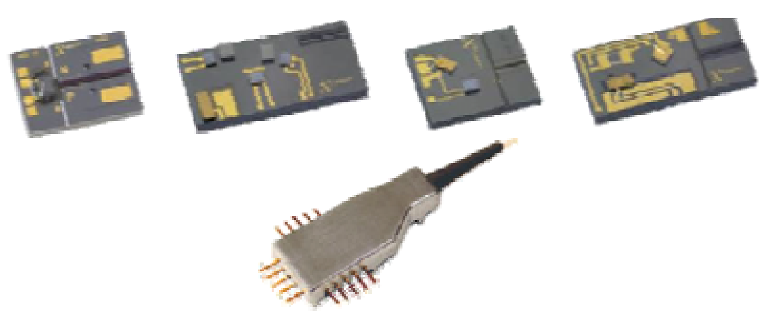
Source: Entroptix Ltd. Bob Musk. HP (1999)

Other non-hermetic approaches

Early 2000s

- PLC (planar light circuit) + flip chip actives and passives



Automated flip-chip assembly; use of silicon/silica optical waveguides

Flip-chip using automated assembly

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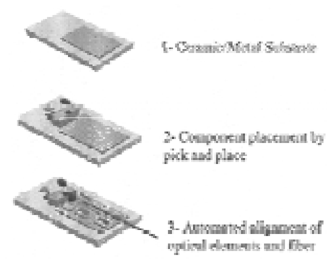
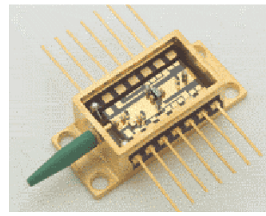
Source: Entroptix Ltd. Bob Musk. Exponent (now Hoya)

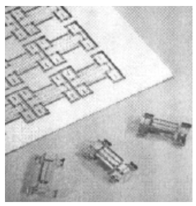
Packaging technology evolution…

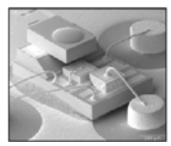
Lightlogic (Intel) – mechanical add on components

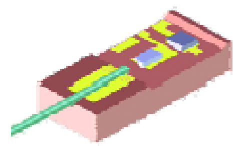


Axsun – mechanical add on components









Agere – Infineon - Agilent etc   Wet etch technology only

Technologies for discrete components

Source: Entroptix Ltd, Bob Musk, Lightlogic (Intel), Axsun, Agere, Infineon, Agilent

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Packaging integrated devices

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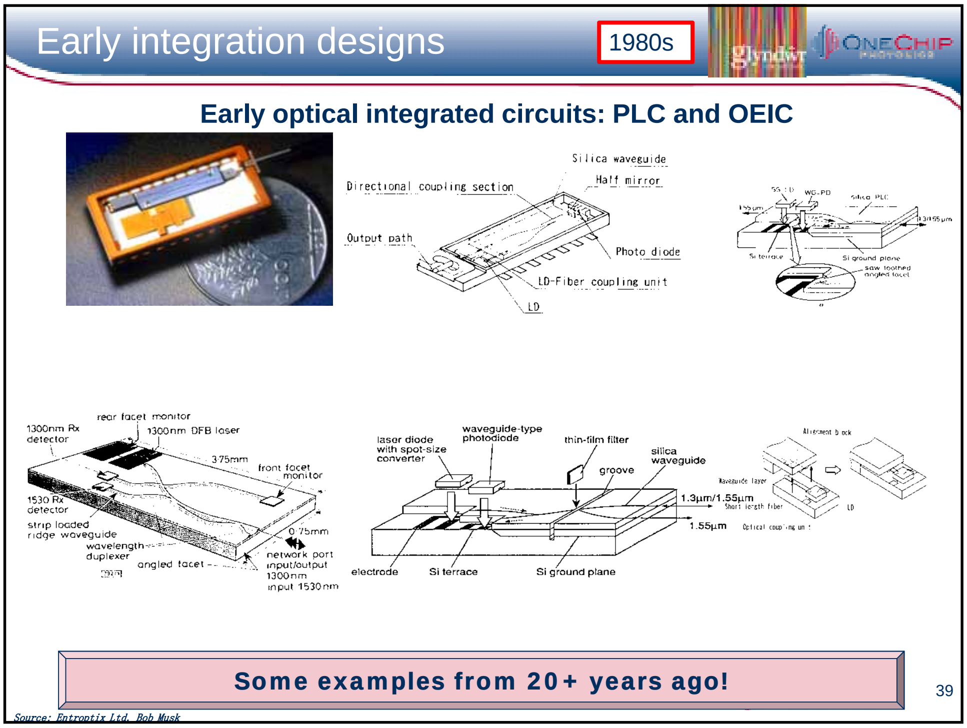
Early integration designs
1980s
Early optical integrated circuits: PLC and OEIC
Silica waveguide
Half mirror
Directional coupling section
Output path
Photo diode
LD-Fiber coupling unit
LD
rear facet monitor
1300nm Rx detector
1300nm DFB laser
3.75mm
front facet monitor
1530 Rx detector
strip loaded ridge waveguide
wavelength duplexer
angled facet
0.75mm
network port input/output 1300nm input 1530nm
laser diode with spot-size converter
waveguide-type photodiode
thin-film filter
silica waveguide
groove
1.3μm/1.55μm
1.55μm
electrode
Si terrace
Si ground plane
Some examples from 20+ years ago!
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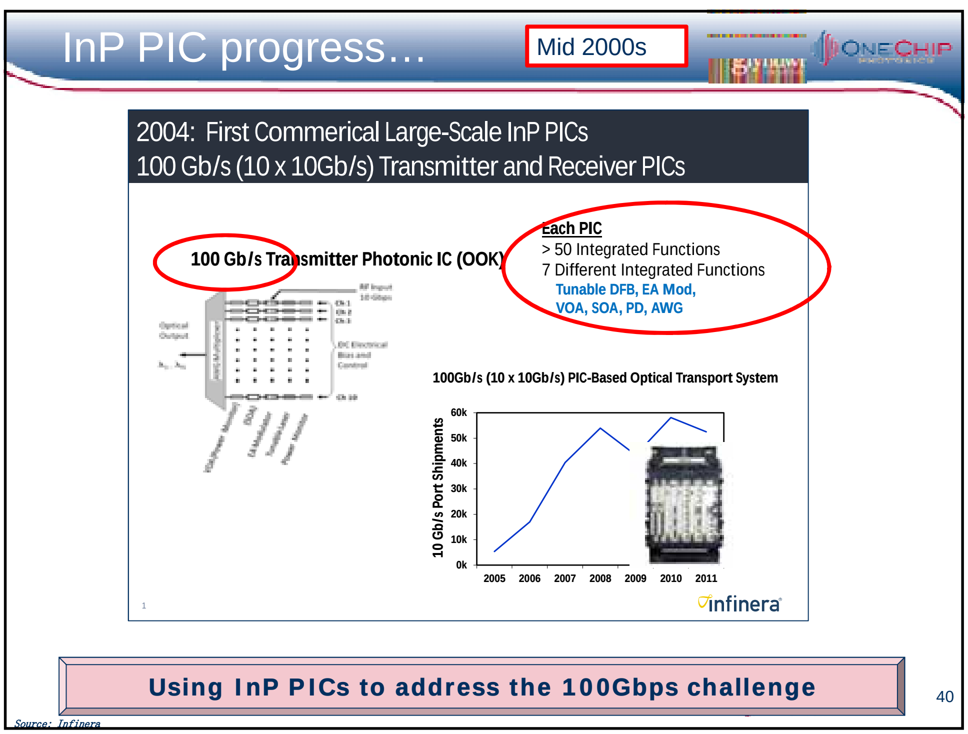
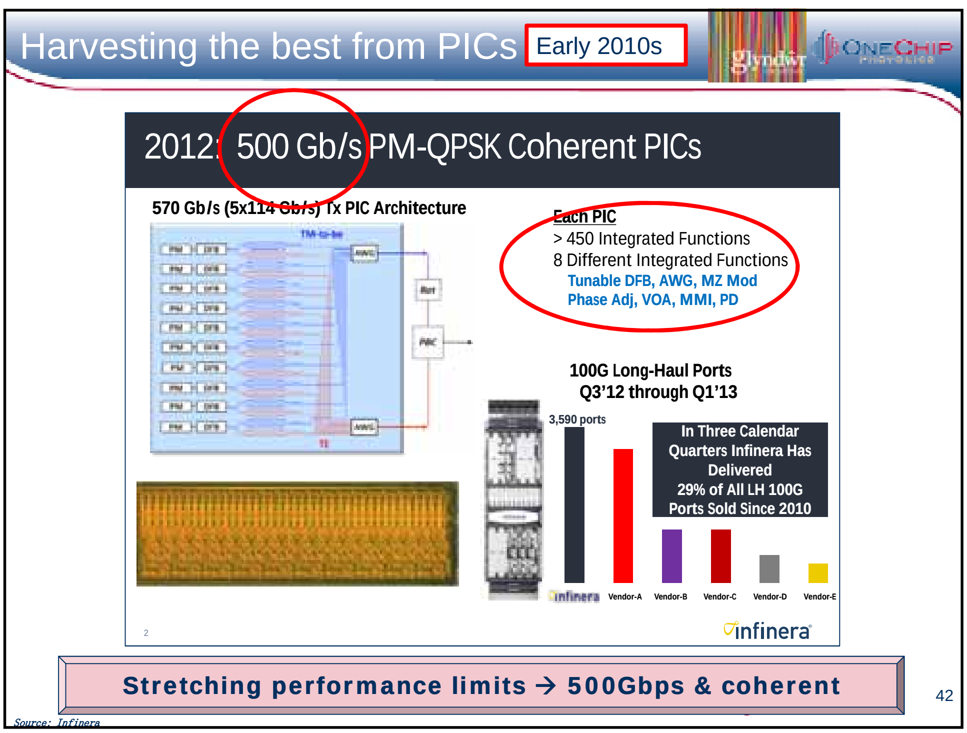
Source: Entroptix Ltd, Bob Musk


InP PIC progress…
Mid 2000s
2004: First Commerical Large-Scale InP PICs
100 Gb/s (10 x 10Gb/s) Transmitter and Receiver PICs
100 Gb/s Transmitter Photonic IC (OOK)
Each PIC
> 50 Integrated Functions
7 Different Integrated Functions
Tunable DFB, EA Mod,
VOA, SOA, PD, AWG
100Gb/s (10 x 10Gb/s) PIC-Based Optical Transport System
10 Gb/s Port Shipments
60k
50k
40k
30k
20k
10k
0k
2005
2006
2007
2008
2009
2010
2011
infinera
Using InP PICs to address the 100Gbps challenge
40
Source: Infinera


Recent focus for PICs
Early 2010s
Examples of PICs Fabricated on Multi-Project Wafers
ASPIC 1: Brillouin strain sensor readout chip
ASPIC 2: Fibre Brag Grating strain sensor readout chip
ASPIC 3: Pulse serialiser for KM3NeT Neutrino Telescope
ASPIC 4: Fast 4x4 switching matrix
ASPIC 5a: WDM-transmitter for FTTH
ASPIC 5b: WDM-receiver for FTTH
ASPIC 6: Variable repetition rate pulse laser
ASPIC 8: Tunable laser with integrated 10 Gb/s MZI modulator
ASPIC 9: Pulse shaper for bio-imaging
...more than 20 different PICs fabricated in MPW runs
Fraunhofer
oclaro
New pkg challenge: bigger die, much more functionality
41
Source: Entroptix Ltd, Bob Musk


Harvesting the best from PICs
Early 2010s
2012: 500 Gb/s PM-QPSK Coherent PICs
570 Gb/s (5x114 Gb/s) Tx PIC Architecture
Each PIC
> 450 Integrated Functions
8 Different Integrated Functions
Tunable DFB, AWG, MZ Mod
Phase Adj, VOA, MMI, PD
100G Long-Haul Ports
Q3'12 through Q1'13
3,590 ports
In Three Calendar Quarters Infinera Has Delivered
29% of All LH 100G Ports Sold Since 2010
infinera
Vendor-A
Vendor-B
Vendor-C
Vendor-D
Vendor-E
Stretching performance limits → 500Gbps & coherent
42
Source: Infinera

How to address PIC/OEIC packaging?

43

European efforts…

Early 2010s

PARADIGM

Photonic Advanced Research And Development for Integrated Generic Manufacturing

PARADIGM
Generic Approach to PIC Packaging

Novel concept???

"Design the chip to fit the package" !!!!

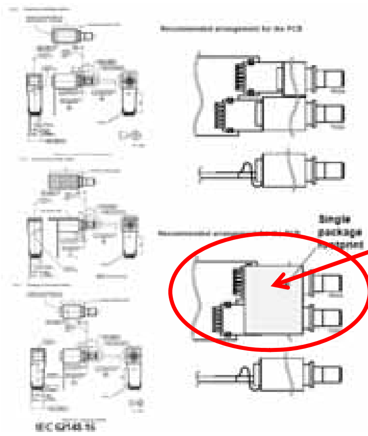
Generic package for PICs/OEICs to lower costs

44

Source: Entroptix Ltd, Bob Musk, Gooch and Housego (2013)

Background and motivation

Early 2010s



Objectives

- •Standardised package format
- •Multiple electrical I/O
- •High speed capability
- •Multiple SMF support
- •TEC support
- •Hermetic capability
- •Maximum PIC applications
- •XFP/CFP/QFSP support
- •Capable of IEC standardisation
  - •Compare existing ROSA/TOSA

POSA
(PIC OSA)

Left standard IEC TOSA/ROSA package outlines. Middle standard TOSA/ROSA side by side – used basic footprint of combined ROSA/TOSA to generate PIC footprint size (POSA).

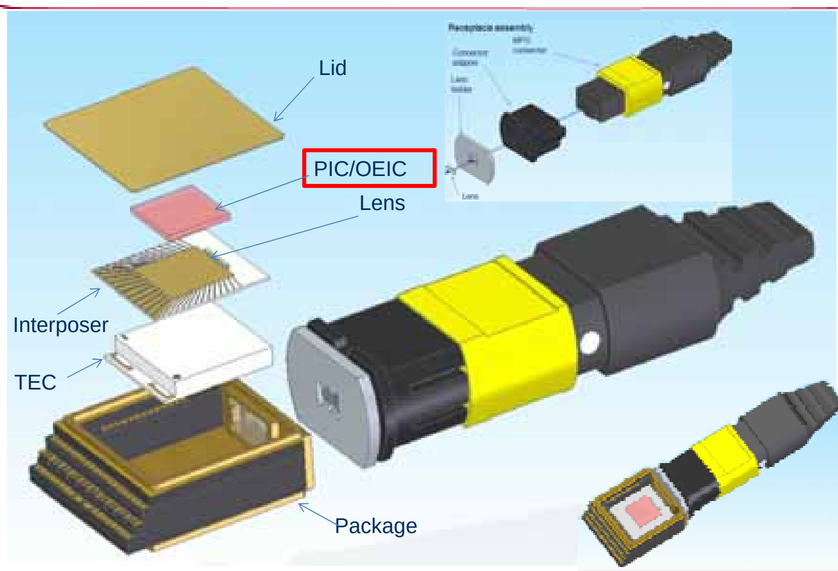
Aim for a standarized format…

45

Source: Entroptix Ltd, Bob Musk, Gooch and Housego (2013)

Standardized approach

Early 2010s



PIC/OEIC is designed to fit the package!!!

46

Source: Entroptix Ltd, Bob Musk, Gooch and Housego (2013)

PIC/OEIC package summary

Early 2010s

- Overall package size – **18.5 x 15.5 x 5.5 mm**
- Package cavity for PIC/interposer – **11.1 x 10.65 mm**
- Supports TEC temperature control if required
- Number of DC/low speed connections – **36**
- Number of high speed (up to 25GHz) connections in GSG configuration – **10**
- High current TEC connections (3.5A) – **2**
- Hermetic package – AR coated sapphire window and welded lid
- High thermal conductivity base – copper tungsten
- Number of fibres supported – up to **12 SMF**
- Detachable connector
- XFP compatible
- IEC standardisation possible

In volume (10k+ pieces) ceramic/CuW high performance package will cost ~30-50Euros (after soft/hard tooling costs). Many connections on package should cover 80%+ PIC designs

All work carried out under ICT Programme 257210 PARADIGM

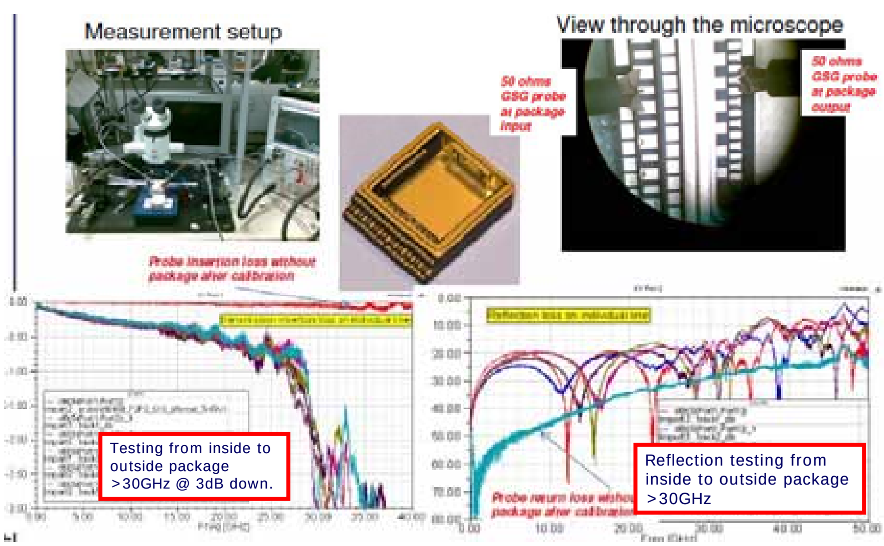
Although parallel connector: the concept is important

47

Source: Entroptix Ltd, Bob Musk, Gooch and Housego (2013), Oclaro (2013)

High performance package

Early 2010s



>25GHz per channel

Initial testing >25GHz per channel

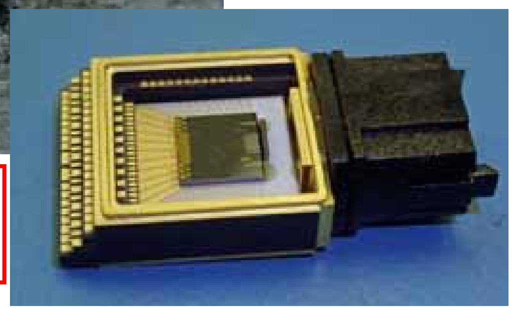
48

Source: Entroptix Ltd, Bob Musk, Gooch and Housego (2013), Oclaro (2013)

Packaged PIC

Late 2013

Silicon array lenses on 250um pitch vertically mounted. With test InP PIC chip fully connected.



Silicon array lenses on 250um pitch vertically mounted inside MPO connector

Wirebonded PIC with silicon array lenses

49

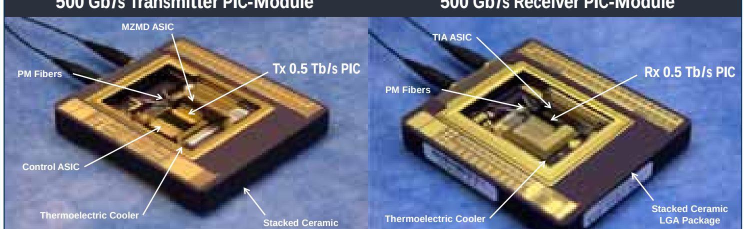
Source: Entroptix Ltd, Bob Musk, Gooch and Housego (2013), Oclaro (2013)

Need for simplicity is key…

2013

Infinera 500 Gb/s Coherent PM-QPSK Modules

500 Gb/s Transmitter PIC-Module	500 Gb/s Receiver PIC-Module



- Stacked Ceramic Hermetic LGA Packages (I/O capability > 1000)
- >24 feet of total wirebonds (Tx+Rx)
- Dual PM Fibers per Module (1x per pol)
- Integrated TIA array (40x14.25 Gbaud), MZMD Array (40x14.25 Gbaud)

3 infinera

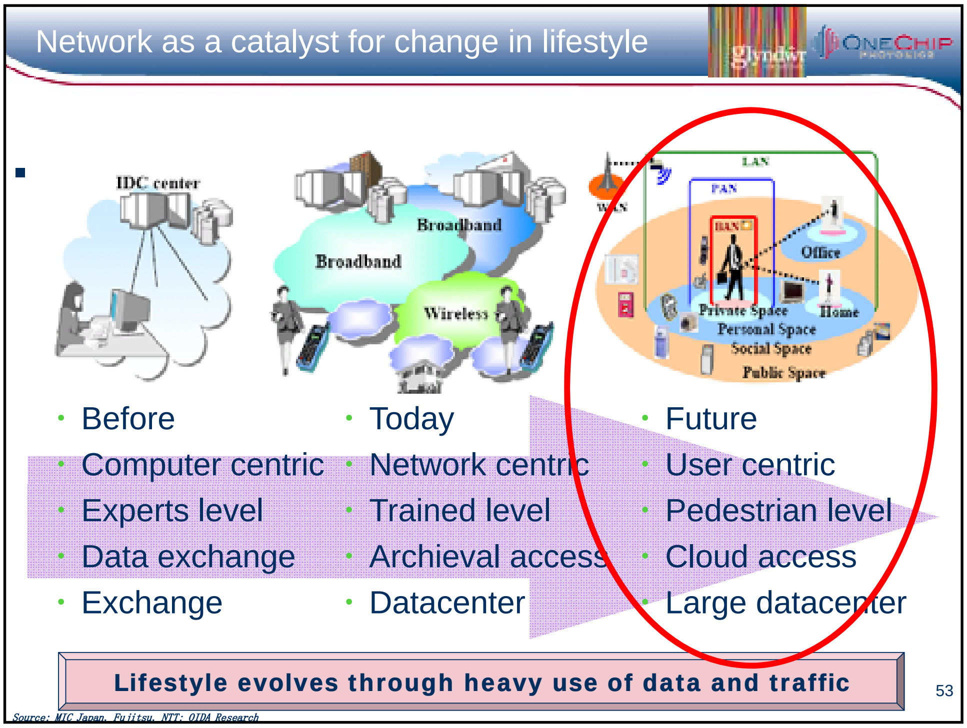
Packaging is becoming complex and expensive

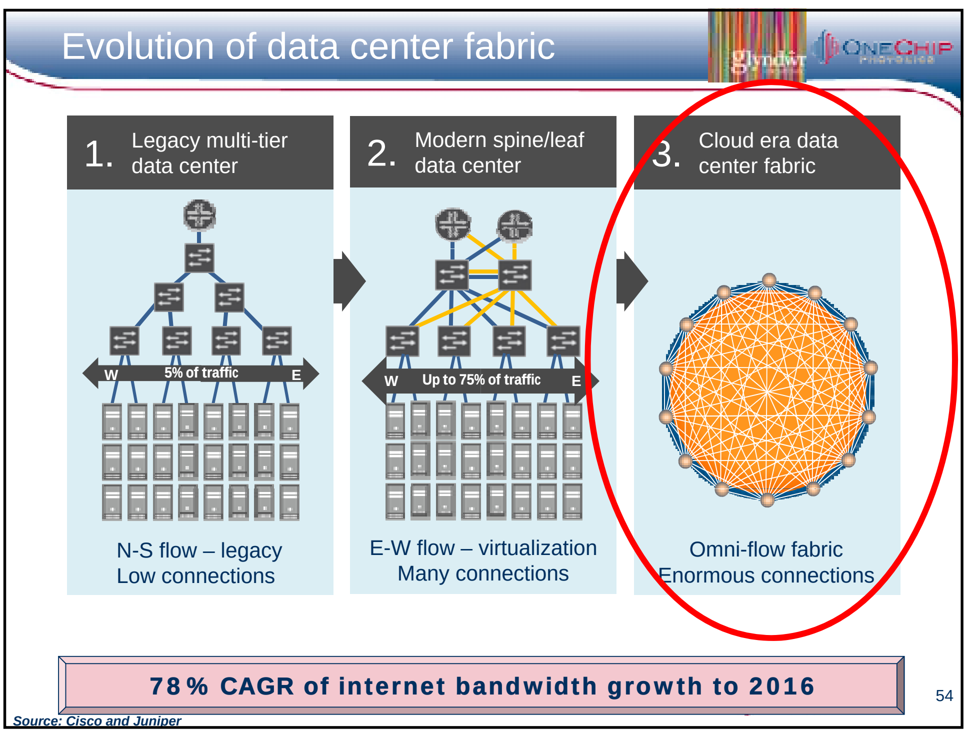
50

Source: Infinera

Part 2
PICs and OEICs

What drives a 'next generation' IC?


Network as a catalyst for change in lifestyle
IDC center
Broadband
Broadband
Wireless
LAN
PAN
WAN
Office
Private Space
Home
Personal Space
Social Space
Public Space
Before
Computer centric
Experts level
Data exchange
Exchange
Today
Network centric
Trained level
Archieval access
Datacenter
Future
User centric
Pedestrian level
Cloud access
Large datacenter
Lifestyle evolves through heavy use of data and traffic
53
Source: MIC Japan, Fujitsu, NTT; OIDA Research

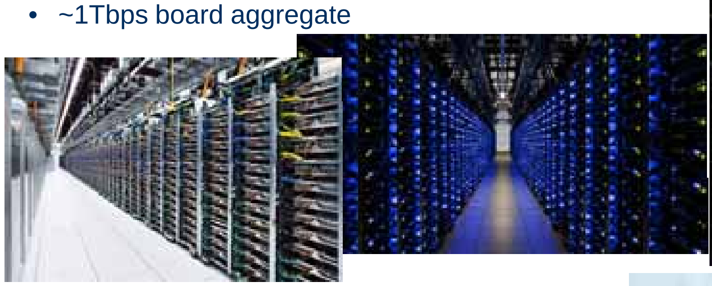

Evolution of data center fabric
1. Legacy multi-tier data center
2. Modern spine/leaf data center
3. Cloud era data center fabric
W
5% of traffic
E
W
Up to 75% of traffic
E
N-S flow – legacy
Low connections
E-W flow – virtualization
Many connections
Omni-flow fabric
Enormous connections
78% CAGR of internet bandwidth growth to 2016
54
Source: Cisco and Juniper

What is a datacenter?

55

Huge buildings that aggregate data…

- Sound of fans whirring
  - ~1Tbps board aggregate



Google datacenters: large buildings use tons of energy…

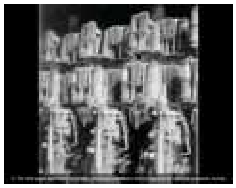
56

Source: Google

Bit like a telephone exchanges in the 60s

- Sound of 1000s of Crickets…
  - ~100kbps 'board/rack' aggregate
  - ~X10,000,000 slower…







Telephone exchanges: large buildings to aggregate traffic…

Source: GPO

57

Datacenters have aroused interest recently…

58

Recent activity in the segment

- 100G technology activity accelerating
- PIC→OEIC integration technology needed

COGO optronics	? <30M$, 2012	TeraXion	Technology sale; 40G/100G discrete components
LIGHTWIRE	271 M$, 2012	CISCO	Technology sale; 40/100G silicon photonics
CyOptics	400 M$, 2013	Avago Technologies	$200M rev (2X) to access InP discrete 40/100G
Kotura	82 M$, 2013	Mellanox Technologies	Technology sale: Silicon Photonics solution 40/100G
ipt	47 M$, 2013	Mellanox Technologies	CMOS VCSEL Driver and TIA 40/100G with ~$20-30M rev (2X)

Datacenter market becoming active again…

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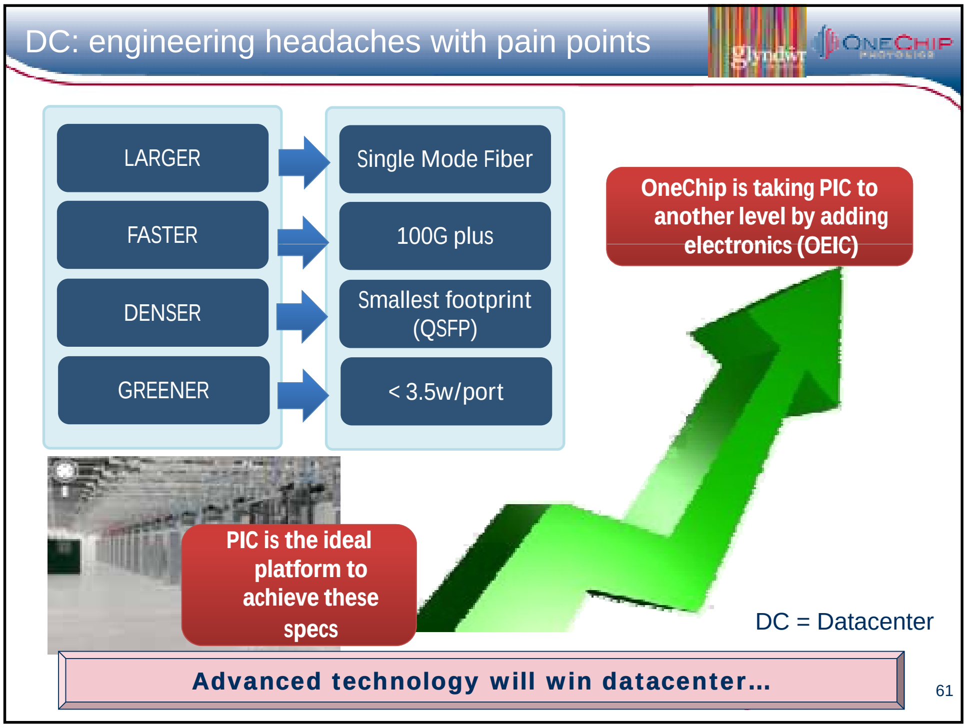
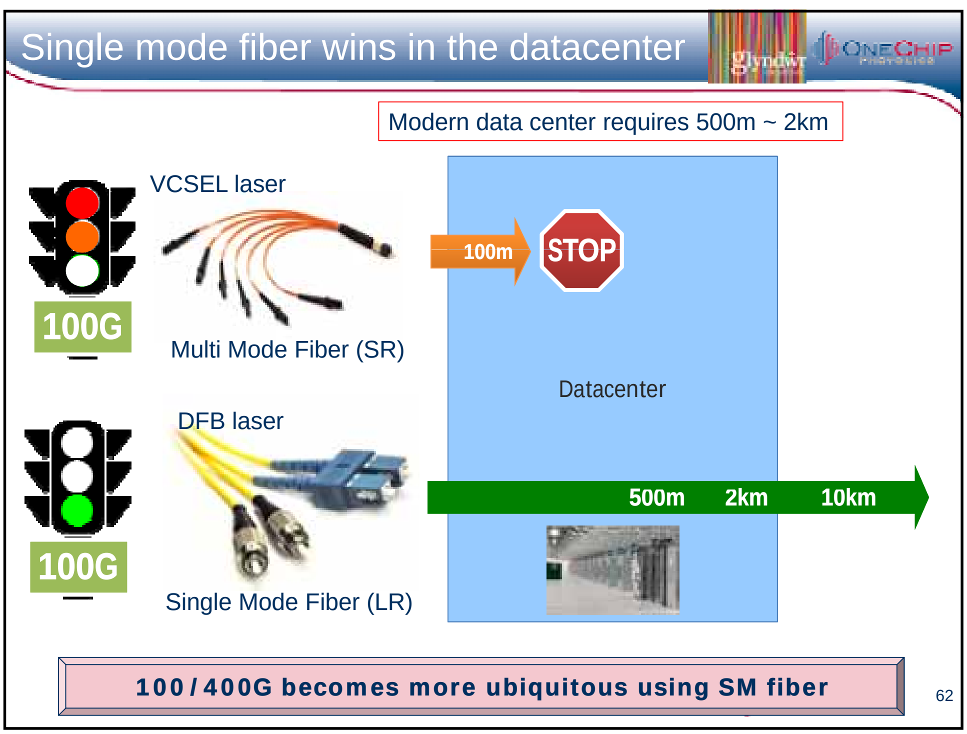
Datacenter pain points

60


DC: engineering headaches with pain points
LARGER
FASTER
DENSER
GREENER
Single Mode Fiber
100G plus
Smallest footprint (QSFP)
< 3.5w/port
OneChip is taking PIC to another level by adding electronics (OEIC)
PIC is the ideal platform to achieve these specs
DC = Datacenter
Advanced technology will win datacenter…
61

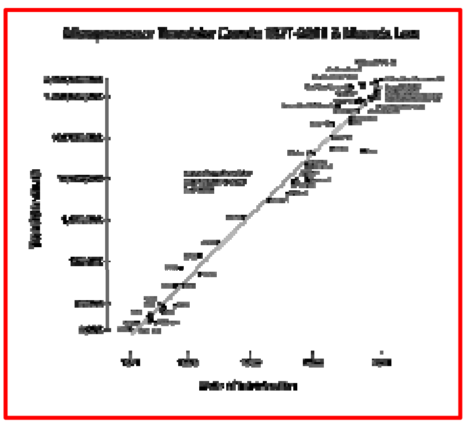

Single mode fiber wins in the datacenter
Modern data center requires 500m ~ 2km
VCSEL laser
100G
Multi Mode Fiber (SR)
100m
STOP
Datacenter
DFB laser
100G
Single Mode Fiber (LR)
500m
2km
10km
100 / 400G becomes more ubiquitous using SM fiber
62

Why do we integrate?

63

Why do we integrate?

- Like any semiconductor IC: to achieve key goals
  - Size, weight, power, performance, and cost
  - Classic CMOS IC allows higher functionality



Integration enables innovative products…

64

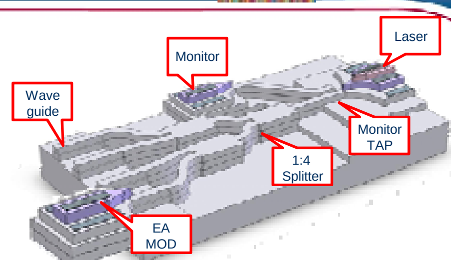
Source: Wikiepedia

Next generation IC → PIC (photonic integrated circuit)

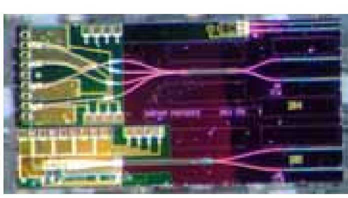
65

Photonic Integrated Circuit (PIC)

- Compound semiconductor platform
  - Indium Phosphide (InP)
  - Epitaxial growth from IQE
  - Fabricated by CST Glasgow
- Photonics devices are all integrated together
  - Waveguides, tracks

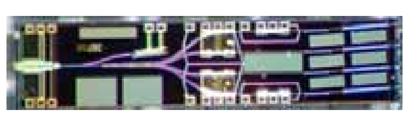


100G transmitter chip using InP compound semiconductor with epitaxy



100G Coherent Receiver (a.k.a. 2x4 90° Hybrid Rx) (TIA at back)

100G Coherent Receiver (a.k.a. 2x4 90° Hybrid Rx) (TIA on side)



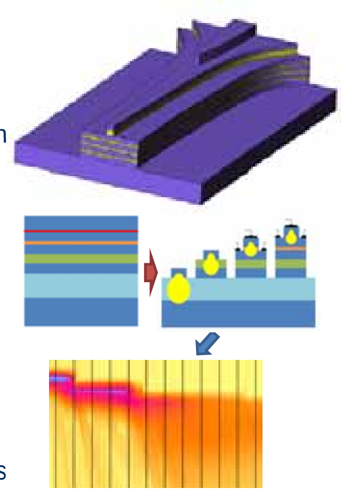
4x25G PSM4 Transmitter

PIC is a circuit with no electronic circuitry

66

OneChip approach to InP PICs

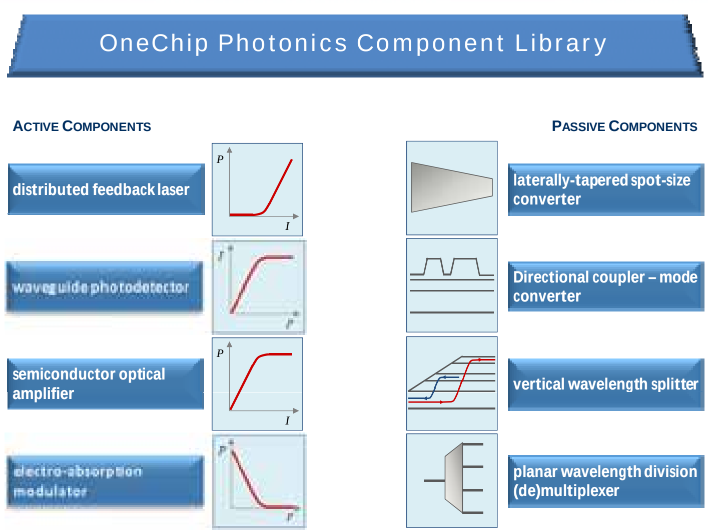
- Fully monolithic InP PIC
  - Avoid multiple re-growth steps
    - Potential re-growth losses
    - Use Fe-doped substrates for electrical isolation
    - Use etching of structure to enable functionality
  - Core strengths
    - Waveguide design
      - Dilute waveguide for package connection
      - Passive guide for routing
    - Integration of electrical components
      - Resistors/capacitors
    - Edge detector for high speeds
    - Laser emitter and modulators (DC/AC)
    - Fabrication of complex InP devices in a fabless model



7yrs of PIC R&D in III-V devices at OneChip

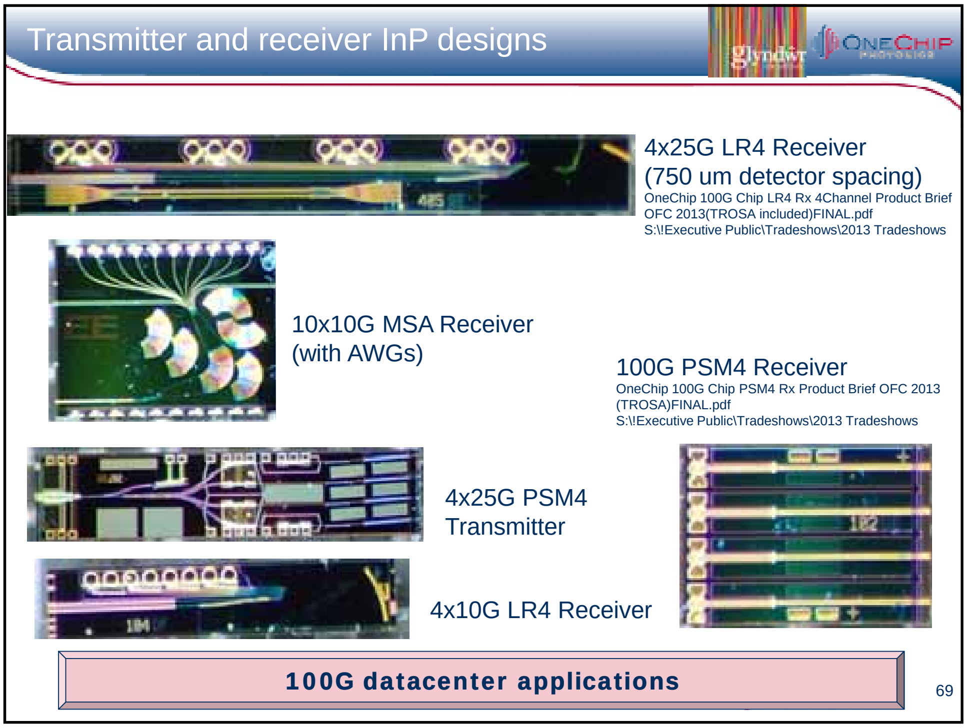
67

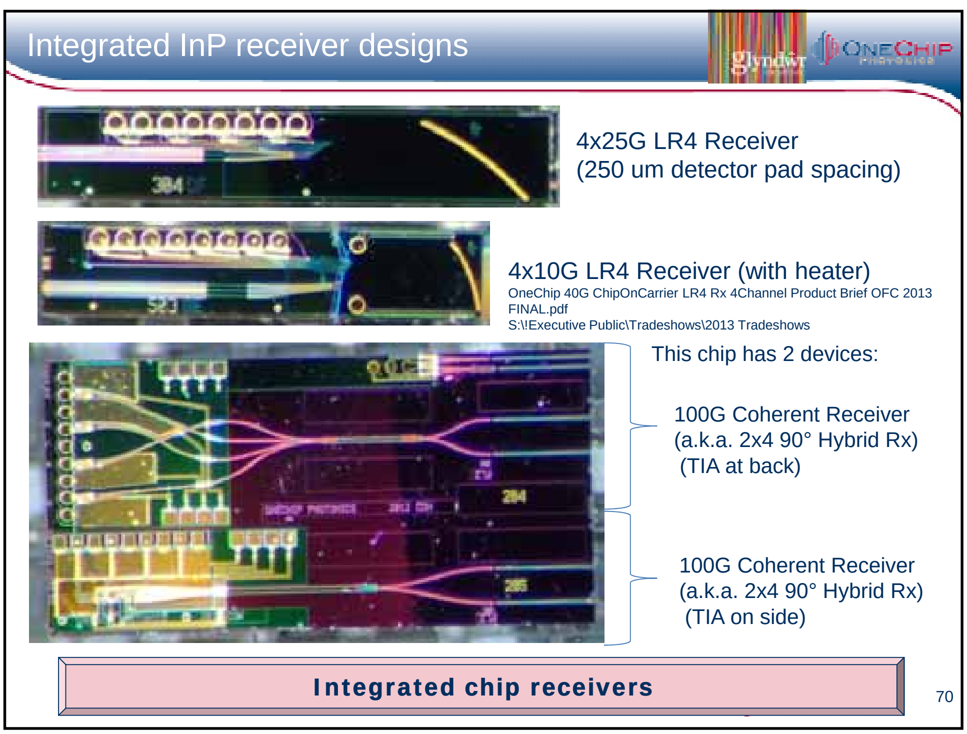
InP PIC building blocks developed…



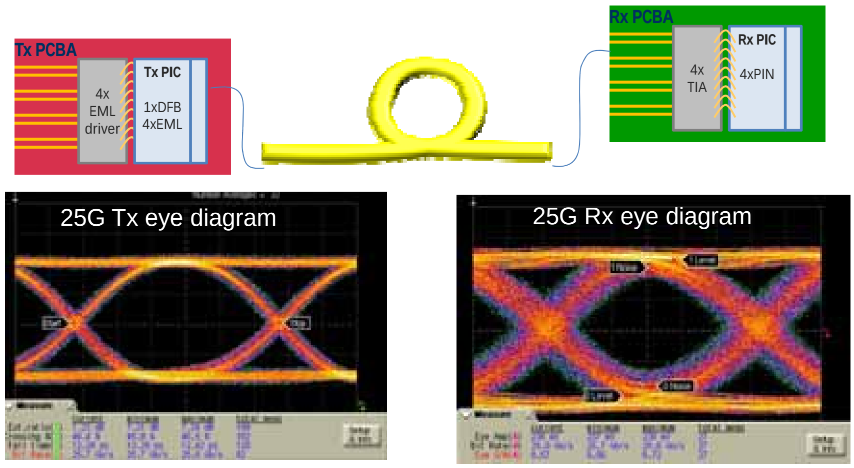
Comprehensive library of components for integration

68


Transmitter and receiver InP designs
4x25G LR4 Receiver
(750 um detector spacing)
OneChip 100G Chip LR4 Rx 4Channel Product Brief OFC 2013(TROSA included)FINAL.pdf
S:\!Executive Public\Tradeshows\2013 Tradeshows
10x10G MSA Receiver
(with AWGs)
100G PSM4 Receiver
OneChip 100G Chip PSM4 Rx Product Brief OFC 2013 (TROSA)FINAL.pdf
S:\!Executive Public\Tradeshows\2013 Tradeshows
4x25G PSM4
Transmitter
4x10G LR4 Receiver
100G datacenter applications
69


Integrated InP receiver designs
4x25G LR4 Receiver
(250 um detector pad spacing)
4x10G LR4 Receiver (with heater)
OneChip 40G ChipOnCarrier LR4 Rx 4Channel Product Brief OFC 2013 FINAL.pdf
S:\!Executive Public\Tradeshows\2013 Tradeshows
This chip has 2 devices:
100G Coherent Receiver
(a.k.a. 2x4 90° Hybrid Rx)
(TIA at back)
100G Coherent Receiver
(a.k.a. 2x4 90° Hybrid Rx)
(TIA on side)
Integrated chip receivers
70

25Gbps optical eye performance…



Demonstrated InP performance for 100G solutions

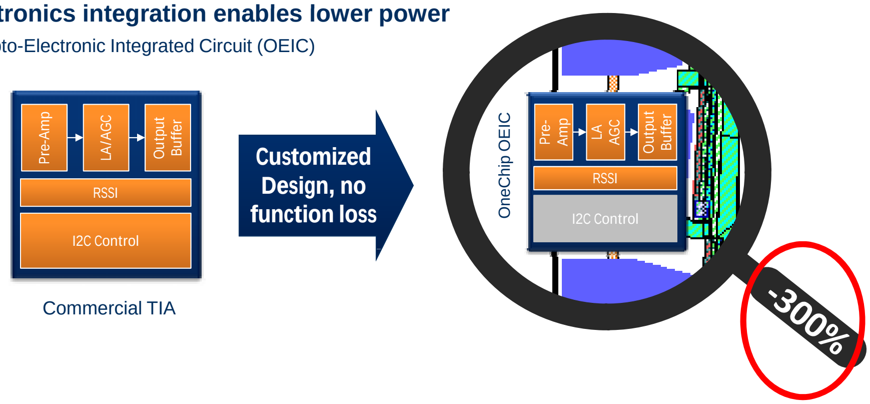
71

Optoelectronic Integrated Circuit (OEIC)

72

The game changer – Integrated electronics

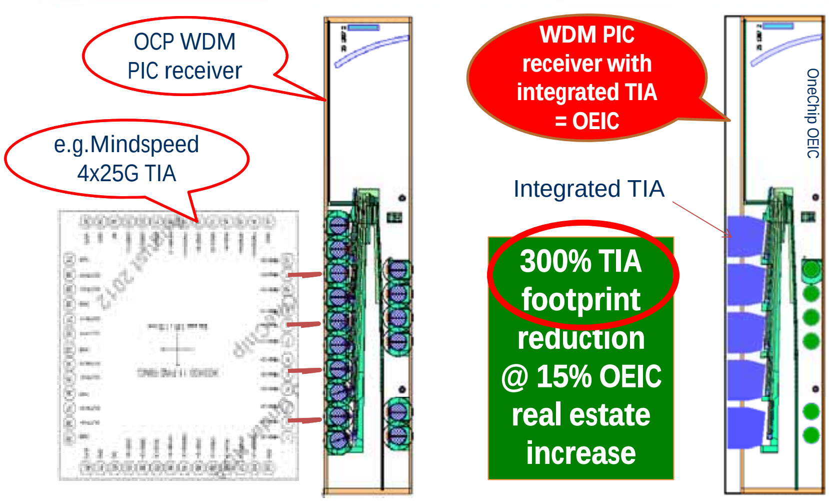
- **Indium Phosphide transistors are faster than Silicon**
  - F_t to 400+ GHz allows for future signaling speeds well over 100 Gbps per channel
- **Electronics integration enables miniaturization**
  - No I2C, no pads fan-out
- **Electronics integration enables lower power**
  - Opto-Electronic Integrated Circuit (OEIC)



Integrated electronics keeps all functionality!

73

OEIC integrates electronics onto the PIC



OEIC = Optoelectronic Integrated Circuit: A PIC chip with integrated electronics

OEIC enables tiny footprint and lower cost solution

Source: Mindspeed/MACOM

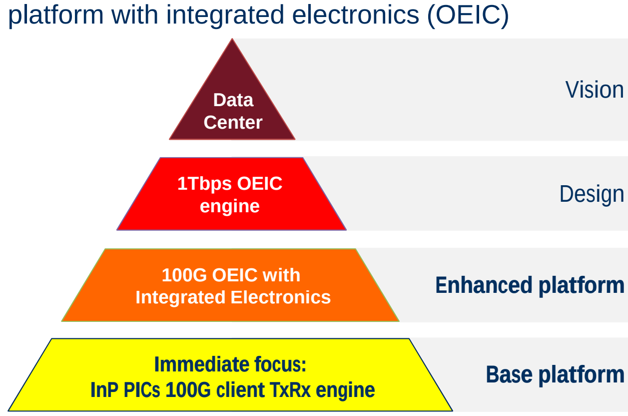
74

Caveat: so long as thermal issues are adequately addressed in packaging…

75

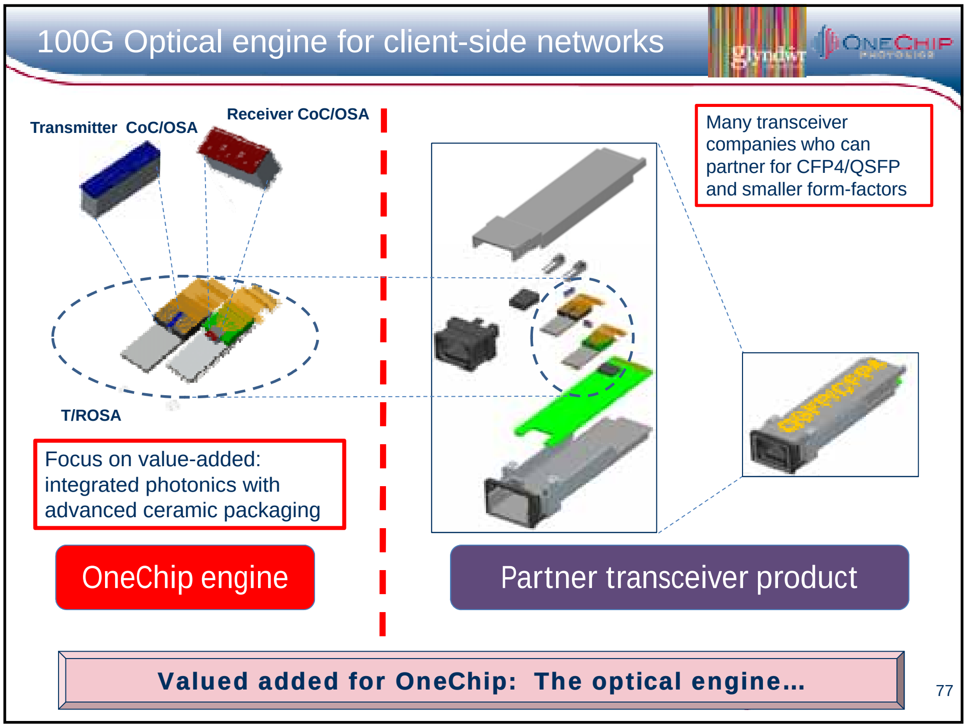
Datacenter PICs → OEICs

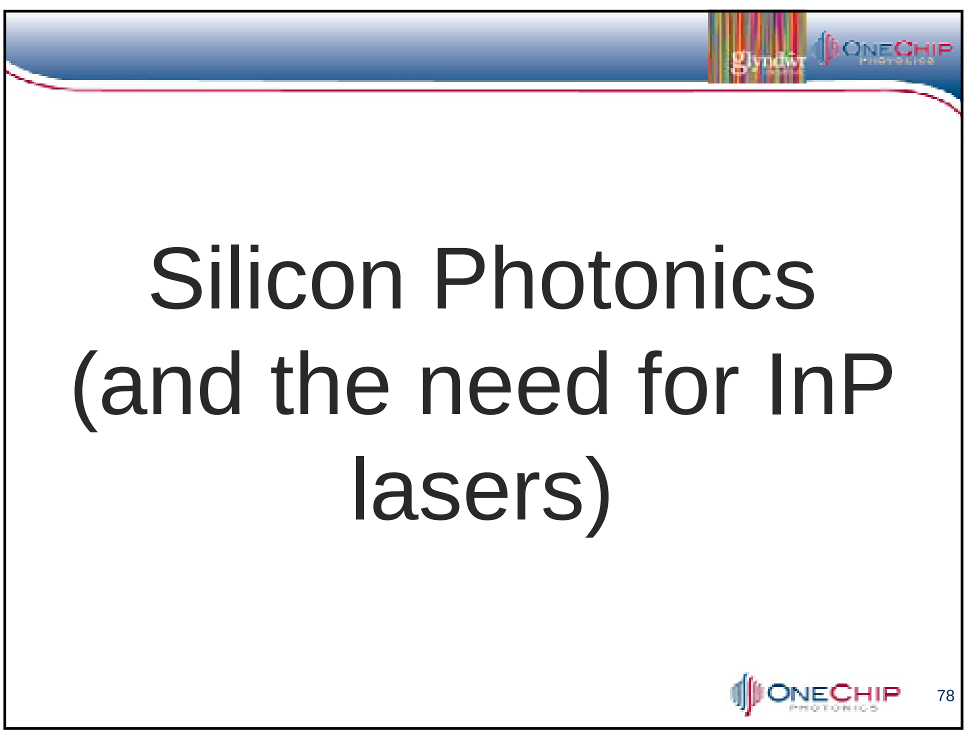
- Addressing datacenter pain-points using PICs →OEICs
  - Base platform of InP PICs
  - Enhanced platform with integrated electronics (OEIC)



Build immediate value using InP PIC base platform

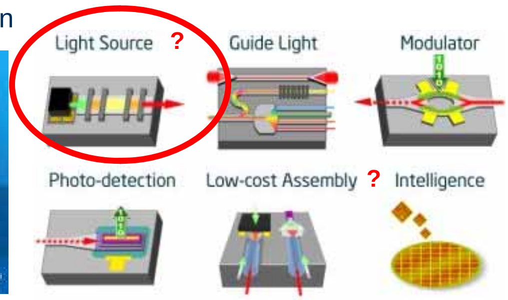
76


100G Optical engine for client-side networks
Transmitter CoC/OSA
Receiver CoC/OSA
T/ROSA
Many transceiver companies who can partner for CFP4/QSFP and smaller form-factors
Focus on value-added: integrated photonics with advanced ceramic packaging
OneChip engine
Partner transceiver product
Valued added for OneChip: The optical engine…
77


Silicon Photonics
(and the need for InP lasers)
78

What is silicon photonics?

- Use the economies of scale of a $B CMOS fab
  - Design photonics devices onto CMOS IC platform
  - Bump/package/bond InP lasers to that platform
    - Silicon laser big problem (at least commercially)
- Issues
  - Volume? <1% of the business of a silicon fab: attention?
  - Lasers? InP best option



Many merits; many questions; InP still plays a role

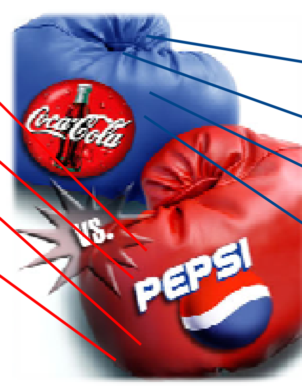
Source: Intel

79

Indium Phosphide vs Silicon Photonics

- Silicon CMOS can utilize large 300mm fabs / infrastructure
- InP has been truly proven to be robust/reliable/high performance platform for communications ✔

Indium Phosphide	Silicon Photonics
Monolithic Integration is the ultimate target	Silicon can't lase!
Opto-Eletronic IC (OEIC) made possible in single chip	Low power CMOS
Simpler packaging	Smaller feature leads to faster IC
Small size	Economies of scale

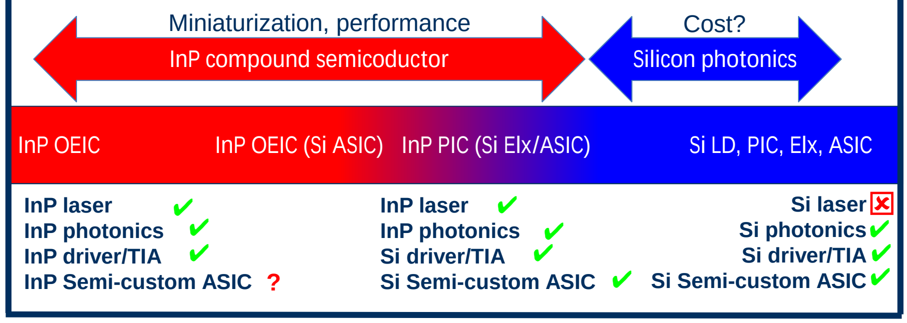


Winner has to achieve metrics: cost, power, perf, reliable

80

Role of InP in photonics integration

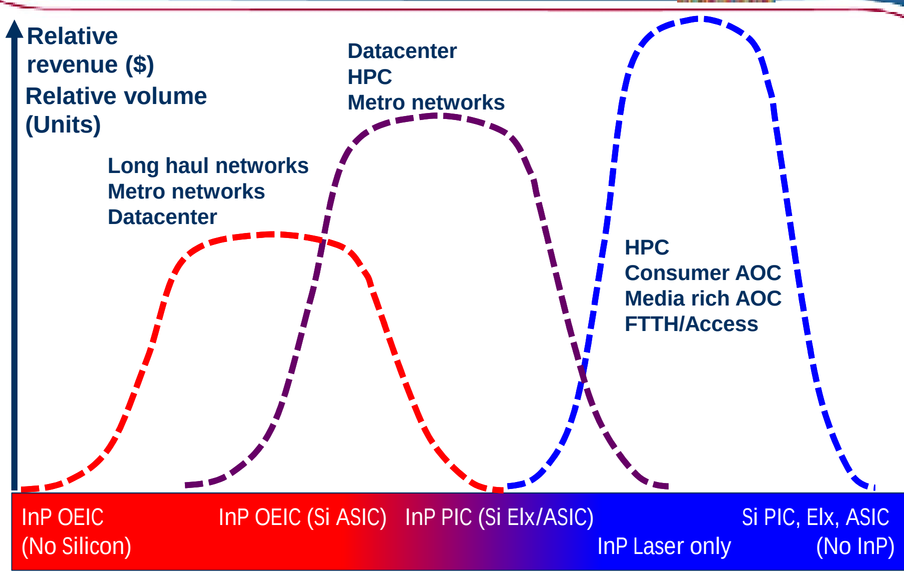
- Significant compound semiconductor platform
  - InP achieves the size, weight, power, performance, and cost challenges
  - Integrating electronics with photonics using InP drives new OEIC solutions



InP based OEICs drive functionality

81

Technology resonates with application…



No one solution fits all: winning requires focus…

82

TSMC IC capacity for silicon

~$1000/ 8"wafer
~$0 chip cost

Installed Capacity

2012 Overall Capacity +14%; 12-inch Capacity +21%

FAB / (Wafer size)		4Q11 (A)	2011 (A)	1Q12 (A)	2Q12 (A)	3Q12 (F)	4Q12 (F)	2012 (F)
Fab-2	(6") [1]	255	1,000	253	247	256	256	1,012
Fab-3	(8")	304	1,184	298	300	304	306	1,208
Fab-5	(8")	136	547	145	146	148	148	587
Fab-6	(8")	286	1,128	298	296	298	298	1,191
Fab-8	(8")	255	1,003	262	263	266	266	1,057
Fab-12	(12") [2]	337	1,334	373	367	378	382	1,500
Fab-14	(12") [2]	504	1,927	549	546	563	552	2,210
Fab-15	(12") [2]	6	9	0	18	69	135	222
WaferTech	(8")	107	429	110	111	112	112	444
TSMC China	(8")	230	772	222	230	232	236	924
TSMC & Subsidiaries (8" Equivalent Kpcs)		3,352	12,963	3,553	3,579	3,776	3,915	14,823
SSMC	(8")	65	258	64	64	65	65	258
Total TSMC-managed (8" Equivalent Kpcs)		3,417	13,221	3,616	3,643	3,841	3,980	15,080

(1) Figures represent number of 6" wafers. Conversion to 8"-equivalent wafers is obtained by dividing this number by 1.78.
(2) Figures represent number of 12" wafers. Conversion to 8"-equivalent wafers is obtained by multiplying this number by 2.25.

Open Innovation Platform™

Smallest fab runs 440k 8" wafers per year

83

Source: TSMC, Fraunhofer, Solid State Technology

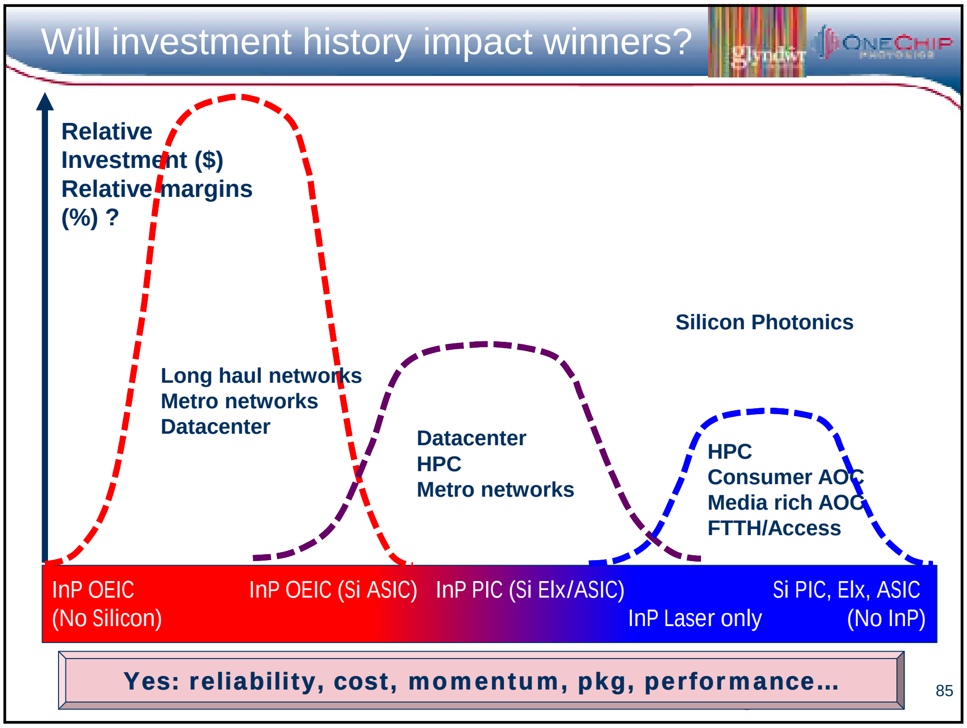
Market opportunity for silicon photonics

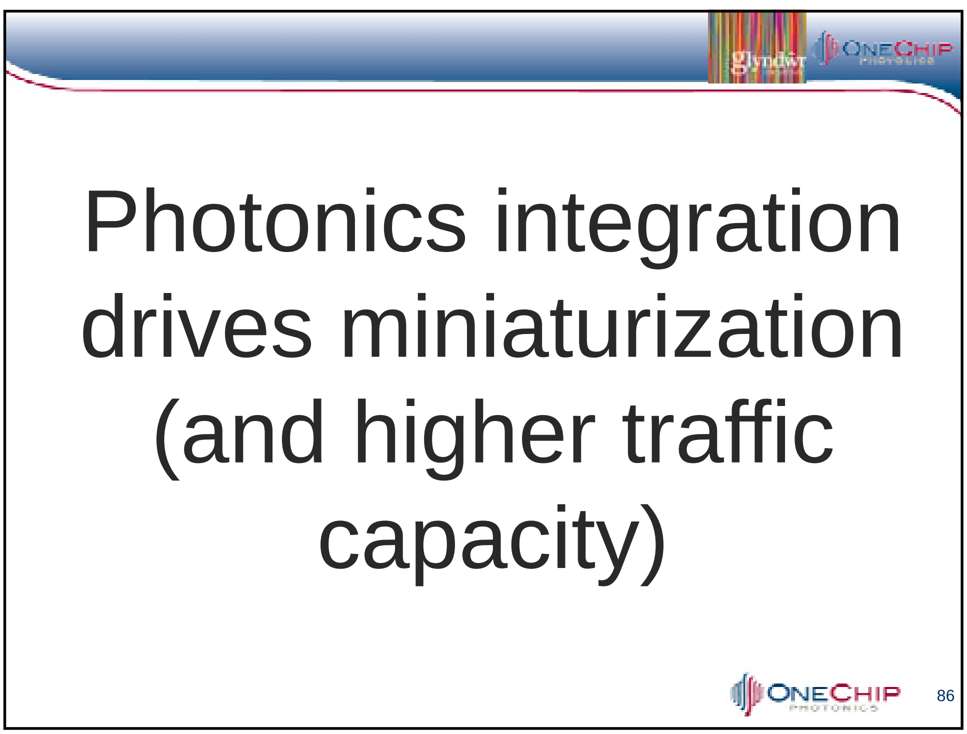
- FTTH (best case) 50M units @ 0.3mm^2 → 3000 8" wafers
- DC (best case) 50M units @ 0.3mm^2 → 3000 8" wafers
- LH/Metro (best case) 1M units @ 5mm^2 → 1000 8" wafers
- Smallest TSMC fab @ 8" → 444,000 8" wafers
- (or 8k wafers/week)
- If all of telecom goes silicon (unrealistic) then maybe 1 weeks work…
  - Assume negligible development costs
- Typical silicon IC upfront costs:
  - 130nm linewidth → fab cost ~$2B, R&D ~10-20% and design ~1-2% of fab cost
  - 22nm linewidth → fab cost ~$8B, R&D ~$1.6B, design ~$80M
- Silicon photonics investment for development today:
  - Skorpios, Luxtera, Lightwire, Kotura, Ranovus, Kaiam maybe → $250M
  - DC and FTTH: $250M/50M units → $5/unit (ok for DC, not so much for FTTH)
  - Telecom: $250M/1M units → $250/unit (seems high for telecom)

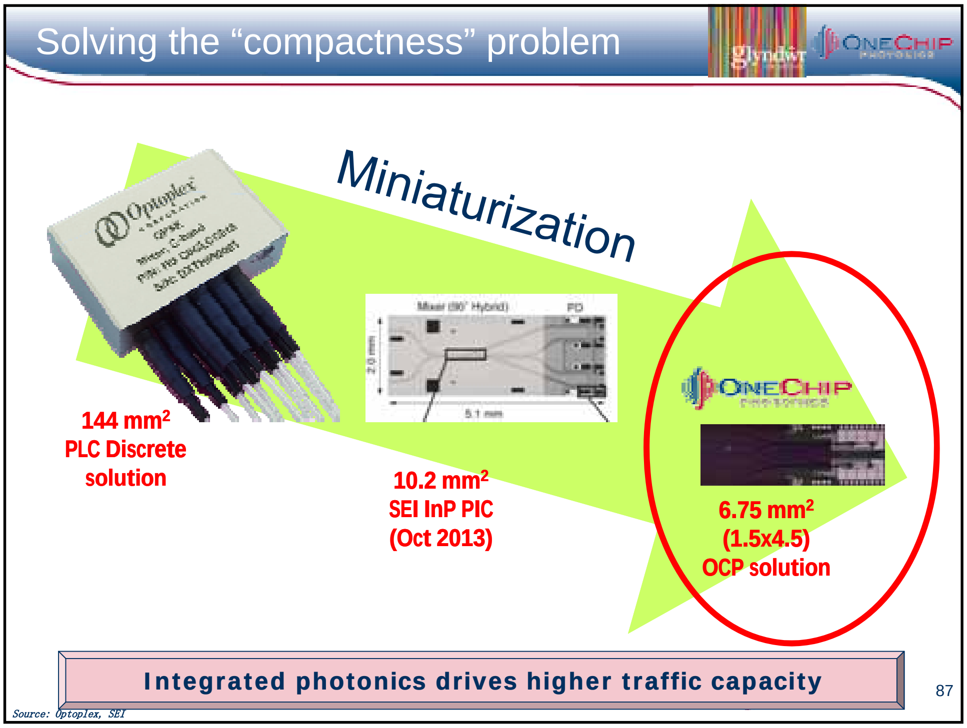
Smallest fab runs 440k 8" wafers per year

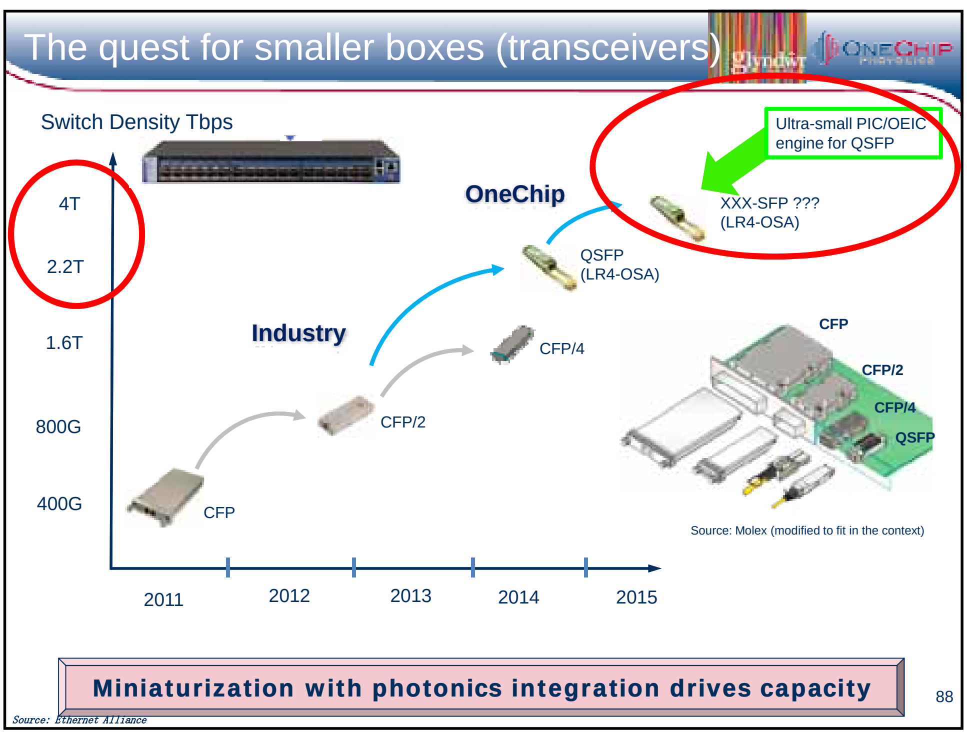
84

Source: Fraunhofer- HHI, TSMC, Solid State Technology


Will investment history impact winners?
Relative
Investment ($)
Relative margins
(%) ?
Silicon Photonics
Long haul networks
Metro networks
Datacenter
Datacenter
HPC
Metro networks
HPC
Consumer AOC
Media rich AOC
FTTH/Access
InP OEIC
(No Silicon)
InP OEIC (Si ASIC)
InP PIC (Si Elx/ASIC)
InP Laser only
Si PIC, Elx, ASIC
(No InP)
Yes: reliability, cost, momentum, pkg, performance…
85


Photonics integration
drives miniaturization
(and higher traffic
capacity)
86


Solving the "compactness" problem
Miniaturization
144 mm^2
PLC Discrete
solution
10.2 mm^2
SEI InP PIC
(Oct 2013)
6.75 mm^2
(1.5x4.5)
OCP solution
Integrated photonics drives higher traffic capacity
87
Source: Optoplex, SEI

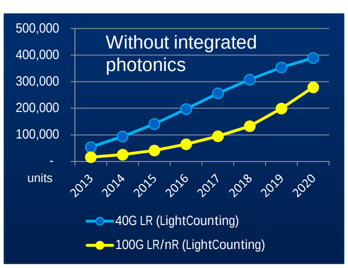

The quest for smaller boxes (transceivers)
Switch Density Tbps
4T
2.2T
1.6T
800G
400G
2011
2012
2013
2014
2015
OneChip
Industry
CFP
CFP/2
CFP/4
QSFP
(LR4-OSA)
XXX-SFP ???
(LR4-OSA)
Ultra-small PIC/OEIC
engine for QSFP
CFP
CFP/2
CFP/4
QSFP
Source: Molex (modified to fit in the context)
Miniaturization with photonics integration drives capacity
88
Source: Ethernet Alliance

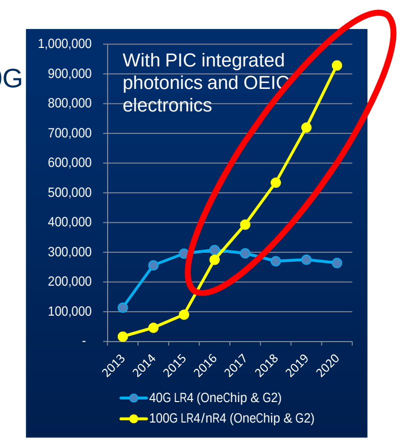
Photonics integration enables fast growing markets

89

Integration allows 100G penetration

- 100G market window opens in 2015
  - Integrated photonics with electronics enables smaller chip real estate OEICs
  - Cost competitive photonics enables OEICs to penetrate market faster at 100G

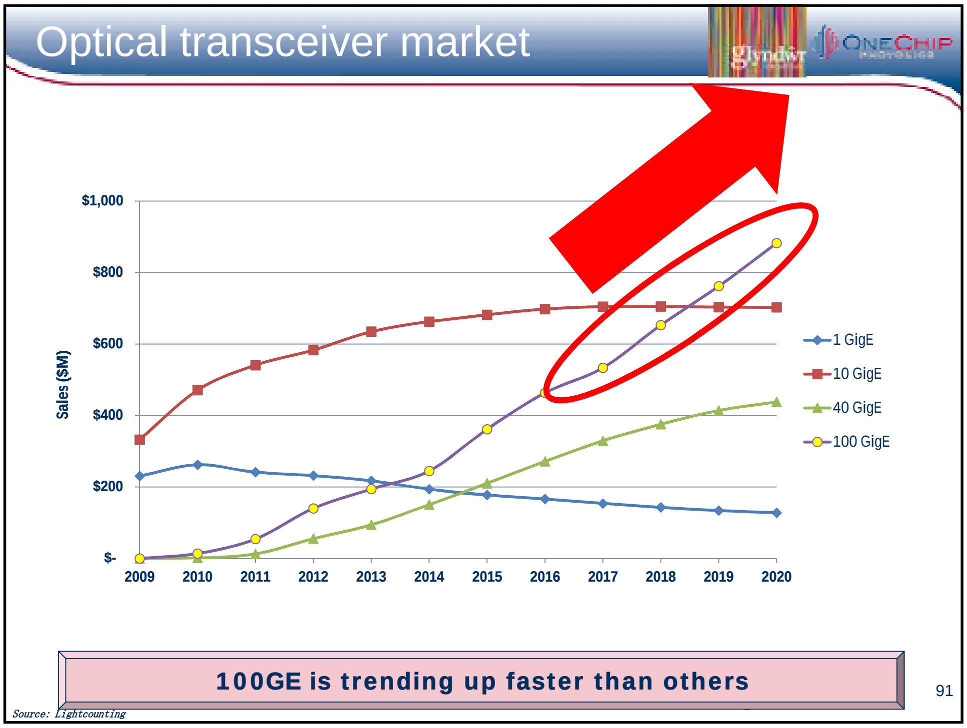


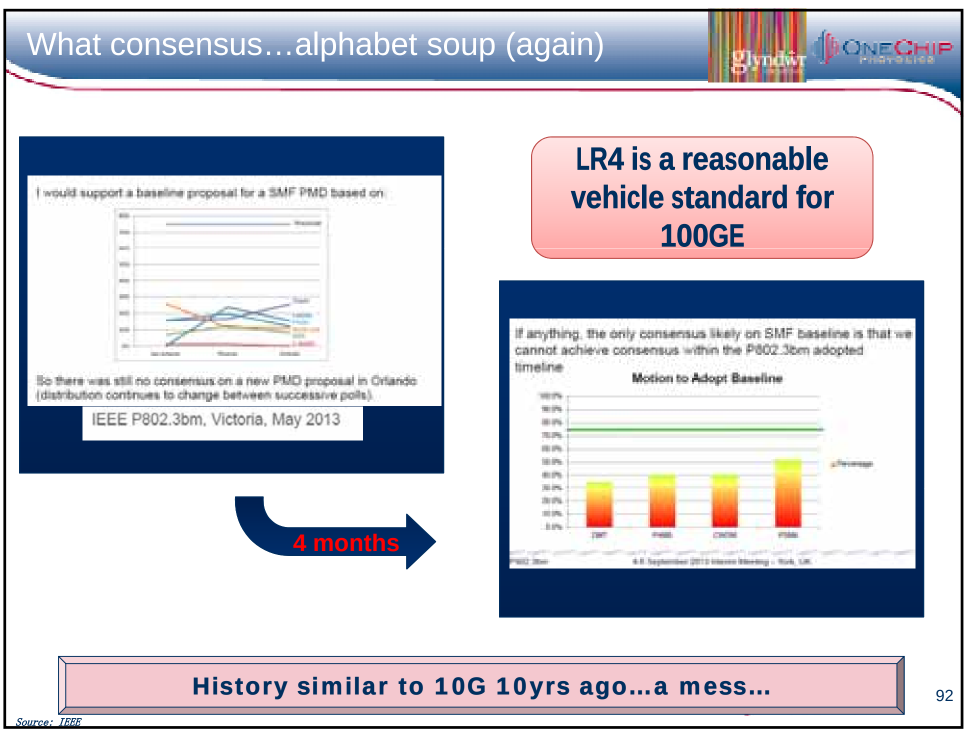


Photonics integration opens 100G market faster…

90

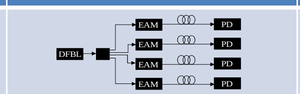
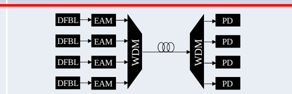
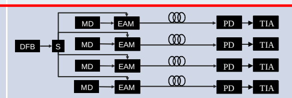
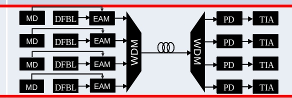
Source: Lightcounting


Optical transceiver market
Sales ($M)
$1,000
$800
$600
$400
$200
$-
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
1 GigE
10 GigE
40 GigE
100 GigE
100GE is trending up faster than others
91
Source: Lightcounting


What consensus…alphabet soup (again)
I would support a baseline proposal for a SMF PMD based on:
So there was still no consensus on a new PMD proposal in Orlando (distribution continues to change between successive polls).
IEEE P802.3bm, Victoria, May 2013
LR4 is a reasonable vehicle standard for 100GE
If anything, the only consensus likely on SMF baseline is that we cannot achieve consensus within the P802.3bm adopted timeline
Motion to Adopt Baseline
4 months
History similar to 10G 10yrs ago…a mess…
92
Source: IEEE

'Holy grail' using InP PIC→OEIC

- InP PIC mkt entry; OEIC with integrated electronics opens more doors (size, weight, power, and cost)

Solution	Link architecture	Market Desire	R&D Complex	Power Dissipation	Footprint Impact
PSM4 -PIC		★ Standards ???	★★★ Quickest TTM	★★★	★★★ CFP4/QSFP
LR4 -PIC		★★★ Attractive	★★	★★	★★★ CFP4/QSFP
PSM4 - OEIC		★ Standards ???	★	★★★	★★★ QSFP/Smaller
LR4 - OEIC		★★★ Very attractive	★ Complex	★★★	★★★ QSFP/Smaller

★★★ 3-star is the best

InP platform will serve LR4 very well

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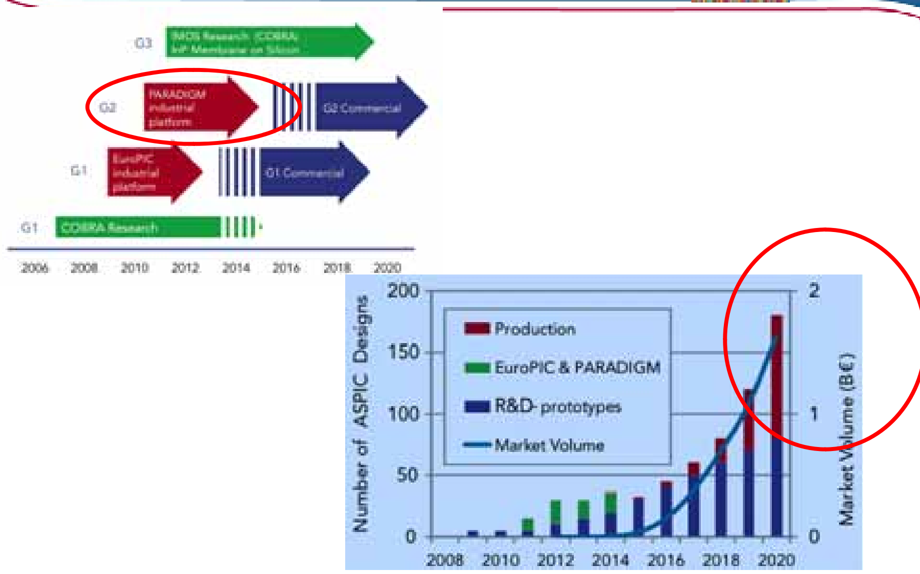
Trends in photonics integration



JePPIX roadmap 2013: Europe drives for PIC solutions

94

Source: JePPIX

Photonics integration is the very essence of 'green photonics'

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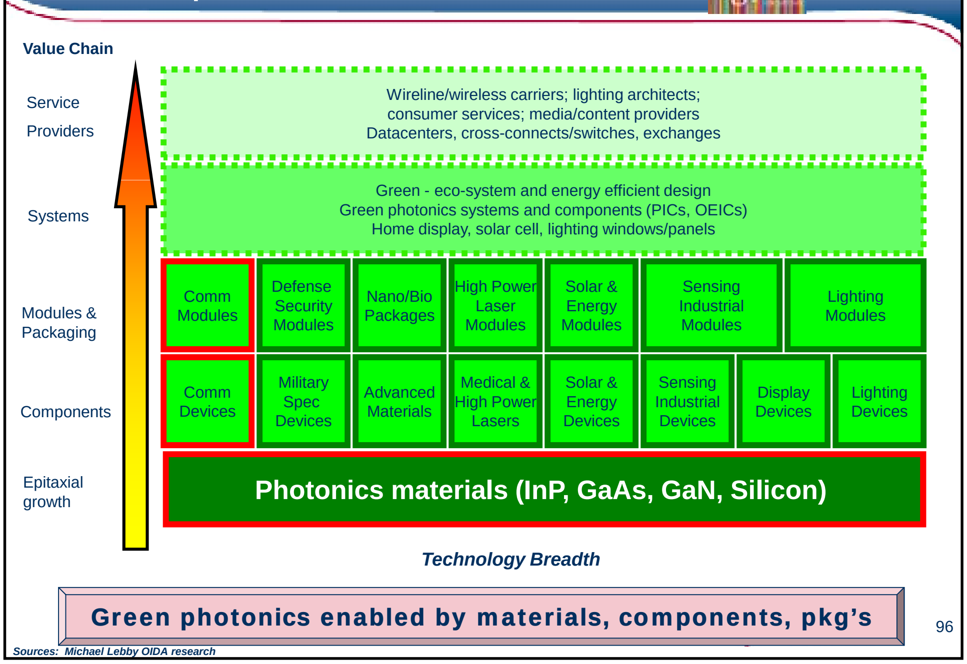
Green photonics value chain



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Drive by OIDA/OSA in 2013

- Status and future of photonic integration:
  - Classic USA roadmap workshop
  - ~60 attendees: all from photonics integration field
    - Both InP and silicon photonics senior engineers/leaders
  - 1 day workshop with sessions on
    - Industry, role of government agency
    - Customer needs for PICs
    - Consortia experience
  - White paper with high points:
    - Growing bandwidth requirements
    - Need to support scaling in challenged industry economics
    - Exploration of industry partnerships sharing common technology and manufacturing platforms
    - Ways to improve the competitiveness of US industry
    - Roadmaps and areas of focus

OIDA Optoelectronics Industry Development Association

Drive to position USA to be more competitive in PICs

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OIDA takeaways (from my perspective)

- Photonics integration is here to stay ✔
  - Complex technology: requires use of CMOS silicon infrastructure and InP experience in communications ✔
  - Combination of silicon and InP will be a successful vehicle for communications (at all levels) consumer, HPC, DC, to metro/long haul ✔
- Stakeholders in USA need:
  - Collaborative programs between industry, government, and academia
  - Testing/characterization sharing of resources
  - Foundry for packaging, assembly and prototyping new PIC/OEIC platforms
  - Building of software libraries for advanced photonic components (both silicon and InP)

Drive collaboration in USA…not an easy thing to achieve

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Takeaways…

- Packaging of photonics now challenged by integration
- Next generation ICs will be integrated photonics
  - Driven by traffic into datacenters
    - Datacenter pain points drive photonics integration
  - Photonics integration will grow to include electronics
    - PIC → OEIC (optoelectronic integrated circuit)
    - Silicon photonics will play a role using InP and impact high volume opportunities
    - Miniaturization through integration drives higher traffic capacity through performance (package & thermal issues important)
    - Photonics is green and will enable new technologies and products that will also be green…
- Photonics integration happening today…
  - OIDA uncovered weaknesses → Innovation, funding, collaboration, design tools for chips/packages, test/characterization…
  - Standards: chips, packages, test, simulation, characterization all needed

Photonics integration is emerging…both InP are Si can win

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End

(thanks for listening)

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michael@lebby.com

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Backup

Background and driver to the workshop

NATIONAL PHOTONICS INITIATIVE

- National Photonics Initiative (NPI)
  - Founding sponsors OSA and SPIE (with APS, IEEE, LIA)
  - Making photonics a priority for USA
- Harnessing Light (National Academy report 1998) → NPI
  - Identify and advance areas of photonics critical to maintaining competitiveness and national security
- (1) Drive funding and investment in areas of photonics critical to maintaining USA competitiveness and national security
  - Advanced manufacturing, defense, energy, health and medicine, IT, and communications
- (2) Develop federal programs that encourage great collaboration between USA industry, academia, and gvt labs
  - To better support the R&D of next-generation photonics technologies
- (3) Increase investment in education and job training programs
  - To reduce the shortage of technically skilled workers in photonics positions
- (4) Expand federal investments for university and industry collaborative research
  - To develop new manufacturing methods that incorporate photonics
- (5) Collaborate with USA industry to review international trade practices
  - impeding free trade and the current USA criteria restricting sale of certain photonic technologies overseas

Make USA more competitive in photonics

Datacenter vs HPC perspective:

- Key observations
  - 10c per Gbps metric (distances up to 2km) maybe 1 solution fits all
  - Expectation that DC pricing fall in line with HPC (soon) ✔
  - 400G to 1.6T range for total data rates
  - HPC thinking about SM fiber in addition to MM fiber ✔
  - Move data rates from 25G to 50G; wavelengths from 4 to ~16
  - Packaging trending towards optics being close to signal sources
  - PIC technologies aiming for next generation super computer
  - Power constraints problematic but not seen to be extreme
  - Creating eco-system that allows performance to go form teraflops to exaflops
  - Create 400G/1T interfaces (100/200G parallel not attractive solution) ✔
  - Extend OOK to alternative modulation techniques (non-coherent), and increase use of DSP as complexity increases

Challenge in cost and performance

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Silicon photonics perspective:

- Silicon photonics observations:
  - Focus on PIC interfacing with optics and chip
  - Focus on testing and evaluation ✔
  - Exploring single materials platform for all device types (going for best overall performance even if device is not best in class)
  - Looking at ubiquitous interfaces with electronics (more work required)
  - Aiming to achieve goals of 1pj/bit in optical links
    - Today Tx ~50pj/bit @10Gbps & Rx 250fj/bit @10Gbps
  - Aiming to communication >1Tbps between photonic chips
  - CMOS industry: leverage, leverage, leverage ✔ ✔
  - 300mm wafers, how to achieve economies of scale (volume) and serious attention when photonic throughput is 1% of CMOS capacity
  - Excite CMOS industry to design and package optics ✔
    - Need package innovation – high performance optics on a par with ICs

Leverage CMOS industry; test / evaluation; package

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InP PIC perspectives:

- InP material system observations:
  - Extend performance to 4Tbyte devices using more complex modulation schemes (line side)
  - Push performance beyond 500Gbps (5x114Gbps) Tx PIC architecture
  - Find easier ways to package using ceramic CoC engines ✔
  - Maintain reliability levels in the <10Fit rates (down to 1Fit)
  - Drive cost reduction 5-10x in $ per Gbps ✔
  - Explore ways to integrate driver/TIA functions in InP ✔
  - Create common platforms for testing and evaluation (similar to ICs)
  - Drive client-side DC solutions to 50Gbps
  - Create more cost effective CoC/OSAs for QSFP and smaller Tx/Rx boxes ✔
  - Challenge to improve packaging → look at 2.5D and 3D assembly with advanced Flip-chip and BGA approaches

Cost reduction, package, higher performance, smaller

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System & fiber perspectives

- System (line-side)
  - Extend use of QPSK even though QAM being deployed in field
    - 16QAM is complex
  - Increase card performance from 100G to 500G with PIC if it helps reduce the overall equipment cost ✔
  - Promote CD ROADM (Colorless, Directionless, ROADM)
  - 80-100 wavelengths/fiber and 50GHz spacing with 32G symbol rates
- System (metro)
  - PIC preferred for many designs ✔ ✔ ✔
- Fiber cable:
  - Explore multicore fiber to increase capacity
  - Explore fiber-chip coupling issues
  - Explore ways to increase MM performance to 300m at 25G (1310nm with SM/MM launch

Make the system more efficient

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Glossary

Glossary

CFP	C (100G) Form-factor Pluggable
CFP2	C (100G) Form-factor Pluggable 2 (half size)
CFP4	C (100G) Form-factor Pluggable 4 (a quarter size)
CoC	Chip on Carrier
EAM	Electro-Absorption Modulator
ECOC	European Conference on Optical Communication
IE	Integrated Electronics
LDD	Laser Diode Driver
LR	Long Reach (10km)
LR4	Long Reach 4 (contrary to PSM4, LR4 uses WDM muxing)
MD	Modulator Driver
MMF	Multi Mode Fiber
Mod	Modulator
nR	Medium Reach (500m)
OEIC	Opto-Electronic Integrated Circuit
OFC	Optics Fiber Conference
PIC	Photonic Integrated Circuit
PSM4	Parallel Single Mode 4
QSFP	Quad Small Form-factor Pluggable
ROSA	Receive Optical Sub-Assembly
SMF	Single Mode Fiber
SR	Short Reach (100-300m)
SSC	Spot Size Converter
TIA	TransImpedance Amplifier
TOSA	Transmit Optical Sub-Assembly
TROSA	Combined TOSA and ROSA
WDM	Wavelength Dvision Multiplexing