Directions in Mobile Device Packaging

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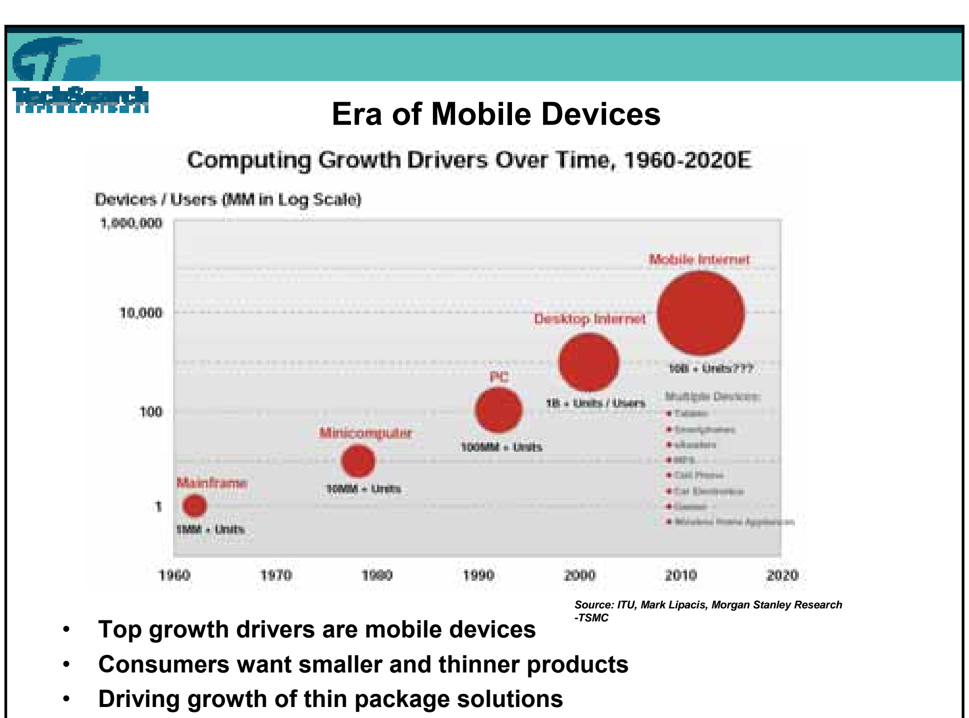

Mobile Devices

- **Mobile Devices**
  - **Laptops**
  - **Smartphones**
  - **Tablets**
  - **Feature phones**
  - **Wearable electronics**
- **Attributes**
  - **Typically shorter lifetimes (2 years)**
  - **Performance varies**
  - **Require high reliability in focused on drop test for high-end smartphones and tablets, some manufacturers not as concerned with drop or reliability because customer does not expect it**
- **System packaging needs**
  - **Small form factor**
  - **High performance, high bandwidth**
  - **Lower power consumption (consumers want longer battery life)**
  - **Thermal issues (air flow difficult)**
  - **Lower cost**
- **Packaging options**
  - **BGA, FBGA, LGA, (including MCM), PoP, stacked die CSP, QFN, SON, CLGA, WLP**
- **Cost/Performance Trade-off Determines Adoption, but Form Factor is Key**

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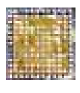
Packages for Mobile Devices

- **Touch screen controllers: quad flat no-lead (QFN), fine pitch ball grid arrays (FBGA)**
- **Antenna: ceramic land grid array (CLGA), QFN**
- **Power amplifiers: LGA (with laminate substrate), typically wire bond moving to flip chip**
- **RFIC: FBGA, flip chip BGA (FC-BGA), wafer level package (WLP), Fan-out WLP (FO-WLP)**
- **Modem IC: FC-BGA, stacked die package (FC and WB), package-on-package (PoP)**
- **Application processor: FC-BGA, bottom package of PoP**
- **NAND flash: FBGA**
- **Power management IC (PMIC): FC-BGA, WLP**
- **WiFi/Bluetooth: CLGA, LGA (with laminate substrate), WLP**
- **Near Field Communications (NFC): FBGA**
- **Sensors: LGA**

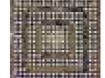
QFN

PoP

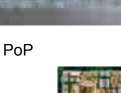
WLP



FO-WLP



FC-BGA



LGA module

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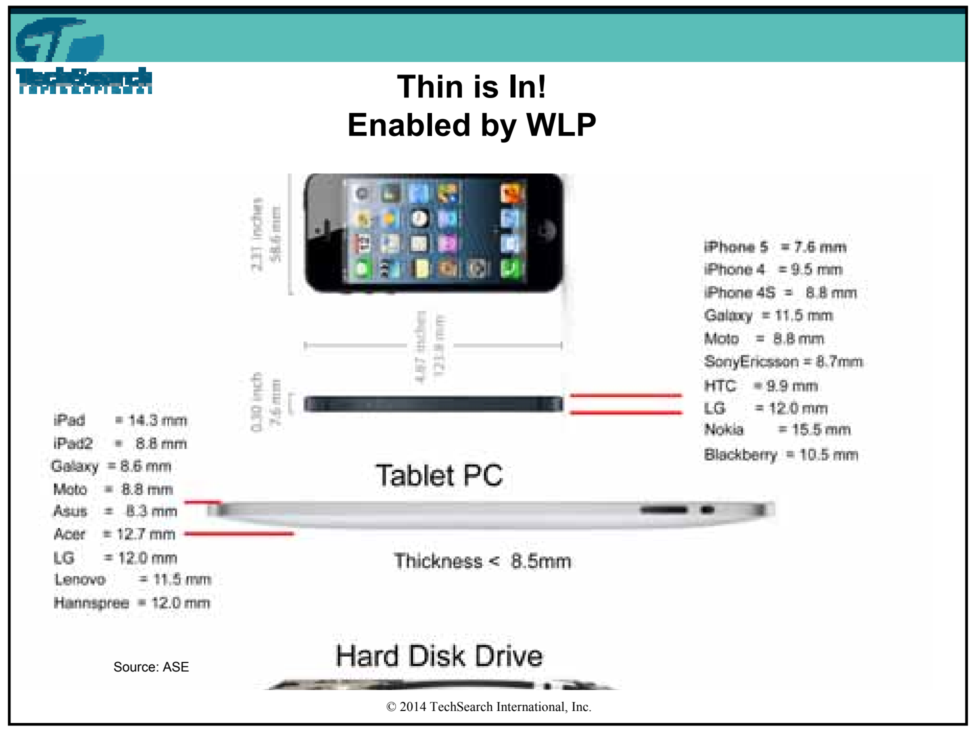
Thin is In!
Enabled by WLP
iPhone 5 = 7.6 mm
iPhone 4 = 9.5 mm
iPhone 4S = 8.8 mm
Galaxy = 11.5 mm
Moto = 8.8 mm
SonyEricsson = 8.7mm
HTC = 9.9 mm
LG = 12.0 mm
Nokia = 15.5 mm
Blackberry = 10.5 mm
iPad = 14.3 mm
iPad2 = 8.8 mm
Galaxy = 8.6 mm
Moto = 8.8 mm
Asus = 8.3 mm
Acer = 12.7 mm
LG = 12.0 mm
Lenovo = 11.5 mm
Hannspree = 12.0 mm
Tablet PC
Thickness < 8.5mm
Hard Disk Drive
Source: ASE
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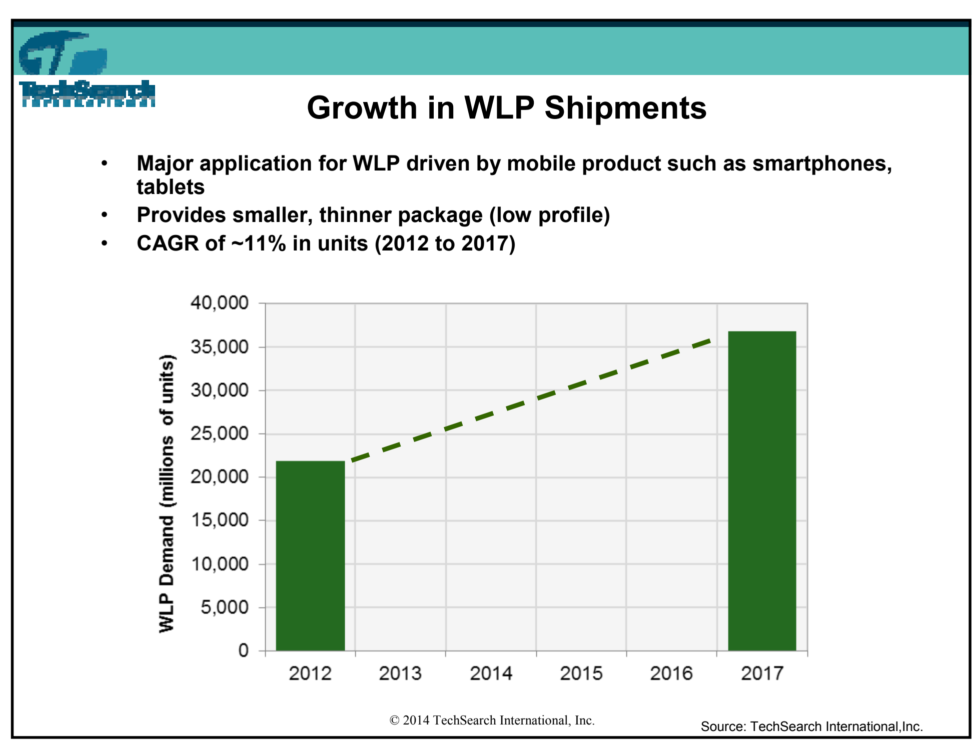
Growth in WLP Shipments
• Major application for WLP driven by mobile product such as smartphones, tablets
• Provides smaller, thinner package (low profile)
• CAGR of ~11% in units (2012 to 2017)
WLP Demand (millions of units)
40,000
35,000
30,000
25,000
20,000
15,000
10,000
5,000
0
2012
2013
2014
2015
2016
2017
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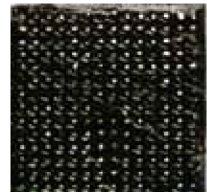
Source: TechSearch International,Inc.

WLP Trends

- Consumer products and other applications
  - Mobile phones (highest volume application)
  - Digital cameras and camcorders
  - MP3 players (such as iPods)
  - Watch modules
  - Laptop and tablet computers
  - Medical
  - Automotive
  - Wearable electronics
- Conventional WLPs for many device types
  - WLPs for analog functions, power management, RF, wireless LAN, IPD, LED driver, sound IC, etc.
  - Highest I/O count 309 (Fujitsu power management IC)
  - Largest body size Apple/Cirrus Logic Audio CODEC 5.72 x 6.03 x 0.59 mm, 121 solder balls, 0.5mm pitch
  - Increasing number of 0.4mm pitch parts, some 0.35mm pitch



Source: TPSS

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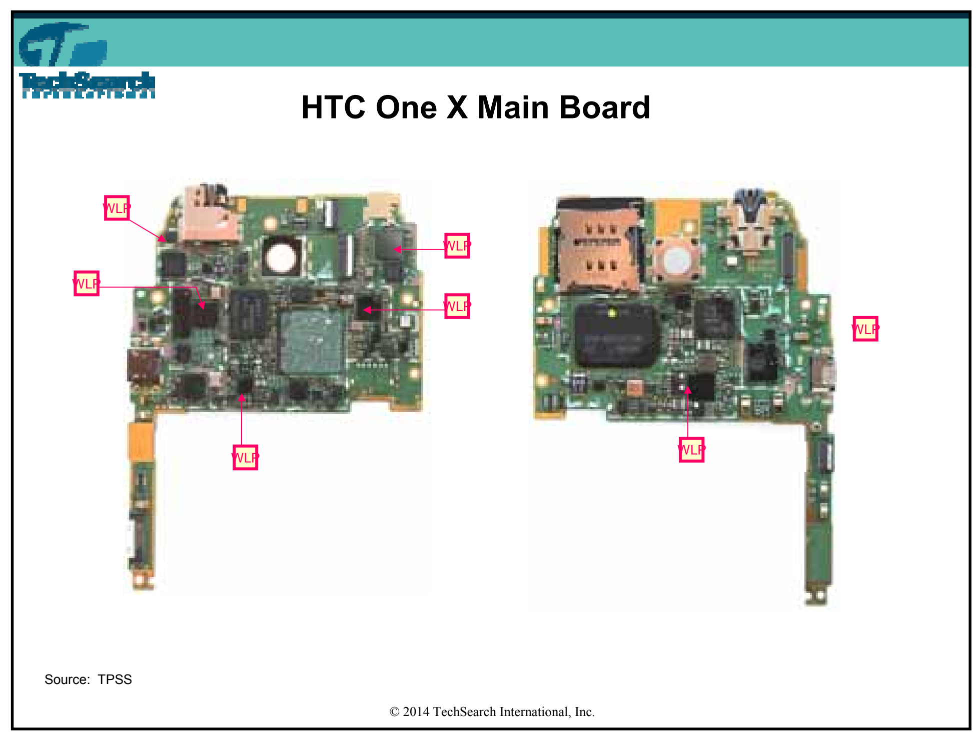
HTC One X Main Board



Source: TPSS

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WLP Examples in Mobile Phones

Mobile Phone (number of WLPs)	Supplier (function)	Ball Count	Size (mm)	Pitch (mm)
Apple iPhone 5 (11+)	Unknown	9	1.49 x 1.43 x 0.57	0.5
	AJY	9	1.58 x 1.59 x 0.45	0.5
	Qualcomm (RF power mgt.)	105	4.63 x 3.88 x 0.57	0.4
	RFMD (antenna)	12	1.91 x 2.08 x 0.53	0.4
	Apple/Cirrus	42	2.79 x 3.53 x 0.45	0.4
	Unknown	8	1.96 x 2.74 x 0.47	0.5
	NXP (LED driver)	36	2.11 x 2.14 x 0.4	0.35
	Broadcom (controller)	72	3.31 x 4.39 x 0.54	0.4
	AKM (electronic compass)	14	1.6 x 1.6 x 0.48	0.4
	TI (touch screen controller)	99	4.64 x 3.81 x 0.64	0.4
	ShellOP (ligh sensor)	6	2.4 x 1.7 x 0.8	_
Samsung Galaxy S3 GT-10300 (6)	Asahi Kasei (compass)	14	2 x 1.98 x 0.51	0.5
	Maxim (PMIC/MU/control)	100	4.52 x 4.54 x 0.69	0.4
	Maxim (PMIC)	144	5.14 x 5.1 x 0.64	0.4
	Broadcom (receiver)	42	3.04 x 2.87 x 0.57	0.4
	Wolfson (CODEC)	90	4.18 x 3.88 x 0.45	0.4
	Intel (RFIC) eWLB	139	5 x 5.3 x 0.67	0.4
HTC One X (7)	Intel (RFIC) eWLB	148	5.39 x 5.03 x 0.67	0.4
	Asahi Kasei (compass)	14	1.98 x 1.97 x 0.48	0.5
	TI (WiFi/Bluetooth/FM tran)	174	5.7 x 5.35 x 0.64	0.4
	TI (PMIC)	81	4.82 x 4.83 x 0.52	0.5
	Unknown	36	3 x 3 0.7	0.4
	TI (PMU for Tegra 3)	154	5.38 x 5.23 x 0.54	0.4
	Unknown	20	2.09 x 1.71 x 0.5	0.4

Source: TPSS

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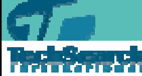
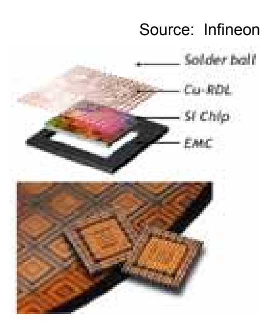


Fan-Out Wafer Level Package

- Reconstituted wafer and perimeter mold compound allows for redistribution of I/O beyond current chip footprint
  - Uses KGD
  - Number of interconnects, pitch of interconnect independent of chip size
  - Mold compound used to support the FO
  - Single, multi-die, or 3D solution
- Considered an embedded package because die is placed with interconnect on top
- Fan-out WLP (FO-WLP) from ADL Engineering, Amkor, ASE, Deca Technologies, Freescale Semiconductor, FCI/Fujikura, J-Devices, NANIUM, Nepes, SPIL, STATS ChipPAC, TSMC, YOUR NAME HERE
- Infineon eWLB (wireless operation acquired by Intel)
  - Technology licensed by ASE, STATS ChipPAC, NANIUM
  - Production lines at STATS ChipPAC and NANIUM today are wafers, panel in future

Source: Infineon



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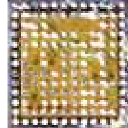
Fan-Out WLP Applications

- Applications
  - RF
  - Baseband processor
  - Potential for memory, PMIC, Application Processor, ASIC, controllers, media chips, medical devices, sensors
- FO-WLP shipments of hundreds of millions of units each year
  - Infineon (now Intel's IMC division) wireless products
  - Others

Intel Wireless Division
LTE analog baseband
5.32 x 5.04 x 0.7mm eWLB
127 balls, 0.4mm pitch



Source: TPSS

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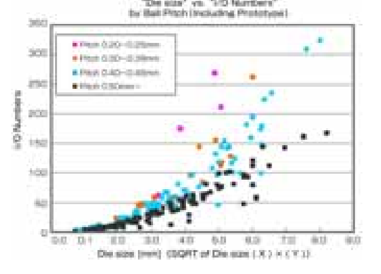
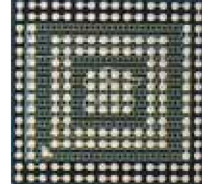
FO-WLP: Drivers

- Smaller form factor, lower profile package: similar to conventional WLP in profile
- Increased I/O density
  - Originally marketed as an alternative to fine pitch fan-in WLP
- Thinner than flip chip package (no substrate)
  - Comparing to FC-CSP
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance
- Fine L/S (10/10µm)
- Can enable a low-profile PoP solution as large as 15 mm x 15 mm
- Multiple die in a low-profile package
  - Die fabricated from different technology nodes can be assembled in one a single package
- Multi layer RDL with FO-WLP
  - Higher routing level with more lines and traces
  - Shield and power dissipation needs
  - Enabler of further form factor reduction



Source: Casio Micronics



Source: IMC

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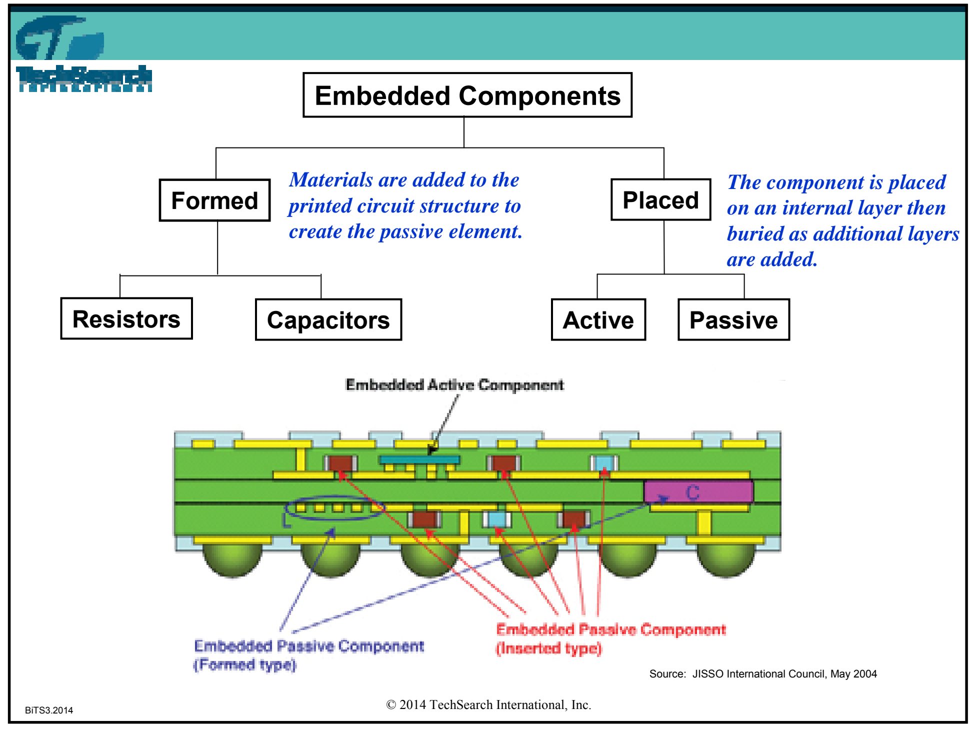
Embedded Components
Formed
Materials are added to the printed circuit structure to create the passive element.
Placed
The component is placed on an internal layer then buried as additional layers are added.
Resistors
Capacitors
Active
Passive
Embedded Active Component
Embedded Passive Component
(Formed type)
Embedded Passive Component
(Inserted type)
Source: JISSO International Council, May 2004
BiTS3.2014
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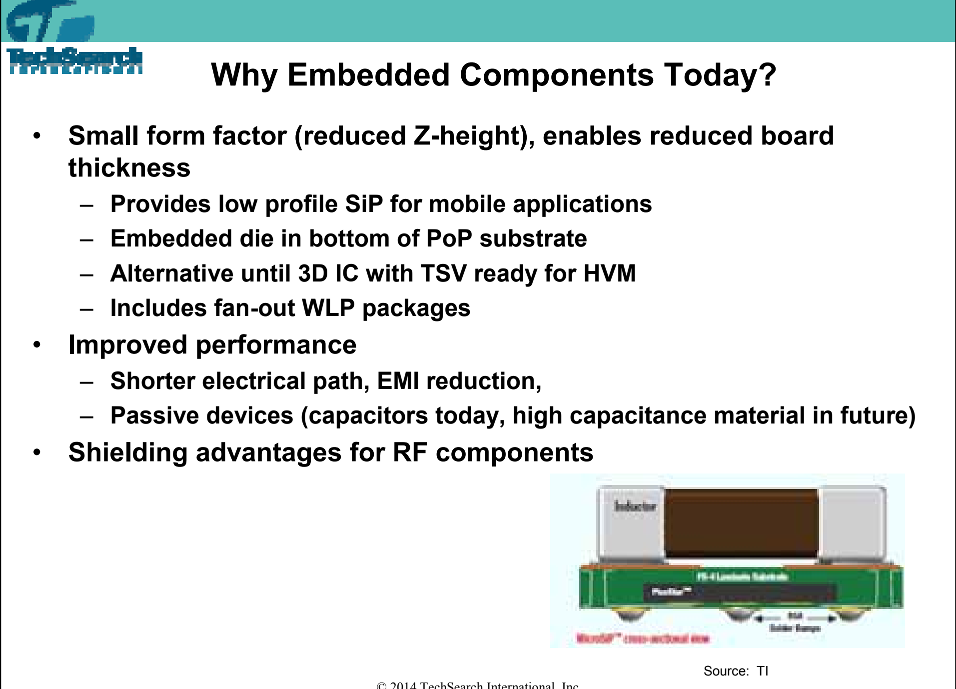
Why Embedded Components Today?
• Small form factor (reduced Z-height), enables reduced board thickness
– Provides low profile SiP for mobile applications
– Embedded die in bottom of PoP substrate
– Alternative until 3D IC with TSV ready for HVM
– Includes fan-out WLP packages
• Improved performance
– Shorter electrical path, EMI reduction,
– Passive devices (capacitors today, high capacitance material in future)
• Shielding advantages for RF components
Source: TI
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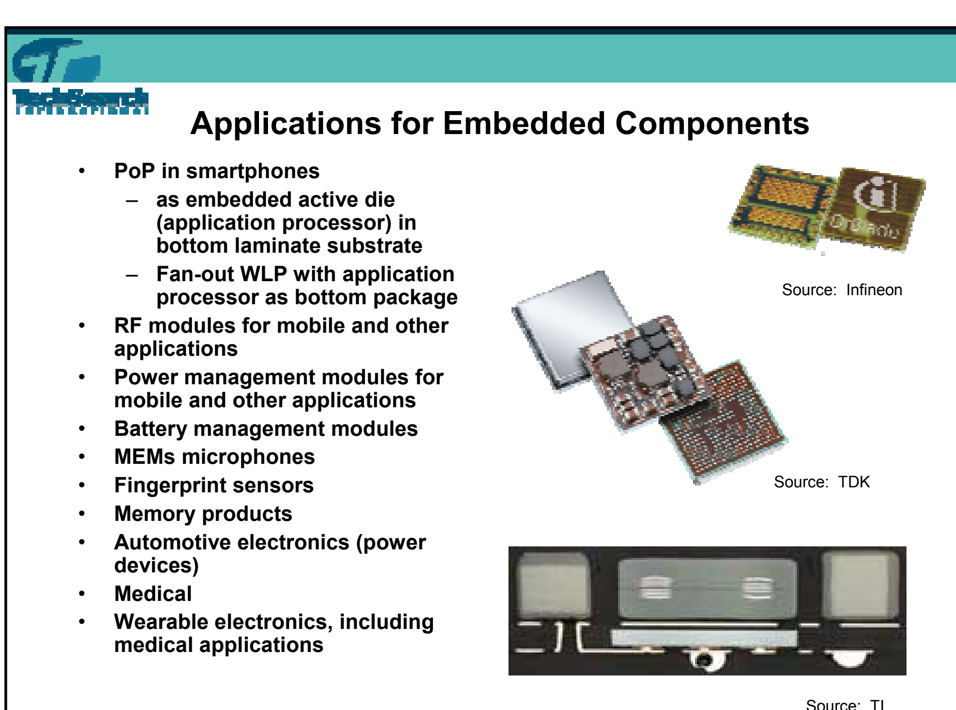
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Applications for Embedded Components
PoP in smartphones
as embedded active die (application processor) in bottom laminate substrate
Fan-out WLP with application processor as bottom package
RF modules for mobile and other applications
Power management modules for mobile and other applications
Battery management modules
MEMs microphones
Fingerprint sensors
Memory products
Automotive electronics (power devices)
Medical
Wearable electronics, including medical applications
Source: Infineon
Source: TDK
Source: TI
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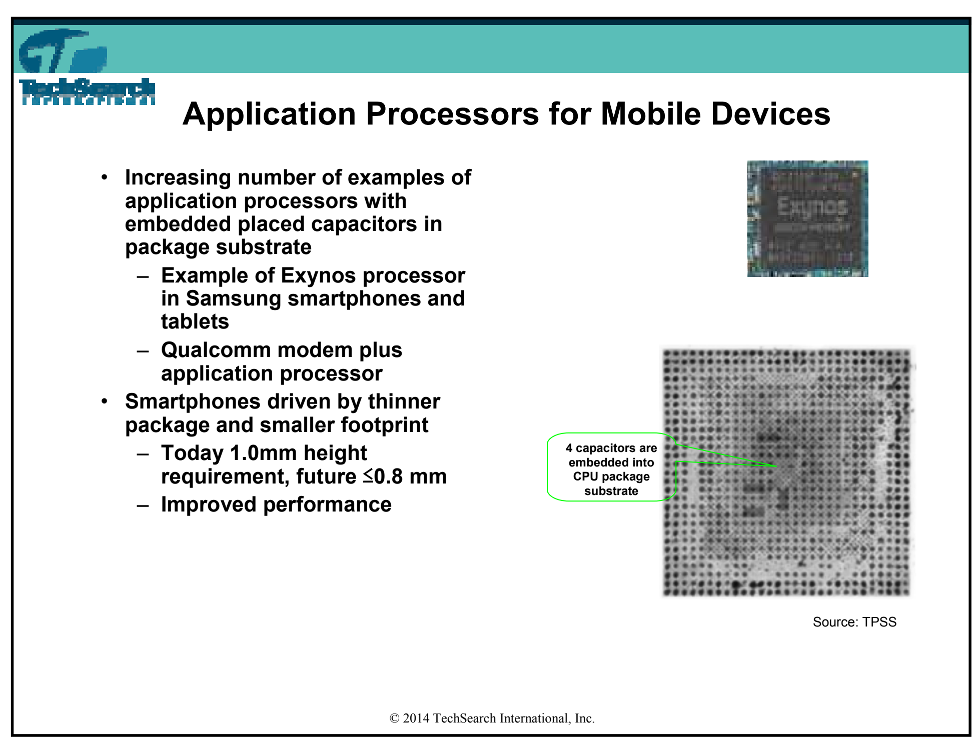
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Application Processors for Mobile Devices
Increasing number of examples of application processors with embedded placed capacitors in package substrate
Example of Exynos processor in Samsung smartphones and tablets
Qualcomm modem plus application processor
Smartphones driven by thinner package and smaller footprint
Today 1.0mm height requirement, future ≤0.8 mm
Improved performance
Exynos
4 capacitors are embedded into CPU package substrate
Source: TPSS
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Application Processor Packaging Trends

- Thinner package and smaller footprint
  - Today 1.0mm height requirement
  - Future ≤0.8 mm
- 3D IC with TSV provides the ultimate in in package height reduction
  - Highest density, highest performance
  - Lowest profile, smallest form factor
- PoP in smartphones
  - Embedded capacitors for improved performance HVM today
  - as embedded active die (application processor) in bottom laminate substrate
  - Fan-out WLP with application processor as bottom package

Source: Renesas

Source: H. Ueda, SemiConsult

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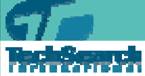

What's Next? Wearable Electronics

- Wearable electronics includes watches and bands, eye wear, hearing aids, fitness and health trackers, conformal electronic skin patches, sensing and touch-based e-textiles, personalized lighted clothing, gaming
- Strong growth market
  - $14B in 2014 to $70B market in 2024
  - 10X growth in unit volumes 2013-2018
- Variety of devices
  - Power management
  - Sensors
  - Microcontrollers
  - LEDs and RFIDs
  - Passives
- Variety of package types
  - BGAs and CSPs
  - Leadframe packages such as QFNs
  - WLPs
  - SiPs
  - Embedded devices and materials
- Challenges: Cost, miniaturization and thermal

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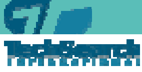

Conclusions

- Mobile world continues to drive…
  - Volumes
  - Package trends
  - Technology development
  - Some future wearable electronics
- Thin products are driving thin package solutions
  - Must meet steep ramp with high volume
- Trend in WLP for mobile devices
  - Conventional WLP
  - FO-WLP
- Old technology, new names
- Adoption of new technology
  - Cost/performance trade-off
  - Test considerations
  - Established infrastructure

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