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Survey and Review of 2.5/3D IC Packaging Technologies Part 1 - Overview

IEEE/CPMT, April 9, 2014

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AGENDA

Part 1

Introduction

Why Complement "2D Silicon Designs" with …
… 2.5D and/or 3D-IC Packaging Technology

Designs Completed // in Progress and Future

Business Considerations

Summary and Q & A

Part 2

Deep Dive into Topics of Interest

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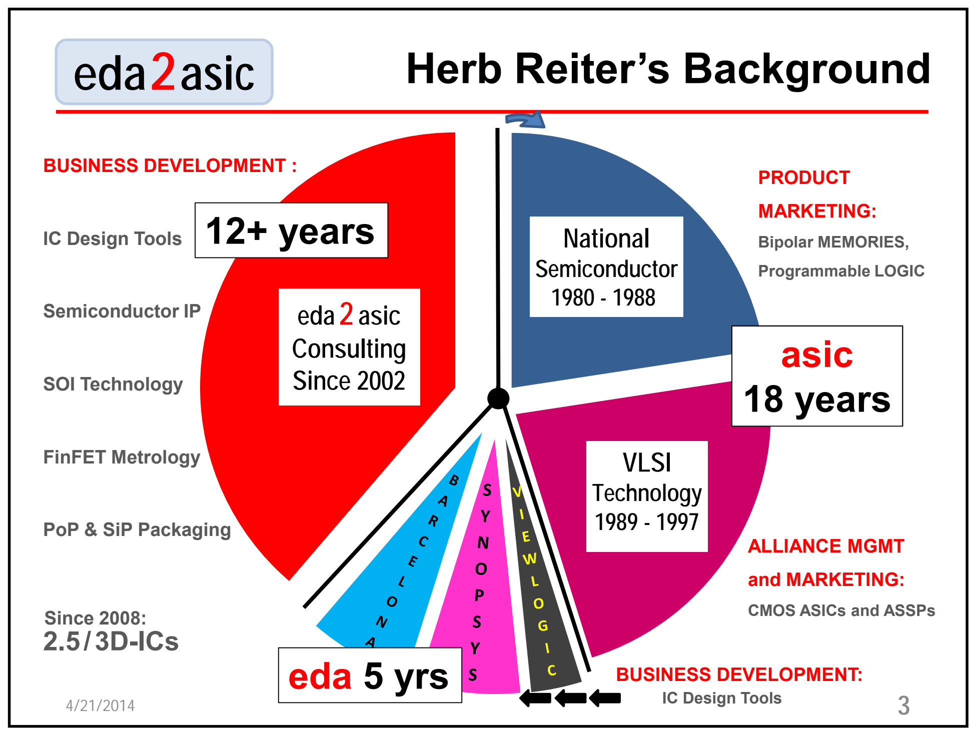

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"House-Keeping"

Keep the meeting interactive & relevant for YOU

Flip Chart to capture "Q's" – and discuss "A's" later

Soft-copies of the slides will be made available

Web-pointers on slides lead to further details

Appendix: 3D books, conferences, R&D partners

Part 2 will be a deep dive into topics of interest

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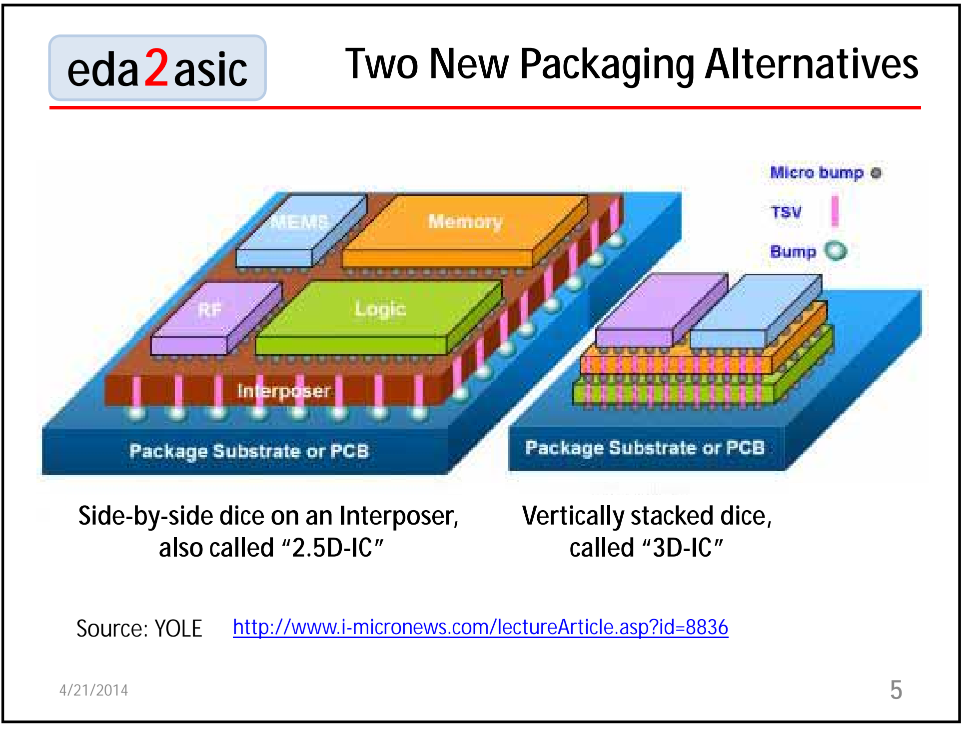
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Two New Packaging Alternatives
Micro bump
TSV
Bump
MEMS
Memory
RF
Logic
Interposer
Package Substrate or PCB
Package Substrate or PCB
Side-by-side dice on an Interposer, also called "2.5D-IC"
Vertically stacked dice, called "3D-IC"
Source: YOLE http://www.i-micronews.com/lectureArticle.asp?id=8836
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http://www.intel.com/technology/mooreslaw/
Why Complement "2D Silicon Designs"...
... with 2.5D and/or 3D-IC Packaging Technology
2D
2.5D
3D
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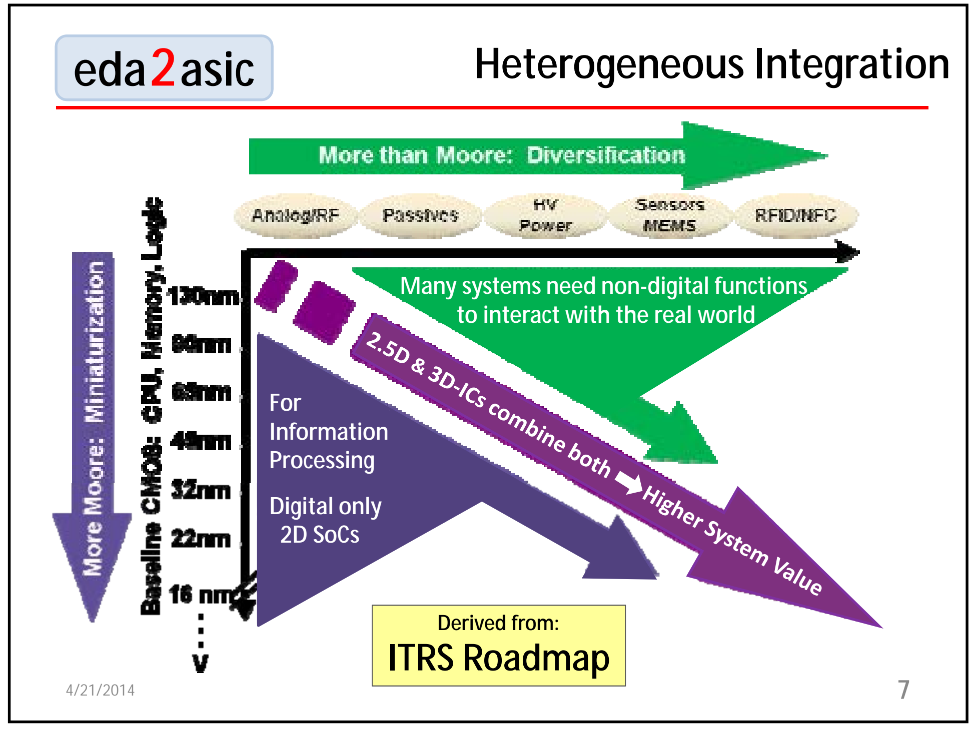
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Heterogeneous Integration
More than Moore: Diversification
Analog/RF
Passives
HV Power
Sensors MEMS
RFID/NFC
More Moore: Miniaturization
Baseline CMOS: CPU, Memory, Logic
130nm
90nm
65nm
45nm
32nm
22nm
16 nm
Many systems need non-digital functions to interact with the real world
2.5D & 3D-ICs combine both → Higher System Value
For Information Processing
Digital only 2D SoCs
Derived from:
ITRS Roadmap
4/21/2014
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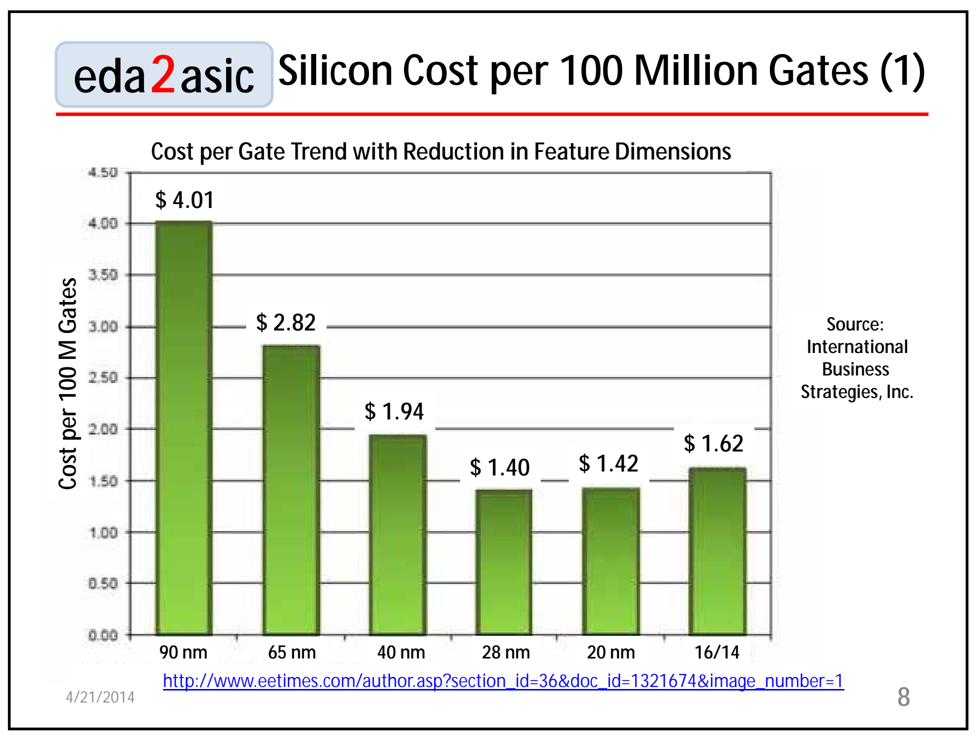
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Silicon Cost per 100 Million Gates (1)
Cost per Gate Trend with Reduction in Feature Dimensions
Cost per 100 M Gates
$ 4.01
$ 2.82
$ 1.94
$ 1.40
$ 1.42
$ 1.62
90 nm
65 nm
40 nm
28 nm
20 nm
16/14
Source: International Business Strategies, Inc.
http://www.eetimes.com/author.asp?section_id=36&doc_id=1321674&image_number=1
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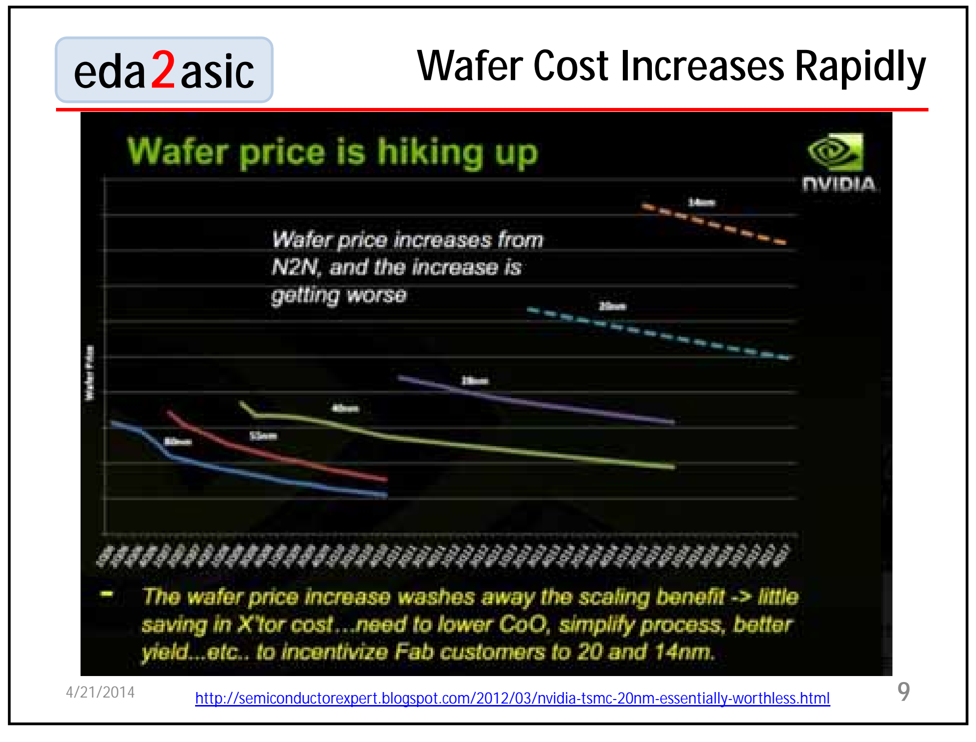
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Wafer Cost Increases Rapidly
Wafer price is hiking up
NVIDIA
Wafer price increases from N2N, and the increase is getting worse
- The wafer price increase washes away the scaling benefit -> little saving in X'tor cost…need to lower CoO, simplify process, better yield…etc.. to incentivize Fab customers to 20 and 14nm.
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http://semiconductorexpert.blogspot.com/2012/03/nvidia-tsmc-20nm-essentially-worthless.html
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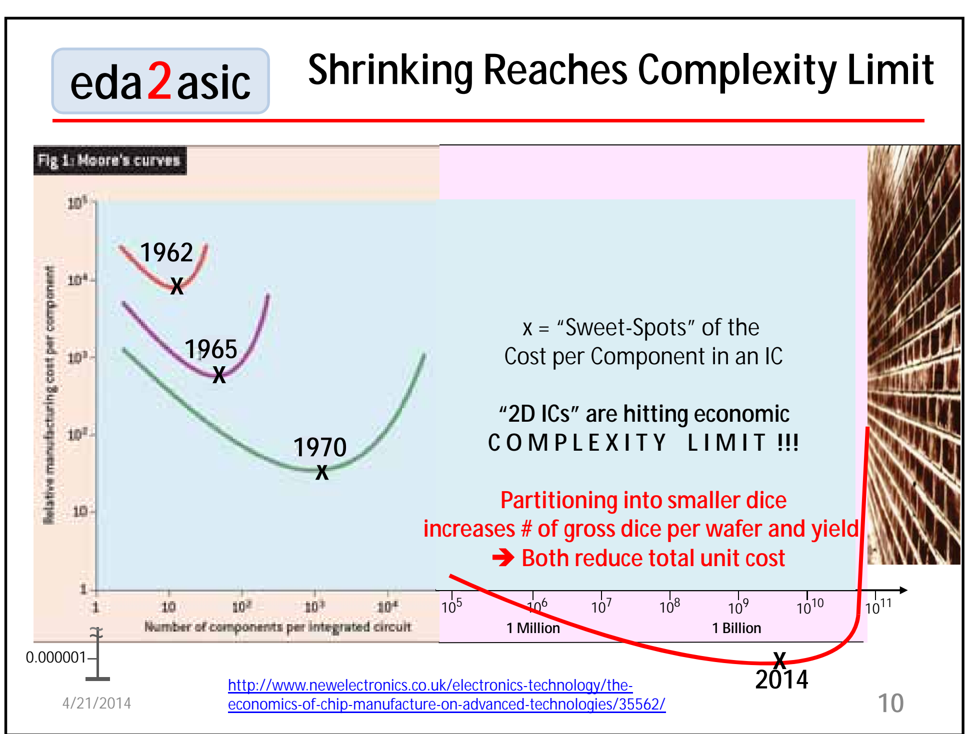
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Shrinking Reaches Complexity Limit
Fig 1: Moore's curves
1962
1965
1970
2014
x = "Sweet-Spots" of the Cost per Component in an IC
"2D ICs" are hitting economic COMPLEXITY LIMIT !!!
Partitioning into smaller dice increases # of gross dice per wafer and yield
➔ Both reduce total unit cost
Relative manufacturing cost per component
Number of components per integrated circuit
1 Million
1 Billion
0.000001
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http://www.newelectronics.co.uk/electronics-technology/the-economics-of-chip-manufacture-on-advanced-technologies/35562/
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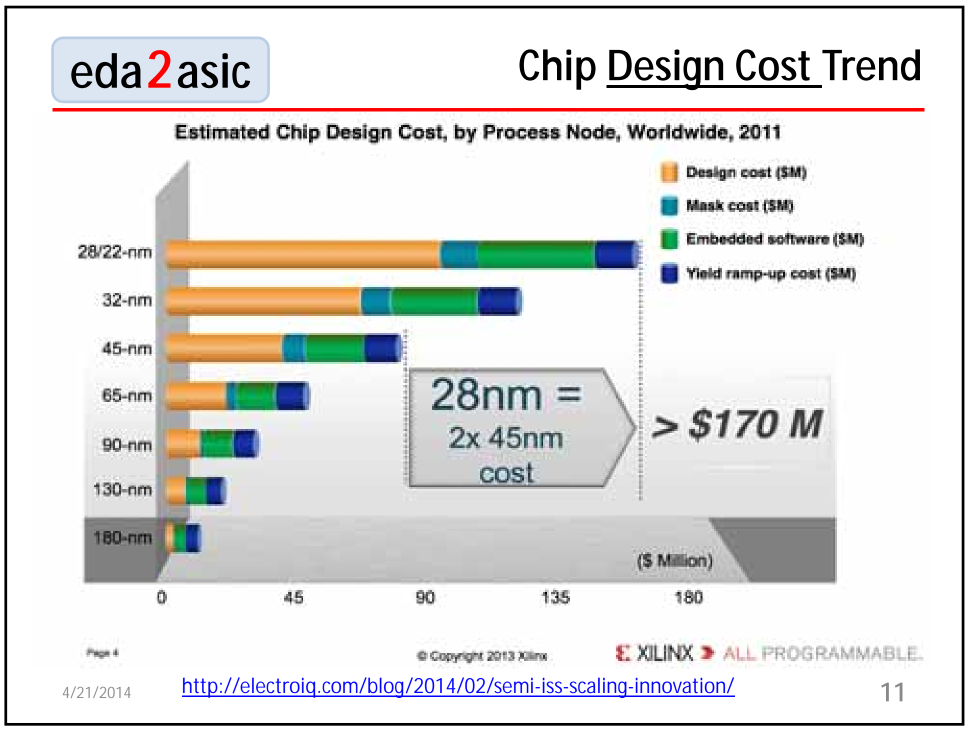
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Chip Design Cost Trend
Estimated Chip Design Cost, by Process Node, Worldwide, 2011
Design cost ($M)
Mask cost ($M)
Embedded software ($M)
Yield ramp-up cost ($M)
28/22-nm
32-nm
45-nm
65-nm
90-nm
130-nm
180-nm
28nm =
2x 45nm
cost
> $170 M
($ Million)
0
45
90
135
180
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http://electroiq.com/blog/2014/02/semi-iss-scaling-innovation/
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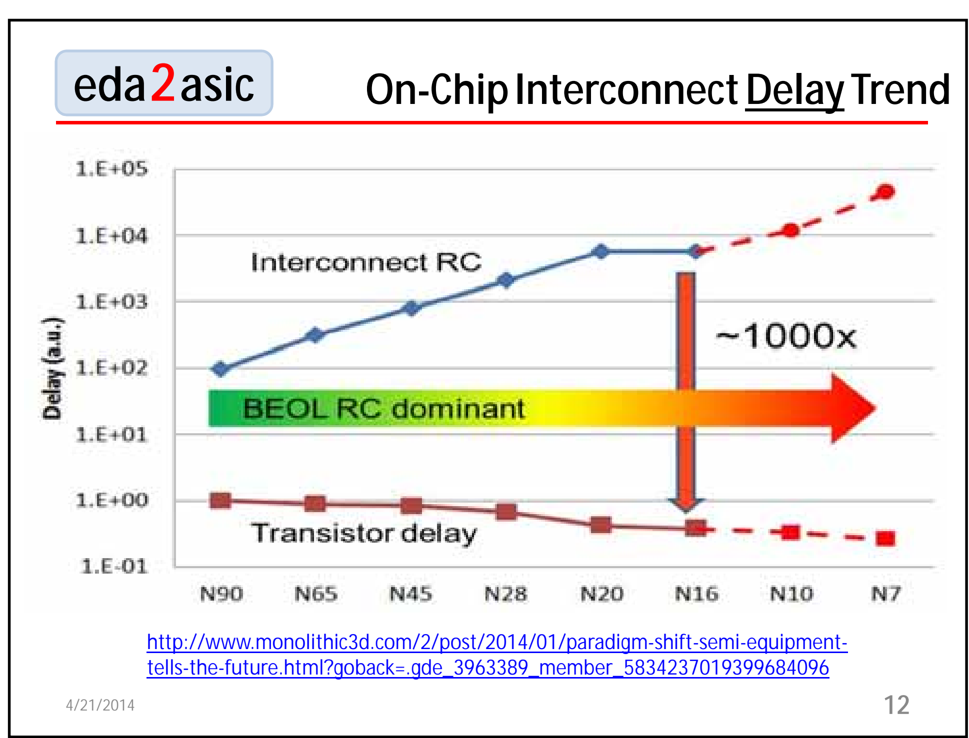
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On-Chip Interconnect Delay Trend
1.E+05
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00
1.E-01
Delay (a.u.)
Interconnect RC
~1000x
BEOL RC dominant
Transistor delay
N90
N65
N45
N28
N20
N16
N10
N7
http://www.monolithic3d.com/2/post/2014/01/paradigm-shift-semi-equipment-tells-the-future.html?goback=.gde_3963389_member_5834237019399684096
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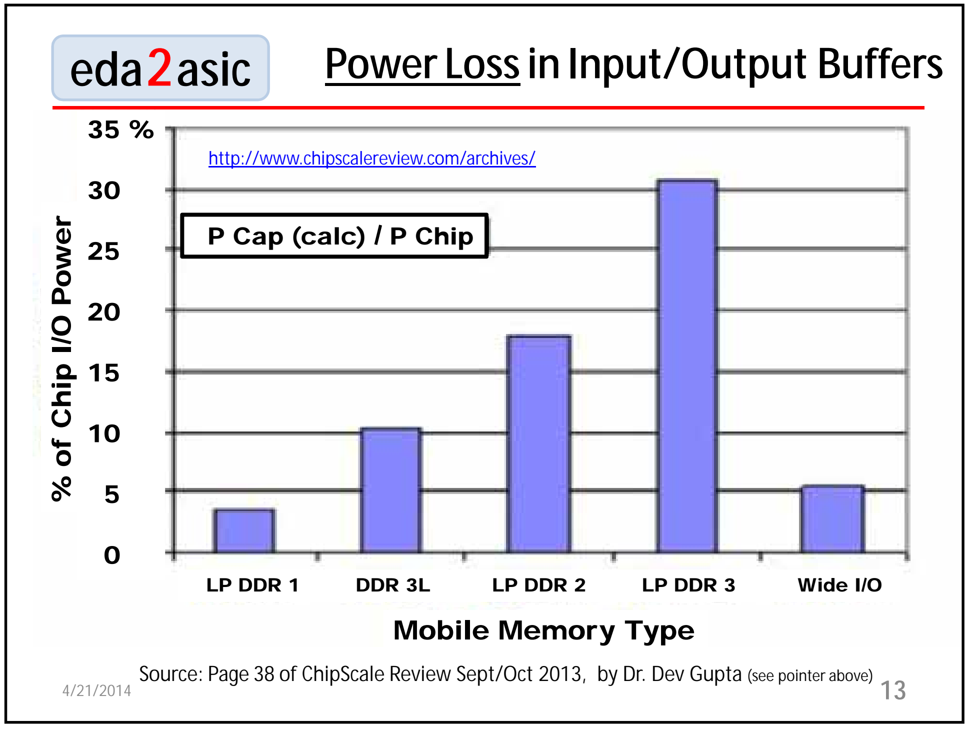
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Power Loss in Input/Output Buffers
http://www.chipscalereview.com/archives/
P Cap (calc) / P Chip
% of Chip I/O Power
35 %
30
25
20
15
10
5
0
LP DDR 1
DDR 3L
LP DDR 2
LP DDR 3
Wide I/O
Mobile Memory Type
Source: Page 38 of ChipScale Review Sept/Oct 2013, by Dr. Dev Gupta (see pointer above)
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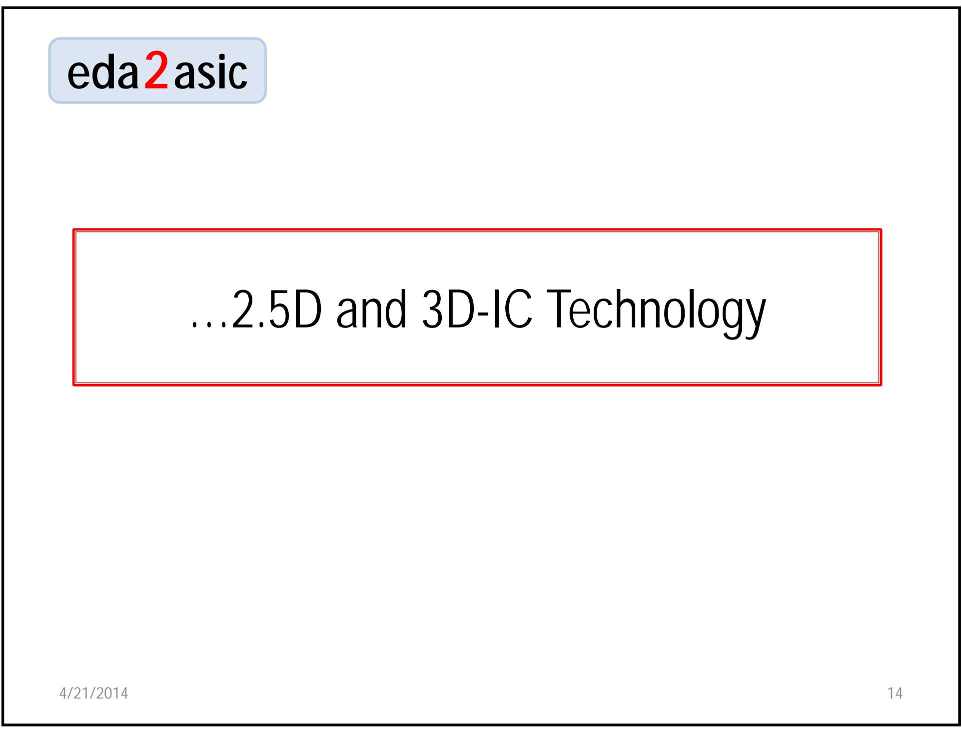
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…2.5D and 3D-IC Technology
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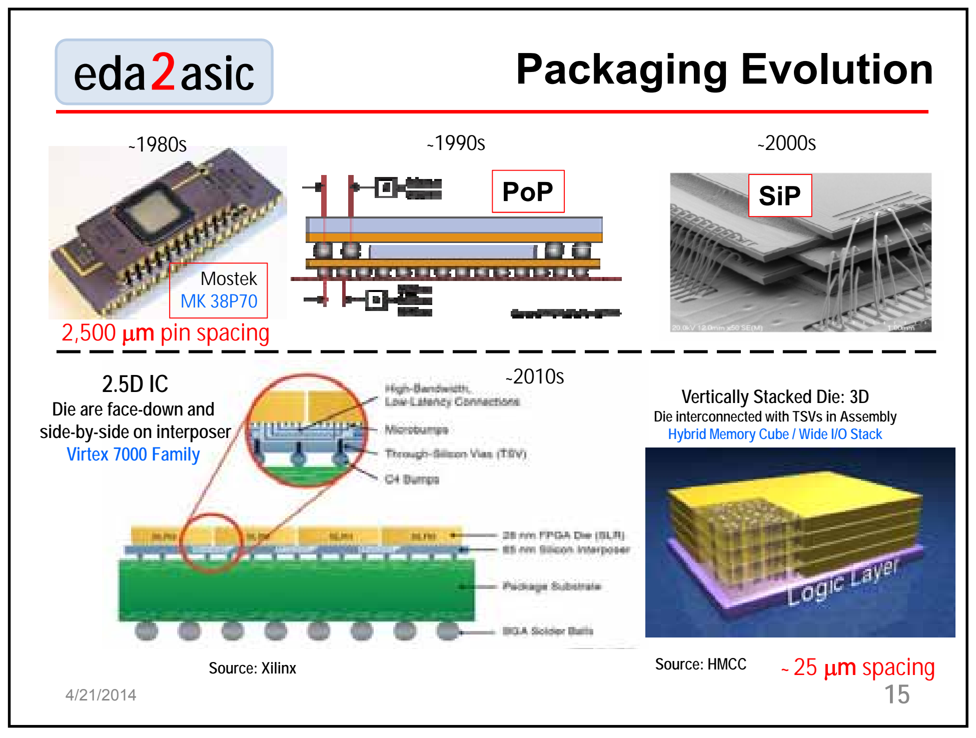
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Packaging Evolution
~1980s
Mostek
MK 38P70
2,500 µm pin spacing
~1990s
PoP
~2000s
SiP
2.5D IC
Die are face-down and
side-by-side on interposer
Virtex 7000 Family
~2010s
Vertically Stacked Die: 3D
Die interconnected with TSVs in Assembly
Hybrid Memory Cube / Wide I/O Stack
Logic Layer
Source: Xilinx
Source: HMCC
~ 25 µm spacing
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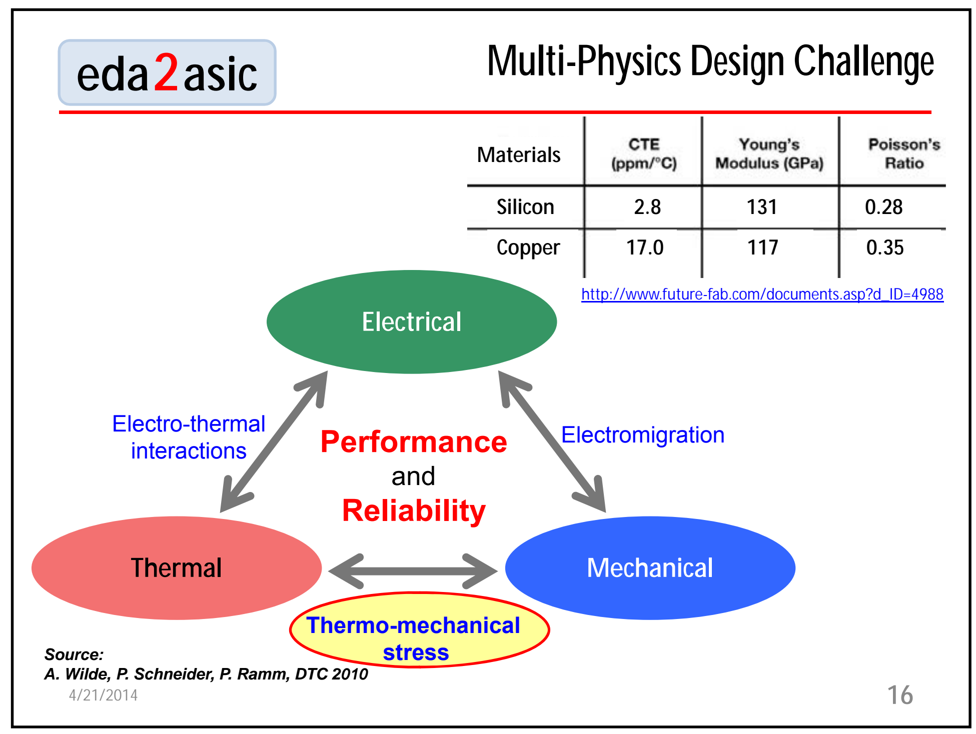
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Multi-Physics Design Challenge

Materials	CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's Ratio
Silicon	2.8	131	0.28
Copper	17.0	117	0.35

http://www.future-fab.com/documents.asp?d_ID=4988
Electrical
Electro-thermal interactions
Performance and Reliability
Electromigration
Thermal
Mechanical
Thermo-mechanical stress
Source:
A. Wilde, P. Schneider, P. Ramm, DTC 2010
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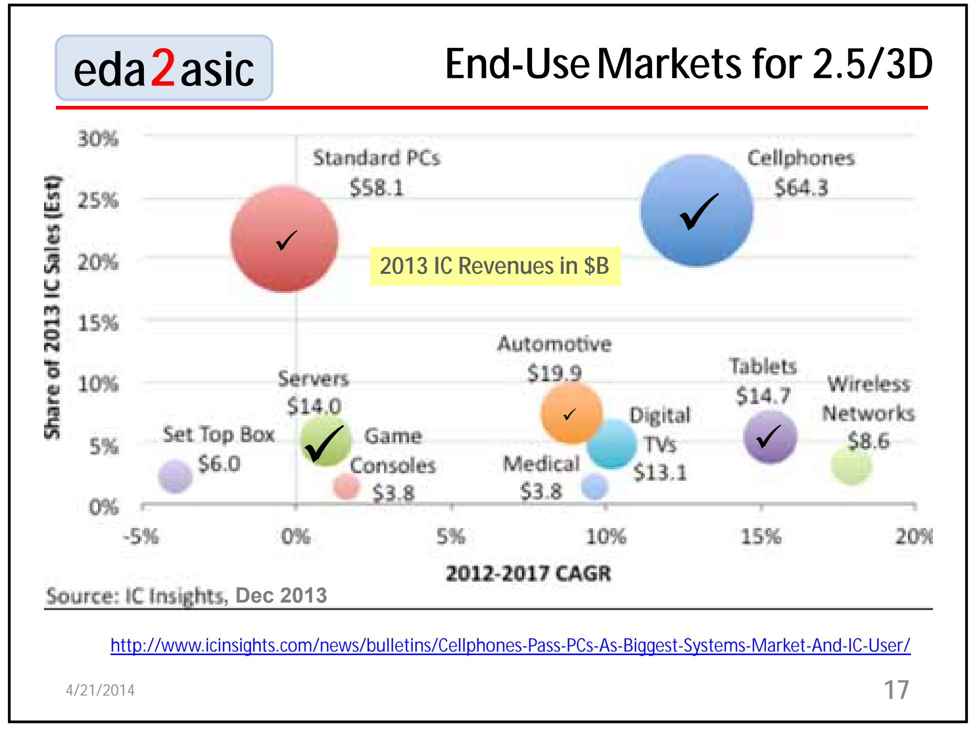

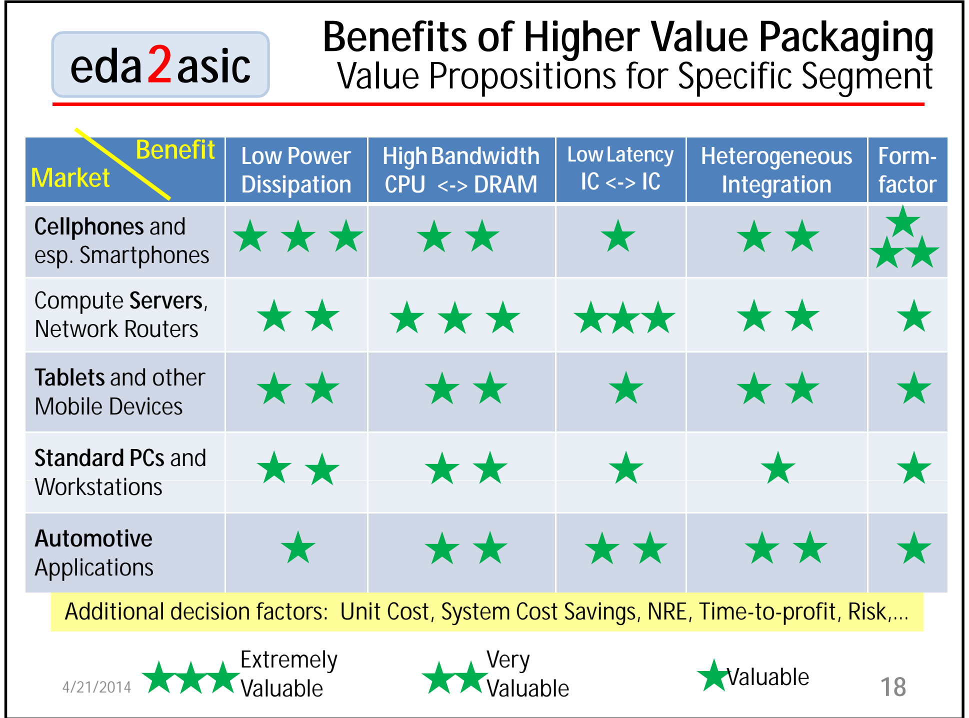

Market \ Benefit	Low Power Dissipation	High Bandwidth CPU <-> DRAM	Low Latency IC <-> IC	Heterogeneous Integration	Form-factor
Cellphones and esp. Smartphones	★★★	★★	★	★★	★★★
Compute **Servers**, Network Routers	★★	★★★	★★★	★★	★
Tablets and other Mobile Devices	★★	★★	★	★★	★
Standard PCs and Workstations	★★	★★	★	★	★
Automotive Applications	★	★★	★★	★★	★

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Comparison of 2.5D and 3D-ICs

Criteria	2.5D	3D	Comments
Unit Cost		Lower	Interposer adds to 2.5D cost
Development cost & time	Lower		Fewer placement considerations
Bandwidth		Higher	Many short, vertical connections
Latency		Lower	- " -
Power Dissipation		Lower	Shorter connections → Lower RC loads
Form-Factor		Smaller	3D needs less board-space
Cooling Challenges	Fewer		Every die directly accessible
Design Flexibility	Greater		Interposer gives additional freedom
Testability	Easier		Every die easier accessible
Current Proto Capabilities	Better	*	*: 3D memories are ready NOW
Current Production Capacity	Check !	Check !	Production supply chain emerging
Overall Risk, currently	Lower		2.5D needs fewer new capabilities
Need for standards	Lower		Vertical stacking: More coordination

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2.5D and 3D solutions can be combined in one IC package ! (5.5D ??)

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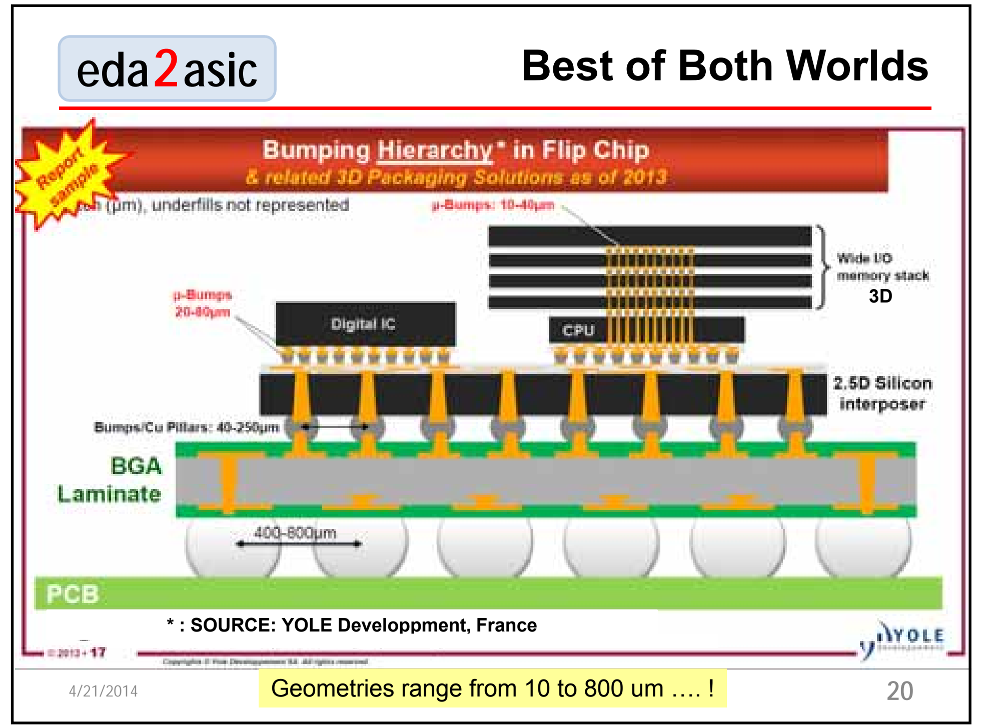
Best of Both Worlds



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Geometries range from 10 to 800 um …. !

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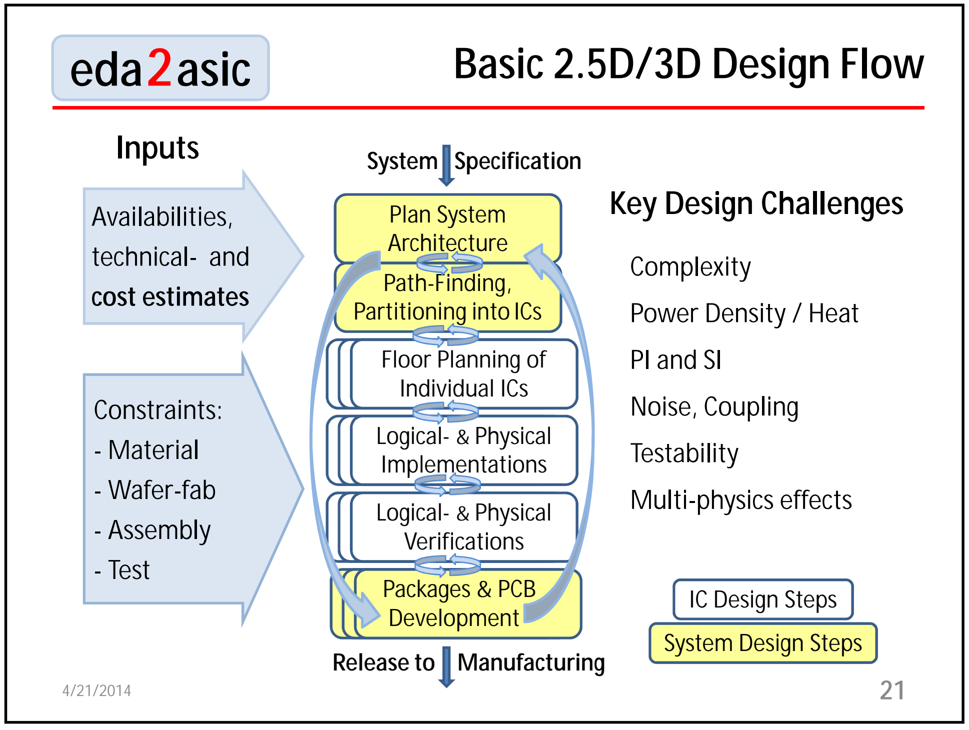
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Basic 2.5D/3D Design Flow
Inputs
Availabilities, technical- and cost estimates
Constraints:
- Material
- Wafer-fab
- Assembly
- Test
System Specification
Plan System Architecture
Path-Finding, Partitioning into ICs
Floor Planning of Individual ICs
Logical- & Physical Implementations
Logical- & Physical Verifications
Packages & PCB Development
Release to Manufacturing
Key Design Challenges
Complexity
Power Density / Heat
PI and SI
Noise, Coupling
Testability
Multi-physics effects
IC Design Steps
System Design Steps
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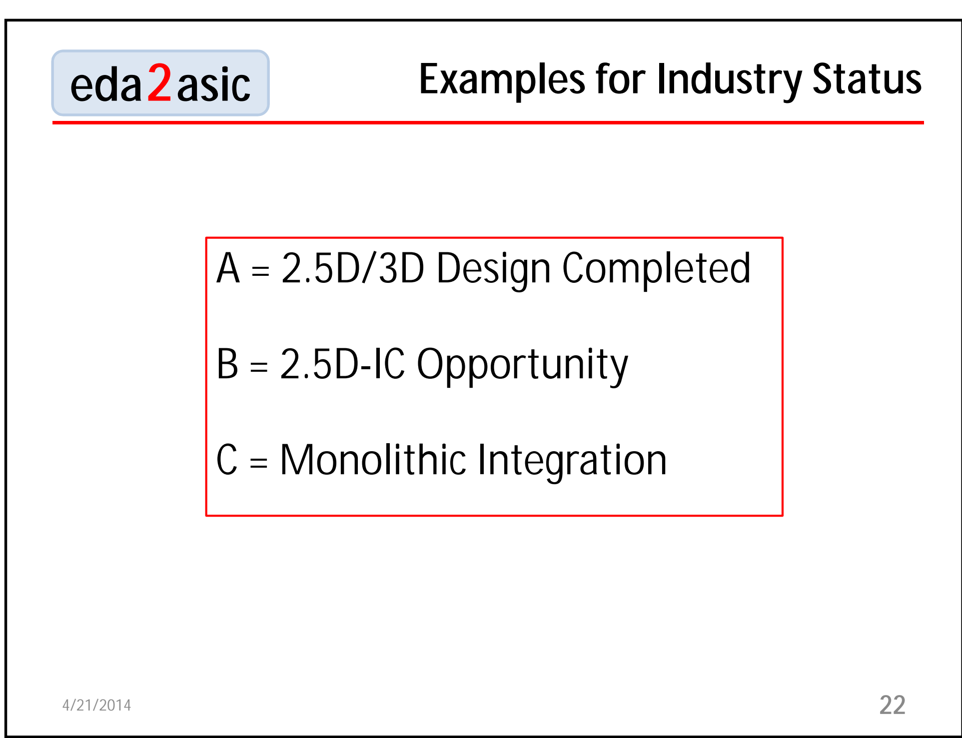
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Examples for Industry Status
A = 2.5D/3D Design Completed
B = 2.5D-IC Opportunity
C = Monolithic Integration
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A: Xilinx Saves Significant Power
Virtex 2000T – 2 million logic cells
4-layer metal Si interposer with TSV
4 FPGA sub-die in package
>10,000 inter-die connections
In production since 2011
Power of these 4 FPGAs: 18 Watts
Versus 120 Watts if individually packaged
Modularity
Much better yields versus one large die
Speed- and power binning possible
Courtesy: Xilinx
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A: Xilinx Integrates Digital and Analog
in a 2.5D-IC
Virtex-7 H580T Heterogeneous FPGA announced May 30, 2012
Two FPGA slices and up to sixteen 28 Gbps and seventy-two 13.1 Gbps transceivers
Single-package solutions for addressing key Nx100G and 400G line card applications
http://www.eetimes.com/electronics-products/electronic-product-reviews/fpga-pld-products/4374071/Xilinx-ships-the-world-s-first-heterogeneous-3D-FPGA?cid=NL_EETimesProducts
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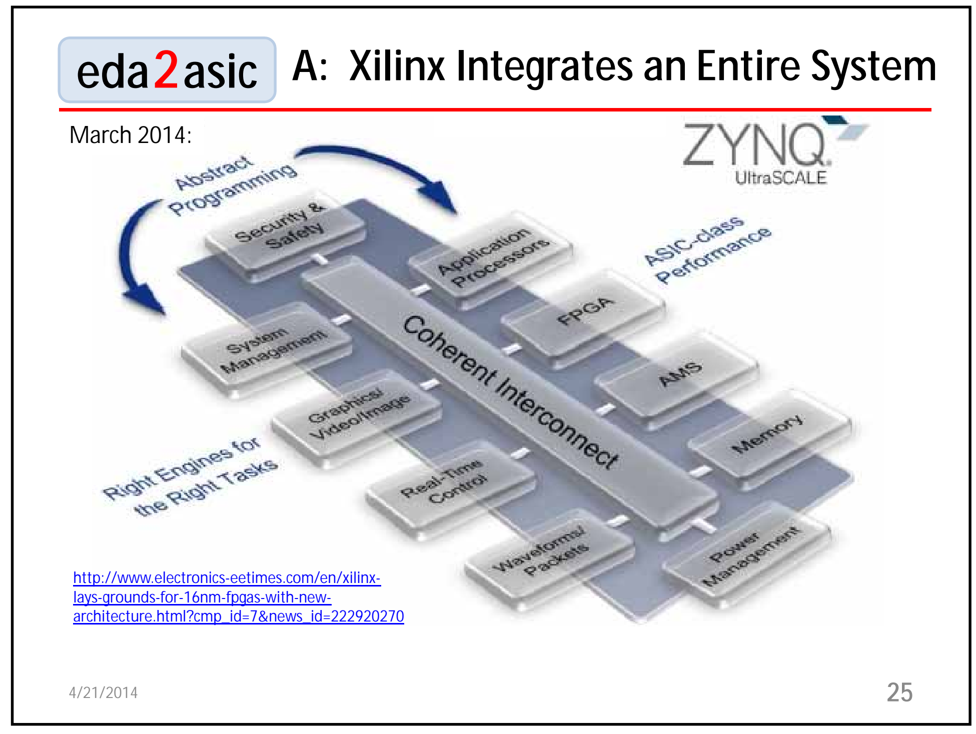
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A: Xilinx Integrates an Entire System
March 2014:
ZYNQ UltraSCALE
Abstract Programming
Security & Safety
Application Processors
ASIC-class Performance
System Management
FPGA
Coherent Interconnect
AMS
Graphics/ Video/Image
Memory
Right Engines for the Right Tasks
Real-Time Control
Waveforms/ Packets
Power Management
http://www.electronics-eetimes.com/en/xilinx-lays-grounds-for-16nm-fpgas-with-new-architecture.html?cmp_id=7&news_id=222920270
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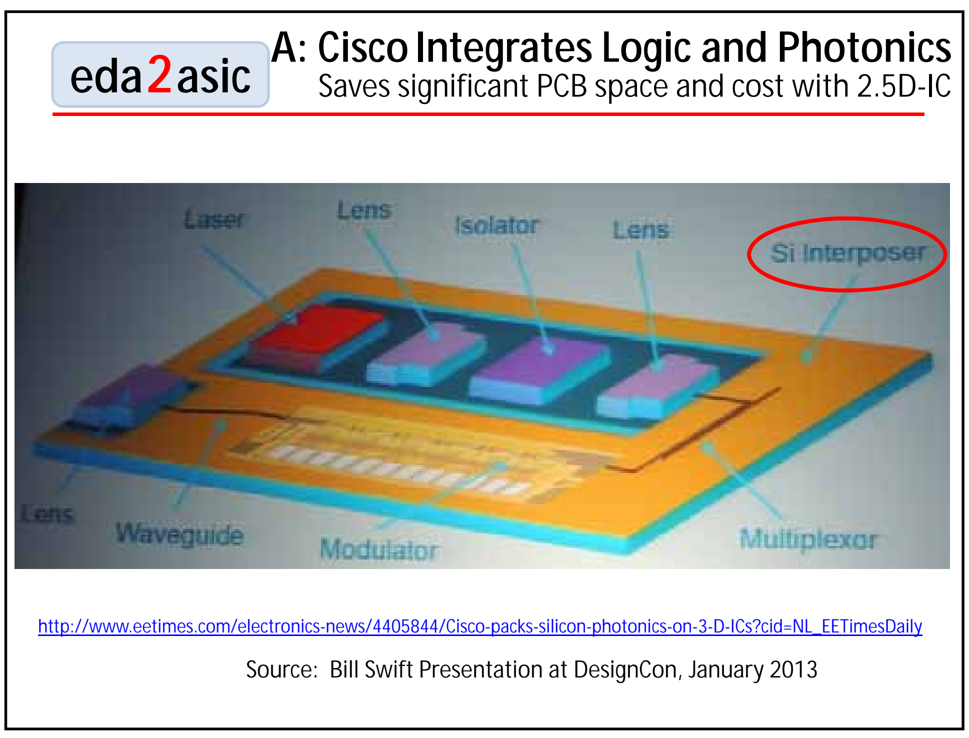
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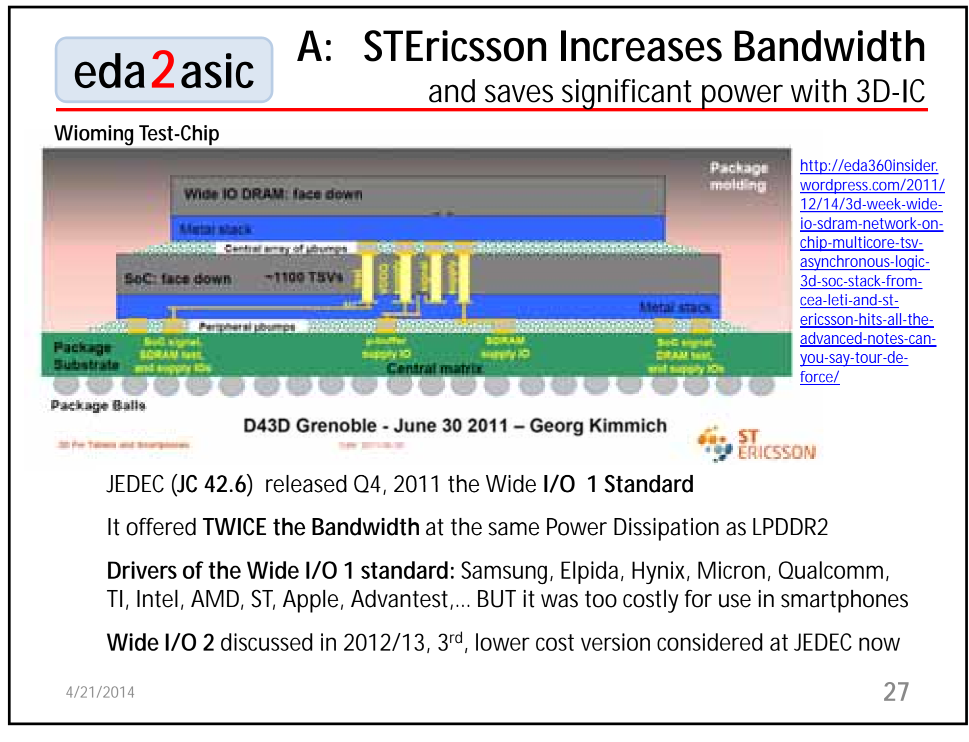
A: Cisco Integrates Logic and Photonics
Saves significant PCB space and cost with 2.5D-IC
Laser
Lens
Isolator
Lens
Si Interposer
Lens
Waveguide
Modulator
Multiplexor
http://www.eetimes.com/electronics-news/4405844/Cisco-packs-silicon-photonics-on-3-D-ICs?cid=NL_EETimesDaily
Source: Bill Swift Presentation at DesignCon, January 2013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A: STEricsson Increases Bandwidth
and saves significant power with 3D-IC
Wioming Test-Chip
Package molding
Wide IO DRAM: face down
Metal stack
Central array of µbumps
SoC: face down
~1100 TSVs
Metal stack
Peripheral µbumps
Package Substrate
SoC signal, SDRAM test, and supply IOs
Central matrix
SDRAM supply IO
Package Balls
http://eda360insider.wordpress.com/2011/12/14/3d-week-wide-io-sdram-network-on-chip-multicore-tsv-asynchronous-logic-3d-soc-stack-from-cea-leti-and-st-ericsson-hits-all-the-advanced-notes-can-you-say-tour-de-force/
D43D Grenoble - June 30 2011 – Georg Kimmich
ST ERICSSON
JEDEC (JC 42.6) released Q4, 2011 the Wide I/O 1 Standard
It offered TWICE the Bandwidth at the same Power Dissipation as LPDDR2
Drivers of the Wide I/O 1 standard: Samsung, Elpida, Hynix, Micron, Qualcomm, TI, Intel, AMD, ST, Apple, Advantest,… BUT it was too costly for use in smartphones
Wide I/O 2 discussed in 2012/13, 3rd, lower cost version considered at JEDEC now
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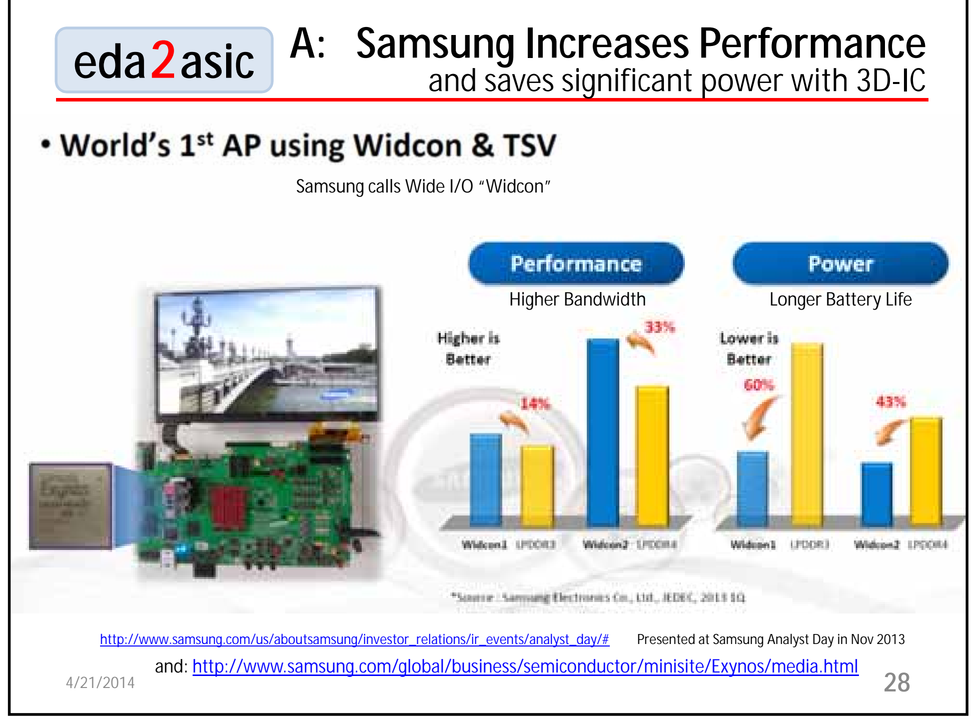
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A: Samsung Increases Performance
and saves significant power with 3D-IC
• World's 1st AP using Widcon & TSV
Samsung calls Wide I/O "Widcon"
Performance
Higher Bandwidth
Power
Longer Battery Life
Higher is Better
14%
33%
Lower is Better
60%
43%
Widcon1
LPDDR3
Widcon2
LPDDR4
http://www.samsung.com/us/aboutsamsung/investor_relations/ir_events/analyst_day/#
Presented at Samsung Analyst Day in Nov 2013
and: http://www.samsung.com/global/business/semiconductor/minisite/Exynos/media.html
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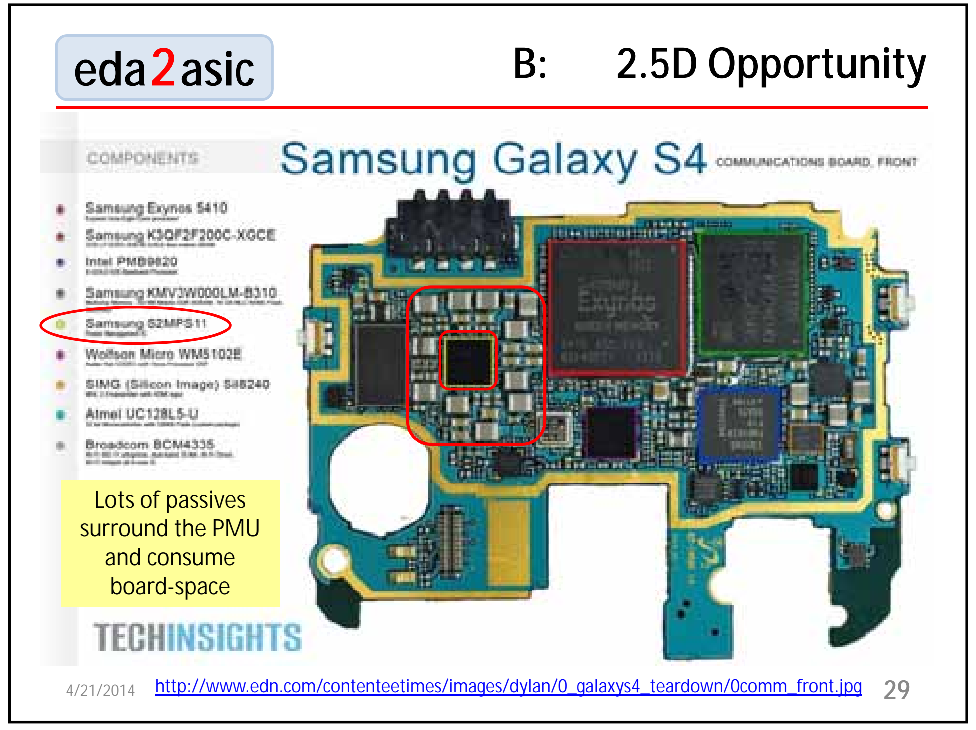
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B: 2.5D Opportunity
COMPONENTS
Samsung Galaxy S4 COMMUNICATIONS BOARD, FRONT
Samsung Exynos 5410
Samsung K3QF2F200C-XGCE
Intel PMB9820
Samsung KMV3W000LM-B310
Samsung S2MPS11
Wolfson Micro WM5102E
SIMG (Silicon Image) Sil8240
Atmel UC128L5-U
Broadcom BCM4335
Lots of passives surround the PMU and consume board-space
TECHINSIGHTS
4/21/2014
http://www.edn.com/contenteetimes/images/dylan/0_galaxys4_teardown/0comm_front.jpg
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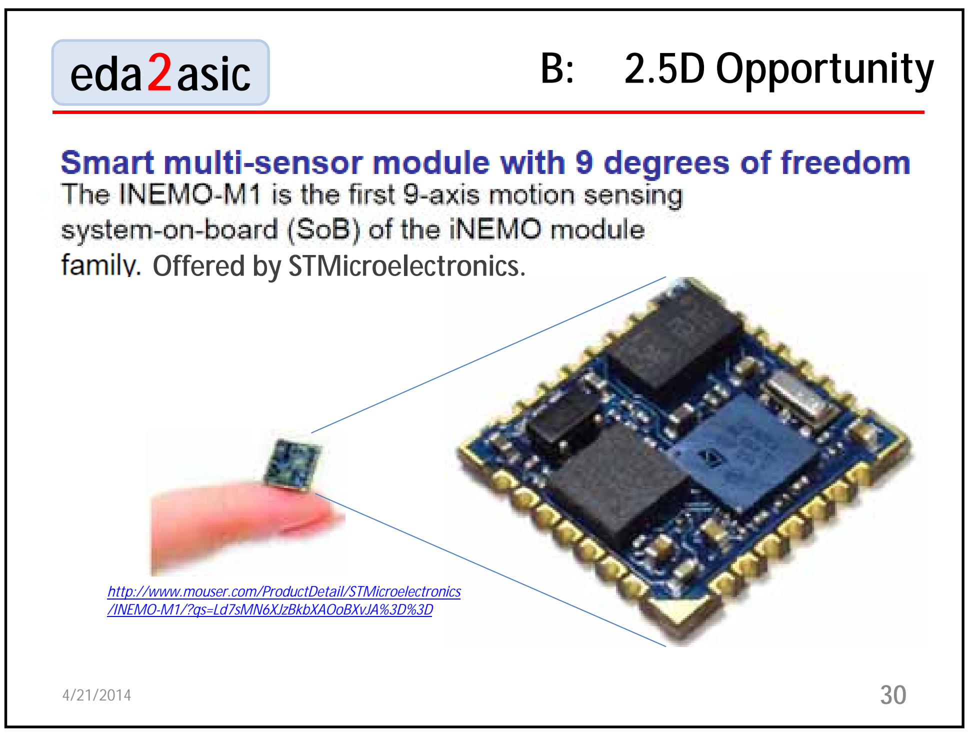
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B: 2.5D Opportunity
Smart multi-sensor module with 9 degrees of freedom
The INEMO-M1 is the first 9-axis motion sensing system-on-board (SoB) of the iNEMO module family. Offered by STMicroelectronics.
http://www.mouser.com/ProductDetail/STMicroelectronics/INEMO-M1/?qs=Ld7sMN6XJzBkbXAOoBXvJA%3D%3D
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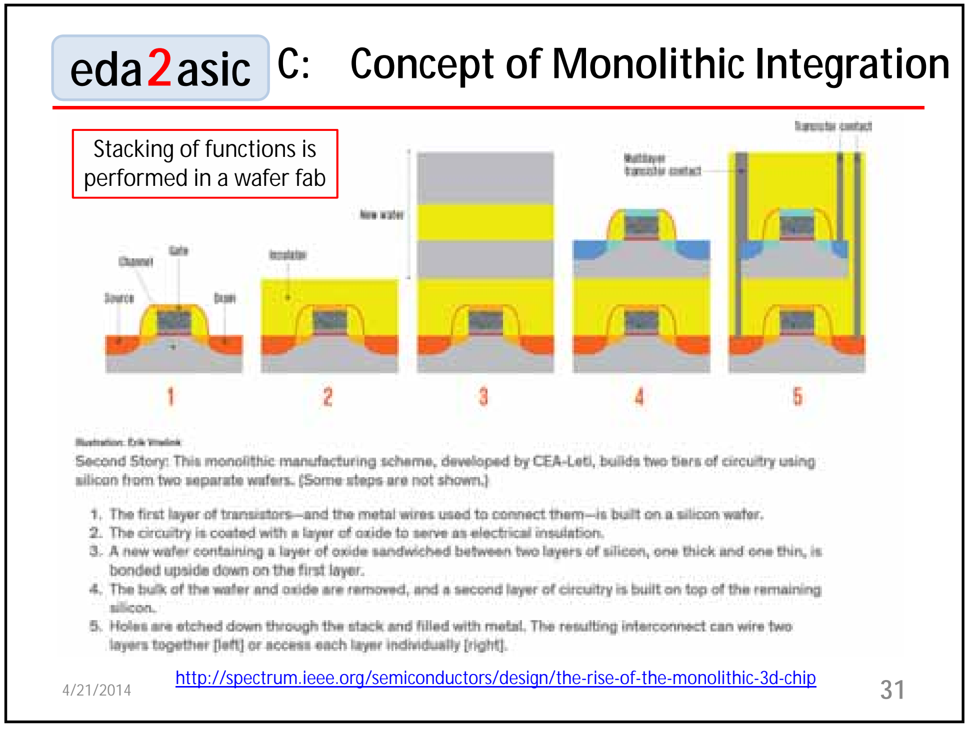
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C: Concept of Monolithic Integration
Stacking of functions is performed in a wafer fab
1
2
3
4
5
Second Story: This monolithic manufacturing scheme, developed by CEA-Leti, builds two tiers of circuitry using silicon from two separate wafers. (Some steps are not shown.)
1. The first layer of transistors—and the metal wires used to connect them—is built on a silicon wafer.
2. The circuitry is coated with a layer of oxide to serve as electrical insulation.
3. A new wafer containing a layer of oxide sandwiched between two layers of silicon, one thick and one thin, is bonded upside down on the first layer.
4. The bulk of the wafer and oxide are removed, and a second layer of circuitry is built on top of the remaining silicon.
5. Holes are etched down through the stack and filled with metal. The resulting interconnect can wire two layers together [left] or access each layer individually [right].
http://spectrum.ieee.org/semiconductors/design/the-rise-of-the-monolithic-3d-chip
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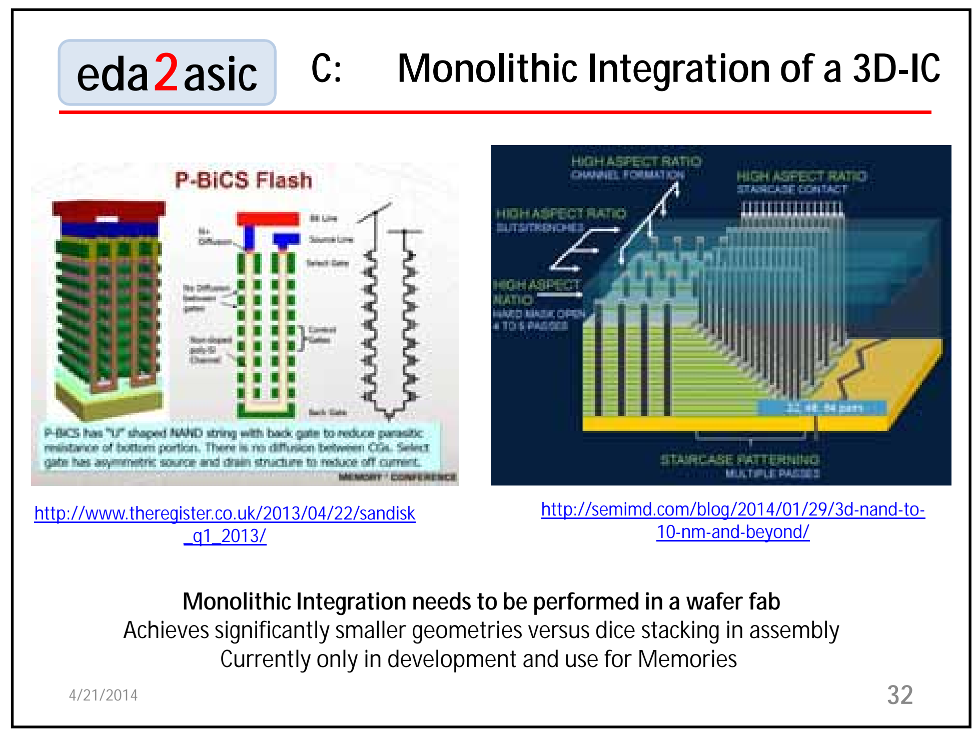
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C: Monolithic Integration of a 3D-IC
P-BiCS Flash
P-BiCS has "U" shaped NAND string with back gate to reduce parasitic resistance of bottom portion. There is no diffusion between CGs. Select gate has asymmetric source and drain structure to reduce off current.
HIGH ASPECT RATIO CHANNEL FORMATION
HIGH ASPECT RATIO STAIRCASE CONTACT
HIGH ASPECT RATIO
STAIRCASE PATTERNING
MULTIPLE PASSES
http://www.theregister.co.uk/2013/04/22/sandisk_q1_2013/
http://semimd.com/blog/2014/01/29/3d-nand-to-10-nm-and-beyond/
Monolithic Integration needs to be performed in a wafer fab
Achieves significantly smaller geometries versus dice stacking in assembly
Currently only in development and use for Memories
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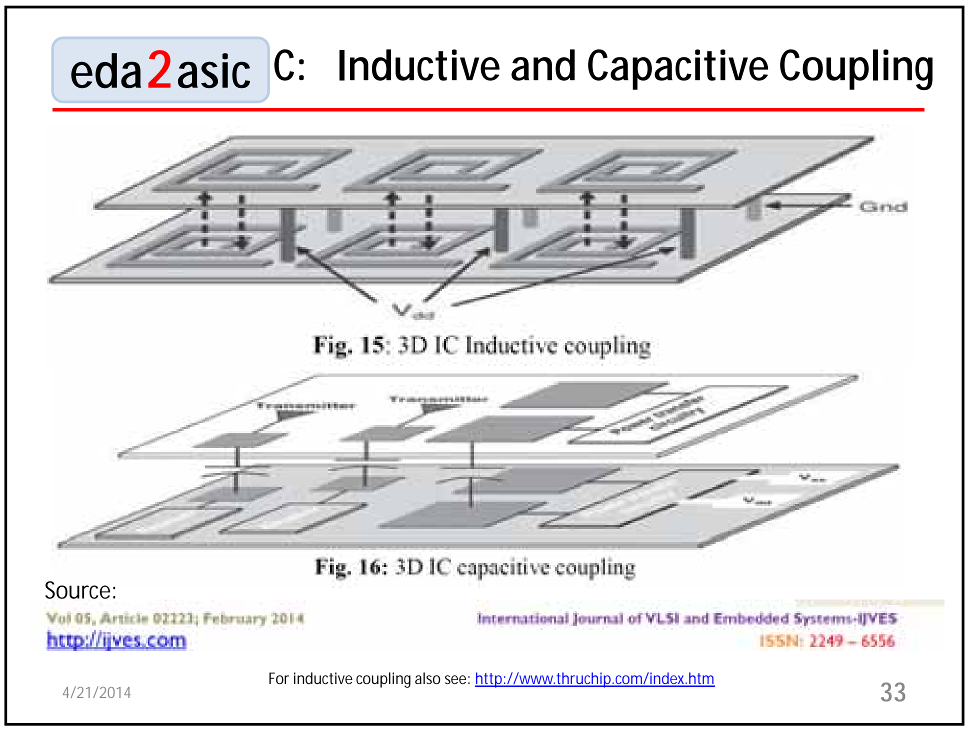
eda2asic C: Inductive and Capacitive Coupling
Gnd
Vdd
Fig. 15: 3D IC Inductive coupling
Transmitter
Transmitter
Fig. 16: 3D IC capacitive coupling
Source:
Vol 05, Article 02223; February 2014
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556
For inductive coupling also see: http://www.thruchip.com/index.htm
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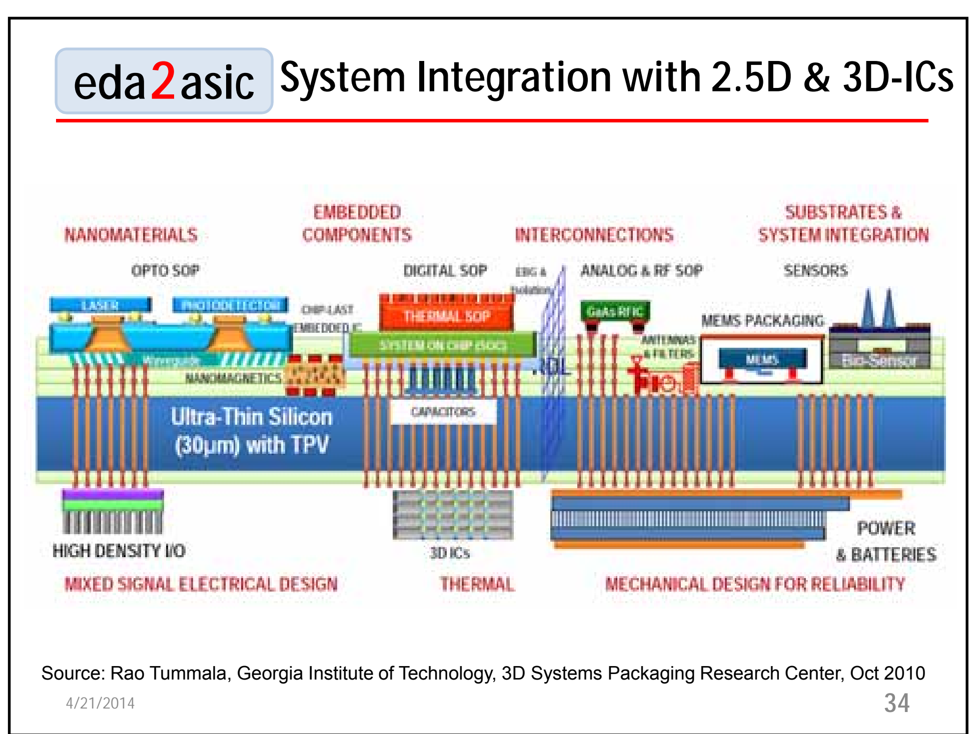
eda2asic System Integration with 2.5D & 3D-ICs
NANOMATERIALS
EMBEDDED COMPONENTS
INTERCONNECTIONS
SUBSTRATES & SYSTEM INTEGRATION
OPTO SOP
DIGITAL SOP
ANALOG & RF SOP
SENSORS
LASER
PHOTODETECTOR
CHIP-LAST EMBEDDED IC
THERMAL SOP
SYSTEM ON CHIP (SOC)
GaAs RFIC
MEMS PACKAGING
ANTENNAS & FILTERS
MEMS
Bio-Sensor
Waveguide
NANOMAGNETICS
Ultra-Thin Silicon (30µm) with TPV
CAPACITORS
HIGH DENSITY I/O
3D ICs
POWER & BATTERIES
MIXED SIGNAL ELECTRICAL DESIGN
THERMAL
MECHANICAL DESIGN FOR RELIABILITY
Source: Rao Tummala, Georgia Institute of Technology, 3D Systems Packaging Research Center, Oct 2010
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Business Considerations

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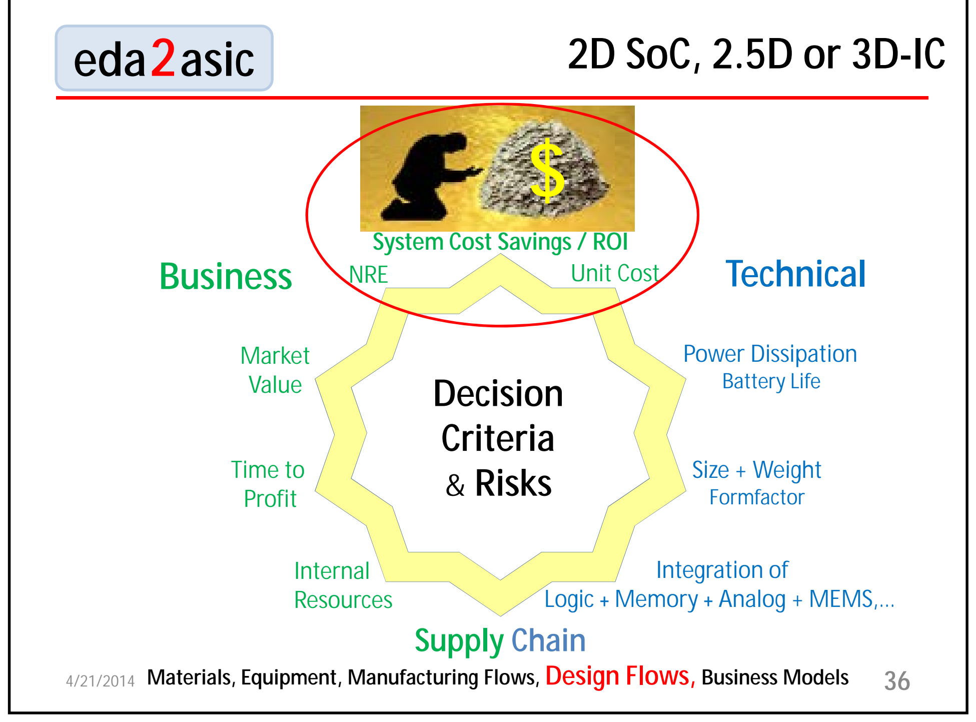

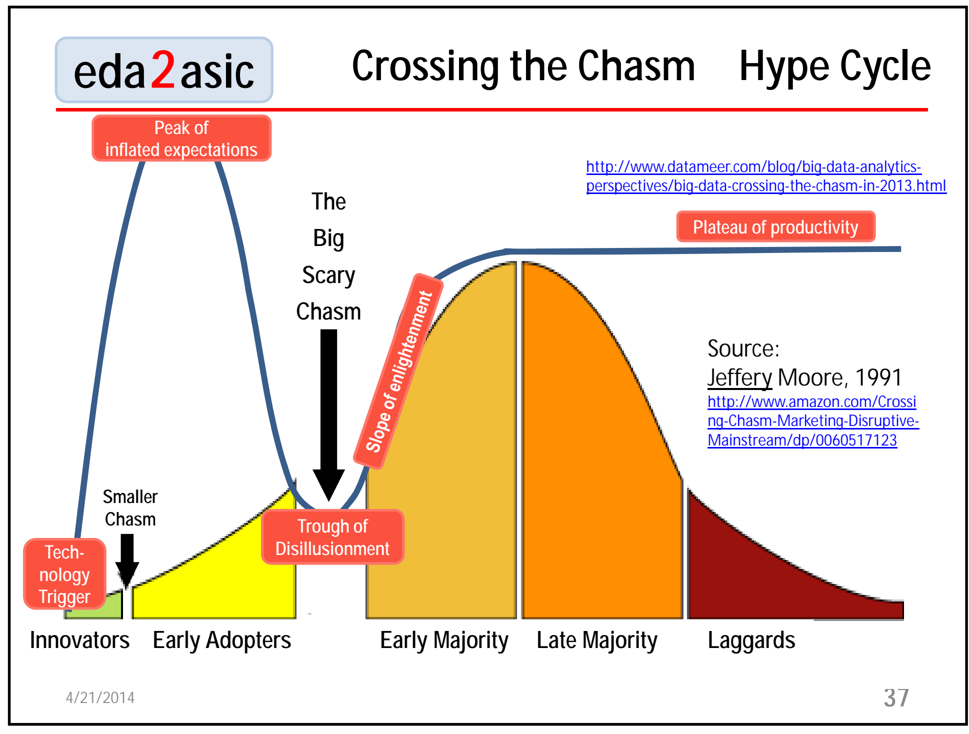
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Crossing the Chasm
Hype Cycle
Peak of
inflated expectations
http://www.datameer.com/blog/big-data-analytics-perspectives/big-data-crossing-the-chasm-in-2013.html
The
Big
Scary
Chasm
Plateau of productivity
Slope of enlightenment
Source:
Jeffery Moore, 1991
http://www.amazon.com/Crossing-Chasm-Marketing-Disruptive-Mainstream/dp/0060517123
Smaller
Chasm
Tech-
nology
Trigger
Trough of
Disillusionment
Innovators
Early Adopters
Early Majority
Late Majority
Laggards
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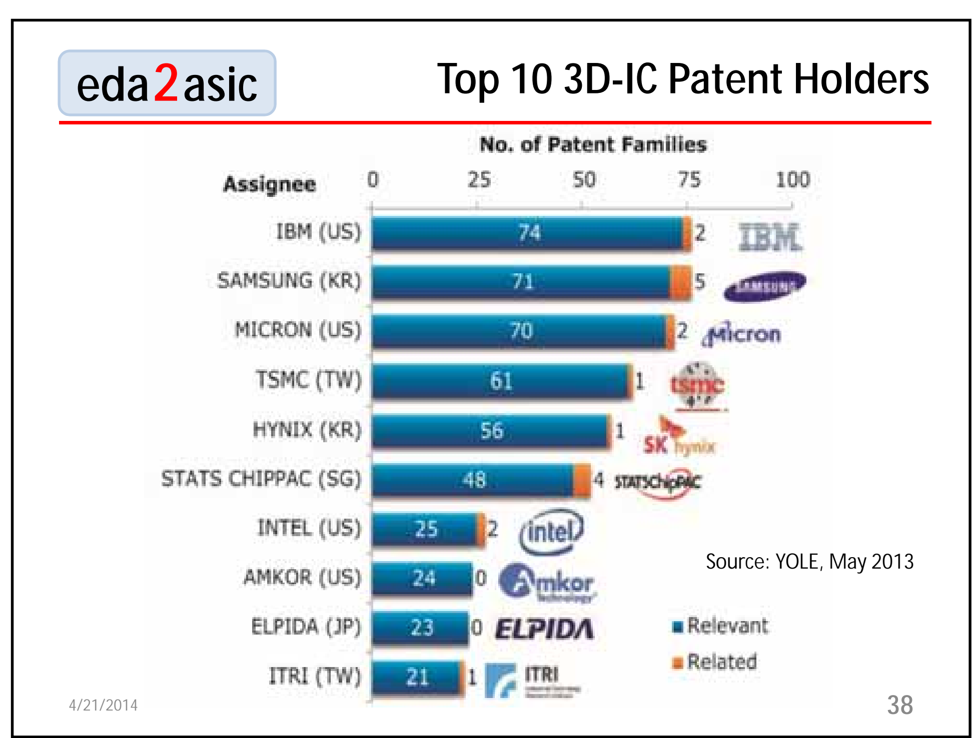
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Top 10 3D-IC Patent Holders
No. of Patent Families
Assignee
0
25
50
75
100
IBM (US)
74
2
SAMSUNG (KR)
71
5
MICRON (US)
70
2
TSMC (TW)
61
1
HYNIX (KR)
56
1
STATS CHIPPAC (SG)
48
4
INTEL (US)
25
2
AMKOR (US)
24
0
ELPIDA (JP)
23
0
ITRI (TW)
21
1
Source: YOLE, May 2013
Relevant
Related
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SUMMARY

- Major challenges IF we only follow Moore's Law
  – Complexity limit, Latency, Bandwidth, Flexibility, Cost, Risk,...
- 2.5D/3D-ICs are gaining significant momentum
  – 450 and EUV are delayed...; $\leq$20nm → high NRE, high wafer cost
  \+ Power Density, Testability, Supply Chain, Cost,... being addressed
- 2D Chips are the Building Blocks for 2.5D/3D-ICs
  \+ Die-level IP-reuse will help reducing NREs and time-to-profit

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Thank You !!!

Q & A

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