Inkjet Printing for Advanced Semiconductor Packaging:
*Pillars and Through-silicon Vias (TSVs)*

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“Smaller, faster, lighter, cheaper…”

CMOS scaling drives the need for denser, higher performance, and higher reliability packaging
The Future of BEOL Packaging

Next Generation Packaging Approaches

FUNDAMENTAL PACKAGE PERFORMANCE METRICS:
- Pin Density
- Pin Count
- Transistor Density

Novel approaches are needed to meet demands of new applications that require higher density and thinner packages.

Conventional Post Processes

Passivation / Under Bump Metallization / Cu Electroplating / Solder Reflow

Complex Process
Prone to Intermetallics
Pb-free solders still problematic
Conventional TSV Processes

Liner Deposition / Cu Electroplating / CMP / Wafer Thinning

Pattern-sensitive
Expensive
Keyholes and Stress Concerns
Difficult Scaling

Inkjet-Printed Electronics

Self-aligned Inverters
Metal Nanoparticle Inks
Highly-controlled Line Morphology
Research-Grade Inkjet Printing

- MicroFab Single Nozzle
- Fuji Dimatix 16 Nozzle
- Fuji Dimatix 128 Nozzles

Toward Commercial/Industrial Scales

Inkjet Printing for Packaging Applications

- Additive
- Adjustable-on-the-fly
- Vacuum-independent
- Mask-independent
- Scalable
- Diverse material set
- New substrate technologies

- Inkjet critical dimension smaller than projected packaging scaling trends

Inkjet printing positioned as a viable long-term solution for packaging materials deposition, but materials and processes still require development
Nanoparticles as Interconnect Materials

Nanoparticles inks offer compatible processing temperatures, improved material and substrate selection, and reduced cost for interconnects


The Challenges:

How can we inkjet-print metal nanoparticle inks in three dimensions?

How does sintering alter the material properties of these structures?

How do these structures compare to conventional materials/processes?
Using a drop-wise printing on heated substrates, we are able to fabricate free-standing pillars. Drop frequency and substrate temperature are primary controls.
High Aspect Ratio Pillars

Increasing Substrate Temperature

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Experimental Details:
- **Ink**: Harima NPG-J gold nanoparticle ink
- **Substrate**: Evaporated Cr/Au pads on SiO$_2$
- **Total drops per pillar**: 50

Images: SEM, all scale bars are 100 µm

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**High Aspect Ratio Pillars**

\[ AR = \frac{\text{sintered height}}{\text{sintered diameter}} \]

Aspect ratio* (AR) of ~6:1 achieved with only 50 drops (h = 233 µm, d = 40 µm)

Adjusting substrate temperature and jetting frequency allows us to achieve pillars with very high-aspect ratios

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*Height and diameter extracted from SEM images post-sinter
Material Properties of Importance

In these relatively large nanoparticle-based structures, how does sintering proceed/determine the ultimate material properties?

Pillar Resistance Model

Thin-film nanoparticle inks commonly use resistance as metric to indicate degree of sintering.

How do we do the same for our pillars?

Resistance Model:
1. Pillar is perfect cylinder
   \[ R_{\text{pillar}} = \frac{\rho_{\text{pillar}} h}{\pi r^2} \]
2. After taper regime:
   \[ h \propto \text{drops} \]
   \[ R_{\text{pillar}} \propto h \Rightarrow R_{\text{pillar}} \propto \text{drops} \]
3. Resistivity a function of sinter condition:
   \[ \rho_{\text{pillar}} \rightarrow \rho_{\text{pillar}}(t, T) \]

When sintering complete, resistivity should be constant as drop number increases and resistance should be proportional to drop count.
Pillar Resistance Model

Thin-film nanoparticle inks commonly use resistance as metric to indicate degree of sintering.

How do we do the same for our pillars?

Resistivity of pillar:

1. Pillar is perfect cylinder
   \[ R_{pillar} = \frac{\rho_{pillar} h}{\pi r^2} \]

2. After taper regime:
   \[ h \propto \text{drops} \]
   \[ R_{pillar} \propto h \rightarrow R_{pillar} \propto \text{drops} \]

3. Resistivity a function of sinter condition:
   \[ \rho_{pillar} \rightarrow \rho_{pillar}(t,T) \]

When sintering complete, resistivity should be constant as drop number increases and resistance should be proportional to drop count and we can extract effective resistivity value.

Experimental Details:
- **Ink:** Harima NPG-J gold
- **Substrate temp:** 100 °C
- **Time between drops:** 4 sec
- **Total drops per pillar:** 30

<table>
<thead>
<tr>
<th>Material</th>
<th>Conductivity (S/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Gold</td>
<td>4.54±05</td>
</tr>
<tr>
<td>Harima Gold (thin film)</td>
<td>1.43±05</td>
</tr>
<tr>
<td>Tin Silver Copper</td>
<td>7.69±04</td>
</tr>
<tr>
<td>Harima Gold (pillars)</td>
<td>7.58±04</td>
</tr>
<tr>
<td>Lead Tin Eutectic</td>
<td>6.94±04</td>
</tr>
<tr>
<td>Gold Tin Eutectic</td>
<td>6.10±04</td>
</tr>
</tbody>
</table>

A 140°C sinter condition and short sinter times resulted in immeasurably high resistance.

Pillar Resistance as a Function of Sintering

Dramatically reducing resistance as sinter temperature increases.

Exponentially reducing resistance as sinter time increases.

Highest extracted conductivity outperforms conventional eutectic solder but still requires higher thermal treatment.

6/12/2014
Nanoindentation

Solder bump loading capacity a critical parameter to extract

Extracted elasticity with nanoindentation at LBNL

\[ E_r \propto S \propto \frac{d}{dd}L(d) \]

Load-Displacement Curves

\[ E_r \approx 29 \text{ GPa} \]

*Sample curves sintered at 200 °C for 75 min and loaded at 200 µN/s

Nanoindentation Test Schematic

1. Contact sample (top of pillar)
2. Apply load and measure force and displacement
3. Hold at maximum load
4. Unload

Nanoindentation

Test Schematic

Load (N)

depth (m)

Load (N)

stress (Pa)

strain

Pillar Elasticity as a Function of Sintering

Dramatic increase in stiffness with higher sinter temperatures

Little to no stiffness improvement at low sinter temperatures

Material | Elasticity (GPa)
---|---
Bulk Gold | 74.4
Lead Tin Eutectic | 31.5
Harima Gold (pillars) | 28.6

Experimental Details:
Ink: Harima NPG-J gold
Substrate temp: 100 °C
Time between drops: 4 sec
Total drops per pillar: 30

Highest extracted modulus (29 GPa) comparable to conventional eutectic solders
Pillar Shear Strength

- Printed arrays of pillars (nominally 20 pillars per array)
- Oven-sintered each array for one hour
- Performed shear testing with Dage 4000 at 100 µm/s shear rate
- SEM images used to characterize failure mechanisms

Observed Failure Mechanisms:
- Interfacial failure
- Sloped Ductile failure
- Flat Ductile failure

Shear Strength and Failure Rates

Key Results:
- Interfacial failures dominant at low sinter temperatures
- Ductile shearing dominant at higher sinter temperatures and two failure modes observed:
  - ‘Sloped’ at lower temperatures
  - ‘Flat’ at higher temperatures
- Absolute shear strength competitive with lead-tin eutectics and bulk gold at 200 C and 300 C, respectively
Pillar Compaction

Using confocal 3D microscope, measured pillar height and width as a function of sintering conditions

**Key Results:**
- Highly uniform printing (fig 1) with height and width tolerances within 1.5 μm each
- Pillars exhibit both lateral AND vertical compaction
- Extracted volume compaction of 53% in highest sintering condition
- Compaction primarily driven by substrate temperature as opposed to sinter time

Properties ⇔ Structure/Composition

- All observed dynamic properties must correlate to change in structure or composition of printed features
- During sintering, de-encapsulation and outdiffusion of nanoparticle encapsulant will cause shifts in electrical and mechanical response of pillars
- Ideal situation is complete removal of all carbon-based encapsulant, but highly likely carbon becomes trapped inside structures
- Tests to investigate these questions include focused ion beam (FIB) and energy-dispersive x-ray spectroscopy (EDX)
FIB Milling of Sintered Pillars

**FIB Milling and Sample Preparation:**

1. Sample placed on 45° and placed into tool
2. Sample tilted 7° to align axis along FIB beam for milling down center of pillar (beam current in nA range)
3. Sample tilted 45° to polish small section of milled pillar to prepare for EDX scans (beam current in pA range)

FIB of pillars sintered to varying degrees result in extremely varied milled surfaces:

**Waterfall effect:** Effect whereby milled surfaces exhibit a curtain-like appearance; often attributed to highly disparate atomic masses in material composition (e.g. C and Au)
- Observed in 150 °C and 175 °C condition but not 200 °C condition
  → Evidence of waterfall effect is qualitative measure of quantity of residual carbon content in pillars

**Cracking:**
- Cracks seen in mildest sintering condition only
EDX Scans of Polished Pillars

- Require smooth surfaces to more confidently assess material composition
  → Only able to perform reliable scans on 200 C sintered structures (after 10 pA polishing prep)

- Results:
  - Compare C and Au peaks throughout pillar
  - In base and center scans (a.-c.), Au is predominant element observed, with C signal roughly half of Au signal
  - At top of pillar (d.-e), C and Au signals comparable and C primarily located at center of pillar

Sintering front moving from bottom to top of pillar and carbon at center has potential to remain trapped in structure (longer path for outdiffusion)

Putting it All Together:
A Cross-Sectional View of Sintering Front

Progression of Sintering Front with Time

- As-fabricated Structure
- Bottom/Sidewall Sintering: Width Compaction
- Top Sintering: Height Compaction and Carbon Entrapment
Pillar Review

- Uniform/reliable 3D-printing process of functional inks
- High conductivity pillar structures at sinter temperatures not to exceed 200 °C
- Elastic modulus comparable to conventional eutectics
- Shear strength comparable to conventional eutectics at eutectic process temperatures and comparable to bulk properties at 300 °C

Through-silicon Vias (TSVs)
Inkjet-Printed TSVs: Fill and Bump

Leverage existing solder bump process to establish TSV nanoparticle process

The ability to both fill AND bump in the same process is a highly impactful and unique capability of inkjet-printed TSVs.

Process Flow

Increasing Drop Count

Si BOX Si

Filling Bumping

Fully-tunable TSV Fill and Bump

Complete arrays of filled and bumped TSVs fabricated by tuning the printing parameters: substrate temperature, drop delay, and total drop count.
Keyhole-free Via Fill and Bump

**Top-Down SEM**
80 µm diameter vias
At a given temperature and wait time, varying drop number leads to pillar growth out of a TSV

50 drops 70 drops 90 drops

**Cross-section SEM**
80 µm diameter vias
Cross-sectional analysis shows keyhole-free filling of TSVs throughout filling/pillar growth regimes

50 drops 70 drops 90 drops

*All scale bars represent 20 µm
*All TSVs sintered at 200 °C for 60 min

TSV Bonding Schemes and Test Structures

**Bonding Schemes**

1. Die-to-die
2. Die-to-wafer

SOI die
Si TSV die
Patterned Si wafer

**Test Structure Fabrication Process**

1. Die-to-wafer bonding
2. Handle removal
3. Oxide patterning
4. Top metal patterning

**Mechanical Test Structure**

**Electrical Test Structure**
## Via Bonding and Reflow

**Bonded TSVs**

Cross-sectional SEM image of die-to-die TSV bonds (20 µm scale bar)

**Reflow**

Drops = 30

TSVs
Bond pads

Drops = 35

TSVs
Bond pads

Drops = 40

TSVs
Bond pads

Bonded die sheared to observe extent of reflow (250 µm scale bar)

Cross-sectional analysis reveals dense filling of TSV and post-shear testing indicates reflow-like behavior of nanoparticle bumps

## Electrical and Mechanical Performance

**Maximum die shear strength = 1.9 kg, for die bonded with 144 TSVs**

Sample bonded and prepared for electrical testing

<table>
<thead>
<tr>
<th></th>
<th>Extracted Resistance (Ω)</th>
<th>Conductivity (S/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV</td>
<td>3.5e-02</td>
<td>3.34e03</td>
</tr>
<tr>
<td>Pillar</td>
<td>1.2e-02</td>
<td>7.58e04</td>
</tr>
<tr>
<td>Bulk Gold</td>
<td>N/A</td>
<td>4.54e05</td>
</tr>
</tbody>
</table>

Extracted resistance less than 1 Ω, but conductivity still much lower than printed pillars and bulk gold

**Metal nanoparticle-based inkjet-printed TSVs show much promise for future TSV filling and bumping applications.**
TSV Review

- Successfully transitioned solder bump inkjet processes to TSV filling and bumping process
- Demonstrated complete process flow for flip-chip bonded TSV die including reflow-like behavior during bond
- TSV mechanical and electrical properties show much initial promise. Plenty of room to improve performance with optimized sintering and bonding processes.

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