Cell Level Soft Error Rate Simulations of Planar and FinFET Processes

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Purpose

- Accuracy verification for cell level SER simulations of the FinFET process
- Discussion for multiple cell upset (MCU) probability of the FinFET SRAM

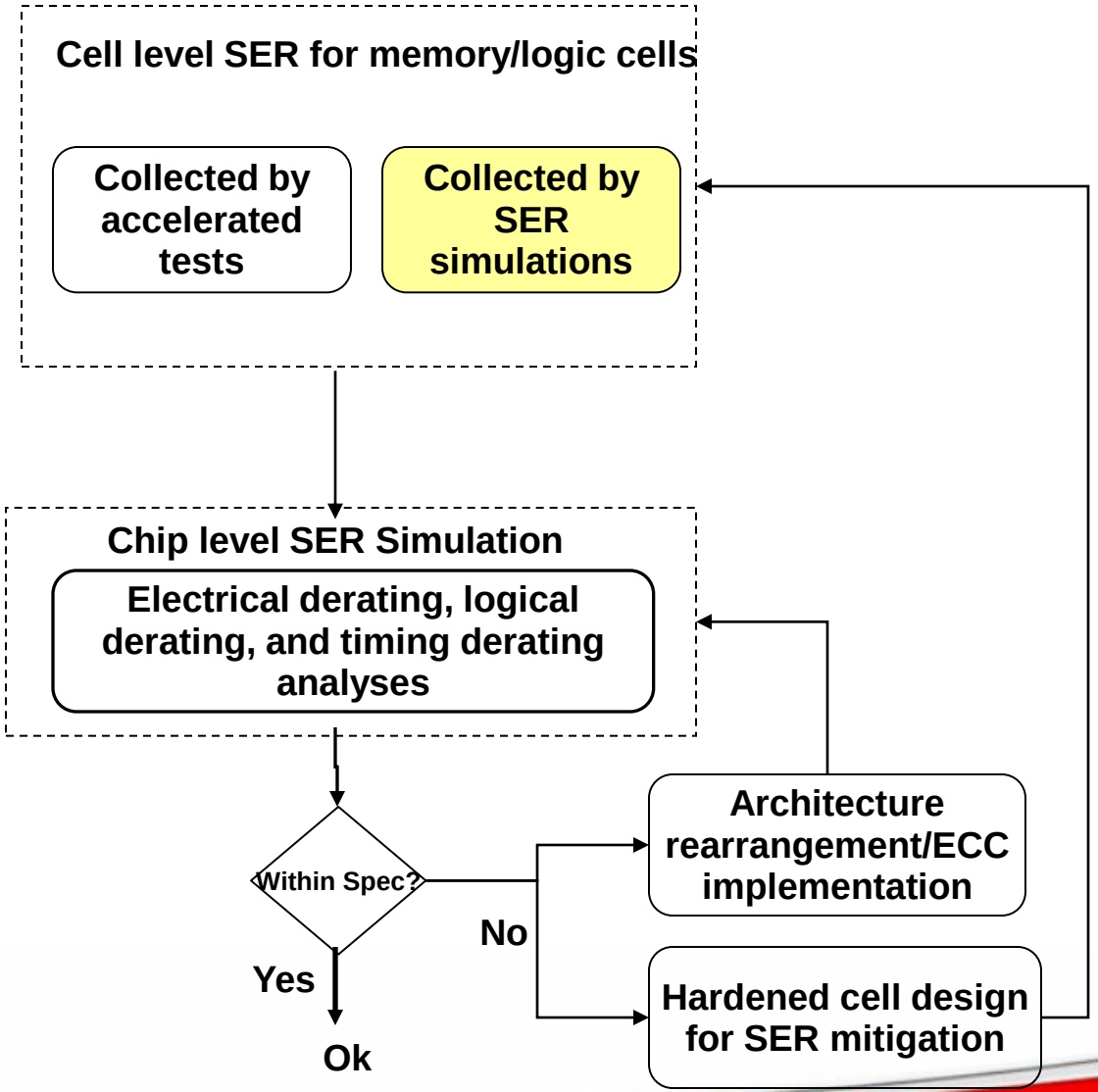
Outline

- Introduction
- TFIT Cell Level SER Simulation Flow
- Accuracy Verification for Simulations of Planar and FinFET Processes
- Discussion for MCU Probability of SRAMs of Planar and FinFET Processes
- Conclusion

Why is Cell Level SER Simulation Important?

- Difficult to collect cell level SER data from accelerated SER tests.
- Rapid to obtain the results. Only take mins to hours for a run.
- Lower cost for simulation compared to the SER test.
- Enable to evaluate vulnerable points in logic cells for SER hardened cell design.

SER Estimation Working Flow for SoC Circuits



A Case of Chip Level SER Simulations

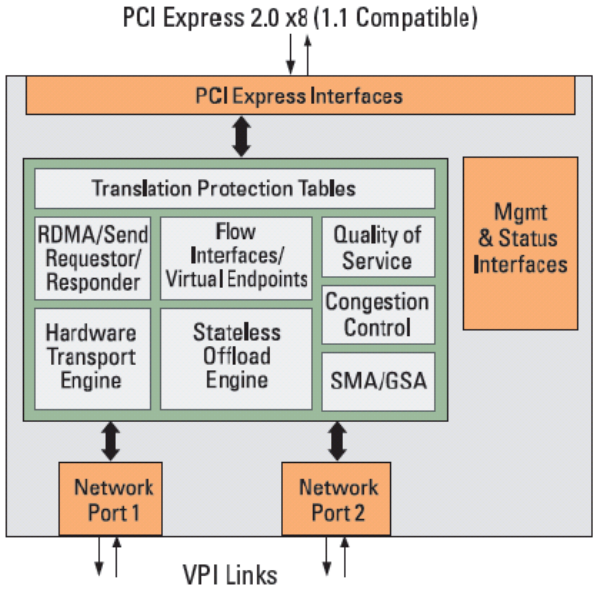


Figure. Block diagram of a infiniband host channel adapter (HCA)

H. Chapman et al, SELSE, 2010

Memory SER on the HCA before and after ECC correction

Table 4. HCA Memory SER/device (in AU)

	SBU SER	MBU SER	Un-Mitigated SER
CRC	57.14	0.00	0.00
Parity	136.14	0.78	0.78
ECC	197.93	0.08	0.08
Extended-ECC	7.89	0.23	0.00
Total	**399.10**	**1.10**	**0.86**

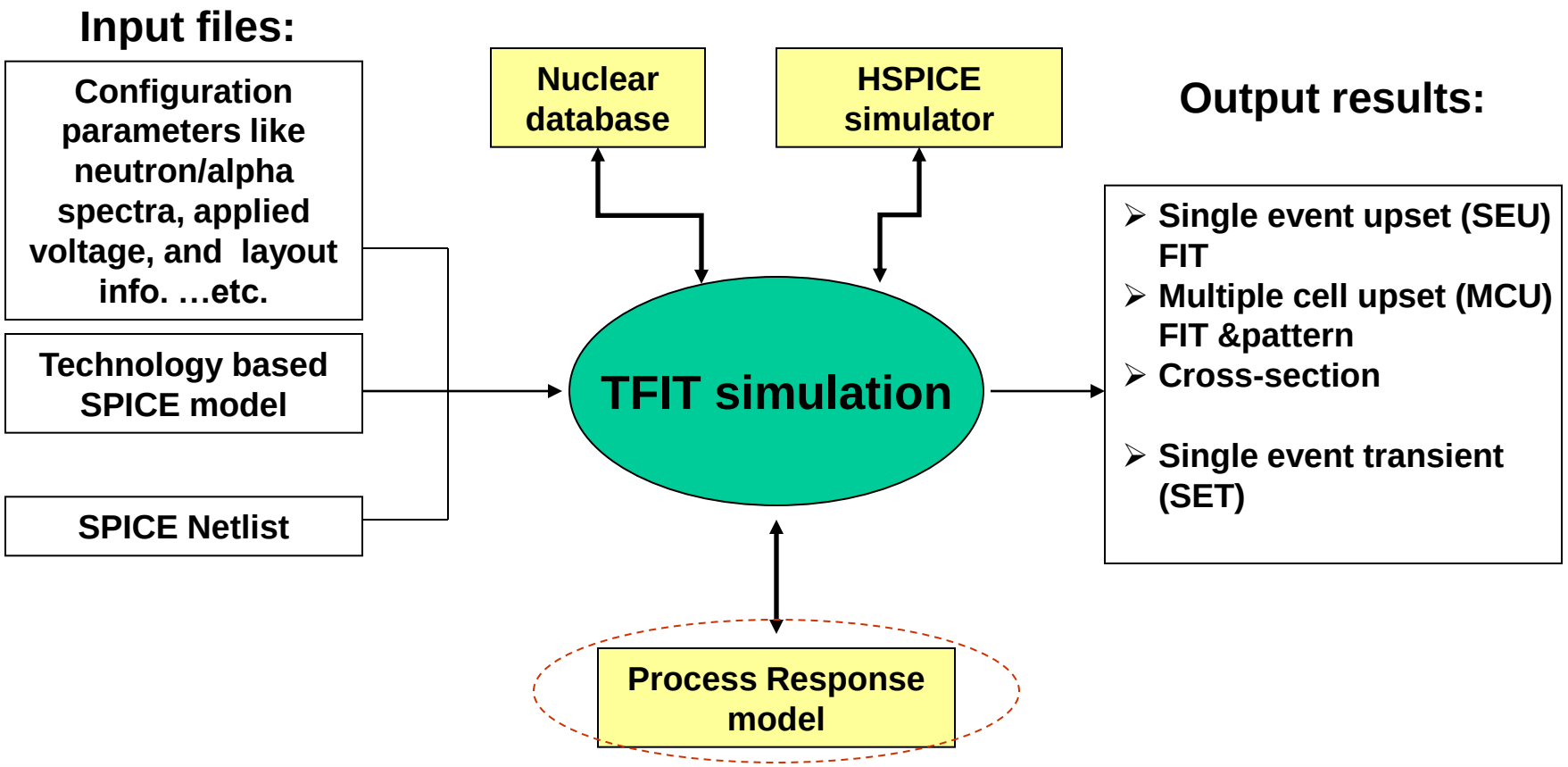
Logic SER on the HCA without any de-rating factor

Table 6. Structural Standard Cell RAW SER of the HCA design

	Raw HCA SER (AU)
Sequential logic	40.87
Combinational logic	6.67
Total standard cell SER	**47.54**

- **This case shows that the customer successfully perform cell level and chip level SER simulations for HCA products.**

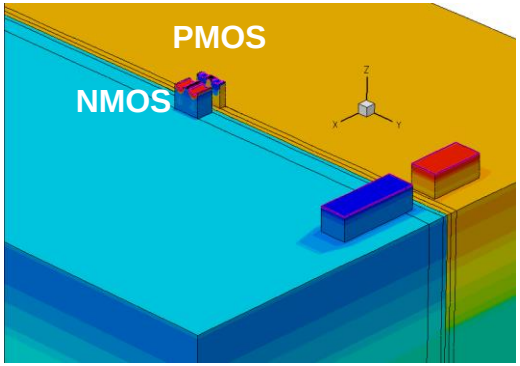
Cell Level SER Simulation Flow



Response single event transients (SET) collected by TCAD simulations for a specific technology. Calibration work is required.

Procedure of Process Response Model Setup for a Specific Technology

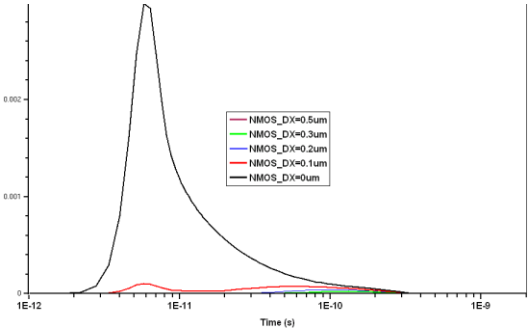
TCAD Process Related Inverter Structure



Design of Experiments (DoEs)

- LETs
- Operation Voltages
- Strike Locations

Collected Response SETs

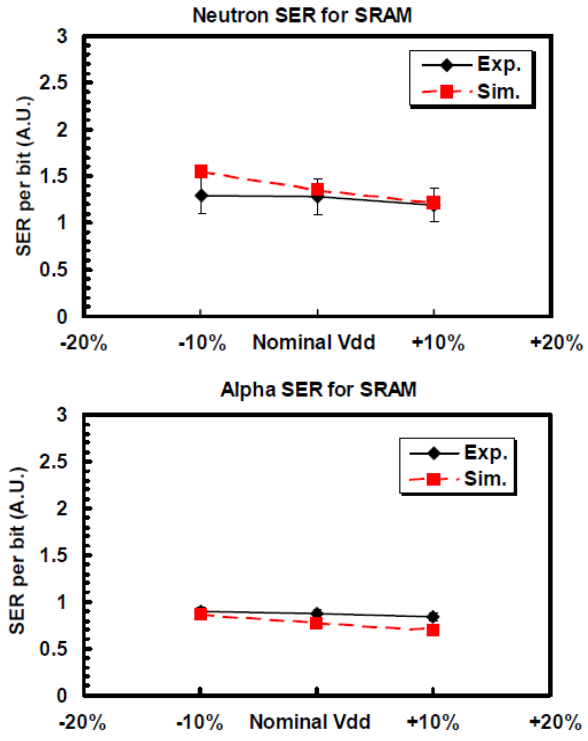


- ~400 TCAD DoE runs.
- DoEs taken several months for each process response model.
- 40nm to 16nm planar and FinFET process response models are now navailable at TSMC.

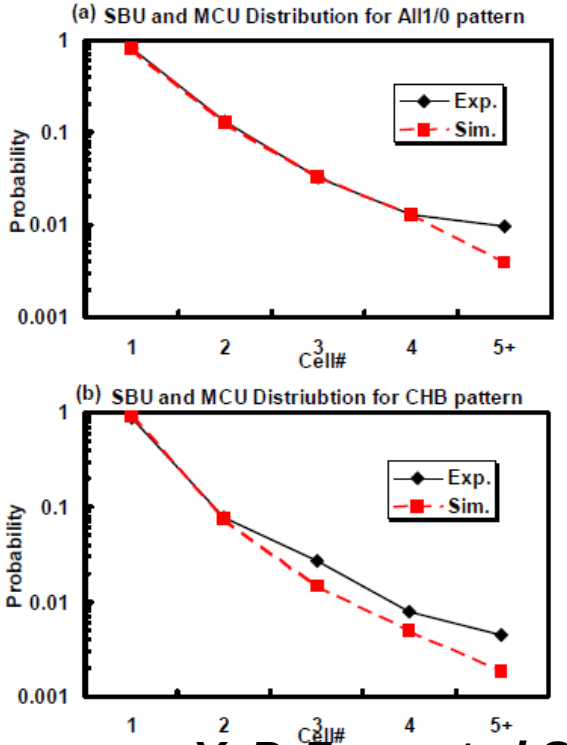
The Accuracy Verification for TFIT Simulations of Planar and FinFET Processes

Simulation Accuracy for a SRAM of a Planar Process

Different Voltage



Different test pattern

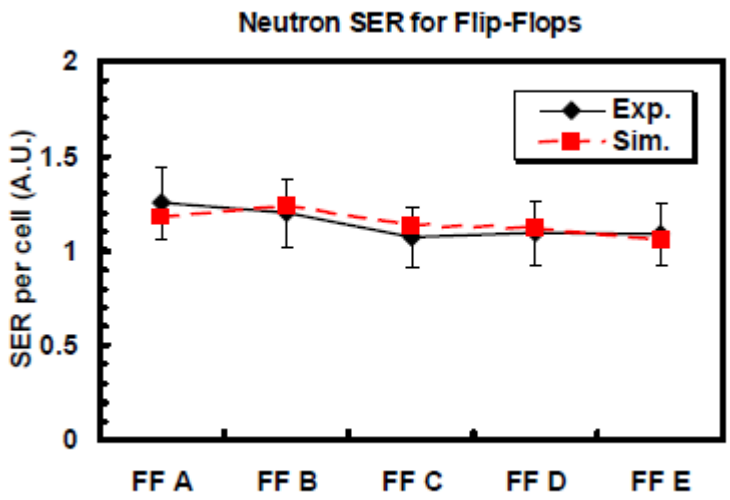


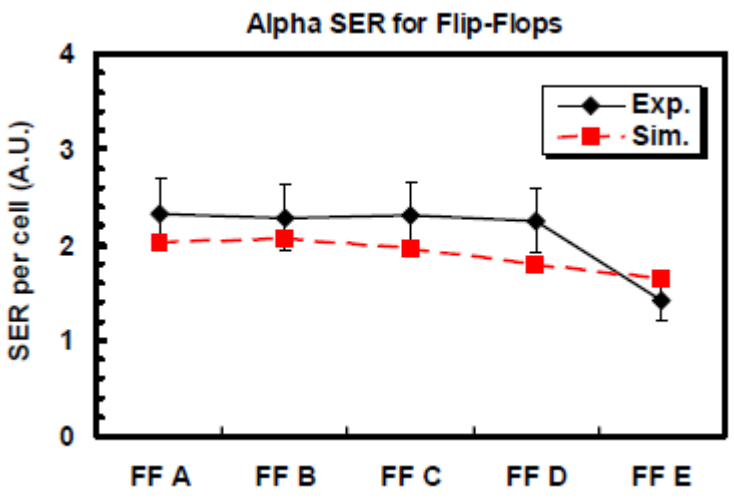
Y.-P. Fang et al SELSE 2013

- Accuracy verified for the SRAM with different Vdd and test patterns.
- Neutron induced MCU(&MBU) distribution can be simulated accurately.

Simulation Accuracy for Logic Cells of a Planar Process

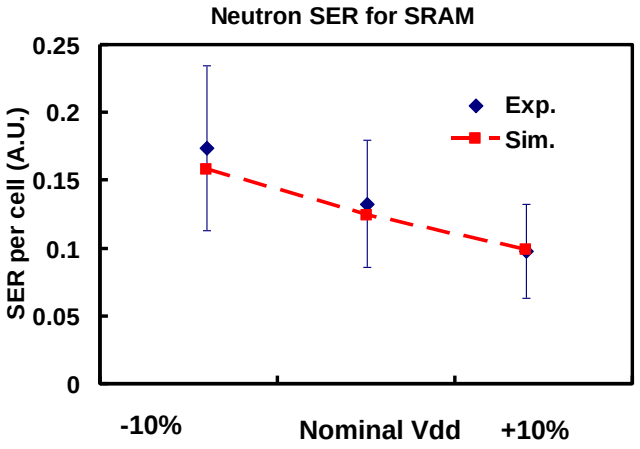
Y.-P. Fang et al, SELSE, 2013

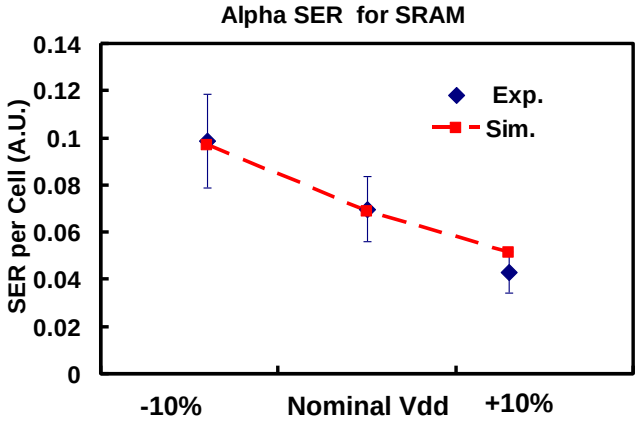


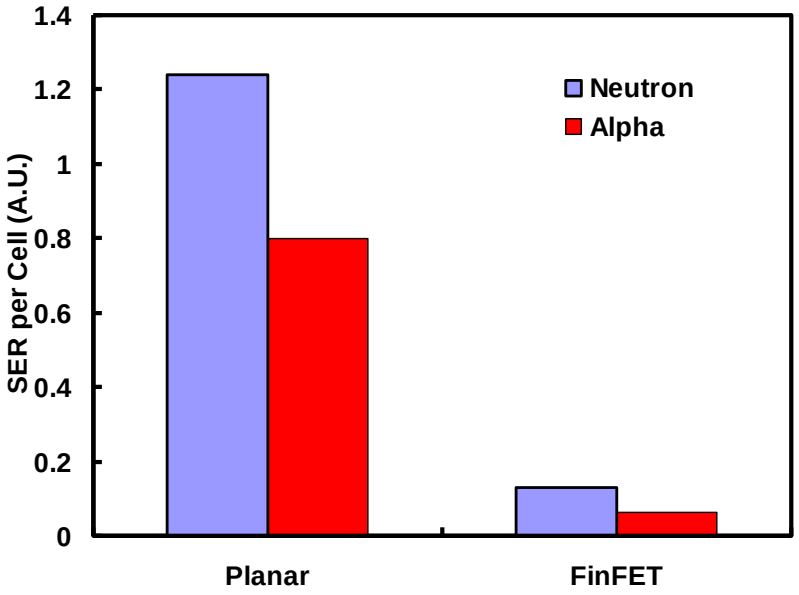


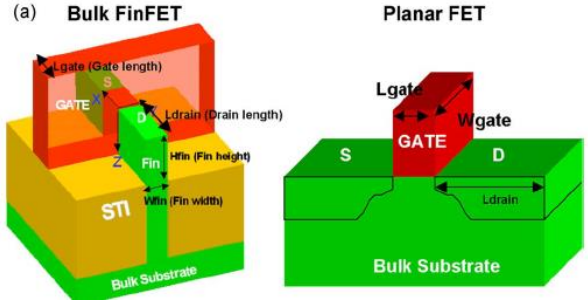
- Accurate simulation results are obtained for different types of sequential logic cells (Flip-Flops).
- Capable for cell level SER simulations.

Simulation Accuracy for the 6T-SRAM of a FinFET Process

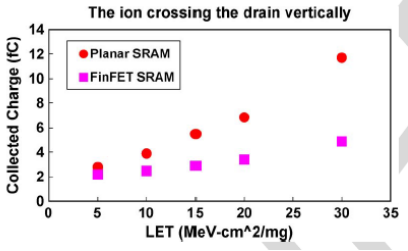








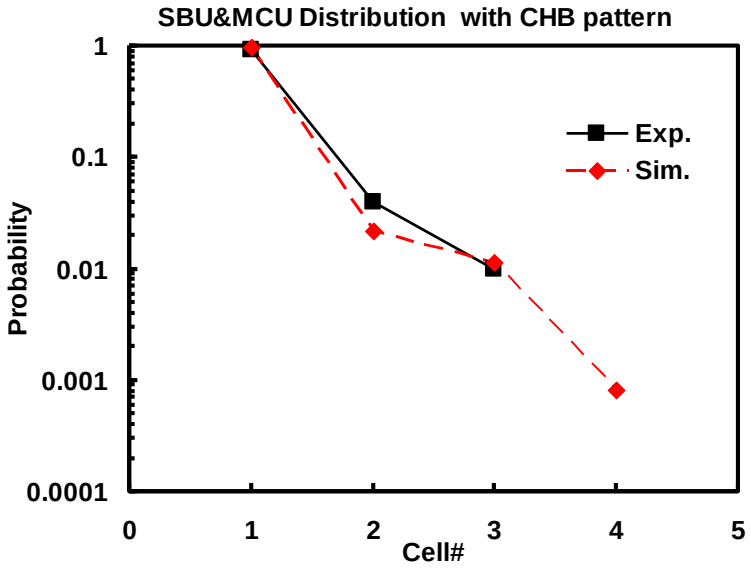
Y.-P. Fang et al, TDMR 2011

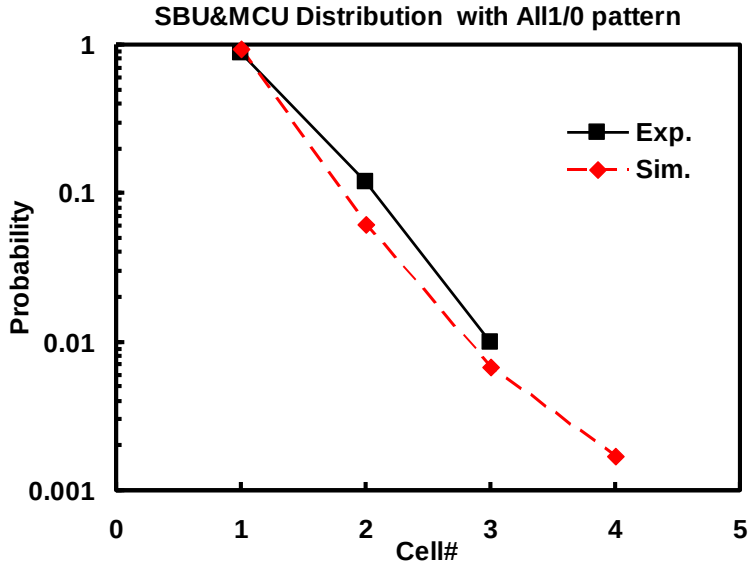


- Capable to simulate FinFET SRAM SER for different voltage
- ~10X neutron and ~15X alpha SER benefit for FinFET SRAM due to the reduction of drain area and collected charge.

Simulated Neutron-Induced MCU Distribution of the FinFET SRAM

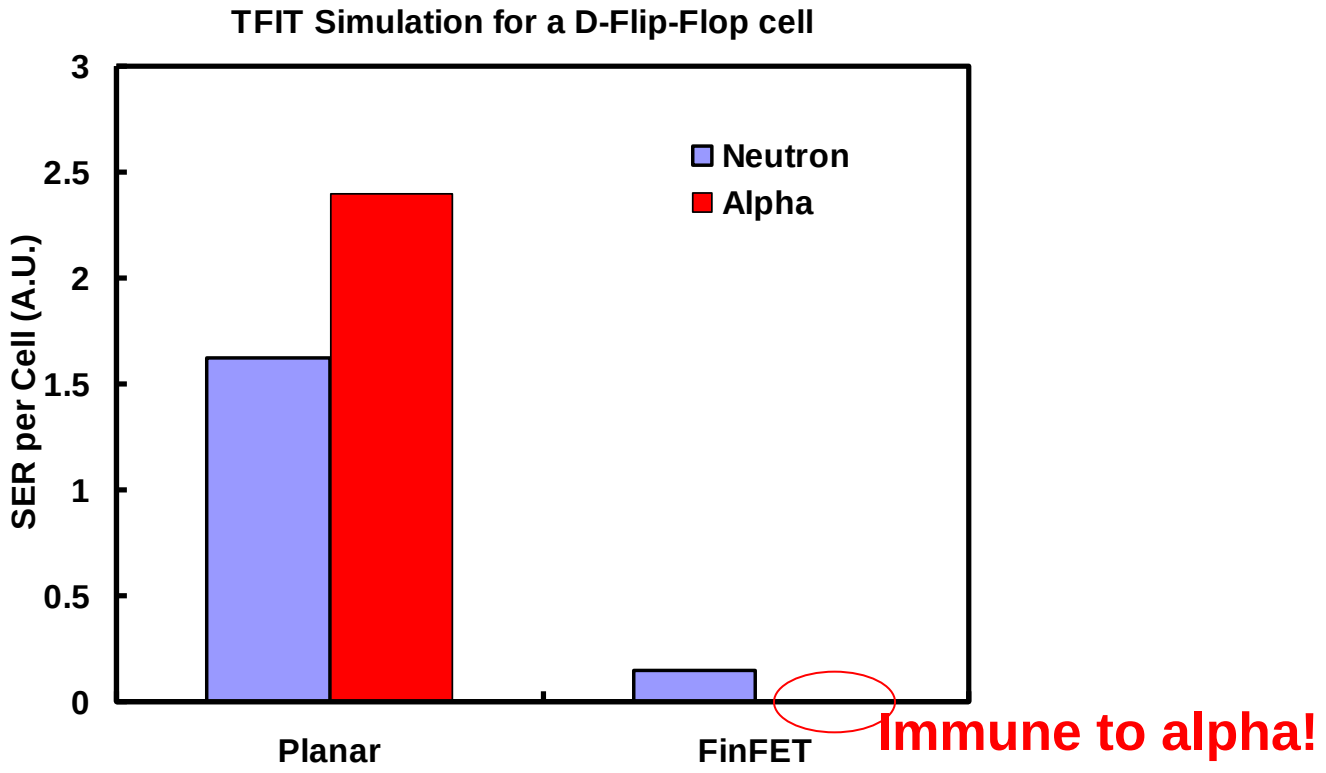
SBU (cell # =1) and MCU (cell # >1)





- **Capable to simulate accurate MCU distributions of the FinFET SRAM for different test patterns.**

Simulations for a Logic Cell of the FinFET Process

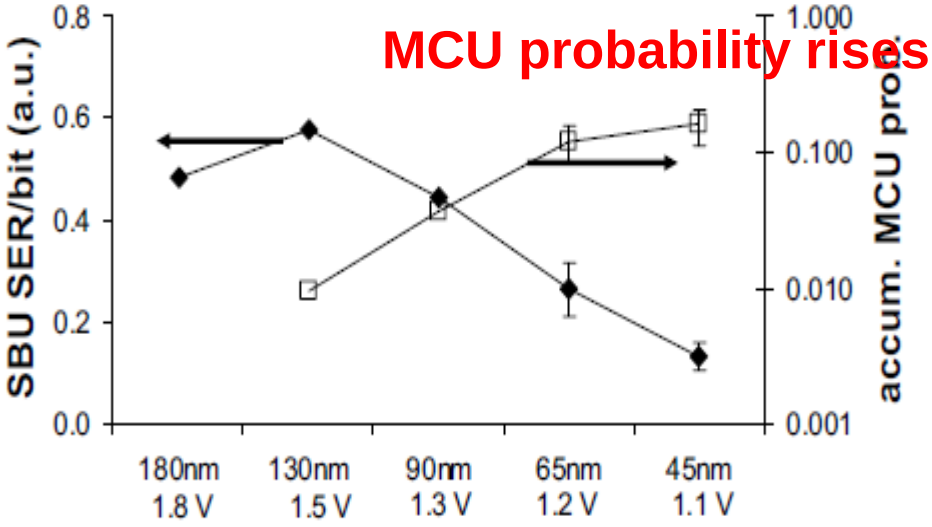


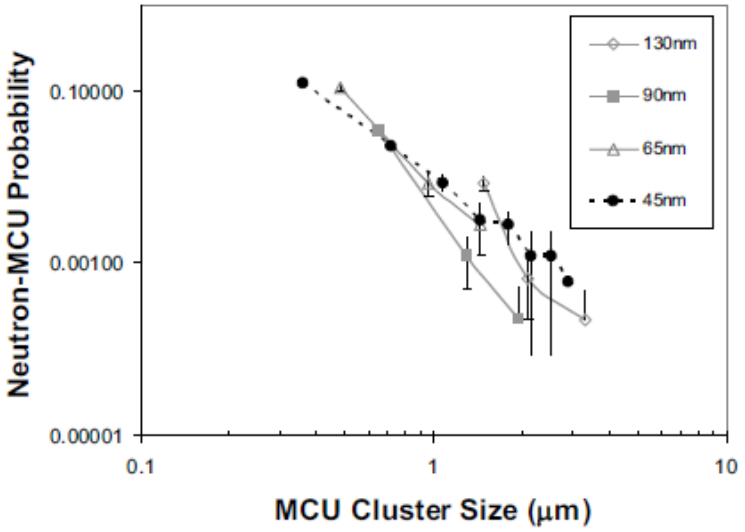
- Compared to a planar cell, neutron SER benefit for the FinFET cell is ~10X.
- The Flip-Flop cell is immune to alpha particles due to its high Qcrit.

Discussion for MCU Probability of SRAMs of Planar and FinFET Processes

Neutron Induced MCU Probability of Planar SRAMs in the Literature

N. Seifert et al, IRPS, 2008

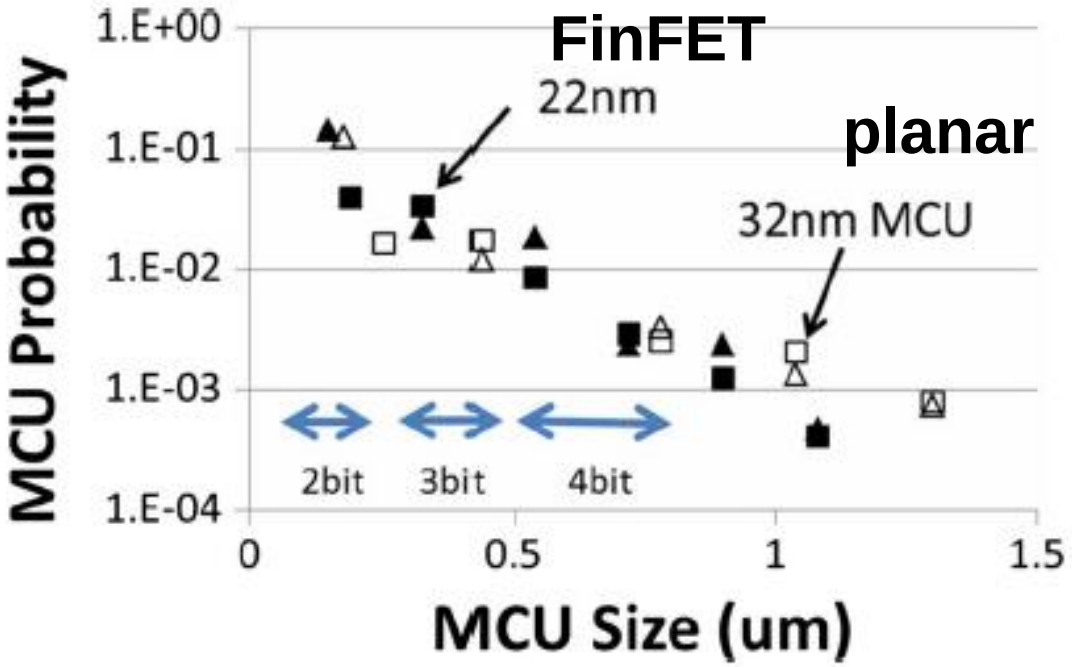




- The advanced technology with smaller bit-cell has higher MCU probability.
- The MCU trends as a function of cluster size are consistent across technology nodes.

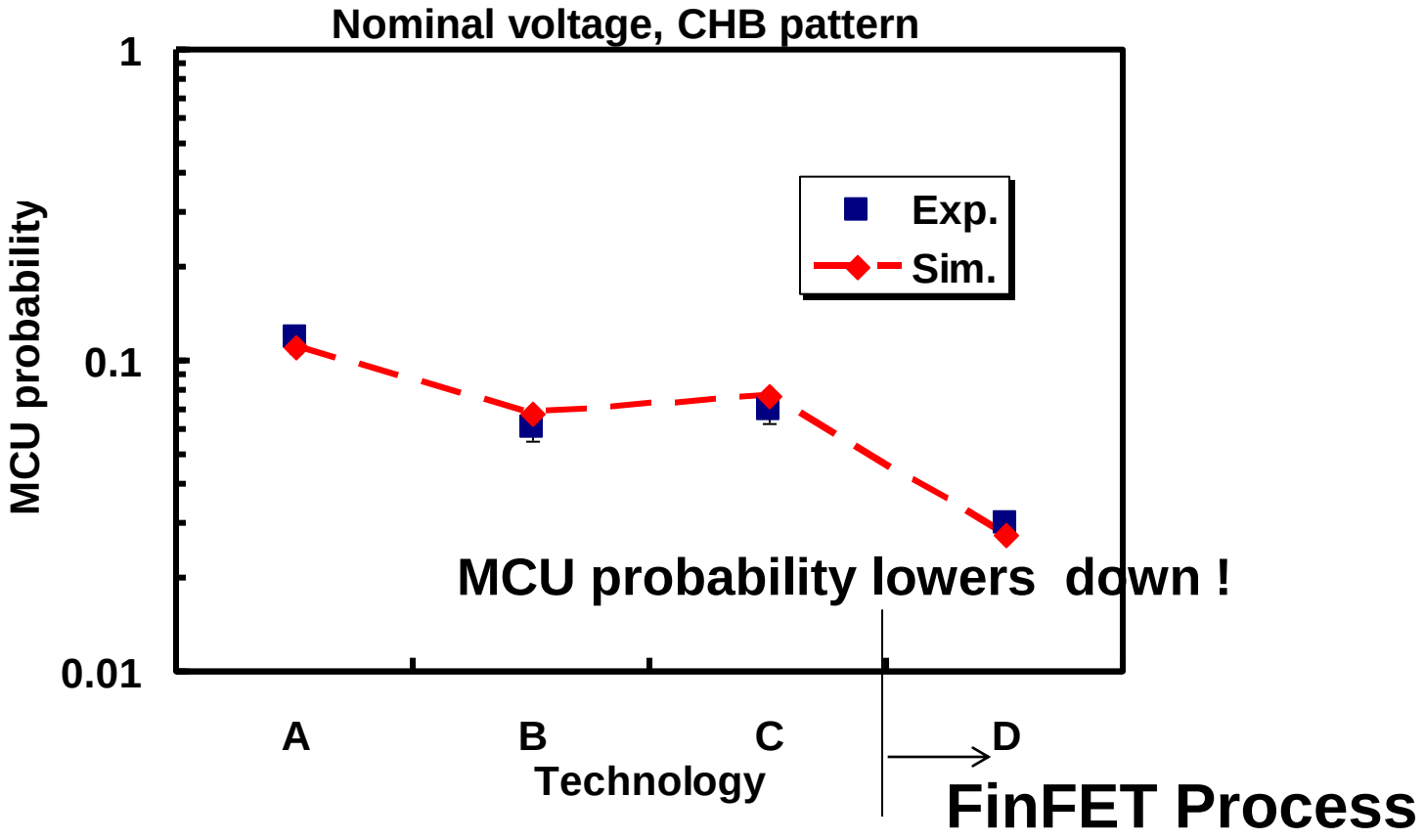
Comparison for MCU Probabilities of Planar and FinFET SRAMs in the Literature

N. Seifert et al, TNS, 2012



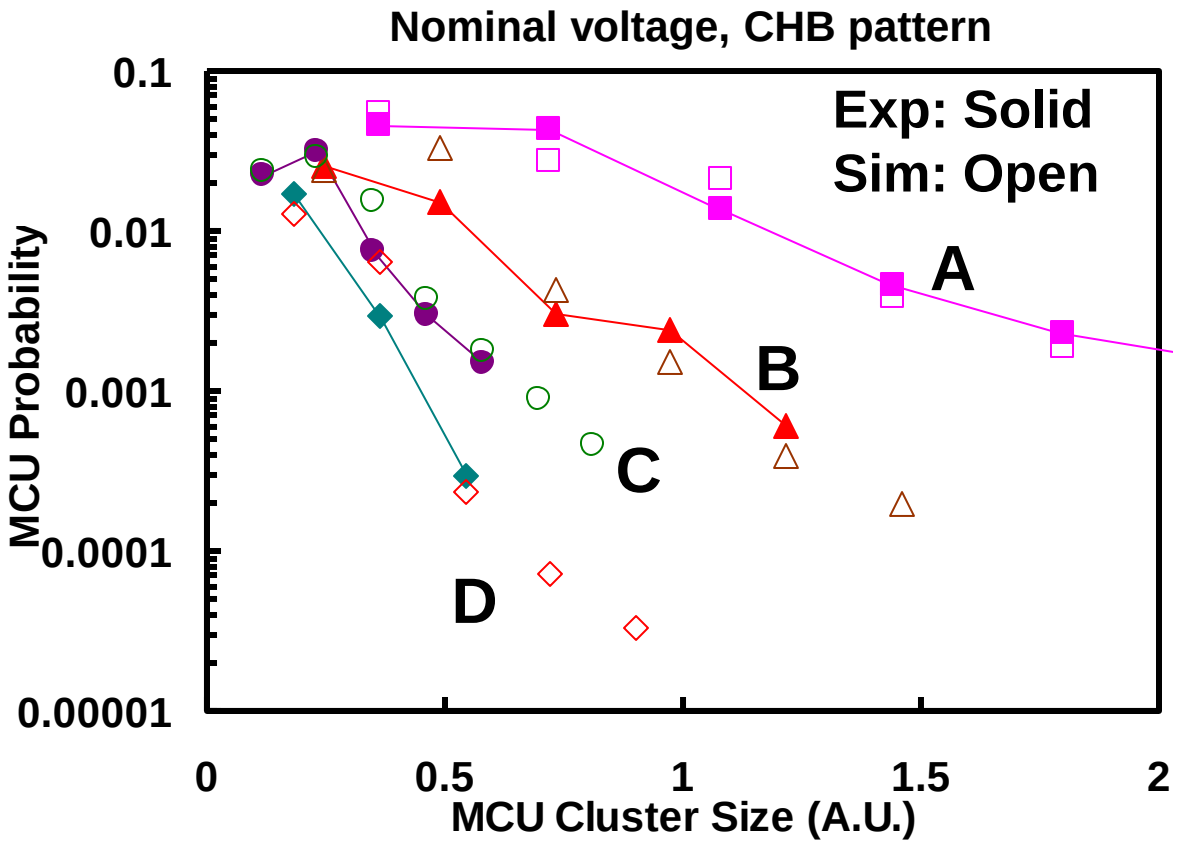
- **Total MCU probability rises for the FinFET SRAM.**
- **Geometry change of the FinFET is not benefit to the reduction of MCU probability.**

MCU Probabilities of SRAMs of Our Processes



- The MCU probability trend of SRAMs is opposite to the literature.
- Exp. and sim. results are in good agreement.

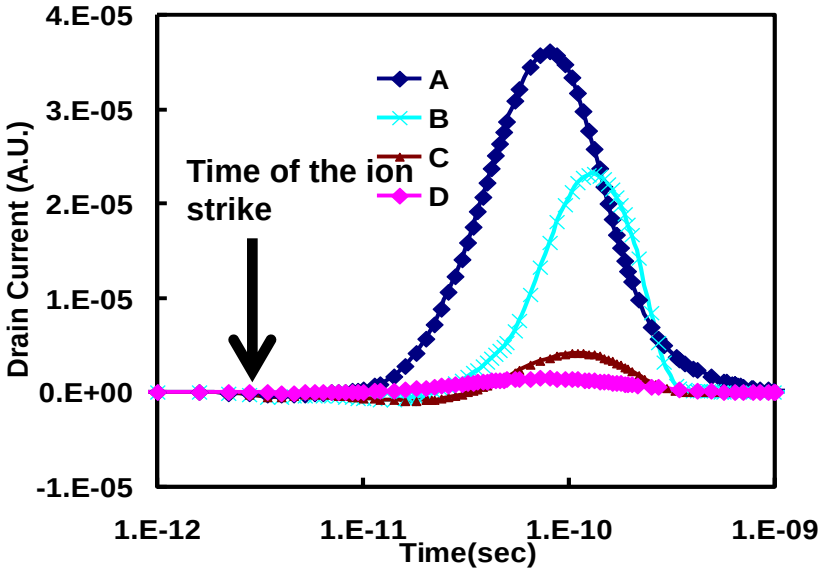
MCU Probabilities as a Function of MCU Cluster Size



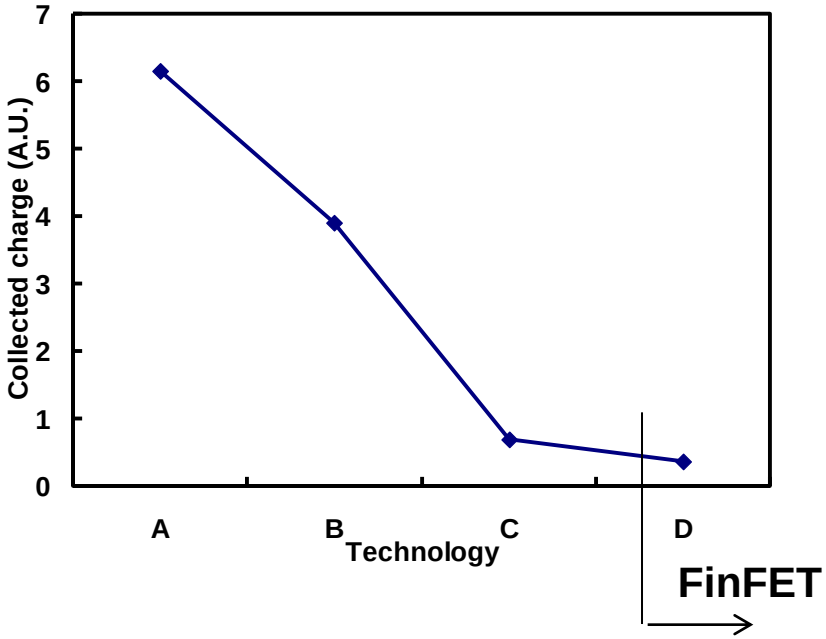
- MCU probabilities of SRAMs are process dependent.

Simulated Transient Currents of Different Processes

Current comparison



Q_{coll} comparison



- In the TCAD simulation, an ion strikes to the location away from the SRAM. Thus charge is collected by diffusion only.
- The results show Q_{coll} of the SRAM decrease with technology scaling due to different substrate doping levels of the processes.

Conclusion

- SER of memory and logic cells can be simulated accurately by TFIT for planar and FinFET processes.
- Neutron SER of FinFETs is ~10X lower than that of planar devices. Alpha SER is almost immune for FinFET process.
- TFIT cell level simulations are now available for technologly from 40nm to 16nm.
- MCU probability of the SRAM is not influenced by the FinFET structure.
- MCU probability of the SRAM is strongly process dependent.

Thank you!