

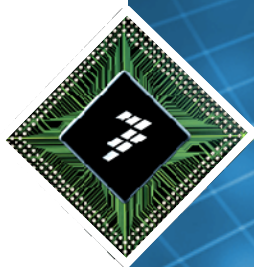


# Accounting for Soft Errors with Functional Safety

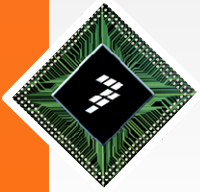
Jehoda Refaeli  
Automotive MCU



IEEE SER workshop  
October 2014

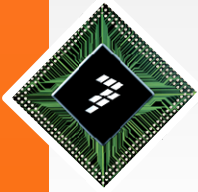


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# Agenda

- Functional Safety at Freescale
- Functional Safety and Microcontrollers
- MCU Safety Context and Safety Concepts
- FMEDA
- Soft errors



# A *Global Leader* in Microcontrollers and Digital Networking Processors

## Five Core Product Groups

## Four Primary Markets

Microcontrollers

Automotive



Digital Networking

Networking



Automotive MCU

Industrial



Analog

Consumer



RF

>50 Year Legacy

>5,500 Engineers

>6,100 Patent Families



# Health & Safety

Several Platforms Key to Making the World a **Healthier, Safer** Place

## Automotive



- Active Safety Systems
- Advanced Driver Assistance
- Radar, Vision Systems
- Functional Safety

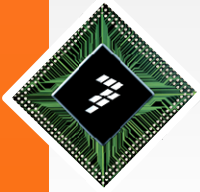
## Industrial



- Connected Home
- Portable Medical
- Factory Automation Systems



*We See a Healthier, Safer Population*



# SAFE ASSURE™ *by Freescale*

## Functional Safety. Simplified.

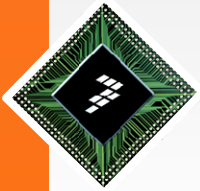
**Simplifies the process** of system compliance, with solutions designed to address the requirements of automotive and industrial functional safety standards

**Reduces the time and complexity** required to develop safety systems that comply with ISO 26262 and IEC 61508 standards

**Supports the most stringent Safety Integrity Levels (SILs)**, enabling designers to build with confidence

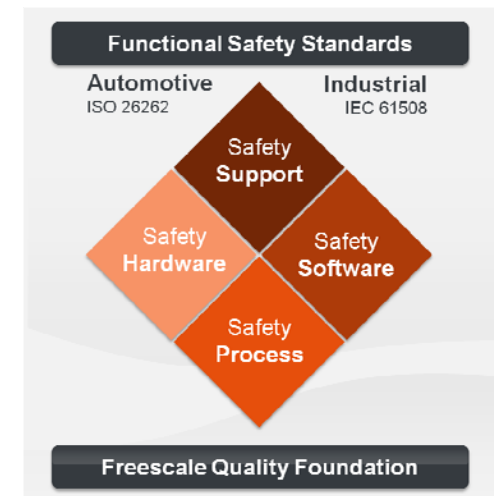
**Zero defect methodology** from design to manufacturing to help ensure our products meet the stringent demands of safety applications

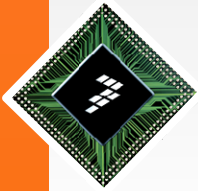




## SafeAssure - *Simplification*

- SafeAssure products are conceived to **simplify** system level functional safety **design** and cut down time to **compliance**
- Component safety measures **augment** system level safety measures
- Key functional safety activities addressed
  - Safety analysis (*FMEA, FTA, FMEDA*)
  - Hardware integration (*Safety Manual*)
  - Software integration (*Safety Manual*)
  - Support interface (*Roles & Responsibilities*)





# History of Auto MCU Functional Safety Solutions

- **Gen 1 Safety** More than 10 years experience of safety development in the area of MCU & SBC
- **Gen 2 Safety** First general market MCU, **MPC5643L** ⇒ **Certified ISO 26262!**
- **Gen 3 Safety** From 2012, multiple MCUs in Body, Chassis and Powertrain are being designed and developed according to ISO 26262

Functional Safety Solutions

2000

Gen 1 Safety



## Custom Safety Platform for Braking

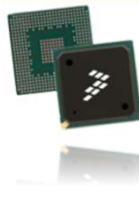
- Started to ship in 2000 first safe MCU for braking applications
- IEC 61508 / ISO 26262 compliance achieved at system level (top down approach)
- MCU features are a key enabler for SIL3 / ASILD



## Custom IC

2008

Gen 2 Safety



## MPC5643L – 90 nm

- **32-bit Dual-Core MCU**
- Developed according to ISO 26262
- Target Applications for Chassis – ASILD

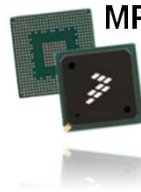


## PowerSBC

- Voltage Supervision
- Fail-Safe State Machine
- Fail-Safe IO
- Advanced Watchdog

2012

Gen 3 Safety



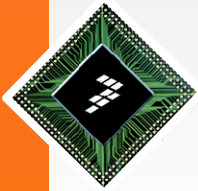
## MPC5744P/MPC5777K/etc 55 nm

- **32-bit Dual/Quad-Core MCU**
- Developed according to ISO 26262
- Target Applications Chassis & P/T for – ASILD
- Safe methodology, Architecture, SW and tools



## PowerSBC

- Voltage Supervision
- Fail-Safe State Machine
- Fail-Safe IO
- Advanced Watchdog



# First ISO 26262 Certified MCU – Qorivva MPC5643L

- Certified by exida – an independent accredited assessor
- Certificate issued based on a successful assessment of the product **design**, applied **development & production processes** against requirements and work products of ISO 26262 applicable to a MCU
- **MPC5643L MCU certified for use for all Automotive Safety Integrity Levels (ASIL), up to and including the most stringent level, ASIL D**

The manufacturer may use the mark:



**Reports:**  
Freescale 11/08-067-C R009 V1 R0  
Results of the ISO 26262 Functional Safety Assessment

**Validity:**  
This assessment is valid for Microcontroller MPC5643L

This assessment is valid until August 31, 2015.

V1 R1 September, 2012



Certificate / Certificat  
Zertifikat / 合格証

FREESCALE 1108067 P0026 C001

*exida* Certification S.A. hereby confirms that the:

**MICROCONTROLLER MPC5643L**

**FREESCALE Halbleiter Deutschland GmbH**  
Munich, Germany

Has been assessed per the relevant requirements regarding  $\mu$ C development and verification & validation of:

**ISO 26262 : 2011 Parts 2, 4, 5, 7, 8, 9 and 10 (to the extent applicable)**

and meets requirements providing:

**Systematic Integrity: ASIL D**

**Safety related function:**  
The  $\mu$ C supports the execution of safety-related software by a dual-core lock-step architecture with memory protection and centralized fault collection and control unit.

**Application restrictions:**  
The microcontroller shall be used per the Safety Application Guide requirements.

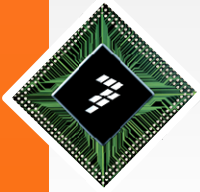


  
 Evaluating Assessor  
  
  
 Certifying Assessor

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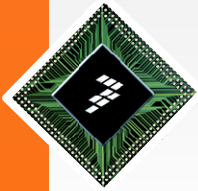







# Agenda

- Functional Safety at Freescale
- **Functional Safety and Microcontrollers**
- MCU Safety Context and Safety Concepts
- FMEDA
- Soft errors

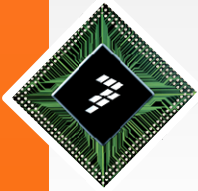


# The World of Functional Safety Standards

	1980	1985	1990	1995	2000	2005	2010	2015
Aeronautic	DO 178 DO 178A		DO 178B — ARP 4754	ARP 4761	DO 254		DO 178C — ARP 4754A	
Rail Transport				EN 50155	IEC 61508 EN 5012X EN 50159			
Generic Standard IEC61508					IEC 61508		IEC 61508 Ed. 2.0	
Industrial Automation					IEC 61508 IEC 61511 IEC 62061	ISO 13849	IEC 61508 Ed. 2.0	
Automotive					(IEC 61508)		ISO 26262	
Medical							IEC 60601 Ed. 3.0	


 Select Freescale products are being defined and designed from the ground up to comply with ISO 26262 and enabled for IEC 61508 Ed. 2.0 & ISO 13849



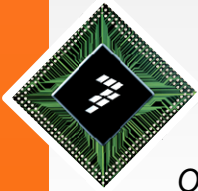


# Comparison of Functional Safety Standards

**Functional Safety** is the absence of unreasonable risk due to hazards caused by malfunctioning behavior of electrical / electronic systems

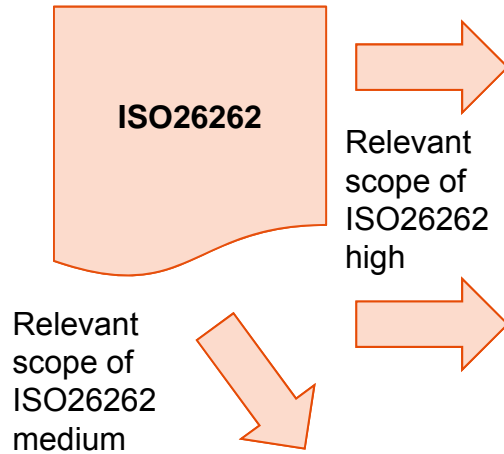
ISO 26262	IEC 61508	ISO 13849
<p><b>Automotive</b> Industry standard, adaptation of IEC 61508 for electrical / electronic systems within <b>road vehicles</b></p>	<p><b>Generic</b> Industry standard, applicable to electrical / electronic / programmable electronic <b>safety-related</b> systems.</p>	<p><b>One</b> of two European Standards to achieve compliance with the <b>Machinery Directive</b> 2206/42/EC</p>
<p><b>Safety Integrity Levels</b> ASIL A, ASILB, ASIL C, ASIL D</p>	<p><b>Safety Integrity Levels</b> SIL 1, SIL 2, SIL 3, SIL 4</p>	<p><b>Performance Levels</b> a, b, c, d, e</p>
<p><b>Publication date</b> 15 Nov 2011</p>	<p><b>Publication date</b> Ed. 2.0 – Apr 2010 <i>Ed. 1.0 - More than 10 years ago</i></p>	<p><b>Categories</b> B, 1, 2, 3, 4</p>

**Freescale** is strengthening its product development cycle, making functional safety an integral part of the process.



# Example Interaction Between Car OEM, Tier 1 & Tier 2 (Freescale)

Overall ISO 26262 compliance is achieved together, we each own a piece of the puzzle



OEM
<ul style="list-style-type: none"> <li>Item definition</li> <li>Hazard analysis and risk assessment</li> <li>Safety Goals</li> <li>Functional Safety Concept</li> </ul>

Safety Manual & Safety Analysis Safety Requirements & DIA

Tier 1
<ul style="list-style-type: none"> <li>Safety Architecture</li> <li>Safety Concept</li> <li>ASIL Classification of Functions</li> </ul>

Safety Manual & Safety Analysis Safety Requirements & DIA

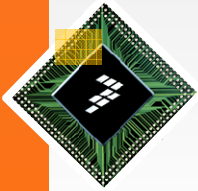
Tier 2 Supplier - Freescale
<ul style="list-style-type: none"> <li>HW / SW offering</li> </ul>

Foundation

Product Safety Measures (implemented in offering, described in Safety Manual, quantified/qualified by Safety Analysis)
Development Process & Methods
Quality & Quality Data

**Freescale**  
Functional Safety Focus  
Safety Element out of Context





# MCU HW Component Developed as SEooC

Safety Manual includes all HW & SW requirements on system level (Assumptions) as well as MCU Safety Concept description

(4-6) MCU Safety Context

(4-7) MCU Safety Concept

MCU SEooC Safety Plan

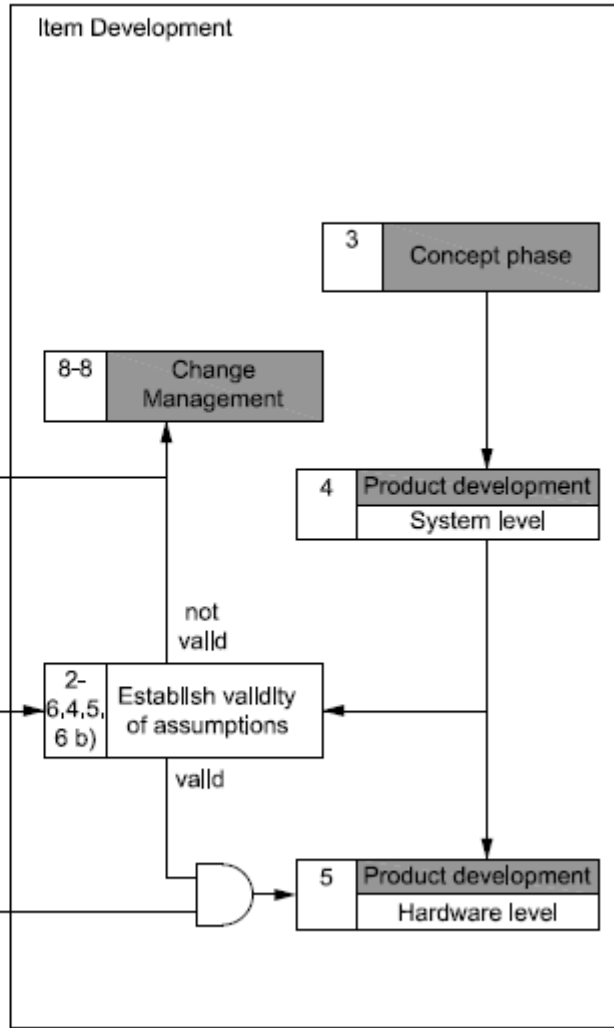
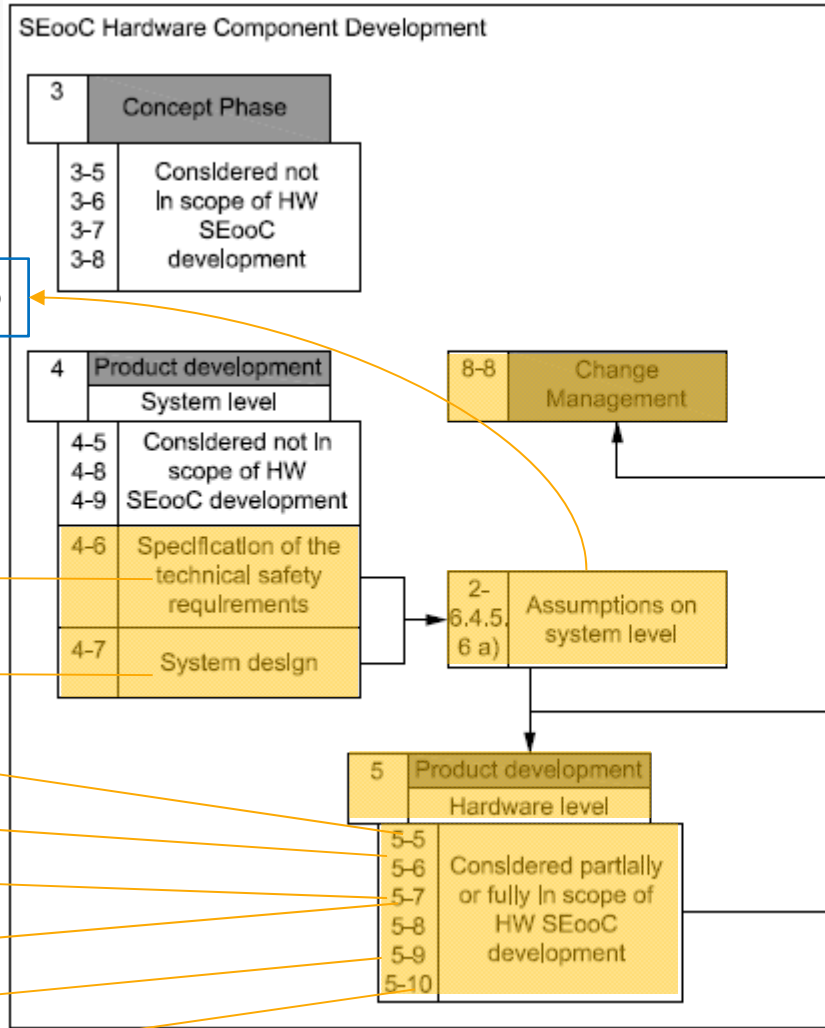
(5-6) MCU HW Safety Requirements

(5-7) MCU HW Design Specification

(5-7) Simulation Testing

(5-8,9) MCU FMEDA

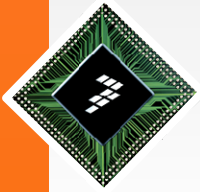
(5-10) Silicon Testing



Applicable to MCU HW Component developed as SEooC

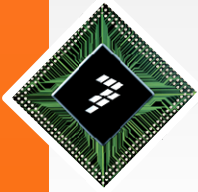
Reference ISO 26262-10:2012



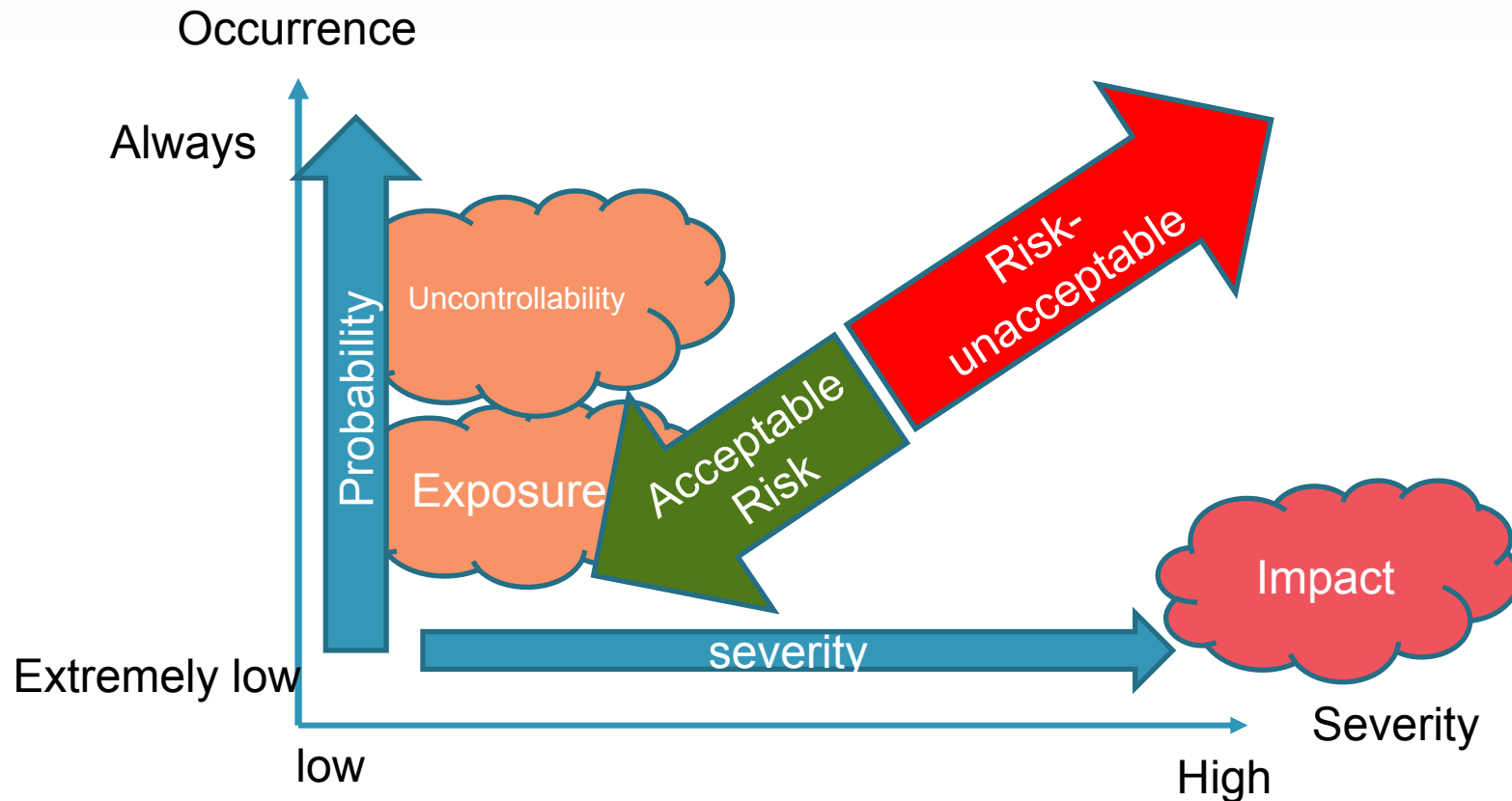


# Contents

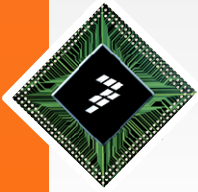
- Functional Safety at Freescale
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- **MCU Safety Context and Safety Concepts**
- FMEDA
- Soft errors



# Functional Safety – Risk definition



**Risk: Combination of the probability and extent of damage**



# Hazard Analysis and Risk Assessment (HARA)

- Identify and categorize the hazards that can be triggered by malfunctions in the system
- The Risk Assessment is carried out using three criteria
  - Severity – how much harm is done?

Class	S0	S1	S2	S3
Description	No injuries	Light and moderate injuries	Severe and life-threatening injuries (survival probable)	Life-threatening injuries (survival uncertain), fatal injuries

- Exposure – how often is it likely to happen?

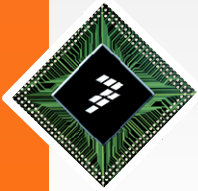
Class	E0	E1	E2	E3	E4
Description	Incredible	Very low probability	Low probability	Medium probability	High probability

- Controllability – can the hazard be controlled?

Class	C0	C1	C2	C3
Description	Controllable in general	Simply controllable	Normally controllable	Difficult to control or uncontrollable

Reference ISO 26262-3:2011





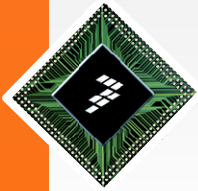
# Determination of ASIL and Safety Goals

- For each Hazardous event, determine the ASIL based on Severity, Exposure & Controllability
- Then formulate **safety goals** to prevent or mitigate each event, to avoid unreasonable risk

Table 4 — ASIL determination

Severity class	Probability class	Controllability class		
		C1	C2	C3
S1	E1	QM	QM	QM
	E2	QM	QM	QM
	E3	QM	QM	A
	E4	QM	A	B
S2	E1	QM	QM	QM
	E2	QM	QM	A
	E3	QM	A	B
	E4	A	B	C
S3	E1	QM	QM	A
	E2	QM	A	B
	E3	A	B	C
	E4	B	C	D

Reference ISO 26262-3:2011



# Target Metrics for ASIL

- Associate the following target metrics to each **safety goal**
  - Single-point fault metric (SPFM)

Table 4 — Possible source for the derivation of the target “single-point fault metric” value

	ASIL B	ASIL C	ASIL D
Single-point fault metric	≥90 %	≥97 %	≥99 %

- Latent-fault metric (LFM)

Table 5 — Possible source for the derivation of the target “latent-fault metric” value

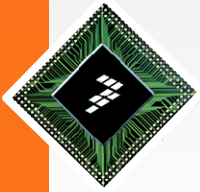
	ASIL B	ASIL C	ASIL D
Latent-fault metric	≥60 %	≥80 %	≥90 %

- Probabilistic Metric for random Hardware Failures (PMHF)

Table 6 — Possible source for the derivation of the random hardware failure target values

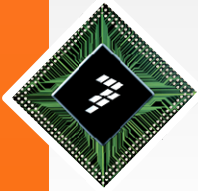
ASIL	Random hardware failure target values
D	$<10^{-8} \text{ h}^{-1}$
C	$<10^{-7} \text{ h}^{-1}$
B	$<10^{-7} \text{ h}^{-1}$

Reference ISO 26262-5:2011



# Example – EPS System

- Application Context
  - **Safety Goal 1 (SG1):** The EPS does not apply unintended force to the steering system (**ASIL D**).
    - Hazard: Unintended steering assist
    - Risk Assessment
      - S3: Life threatening injuries (survival uncertain), fatal injuries
      - E4: High probability
      - C3: Difficult to control or uncontrollable
  - Typical FTTI = 20 ms
  - System Safe State: disable EPS and notify driver of problem (fail-safe, fail-indicate)
- MCU Assumptions
  - **Safety Function 1 (SF1):** Execute software instructions, process data, write back result (**ASIL D**)  
-> mapped to SG1
  - Portion of FTTI: 10 ms
    - 50% of SG1 FTTI for HW safety measures
  - Define portion of ASIL target allocated to each safety function
    - **SPFM: 99%, LFM: 90%, PMHF:  $10^{-10}$  hour<sup>-1</sup>** (1% of safety goal ASIL target)
  - MCU Safe State (fail safe, fail indicate)
    - Reset, indicating an error



# Defining the MCU Safety Concept

- Objective
  - Define how MCU ASIL targets will be achieved between a mix of on-chip HW safety measures and system level safety measures (HW/SW)
- ISO 26262-5 Annex D – Elements related to MCU
  - Low application dependency: Power, Clock, Flash, SRAM & Processing Unit
  - High application dependency: Digital IO & Analog IO

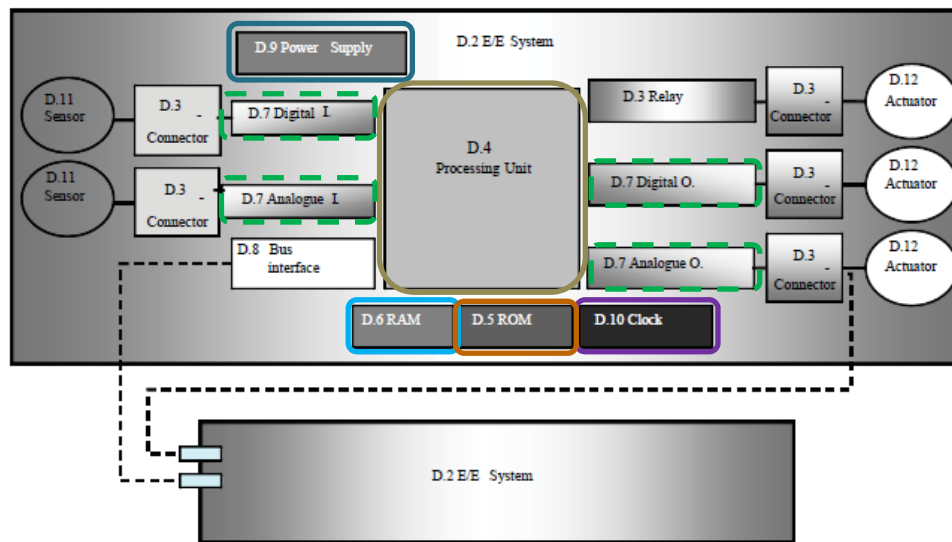
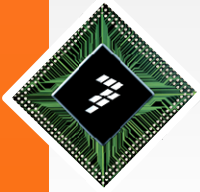
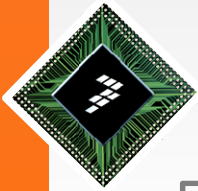


Figure D.1 — Generic hardware of a system Reference ISO 26262-5:2011



# Contents

- Functional Safety at Freescale
- Functional Safety and Microcontrollers
- MCU Safety Context and Safety Concepts
- **FMEDA**
- SER



# Safety Support – Tailoring of FMEDA

## Objective

- Tailor FMEDA to match application configuration
- Enables customers, by supporting their system level architectural choices

## Content

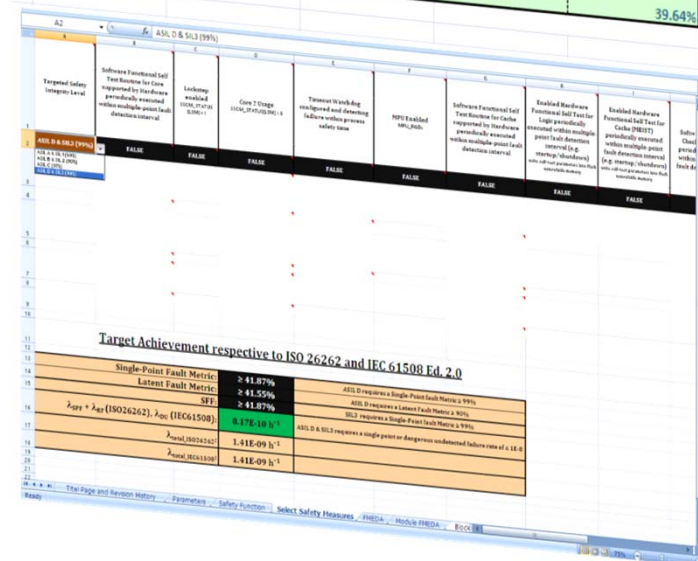
- FMEDA methods aligned with functional safety standards
  - SPFM & LFM, PMFH – ISO 26262
  - SFF & PFH- IEC 61508 Ed. 2.0
  - $\beta$ ic – IEC 61508 Ed. 2.0 part 2, Annex E
- Dynamic/Tailored FMEDA covers elements with low application dependency: Clock, Power Supply, Flash, SRAM, Processing Unit...

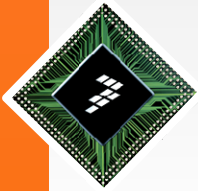
## Work flow and result

- Customer specifies the failure model (dependent on Safety Integrity Level) required by their application, and then confirms the Safety Measures that will be used or not be used
- A tailored FMEDA is then supplied to customer's for their specific application

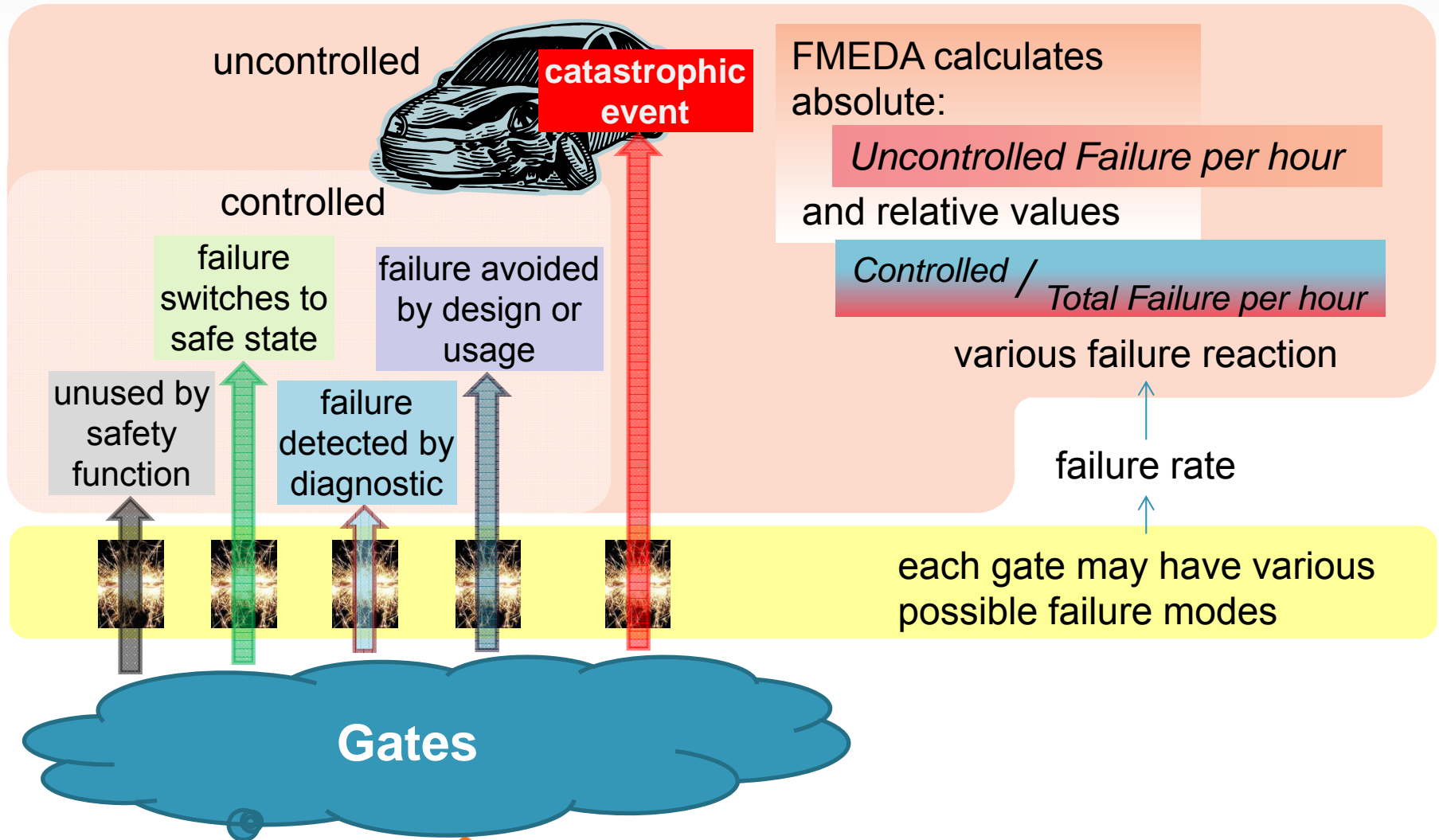
Temperature Profiles to calculate equivalent "average" temperature

time	temperature		Logic Gate	SEL
	$t_{\text{exposed}}$ in h	$T_{\text{mediate}}$	failure acceleration GATE	failure acceleration
0 h	-30 °C	-40 through -20	4.01E-07	1.84E-02
80 h	-10 °C	-20 through 0	5.57E-06	3.75E-02
400 h	20 °C	0 through 40	1.47E-04	9.12E-02
1000 h	50 °C	40 through 60	2.12E-03	1.88E-01
1400 h	70 °C	60 through 80	9.67E-03	2.84E-01
3000 h	90 °C	80 through 100	3.74E-02	4.10E-01
1700 h	110 °C	100 through 120	1.25E-01	5.69E-01
300 h	130 °C	120 through 140	3.73E-01	7.65E-01
120 h	150 °C	140 through 160	1.00E+00	1.00E+00
0 h	170 °C	160 through 180	2.45E+00	1.28E+00
8000 h	100 °C		7.16%	39.64%
		131 °C		





# What is an FMEDA



FMEDA calculates absolute:

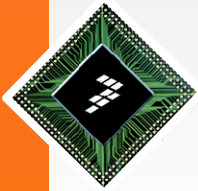
*Uncontrolled Failure per hour*

and relative values

*Controlled / Total Failure per hour*

various failure reaction

failure rate



# ISO 26262-5 (elements and failure models)

Table D.1 — Analyzed faults or failures modes in the derivation of diagnostic coverage

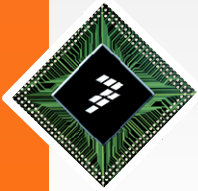
Element	See Tables	Analyzed failure modes for 60 %/90 %/99 % DC		
		Low (60 %)	Medium (90 %)	High (99 %)
<b>General semiconductor elements</b>				
Power supply	D.9	Under and over Voltage	Drift Under and over Voltage	Drift and oscillation Under and over Voltage Power spikes
Clock	D.10	Stuck-at <sup>a</sup>	d.c. fault model <sup>b</sup>	d.c. fault model <sup>b</sup> Incorrect frequency Period jitter
Non-volatile memory	D.5	Stuck-at <sup>a</sup> for data and addresses and control interface, lines and logic	d.c. fault model <sup>b</sup> for data and addresses (includes address lines within same block) and control interface, lines and logic	d.c. fault model <sup>b</sup> for data, addresses (includes address lines within same block) and control interface, lines and logic
Volatile memory	D.6	Stuck-at <sup>a</sup> for data, addresses and control interface, lines and logic	d.c. fault model <sup>b</sup> for data, addresses (includes address lines within same block and inability to write to cell) and control interface, lines and logic <b>Soft error model<sup>c</sup> for bit cells</b>	d.c. fault model <sup>b</sup> for data, addresses (includes address lines within same block and inability to write to cell) and control interface, lines and logic Soft error model <sup>c</sup> for bit cells
Digital I/O	D.7	Stuck-at <sup>a</sup> (including signal lines outside of the microcontroller)	d.c. fault model <sup>b</sup> (including signal lines outside of the microcontroller)	d.c. fault model <sup>b</sup> (including signal lines outside of the microcontroller) Drift and oscillation
Analogue I/O		Stuck-at <sup>a</sup> (including signal lines outside of the microcontroller)	d.c. fault model <sup>b</sup> (including signal lines outside of the microcontroller) Drift and oscillation	d.c. fault model <sup>b</sup> (including signal lines outside of the microcontroller) Drift and oscillation

FMEDA SRAM

Reference ISO 26262-5:2011





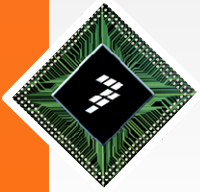


# ISO 26262-5 (elements and failure models)

Table D.1 — Analyzed faults or failures modes in the derivation of diagnostic coverage

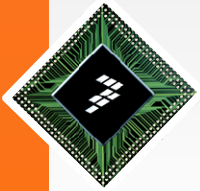
Element	See Tables	Analyzed failure modes for 60 %/90 %/99 % DC			
		Low (60 %)	Medium (90 %)	High (99 %)	
<i>Specific semiconductor elements</i>					
Processing units	ALU - Data Path	D.4/D.13	Stuck-at <sup>a</sup>	Stuck-at <sup>a</sup> at gate level d.c. fault model <sup>b</sup> Soft error model <sup>c</sup> (for sequential parts)	
	Registers (general purpose registers bank, DMA transfer registers...), internal RAM	D.4	Stuck-at <sup>a</sup>	Stuck-at <sup>a</sup> at gate level Soft error model <sup>c</sup> d.c. fault model <sup>b</sup> including no, wrong or multiple addressing of registers Soft error model <sup>c</sup>	
	Address calculation (Load/Store Unit, DMA addressing logic, memory and bus interfaces)	D.4/D.5/D.6	Stuck-at <sup>a</sup>	Stuck-at <sup>a</sup> at gate level Soft error model <sup>c</sup> (for sequential parts)	d.c. fault model <sup>b</sup> including no, wrong or multiple addressing Soft error model <sup>c</sup> (for sequential parts)
	Interrupt handling	D.4/D.10	Omission of or continuous interrupts	Omission of or continuous interrupts Incorrect interrupt executed	Omission of or continuous interrupts Incorrect interrupt executed Wrong priority Slow or interfered interrupt handling causing missed or delayed interrupts service
	Control logic (Sequencer, coding and execution logic including flag registers and stack control)	D.4/D.10	No code execution Execution too slow Stack overflow/underflow	Wrong coding or no execution Execution too slow Stack overflow/underflow	Wrong coding, wrong or no execution Execution out of order Execution too fast or too slow Stack overflow/underflow
	Configuration Registers	D.4	—	Stuck-at <sup>a</sup> wrong value	Corruption of registers (soft errors) Stuck-at <sup>a</sup> fault model
	Other sub-elements not belonging to previous classes	D.4/D.13	Stuck-at <sup>a</sup>	Stuck-at <sup>a</sup> at gate level	d.c. fault model <sup>b</sup> Soft error model <sup>c</sup> (for sequential part)

FMEDA  
Processing Unit



# Contents

- Functional Safety at Freescale
- Functional Safety and Microcontrollers
- MCU Safety Context and Safety Concepts
- FMEDA
- **Soft Errors**



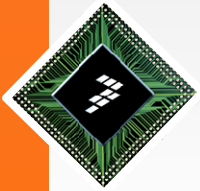
## How SER is measured?

JEDEC specifies SER test and analysis procedures in JESD89A

- System-level Tests
- Data in 1000 devices is monitored for > 1000 hours (2 months)
- Measure number of failures in 10<sup>6</sup> device-hours
- Used to scale accelerated results to field conditions

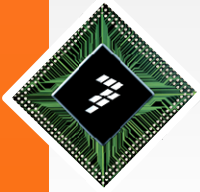
### Accelerated Tests

- Data in 2 to 10 devices exposed to an accelerated source is monitored for a few minutes
- Results are decelerated to operating conditions
- Tests require little time to collect substantial data (10<sup>8</sup> acceleration)
- JEDEC standards for converting to operating conditions
- Most SER characterization is performed with accelerated tests



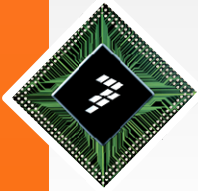
## Alpha Accelerated ( $\alpha$ ASER) Tests

- Freescale uses a  $^{232}\text{Th}$  Thorium foil to accelerate alpha particles
  - Th232 foil flux 3.2e6 alpha.cm2/hr.
- The active-side of the device must be exposed to the Thorium foil
  - Any Mold compound must be removed
  - Cannot perform  $\alpha$ ASER on lead-over-chip (e.g. bumped) devices
- Source-to-die spacing : <1mm
- Alpha source calibration : done periodically
- Type and number of devices tested : 4 die from 2 wafers
- Number of errors per unit time : typically < 5% of bit fails on 1Mb after 1min
  - No multiple events can flip fails back into a passing mode
- Noise : no errors in the DUT for the total test time when no source was present
- Latchup : no high-current behavior observed during the testing
- Package lid : removed, Polyimide : removed, if used

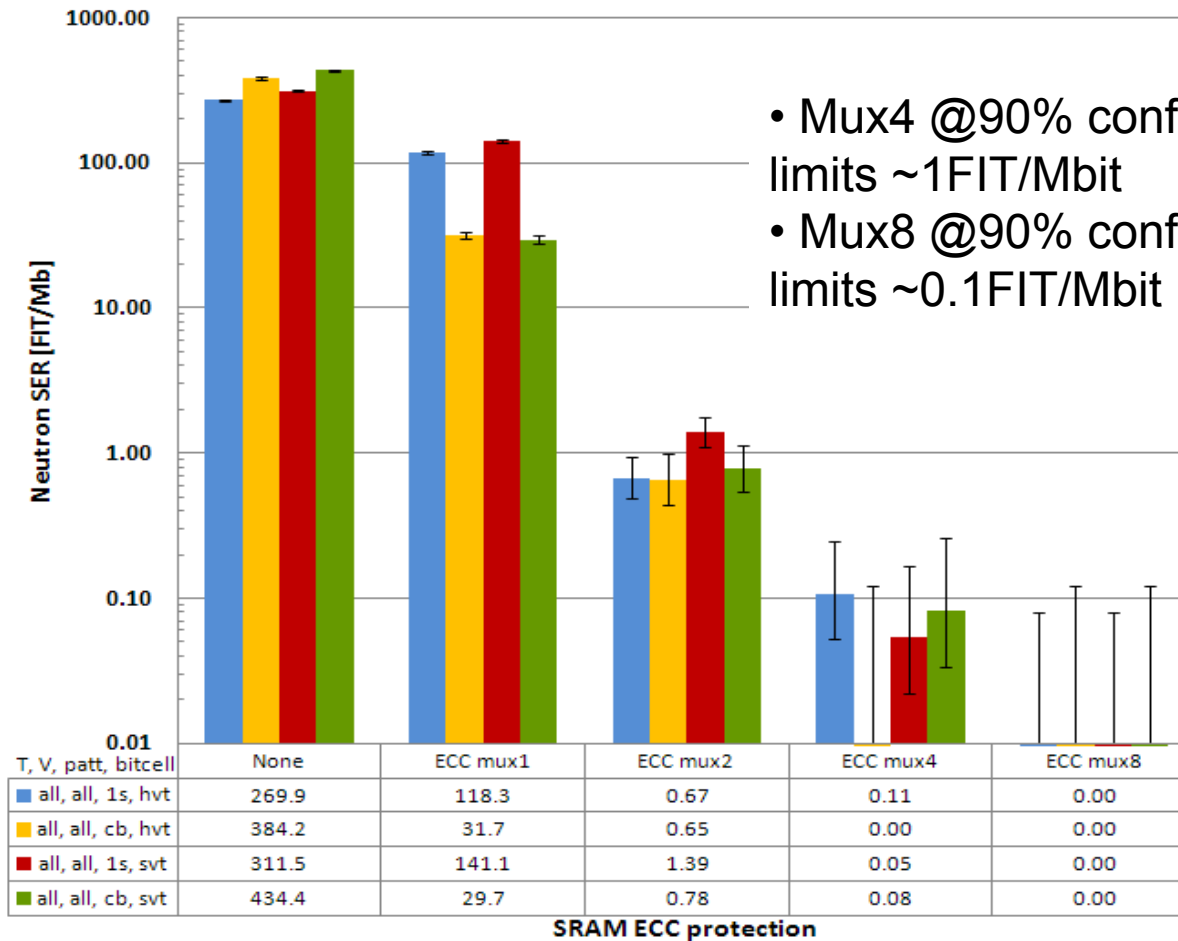


## Neutron Accelerated (nASER) Tests

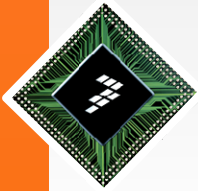
- Type of neutron source used : Los Alamos WNR or TRIUMF, broad energy spectrum.
- Beam fluence (flux\*testing\_time) : a minimum of 1E8 neutrons/cm<sup>2</sup> struck the DUT
- Beam divergence with distance : DUTs are located close to the beam output
- Neutron scattering in the parallel DUTs : avoided with a 30cm DUT-to-DUT spacing
- Type and number of devices tested : 4 dies from 2 wafers
- Number of errors per unit time : typically < 1% of bit fails on 1Mb after 1hour
  - No multiple events can flip fails back into a passing mode
- Noise : no errors in the DUT for the total test time when no source was present
- Latchup : no high-current behavior observed during the testing
- Multiple Bit Upset : checked at topology and system level
- nASER data is decelerated to NYC ground-level conditions.



# Example Results for nASER Showing ECC Effectiveness Against Multi-Bit Upsets



- Mux4 @90% confidence limits ~1FIT/Mbit
- Mux8 @90% confidence limits ~0.1FIT/Mbit



# Supporting Material for Functional Safety

- SafeAssure @ [www.freescale.com/SafeAssure](http://www.freescale.com/SafeAssure)
- Certification Package under NDA
- App-Notes, White Papers, Articles
- On-demand Training

Freescale | SafeAssure Functional Safety Program

## SafeAssure Functional Safety Program



As industry standards such as IEC 61508 and ISO 26262 require more sophisticated functional safety concepts, real-time control of safety-critical applications increases in complexity. The Freescale SafeAssure functional safety program is designed to help you simplify the process of achieving system compliance with functional safety standards in the automotive and industrial markets. Freescale's SafeAssure solutions reduce the time required to develop safety systems that comply with the International Standards Organization (ISO) 26262 and International Electrotechnical Commission (IEC) 61508 standard.

The Freescale SafeAssure program supports the most stringent Safety Integrity Levels (SILs) to help developers more easily attain system compliance. Whether your need is to attain ASIL-A to D or SIL-1 to 4 system compliance, the SafeAssure program identifies products that are targeted for use in the effective implementation of functional safety technologies.

### SafeAssure Program Features

- A breadth of Freescale technologies, including microcontrollers, analog and power management ICs and sensors.
- Hardware safety concepts that focus on detecting and mitigating random hardware failures, achieved through built-in safety features, including self-testing, monitoring and hardware-based redundancy.
- Software that seamlessly integrates with hardware to achieve system-level functional safety goals.
- Comprehensive support capabilities that extend from customer-specific training and system design reviews regarding functional safety architecture to extensive safety documentation and technical support.



### Freescale Approach to Functional Safety

To learn more about Freescale's unique approach to functional safety, click on the diagram above.

### SafeAssure Solutions

To guide you to the right solution for your design needs, look for the SafeAssure by Freescale mark. It designates products whose implementation of functional safety technologies is truly optimal and are fully enabled to facilitate system-level design and functional safety standard compliance, including support for failure analysis, hardware and software integration. Helping you achieve your system-level functional safety compliance – simply.

Live Chat Available

### Training & Events

#### On-Demand Training

- Addressing Safety Standard Requirements for IEC61508 (SIL3) and ISO26262 (ASIL-D) with the Qorivva MPC5843L

#### Read More

- Functional Safety Overview
- Addressing the challenges of Functional Safety in the Automotive and Industrial Markets — White Paper

#### Connect With Us



White Paper

## Addressing the Challenges of Functional Safety in the Automotive and Industrial Markets



www.freescale.com/SafeAssure



