Tools for Thermal Analysis: *Thermal Test Chips*

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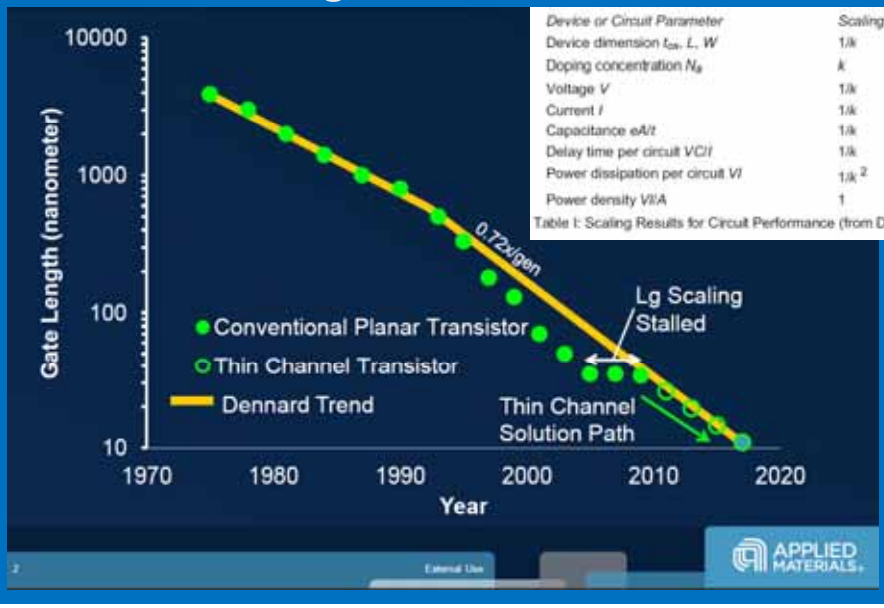
Introduction

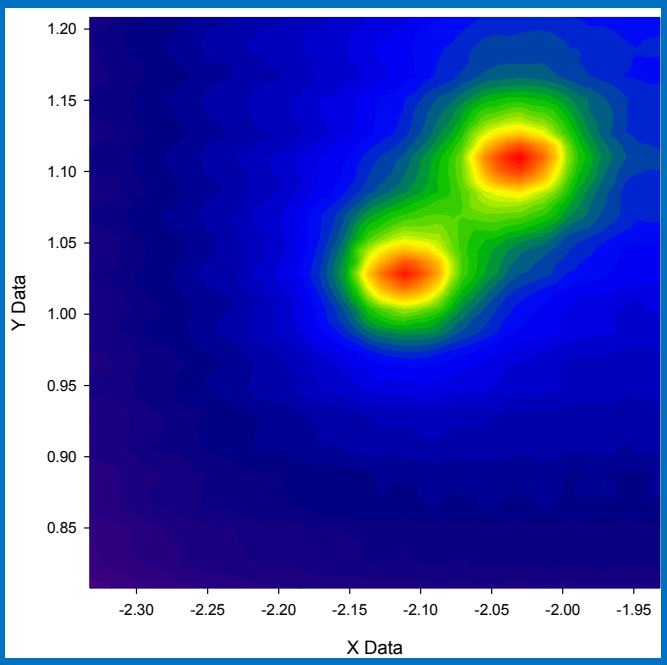
- Most products today need some knowledge of the cooling solution, often before the device or system is complete
- Many times prior to having working silicon or complete system information the thermal components must be identified, procured and evaluated
- Estimations based on experience, models, supplier input, data sheets, etc. guide the design team to the most cost-effective solution
- With decreasing gate length and pitch, many more functions can be placed in smaller regions, creating hot spots and temperature gradients

Device Scaling Trend



Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/k$
Doping concentration N_a	k
Voltage V	$1/k$
Current I	$1/k$
Capacitance eA/t	$1/k$
Delay time per circuit VC/I	$1/k$
Power dissipation per circuit VI	$1/k^2$
Power density VI/A	1

Table I: Scaling Results for Circuit Performance (from Dennard)



T_{JMAX}

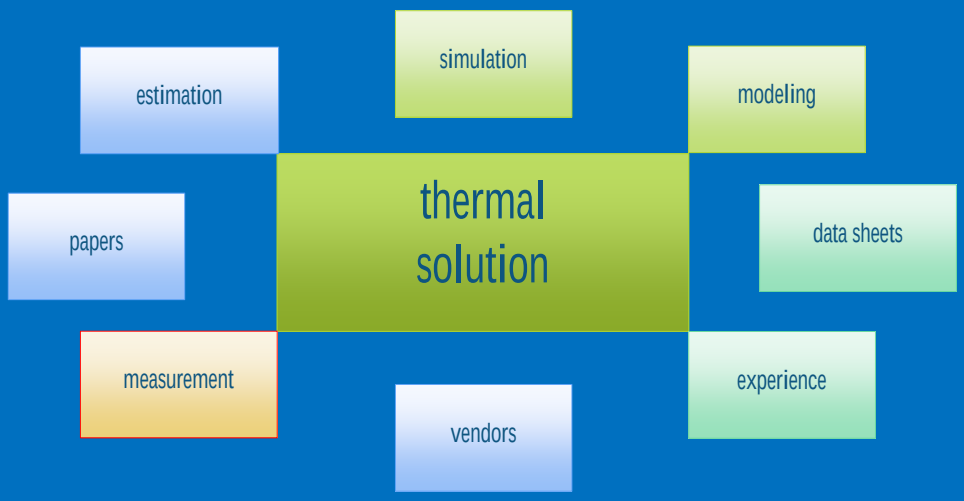
T_{JAVG}

Location

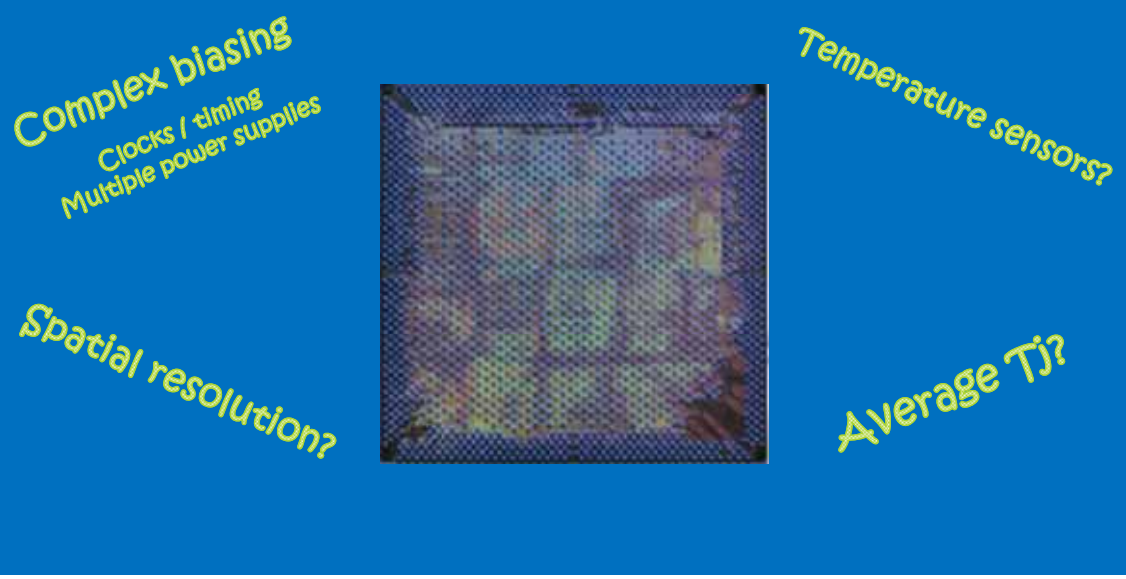
How hot is it?
How hot will it get?
Is the cooling solution adequate?
How do I measure it?

Thermal Toolbox

NOTES



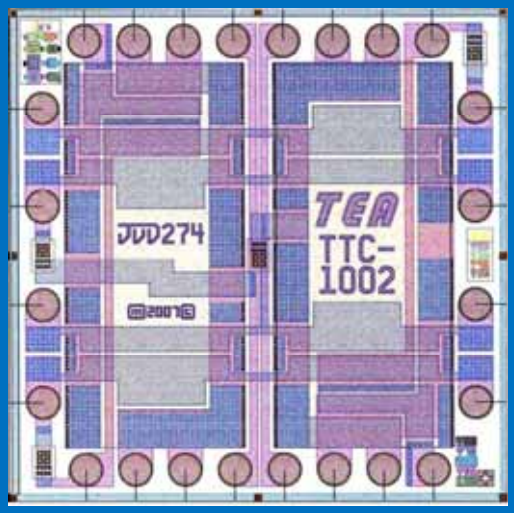
Measurement (live die)

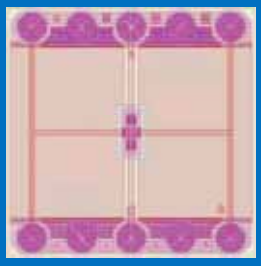


Thermal Test Chip (TTC)

2.5mm and 1mm unit cell

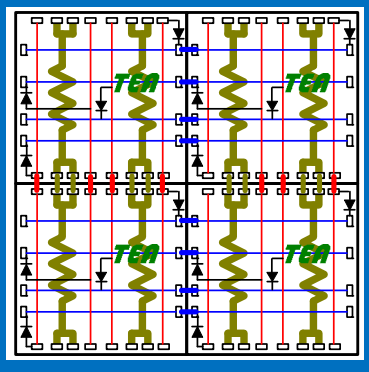
- Heating Resistors
- Temperature Sensors
- Arrayable
- Addressable
- 50um – 625um thick
- Any backside metallization



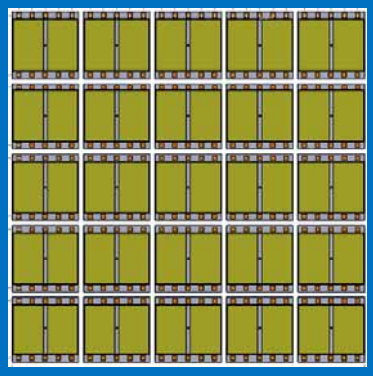


- Wirebond – Flip-chip
- Ease of use
- High power density

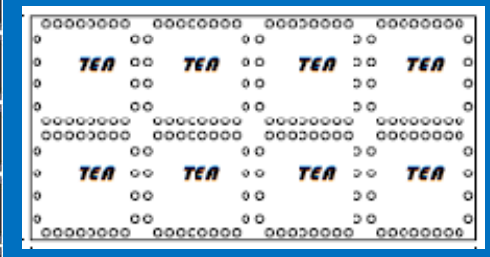
Array Example



2.5mm unit cell
2x2 array



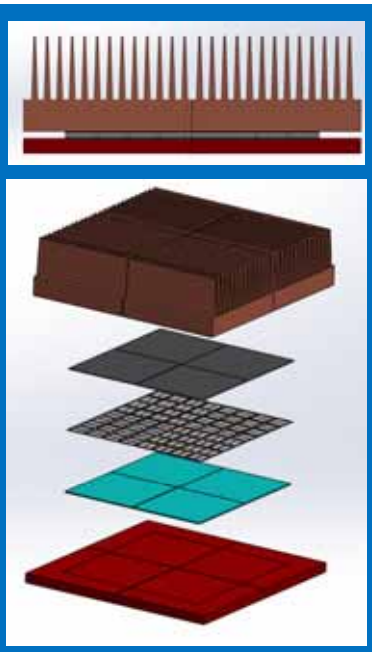
1mm unit cell
5x5 array



2.5mm unit cell
4x2 array

Test Chip Study

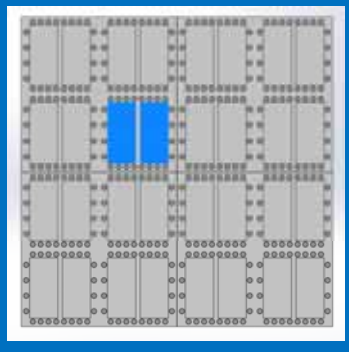
- Thermal models are generated to illustrate an application of an array of unit cells
- Meant to simulate a typical flip-chip attached microprocessor or ASIC chip on a package
- Shows the capability to produce hot spots and the versatility of a typical array
- Quarter symmetry



Full Assembly

¼ of Modeled Array

64 discrete locations
256 sensors



4x4 Array TTC-1002

400 discrete locations
400 sensors

10x10 Array TTC-1001

Table 1. Model components

Component	*Geometry*	*Description*
Chip array	20.32mm, square	8x8 (1002), 20x20 (1001)
Bump	24x165um bumps per unit cell	100um standoff height, underfill
TIM	20.32mm x 0.1mm	Between chip backside and heat sink
Heat sink	27mm, 2.54mm base, 5mm fin	Cu, 1mm pitch
Substrate	27mm x .5mm	BGA package

Table 2. Power Density (PD) $T_J \leq 125°C$

Parameter	*2.5mm*	*1mm*	*Unit*
I_{IM}	0.89	0.55	A
R	7.5	10	Ω
Pd (per R)	5.9	3.0	W
Area (min)	0.018	0.00606	cm^2
PD_{MAX}	330	499	W/cm^2

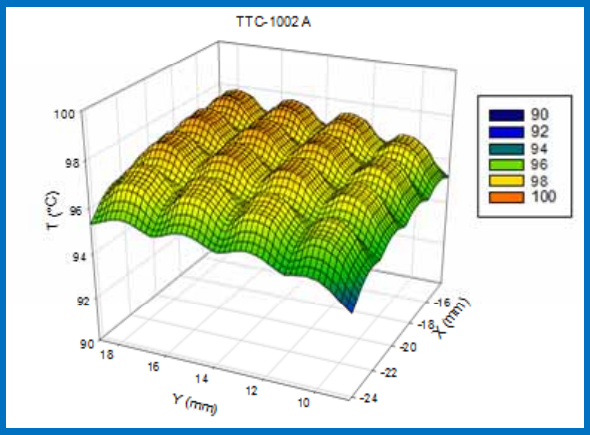
Table 3. Power Mapping (20mm square die size)

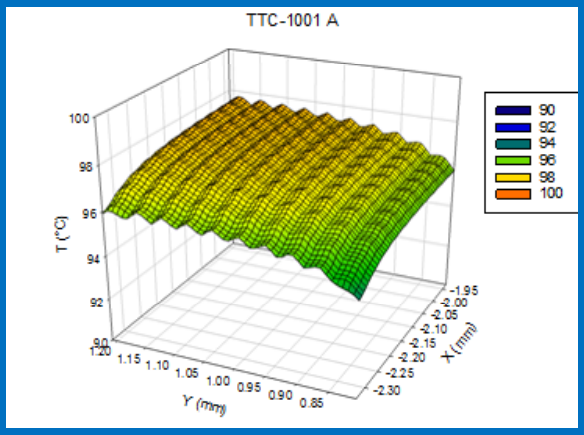
Cell Size	*No. Resistor*	*Pd/ Cell*	*Pd/ Hotspot**	*No. Hotspot*	*Pd Total*
2.5mm	128	0.5		0	64
2.5mm	127	0.5	5	1	68.5
2.5mm	127	0.5	5	2	73.5
1mm	800	0.08		0	64
1mm	798	0.08	1.66	1	65.5
1mm	796	0.08	1.66	2	67
*Power density is equivalent for both chip sizes					

Table 4. Power Calculations, smallest area in cell

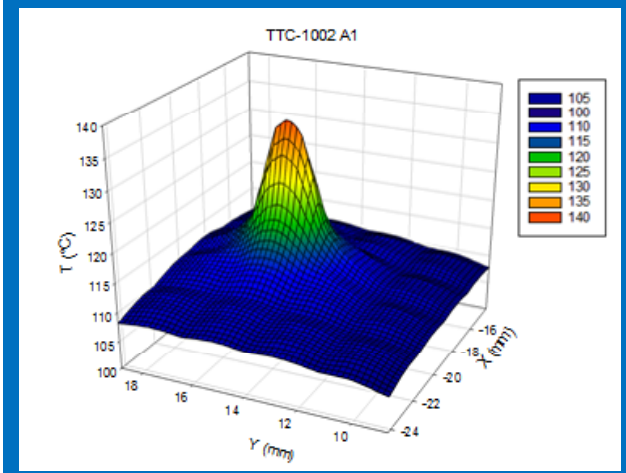
Cell Size	*Cell R Area (cm^2)*	*Pd/ R (W)*	*PD (W/cm^2)*	*Cell R Dim (mm)*
2.5mm	0.0182513	0.5	27.39525	1.986 x .919
1mm	0.0060613	0.08	13.19845	.678 x .447 (2)
2.5mm	0.0182513	5	273.9525	1.986 x .919
1mm	0.0060613	1.660	273.8677	.687 x .447 (2)

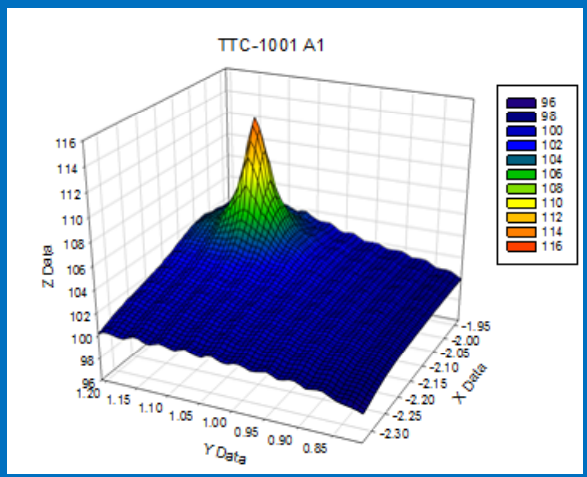
Uniform Power Density



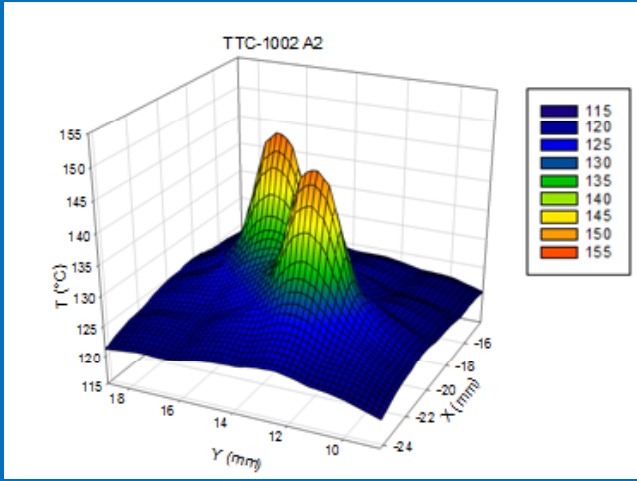


One Hot Spot





Two Hot Spots



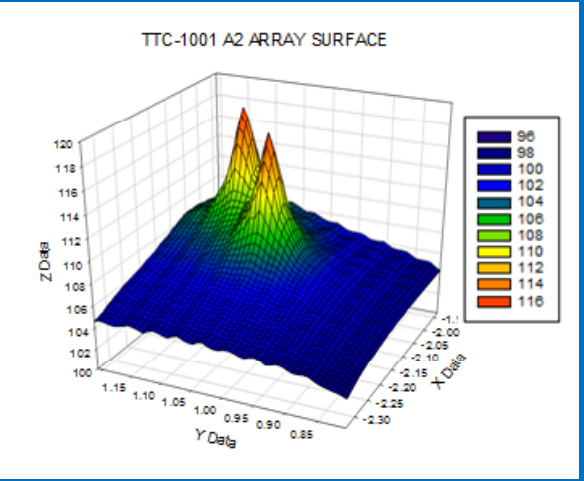


Table 5. Min, Max, Average Array Model Results

Tjmin	*2.5mm*	*ΔT*	*1mm*	*ΔT*
uniform	93.75	---	94.36	---
1 hot spot	105.9	12.15	98.4	4.04
2 hot spot	119.7	25.95	102.6	8.24
Tjmax	*2.5mm*	*ΔT*	*1mm*	*ΔT*
uniform	98.1	---	97.7	---
1 hot spot	135.8	37.7	114	16.3
2 hot spot	150	51.9	119.2	21.5
Tjavg	*2.5mm*	*ΔT*	*1mm*	*ΔT*
uniform	95.925	---	96.03	---
1 hot spot	120.85	24.925	106.2	10.17
2 hot spot	134.85	38.925	110.9	14.87

Model Summary

- Shows versatility of test chip for evaluating thermal behavior
- Can create hot spots, sections with varied power dissipation
- Very high power density, allows simulation of extreme chips
- Can array into any size, up to ~100mm square

Why Use Test Chips?

- EASE OF USE
- ACCURACY
- ARRAYABLE – ADDRESSABLE - VERSATILE
- LOOK AHEAD
- STACKED, MCM, 2.5 or 3D packaging
- Reduces Time-to-Market
- COOLING SOLUTION AT THE RIGHT TIME, RIGHT COST

THANK YOU!

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- Precision Materials to Meet Scaling Challenges Beyond 14nm, Semicon 2013, Adam Brand, SSG Transistor Technology Group, Applied Materials
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