Tools for Thermal Analysis: Thermal Test Chips

Thomas Tarter
Package Science Services LLC
ttarter@pkgscience.com

INTRODUCTION

Irrespective of if a device gets smaller, larger, hotter or cooler, some method is needed to determine the thermal behavior of a given chip/package/heatsink configuration. This is typically achieved by a combination of models and measurements and is useful in guiding the design team to the most cost-effective and reliable package and cooling solution. Most production chips have few or no available connections for temperature sensing and require complex biasing schemes and clock signals to achieve maximum power dissipation. Although some live devices may be evaluated for thermal performance only the average junction temperature is reported and there is no indication of the spatial location of the temperature measurement. As we shrink feature size and combine more functions onto a given chip the problem of temperature distribution becomes critical. Now, and as we move into more integrated chip functionality, temperature gradients and 'hot spots' must be considered to evaluate thermal performance and reliability. Another scenario that is difficult or impossible using live die is to determine the junction temperature of chips in various locations in a multi-chip application. In stacked, SiP, 2.5 and 3D packaging the problem also includes measuring temperatures across the stack or array of chips.

These factors, among others, can make using production die for thermal test expensive, inconclusive, or impossible.

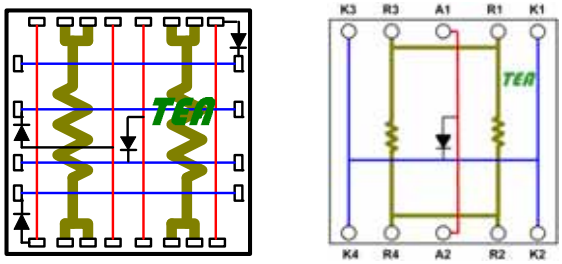
The alternative is to use specially designed thermal test chips. These chips make available power dissipating elements and temperature sensors in unit-cells, arrayable into various die sizes. Sensors are addressable for each unit-cell on the array and resistor elements may be combined in various circuit configurations to allow power variation anywhere in the array. Very high power density can be achieved in these die, limited only by interconnect current density and maximum temperature. Power supply and sensor reading does not require switching and allows simple connection and data collection. This chip set is a valuable tool in the modern design arsenal.

Nomenclature

T_J	junction temperature
T_{JMAX}	maximum junction temperature
T_A	ambient temperature, °C
P_d	power dissipation, W
P_D	power density, W/cm^2
k	thermal conductivity, W/m-K
h	convection heat transfer coefficient, W/m^2-K
WB	wire bond
FC	flip-chip
TTC	thermal test chip
I_M	measurement current, A
I_{IM}	maximum interconnect current
V_M	measurement voltage, V
I_H	heating current, A
V_H	heating voltage, V
BGA	ball-grid-array
PCB	printed circuit board
TTB	thermal test board

Thermal Test Chip Study

The study described here uses specialized test chips developed and manufactured by Thermal Engineering Associates. The chips are available in two unit cell sizes of 2.54mm x 2.54mm and 1mm x 1mm. Schematic representations of the 2.5mm and 1mm chips are shown in Fig. 1. Each 2.5mm unit cell has two metal film resistors for heat flux generation and four PN Junction diodes for temperature sensing. The 1mm unit cell includes two resistors and one temperature sensor. Larger die sizes can be created by selective sawing to square or rectangular patterns in unit cell increments. Fig. 2 shows an example of a 2x2 array with electrical connections. The test chips are available in either wire-bond (WB) or flip-chip (FC) versions.



1002 Schematic 1001 Schematic

Figure 1.Thermal Test Chip

Thermal Test Chip Features

Arrays of unit cells may be generated to simulate various die sizes. If wirebonding is used as the interconnect method, resistors are available in series strings across the array as shown in Fig. 2, a 2x2 array of the 2.5mm unit cell. Resistor and diode connections are at the periphery of the array. In this configuration, strings of resistors can be arranged in series or parallel combinations to achieve a reasonable voltage and current for heating power

dissipation. The diode temperature sensors are arranged in a matrix format making every diode sensor on every cell in the array accessible from the periphery of the array. When using flip-chip interconnects the resistors and temperature sensors are available from each unit cell individually, allowing discrete programming of power density and temperature measurement in each cell.

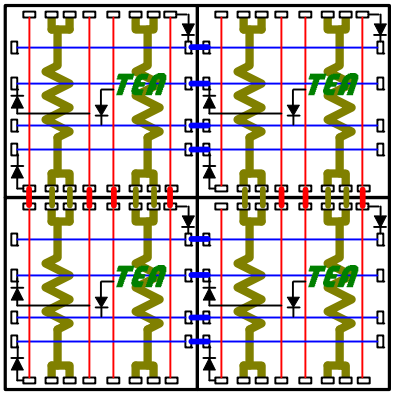


Figure 2. 2x2 TTC Array

Models

Thermal models are developed to illustrate an application of an array of unit cells. The application is meant to simulate a typical flip-chip attached microprocessor or ASIC chip on a package. Models are simplified to allow efficient meshing and solution. Quarter symmetry is used in the solution to reduce computational time and memory use. The model includes the chip, solderbump and underfill, package substrate, thermal interface material (TIM) on the back of the chip and a finned Cu heatsink. Table 1 lists the components with dimensions and description. Heat removal is provided by forced-air across the heatsink fins and package body with a bulk temperature of 26°C. A constant temperature of 50°C is imposed on the bottom of the substrate to simulate the mounting surface temperature. Fig. 4 shows the model solids.

Table 1. Model components

Component	*Geometry*	*Description*
Chip array	20.32mm, square	8x8 (1002), 20x20 (1001)
Bump	24x165um bumps per unit cell	100um standoff height, underfill
TIM	20.32mm x 0.1mm	Between chip backside and heat sink
Heat sink	27mm, 2.54mm base, 5mm fin	Cu, 1mm pitch
Substrate	27mm x .5mm	BGA package

Cell Model Detail

Fig. 5 shows the quarter symmetry die model for the study using a 4x4 array of the 2.5mm unit cell. Highlighted areas shown are the heating resistors. There are two areas

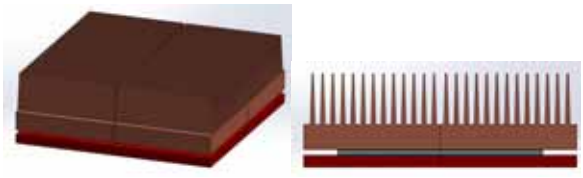


Figure 4. Model Solids

per unit cell which can be assigned heating power individually. In the case of an 8x8 array (~20mm square die size), there are 64 unit cells with 128 individual resistors and 512 temperature sensors. The individual resistors allow an opportunity to simulate uneven power dissipation and hot spots in the array. Sensors allow temperature mapping across the entire array. The use of diodes for temperature sensors provides very accurate sensing local to the heating resistors. The diodes can be calibrated to provide resolution better than 0.1°C.

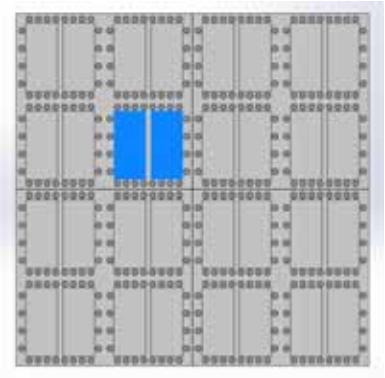


Figure 5. Resistor and Bump locations
4x4 array, 2.5mm unit cell

Fig. 6 shows a similar size model using a 10x10 array of the 1mm unit cell. For a ~20mm square die size there are 400 unit cells with a total of 800 resistors and 400 temperature sensors. The 10x10 array of the 1mm cells shown is one quarter of the total modeled die size. For the 1mm cell there are two resistors connected in parallel

Figure 6. Resistor and Bump locations
10x10 array,1mm unit cell

Power Density
Power dissipation in each cell is limited by two factors:

1. Maximum interconnect current (I_{IM})
2. Maximum chip temperature (T_{JMAX})

Maximum interconnect current is limited to 0.89A for the 2.5mm cell and 0.55A for the 1mm cell. For the 2.5mm unit cell the maximum power density is greater than 300 W/cm^2. For the 1mm cell the maximum power density is nearly 500W/cm^2. Both of these statements are true if T_{JMAX} is controlled to ≤125°C. Table 2 lists power density limits.

Table 2. Power Density (PD) T_J ≤125°C

Parameter	*2.5mm*	*1mm*	*Unit*
I_{IM}	0.89	0.55	A
R	7.5	10	Ω
Pd (per R)	5.9	3.0	W
Area (min)	0.018	0.00606	cm^2
PD_{MAX}	330	499	W/cm^2

Model Studies
To illustrate the versatility of the thermal test chip, models are solved for three primary cases for both 2.5mm and 1mm unit cells in a 20mm square overall die size:

1. Power dissipation distributed equally across the array
2. A single minimum area hot spot
3. Two minimum area hot spots

Because the number of cells and resistor areas differ, power is adjusted in each array to generate equivalent total power dissipation. A power dissipation of 0.5W is applied in each of the resistor areas in the 2.5mm cells. This gives a total of 64W for the 20mm simulated die. To match the power dissipation, 1mm cell resistor areas are set to dissipate .08W. Table 3 shows the resistor count, power per resistor and hot spot power for each model run.

Table 3. Power Mapping (20mm square die size)

Cell Size	*No. Resistor*	*Pd/ Cell*	*Pd/ Hotspot**	*No. Hotspot*	*Pd Total*
2.5mm	128	0.5		0	64
2.5mm	127	0.5	5	1	68.5
2.5mm	127	0.5	5	2	73.5
1mm	800	0.08		0	64
1mm	798	0.08	1.66	1	65.5
1mm	796	0.08	1.66	2	67
*Power density is equivalent for both chip sizes					

Total power dissipation diverges when hot spots are added due to dissimilar areas and the desire to keep the power density in the resistors equivalent for both cell sizes. The hot spot(s) are defined to have similar *power density* on the 2.5mm and 1mm arrays. A value of 10 times the uniform power is assigned arbitrarily. For the 2.5mm cell the power is assigned to one resistor area. This results in a power density of ~274 W/cm^2. To match this value in the 1mm cell, 1.6W is assigned to the two-resistor set (0.8W each). Because the two cells are interconnected at the die-level metal on the 1mm cell the smallest accessible area for heating is ~.678mm x .89mm.

Table 4. Power Calculations, smallest area in cell

Cell Size	*Cell R Area (cm^2)*	*Pd/ R (W)*	*PD (W/cm^2)*	*Cell R Dim (mm)*
2.5mm	0.0182513	0.5	27.39525	1.986 x .919
1mm	0.0060613	0.08	13.19845	.678 x .447 (2)
2.5mm	0.0182513	5	273.9525	1.986 x .919
1mm	0.0060613	1.660	273.8677	.687 x .447 (2)

Model Results
Quarter-symmetry finite-element models are solved for steady-state thermal behavior using standard material properties for the components. Mesh density is optimized to capture thin layers.

2.5mm (TTC-1002) Array Results
Fig. 7 shows the results for uniformly distributed power dissipation of 0.5W per resistor. The maximum temperature result is 98.1°C. This shows that the heat sink and forced air condition is sufficient to maintain the die temperature below 100°C. One hot spot is introduced in Fig. 8. increasing T_{JMAX} to over 135°C. Fig. 9 shows the result of adding two hot spots to the 2.5mm array; T_{JMAX} rises to 150°C. Note that the addition of the hot spots also causes the minimum chip temperature to rise. In Figs. 7-12, the center of the die is in the far corner of the plot.

1mm (TTC-1001) Array Results
The results for the 1mm cell array are shown in Figs. 10-12. Fig. 10 shows the uniformly heated array. The maximum temperature reported is 97.7°C. Fig. 11 shows the addition of one hot spot and results in a Tjmax of 114°C. As follows, Fig. 12 shows the result of the addition of two hot spots with a maximum temperature of 119.2°C.

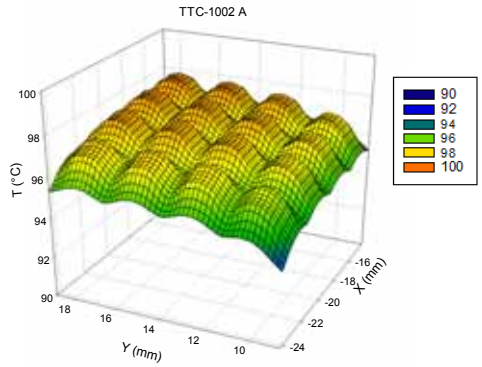


Figure 7. 2.5mm, uniform power distribution

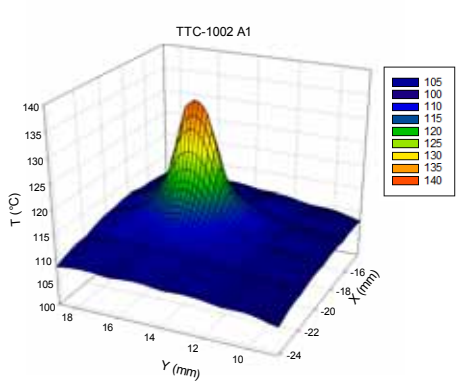


Figure 8. 2.5mm array with one hot spot

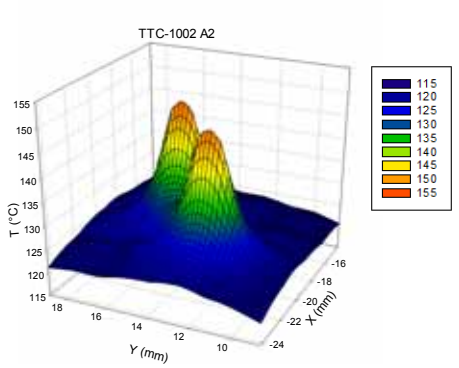


Figure 9. 2.5mm array with two hot spots

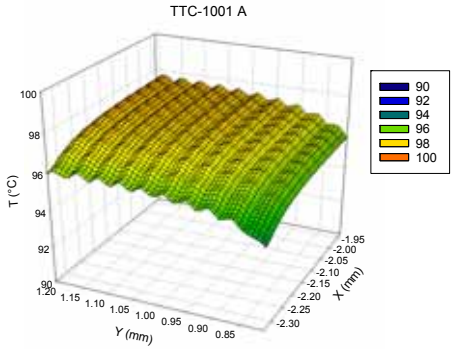


Figure 10. 1mm, uniform power distribution

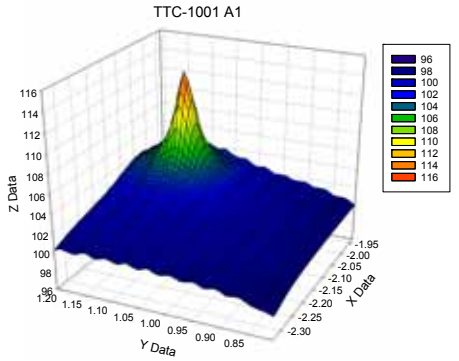


Figure 11. 1mm array with one hot spot

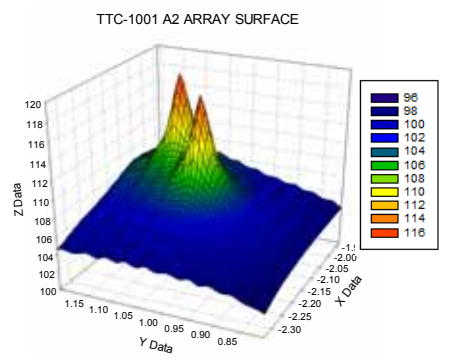


Figure 12. 1mm array with two hot spots

The results show that variations in power density can cause high local temperatures with heat sinks designed to maintain average temperatures. When using live devices for thermal measurements the average temperature is reported and peak temperatures may not be captured affecting the cooling solution design. Table 5 lists the minimum, maximum and average array temperatures, and the change in temperature due to the addition of hot spots. It can be seen from the result data that average temperatures collected from live die may underestimate peak temperatures by tens of degrees.

Table 5. Min, Max, Average Array Model Results

Tjmin	*2.5mm*	*ΔT*	*1mm*	*ΔT*
uniform	93.75	---	94.36	---
1 hot spot	105.9	12.15	98.4	4.04
2 hot spot	119.7	25.95	102.6	8.24
Tjmax	*2.5mm*	*ΔT*	*1mm*	*ΔT*
uniform	98.1	---	97.7	---
1 hot spot	135.8	37.7	114	16.3
2 hot spot	150	51.9	119.2	21.5
Tjavg	*2.5mm*	*ΔT*	*1mm*	*ΔT*
uniform	95.925	---	96.03	---
1 hot spot	120.85	24.925	106.2	10.17
2 hot spot	134.85	38.925	110.9	14.87

CONCLUSION

The use of specialized thermal test chips is a convenient and efficient approach for developing package and cooling solutions. Thermal test chips, as compared to live device measurements, provide measurement accuracy and the ability to simulate high power density areas. The arrayable cell configurations are capable of small to large die sizes. Measurement data acquisition is simplified allowing the use of standard lab equipment for powering the resistors and sensing temperatures. No specialized switching equipment is required, reducing the cost for thermal test. The thermal test chip is also suited for advanced development of stacked, 2.5 and 3D packaging and in some cases is the only way temperatures can be

detected in a stacked or 3D configuration. A model study is underway using a TSV stacked chip application using 2.5mm and 1mm cell arrays.

Acknowledgements
The author wishes to acknowledge Mr. Bernie Siegal of Thermal Engineering Associates, Inc. for information on the thermal test chips and related support.

References

1. B. Siegal, J. Galloway, "Thermal Test Chip Design and Performance Considerations", 24th Annual SEMI-THERM Symposium, 2008.
2. EIA/JEDEC Standard JESD15 Methodology for the Thermal Measurement of Component Packages, Standards JESD51-1, 51-2, 51-3, 51-4 and 51-5, Electronic Industries Association, JC15 committee, 1995.
3. B. Siegal, An Introduction to Diode Thermal Measurements, TEA Handbook, Thermal Engineering Associates, 2009.
4. "Ball Grid Array Technology", J. H. Lau, Editor, Mcgraw-hill, Inc. 1995, ISBN 0-07-036608-X
5. K. Matsumoto, S. Ibaraki, K. Sueoka, K. Sakuma, H. Kikuchi, Y. Orii and F. Yamada, "Experimental Thermal Resistance Evaluation of a Three-Dimensional (3D) Chip Stack, 28th IEEE SEMI-THERM Symposium on Thermal Management, March 2011.
6. K. Matsumoto; K. Sakuma; F. Yamada; Y. Taira, "Investigation of the thermal resistance of a three-dimensional (3D) chip stack from the thermal resistance measurement and modeling of a single-stacked-chip", International Conference on Electronics Packaging, p.478, 2008.
7. T.-Y. Chiang; K. Banerjee; K. C. Saraswat,. "Analytical thermal model for multilevel VLSI interconnects incorporating via effect", IEEE ELECTRON DEVICE LETTERS, vol.23, p.31, 2002.
8. B. Zhan, "Evaluation of Simplified and Complex Thermal Fnite Element Models for a 3-die Stacked Chip Scale Ball Grid Array Package", 29th IEEE/CPMT/SEMI International Electronics Manufacturing Technology symposium, July, 2004.
9. Z. Celik, "Thermal Characterization of Various 2.5 and 3D Package Configurations for Logic and Memory Applications", MEPTEC 2.5D, 3D and Beyond: Bringing 3D Integration to the Packaging Mainstream seminar, MEPTEC/SEMI, November, 2011.
10. M. Janicki, A. Napieralski, J. H. Collet and A. Louri, "Hot Spots and Core-Core Thermal Coupling in Future Multicore Architectures", 26th Annual IEEE SEMI-THERM Symposium, March 2010.
11. T. Tarter, "Design of High Density & 3D Packaging: Tools and Knowledge", Presentation at IEEE/CPMT Technical Meeting, September 2010.
12. Thermal Engineering Associates, Inc. Technical Briefs, www.thermengr.net/TechBrief/.

For more information on thermal test chips browse to:

www.thermengr.net