EoPlex™

A Member of ASTI

Configurable Sintered Interconnect (CSI™) for Semiconductor Packaging

EoPlex

About EoPlex

- Headquartered in San Jose, CA
- Subsidiary of ASTI since 2012
  - 14 factories, 4 R&D centers located in 8 countries
  - 2,300 employees world wide
- Production Facilities in Penang
- Expanding Manufacturing Capability in Cavite, Philippines - Q3 2015
- Creator of 3D High Volume Print Forming process (HVPF™) for multi material 3D printing

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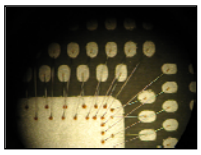
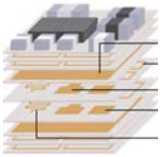
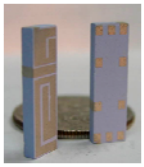
3D HVPF™Product Areas

Semiconductor Packaging Configurable Sintered Interconnect (CSI™)

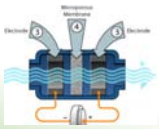


Internet of Things: Micro Antenna

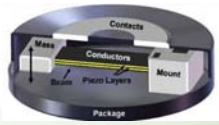




Fluidics



Energy Harvesters



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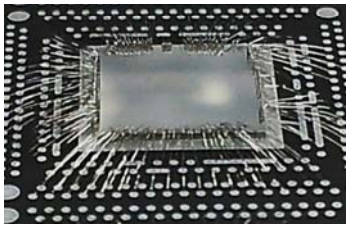
CSI™ Vehicle for Packages with Lead Counts from 2 to 500 +

01005 (.4mm X .2mm), 2 lead

12mm X 12mm, 224 Leads, 437 wires



CSI™ QFN replaced 4 layer BGA

CSI™ Package Benefits

- ✓ Wide lead count range
- ✓ Min. metal = higher performance
- ✓ Improved thermals
- ✓ Finished package to ≤ 250µ thin
- ✓ Design flexibility

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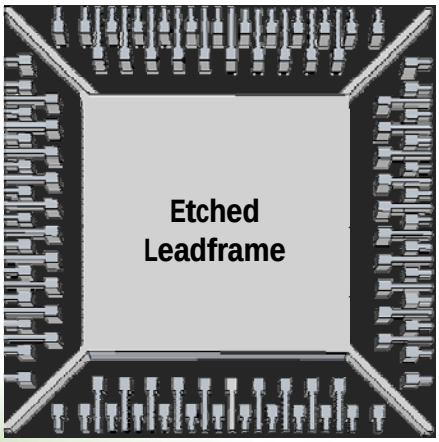
CSI™ Eliminates Tie Bars
Package Shrinks, Electricals Improve



Allows for more complex interconnect

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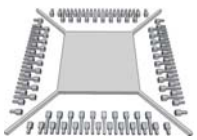
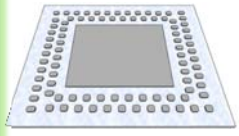
CSI™ - Array of Package Components on a Temporary Carrier

Std Lead Frame

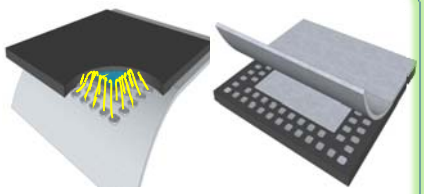


Tie bars stay with finished package: poor signal integrity

CSI™ LeadCarrier



CSI™ : leads on temporary carrier



Carrier removed leaving only metal for interconnect

The carrier provides needed mechanical properties, Leads are only as thick as required – nominally 40µ

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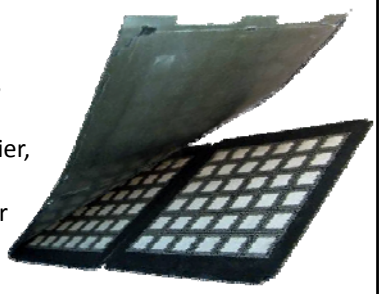
Temporary Carrier Improves the Process and the Product

- A Better Process
  - Steel carrier is cheap and robust
  - The carrier eliminated the need for tape
  - Displacement of leads in any direction is virtually eliminated
  - All pads are securely bonded to the carrier, eliminating deflash
  - Pads are electrically isolated after carrier removal allowing for test in strip form
  - Singulation requires cutting only EMC
- A Better Product
  - Thinnest possible pads (40µ) means thinnest possible package (<250µ)
  - Residual tie bars are eliminated
  - Greatly expand design freedom



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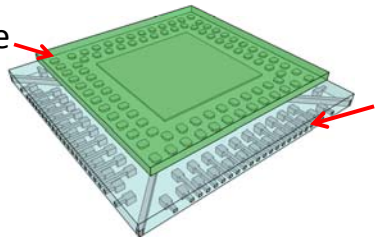
CSI™ Based Packages Have Smaller Footprints and Less Volume/Mass

88 lead package based on CSI™



88 lead package based leadframe

- This CSI™ based package example has:
  - 23% smaller footprint
  - 50% less volume
  - 66% less mass

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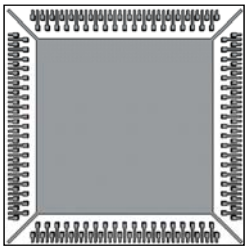
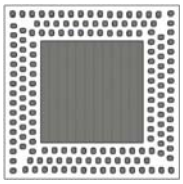
CSI™ is Even More Efficient with More Than Two Rows

156 ld. Leadframe
9 mm DAP





160 ld. CSI™
5.25 mm DAP

- Most die don't need the DAP size available in dual row QFN
- With three row CSI™:
  - 44% smaller footprint than with dual row leadframe
  - 130% more package sites per 70mm x 250mm strip
  - Average wire bond length is at least 2mm shorter

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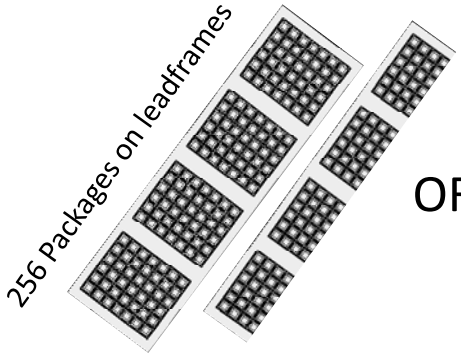
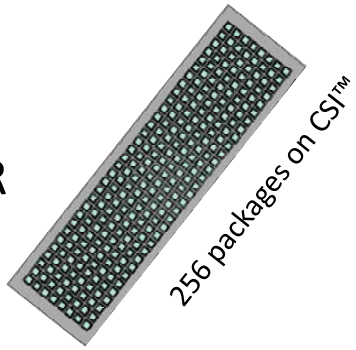
More Efficient Use of Strip Space Lower Cost Per Package Site



OR



CSI™ strip allows 52% more leadframes

Based on 88 lead package sites on 70mm X 250mm strips

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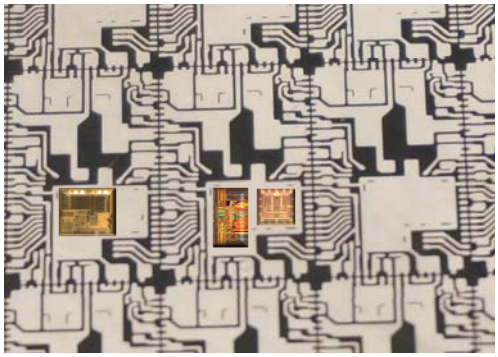
Previously Impossible Design Options On a Single layer

- Multiple rows
- Multiple DAPs
- Floating structures
- More than 500 leads
- 300µ bond pad pitch
- 200µ interconnect pitch
- Wettable flank for solder inspection



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CSI™ Addresses Mobility Market Smaller, Thinner Form Factor

QFP: Big Footprint | Very Thick | Poor Electrical

BGA: Big Footprint | Thick | Poor Electrical

fBGA: Thick | Poor Electrical | Expensive

DCA: Limited Applicability | Special Board Requirements

250 microns thin

CSI™

2 to 500+ leads

300 microns solder pad pitch

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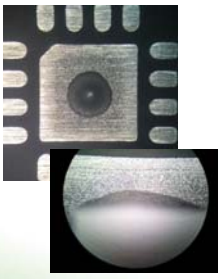
CSI is Fully Compatible with Standard QFN Infrastructure

No Etching or plating required

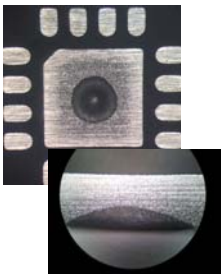
Uses Standard Die Attach Materials

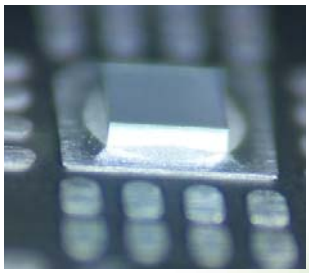
Excellent Die attach performance,
strong adhesion of die to silver bond pad

0 hrs



3 hrs staging





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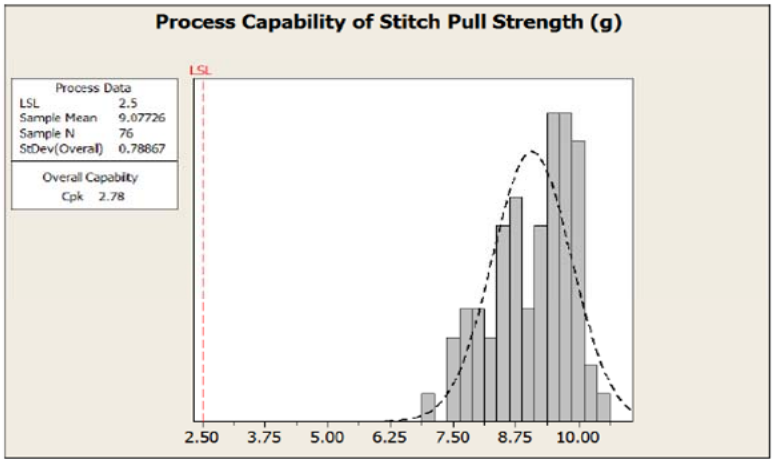
Highly Compatible with Cu & Au wire bonding

Stitch pull histogram for 0.8 mil Cu Wire



More than 70% breaking mode at wire span after stitch pull test.

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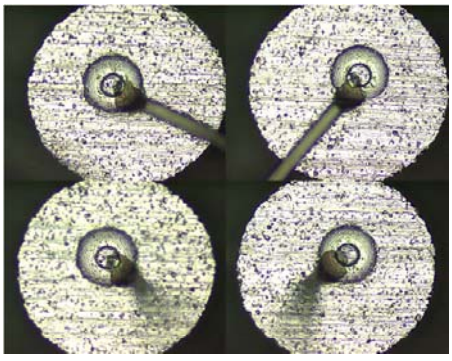
Cu Wire Bonding

0.8mil Pd Coated Cu Wire



Cu stitch bonds on thick Ag look different, but are strong and reliable with more than 70% breaking in the wire span.

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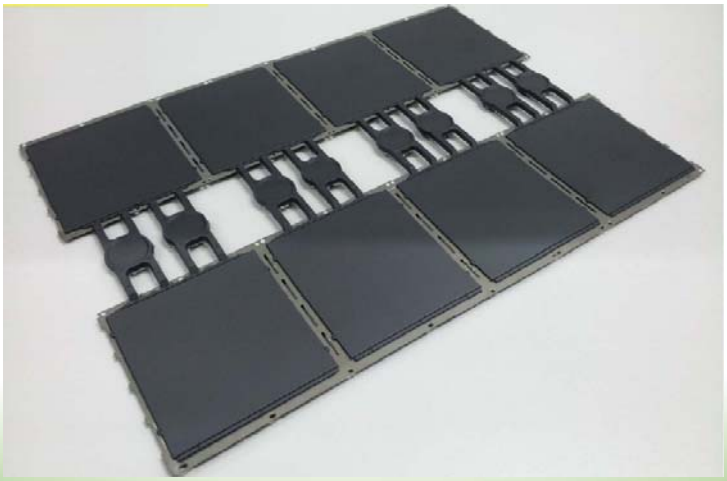
Works with Standard QFN Molding Materials and Process



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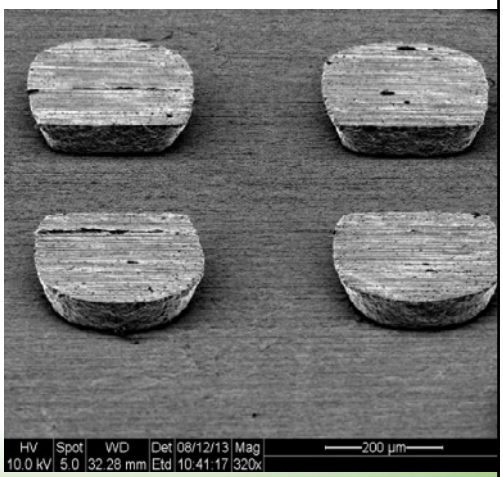
Pad Shape Provides Lock-in Feature and Surface Texture Improves MSL Performance

- Surface roughness of sintered silver improves adhesion
  - Die Pad Avg : 0.87um
  - Bond Pad Avg : 0.45um
- Conical frustum shaped pads
  - Excellent locking of Leads with mold compound



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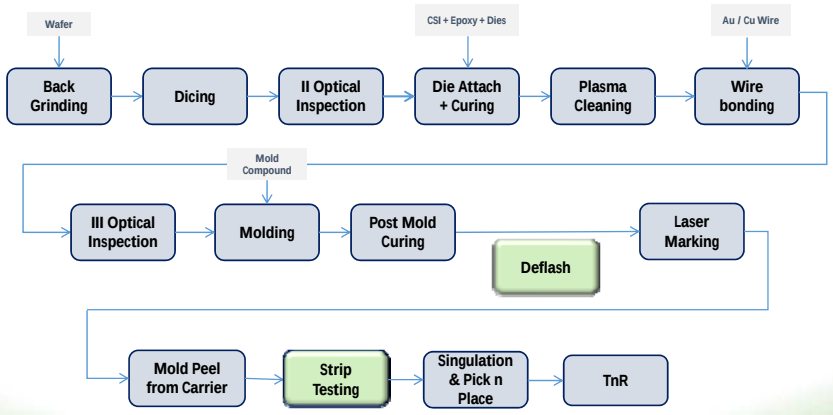
CSI™ - Standard Process Flow

Deflash is Eliminated, Strip Test Enabled



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CSI™ Platform Reliability Matrix

Test	Conditions	Status
Biased HAST	130˚C, 85% rh, 5v, 96 hr	PASSED
Solderability	Per JESD22-B102E, Cond. A, Method 1, Pb free	PASSED
MSL JEDEC Level 1	85˚C / 85% rh, 168 hr.	PASSED[1]
MSL JEDEC Level 3	30˚C / 60% rh, 192 hr.	PASSED[2]
High Temp Storage	150˚C, 1,000 hr.	PASSED
Temp/Humidity	85˚C / 85% rh, 1,000 hr.	PASSED
Temp Cycle	-65˚C to 150˚C, 500 cycles, 30 min. /cycle	PASSED

Notes:
1) Package size and BOM dependent
2) BOM dependent

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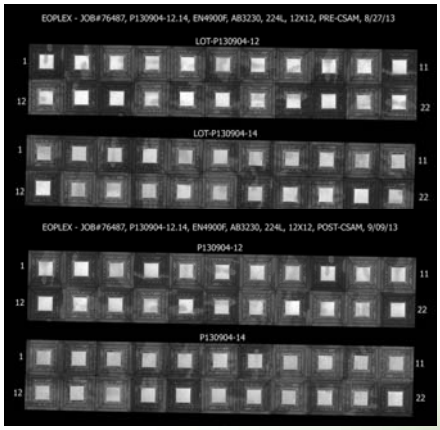
MSL results on 224 Lead, 12x12 Package built on CSI™ Platform

Description		
Build	P130904 – 12	P130904 – 14
Package	224L 12x12 / 44 units	224L 12x12 / 44 units
Die Size	**5x5 mm**	**5x5 mm**
Epoxy	**Hitachi EN4900F**	**Able bond 3230**
Plasma	**With Plasma**	**With Plasma**
Wire	No Wire; thermal simulation	No Wire; thermal simulation
Mold Compound	CEL 9240	CEL 9240
MSL 3 Pre Con	**MSL 3 / 192 hrs @ 30degC/60% RH**	



Pre CSAM

Post CSAM

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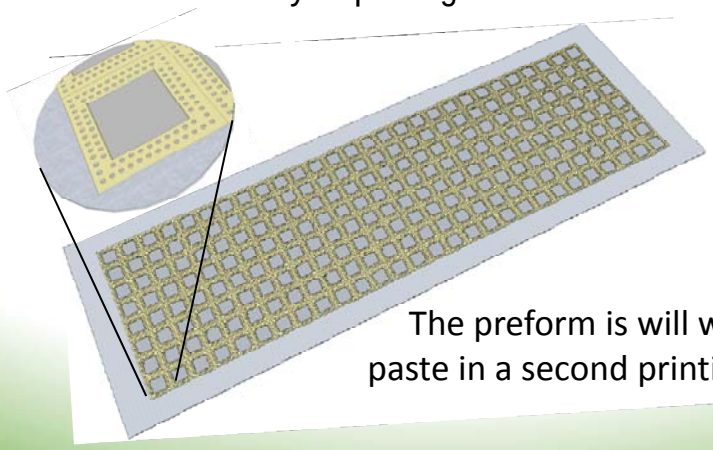
Manufacturing Process For EoPlex CSI™ LeadCarrier

Making an CSI™ LeadCarrier™

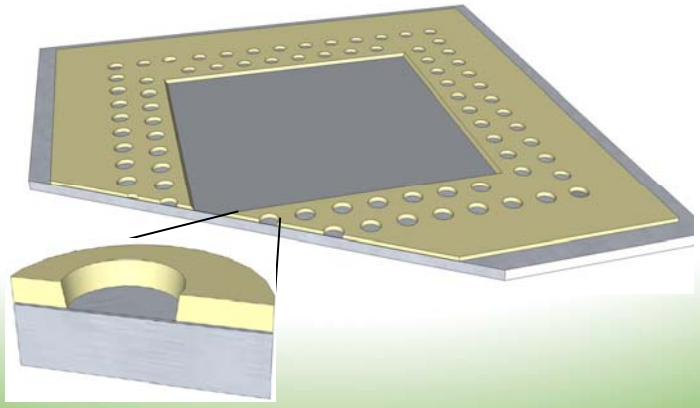
A precise sacrificial preform is print-formed to create the array of package sites



The preform is will with a silver paste in a second printing process

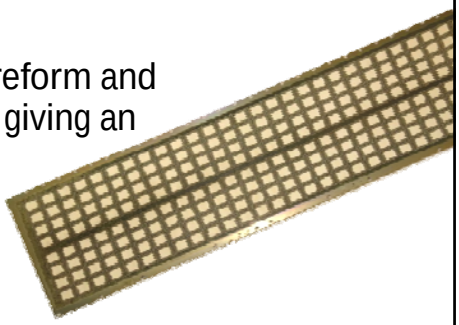
Creating the CSI™ Lock-in Feature

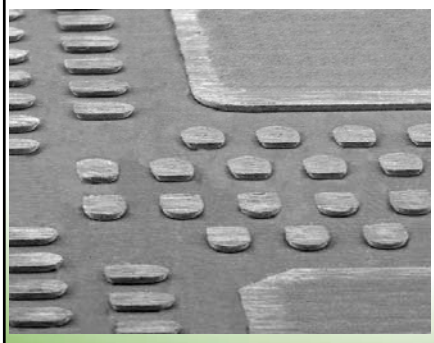
The preform is designed to yield sloped features to lock all pads into the mold compound



Remove the Preform & Sinter the Silver

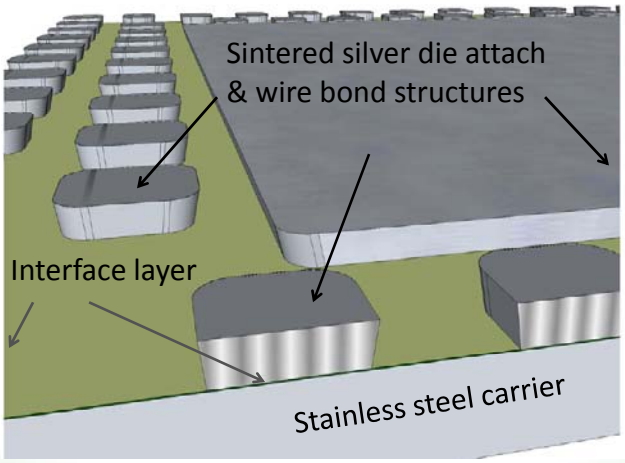
Strips are fired to remove the preform and sinter the metal to high density, giving an excellent wire bonding surface





Result is an array of pads with excellent bonding surfaces, controlled adhesion to the carrier and a shape that locks the pads to the mold compound

Interface Chemistry: A Key to CSI™Success



Chemistry of the interface layer provides good adhesion and clean release, with no treatment of solderable surfaces necessary.

Comparison to Standard Etched Leadframe

Relative to total cost of ownership

- Strip pricing: ≈50% higher
- Strip utilization: As much as 50% greater
- No tape required
- Cut only thin EMC for singulation
- Test in strip is possible

Relative to performance metrics

- Multiple rows, up to around 500 leads
- Design freedom includes multi-chip, redistribution
- Minimum package thickness to 0.2mm vs 0.3mm
- No tie bar stubs = better electrical performance
- Very low thermal resistance
- Solderable lead flank as singulated

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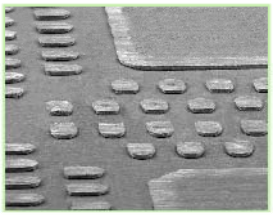
Summary: EoPlex CSI™ Platform Driving a New Interconnect Paradigm

Final cost per lead up to 50% less

- Improves strip density by up to 50%
- No tape backing - saves cost and disposal
- Faster lower cost singulation - only plastic is cut
- Electrical testability in the strip after peel
- No plating or etching - “green process”
- Fits standard process



Improved performance, enables replacement of more expensive packages like BGAs

- Packages from 2 to 500+ leads
- Minimum metal = better electrical performance
- Excellent thermal performance
- Enables smaller and thinnest (200u) packages

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Thank you