

**Embedding Passive and Active Devices in Substrates**

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**AT&S**

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**Who is AT&S?**

- Austria based global technology group focused on High Density Interconnect (HDI) Printed Circuit Boards, Advanced Packaging and IC Substrates.
- AT&S commercializes leading-edge technology for the mobile devices, automotive & aviation, industrial electronics, medical & healthcare and advanced packaging sectors.
- AT&S offers Embedded Component Packaging (ECP®) as a patent protected packaging solution. ECP® embeds active or passive components inside a PCB or IC Package.
- AT&S has 6 manufacturing sites in Austria (2), China (2), India, and South Korea.

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## Global Footprint ensures Cost Efficiency AT&S

- European production facilities: high mix/low volume
- Sales network spanning three continents
- Asian production facilities: high volume/low mix
- About ~8100 employees



Plant Leoben, Austria  
Headquarters



Plant Fehring, Austria



Plant Nanjangud, India



Plant Chongqing, China  
under construction



Plant Shanghai, China



Plant Ansan, Korea



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## AT&S Main Product Portfolio AT&S



Double-sided printed circuit boards	Multilayer printed circuit boards	HDI micro via printed circuit boards	HDI any-layer printed circuit boards	IMS printed circuit boards
HDI rigid-flex printed circuit boards	Flexible printed circuit boards on aluminium	Rigid-flexible printed circuit boards	Semi-flexible printed circuit boards	Flexible printed circuit boards

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## What is ECP®?

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- ECP® (Embedded Component Packaging) is patent protected packaging solution.
- ECP® offers miniaturization, performance and reliability benefits.
- ECP® uses the space inside an organic, laminate substrate (Printed Circuit Board) to embed active and/or passive components.
- Components will be integrated in the core of the substrate and connected by copper plated micro vias.

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## Basic Process and Architecture

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## How is ECP® achieved?

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Breaking it down into three main steps to build an ECP® core:

- Component assembly
- Lamination
- Structuring

The diagram illustrates the three-step process of building an ECP core. Step 1, 'Component assembly', shows a component being placed on a substrate. Step 2, 'Lamination', shows the component being pressed between two layers of material. Step 3, 'Structuring', shows the final core with a central component and surrounding layers. A label 'Subsequent HD / Mfg build-up possible' points to the top of the core.

□ Once this ECP® core structure is built a wide variety of stack ups can be created

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## ECP® Stack Up Structures

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The diagram shows a 'Structured 2 layer core with embedded component' at the bottom left. Three arrows point to different stack up configurations: 1. 'Finish as 2 layer module' (top), 2. 'Sequential 4, 6, 8, ... layer build up' (middle right), and 3. 'Multiple Core build ups' (bottom right).

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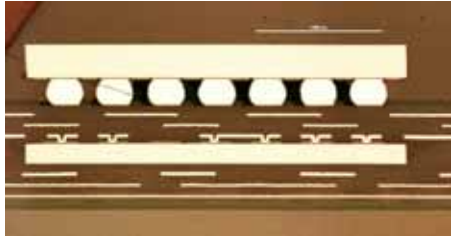
## ECP® Cross Sections

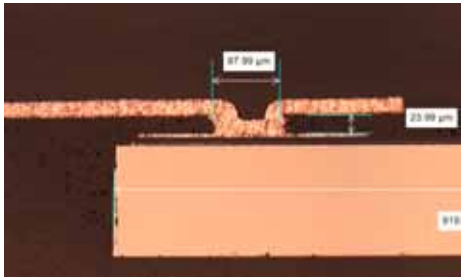
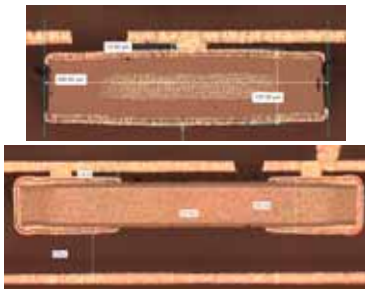
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X-section of embedded components

Surface mount CSP

Substrate with embedded IC



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## Why ECP®?

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Advantages	
<b>Miniaturization</b>	<ul style="list-style-type: none"> <li>Footprint reduction, z-height reduction</li> <li>Higher component integration (additional assembly layer 3 vs 2)</li> </ul>
<b>Electrical Performance</b>	<ul style="list-style-type: none"> <li>Improved signal integrity</li> <li>Reduction of parasitic influence (higher data rates)</li> </ul>
<b>Mechanical Performance</b>	<ul style="list-style-type: none"> <li>Higher durability and reliability through copper-to-copper connections (with copper filled micro vias)</li> <li>Package functions as protective enclosure</li> <li>High drop, shock and vibration tolerance</li> </ul>
<b>Thermal Management</b>	<ul style="list-style-type: none"> <li>Improved heat dissipation through direct copper connection</li> <li>Improved heat dissipation FR4 versus air (compared to SMD)</li> </ul>
<b>Additional functions</b> - Reduction of overall cost - EMV Shielding	<ul style="list-style-type: none"> <li>EMV shielding (partial or full shielding of a package)</li> <li>Package is the housing no additional molding required</li> </ul>
<b>Supporting the trend toward modularization</b>	<ul style="list-style-type: none"> <li>Lower set-up costs compared to other packaging technologies (packaging versus substrate processes)</li> <li>Customization of module variants accomplished with digital imaging – no expensive tooling necessary (e.g. QFN,...)</li> </ul>
<b>Anti-Tamper / Security</b>	<ul style="list-style-type: none"> <li>Hidden electronics preventing reverse engineering and counterfeiting</li> </ul>

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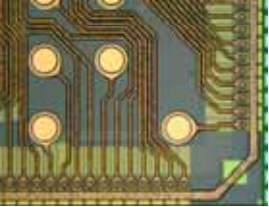
## ECP® Component Basic Requirements AT&S

Wafer based embeddables

- Pad finish: Cu plating needed for contacting with micro vias = existing process for WLP components
- Pad pitch: adaptation to organic substrate design rule through RDL
- Wafer thinning: 100-150µm (recommended thickness)


Passive - discrete embeddables

- Use of thin components with copper terminations
- Capacitors and resistors available
- Other discrete components in development
- Component thickness 100µm – 330µm
- Case sizes 0201, 0402



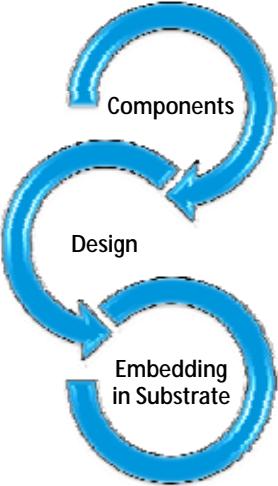
Components are connected by using copper plated micro vias

RDL...redistribution layer  
WLP...Wafer Level Package



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## What is needed for an ECP® project? AT&S



- AT&S works with the leading passive component suppliers and semiconductor companies and can provide support or take over component sourcing
- AT&S offers layout routing including embedded components, or directly supports customers during design creation
- AT&S has years of experience in production of PCBs and packages with embedded components and can combine embedding with different package stack up technologies

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## Design Creation AT&S

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### Design Tools with ECP® design capability

Design systems:

- Mentor Graphics Expedition 7.9.x including embedding tool
- Cadence Allegro 16.5 or higher, including miniaturization tool
- Zuken CR 5000

A presentation slide titled "A Design Flow For Embedded Active Components" featuring a 3D visualization of a circuit board with various components and the Mentor Graphics logo.

- AT&S offers layout routing including embedded components, or directly supports customers during design creation

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## Reliability Testing AT&S

The slide features a background of a blue circuit board with white traces and components.

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## ECP® Reliability Tests and Results



Test Item	Specification/Requirement	Samples size	Result
Reflow Sensitivity (RS)	IPC/JEDEC J-STD-020, MSL2 cond. 3 x Reflow, no delaminations	5 Arrays (7500 single cards)	Passed
Temperature cycling test (TCT) (-55 /+125°C /1,000 cycles)	Jedec JESD22-A104C, increase of resistance not more than 10%	5 Arrays (7500 single cards)	Passed
Drop Test (DT)	Jedec JESD22-B111, B104	9 Drop Test boards	Passed (Stopped at 1000 Drops)
Temperature humidity storage (THS) (85°C/85%RH /1,000h)	IPC-TM-650 2.6.3, Increase of resistance not more than 10%	5 Arrays (7500 single cards)	Passed
High temperature storage THS (150°C – 1,000 hrs)	JEDEC JESD22-A103, increase of resistance not more than 10%	5 Arrays (7500 single cards)	Passed
HAST Electrochemical migration (130°C/85%RH – 96hrs?)	JEDEC JESD 22-A110-B No events with resistance below 1E07 Ohm	9 EM Testboards	Passed
Solder float test (288°C, 10sec)	IPC J-STD-003, Solderbath	Q-Lot, Process control	Passed
Solder Dip Test (270°C, 10sec)	IPC J-STD-003, Solderbath	Q-Lot, Process control	Passed
Solderability Test (250°C)	IEC 60068-2-69, IPC J-STD-003, Must # wetting balance methode	Q-Lot, Process control	Passed
Glas Transmission Point	IPC-TM-650 2.4.25	Q-Lot, Process control	Passed

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## ECP® Reliability



### Reliability test board for embedded passives - Technology Qualification

- 112 components in total: 56 SMD, 56 EC
- 8 components per daisy chain
- 7 daisy chain for SMD and EC each

- Standard 10 Ohm 0402 resistors
- Embedded and SMD same in x,y axis dimension
- Difference in z axis (ECs thinner)
- Same manufacturer
- Terminals differ: Cu vs. Sn


**Test Vehicle Stack-up**

White paper available

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## ECP® Reliability Results

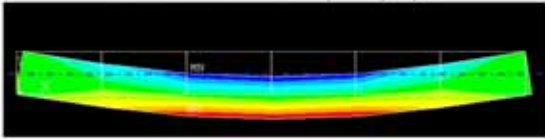


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### Reliability test board for embedded passives - Results

#### Evaluation – Drop Test

Model of tension distribution at drop test impact point



-- Neutral Axis  
 MCI – Maximum tension  
 MDC – Maximum tension

- Blue and red represent highest rate of compression and tension respectively; SMD components are more subject to these forces
- Green indicates where the EC's are located; i.e. along the neutral axis


□ Temperature Cycle Test per JEDEC JESD22-A104  
 -40°C/+125°C

All EC and SMD components passed 1000 cycles without failures

White paper available

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## ECP® Reliability Results



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### Reliability test board for embedded passives - Results

□ Drop Test per JEDEC JESD22-B111  
 1500g/0,5ms


Card	Time Failure	SMD								EC								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14			
0	300																	
1																		
2																		
3		975																
4																		
5																		
6																		
7																		
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Drop Test – Defect Modes (SMD)

Track Breakage




Component Crack



- Earliest recorded drop failure for SMD was at 304 drops
- 2 out of 7 delay chains survived 1000 drops
- Delay chain 4 exhibited the lowest drop survivability
- There were 2 component cracks, other defects attributed to track breakage between components

Drop Test – Defect Modes (EC)



- Single failure event registered at 832 drops
- Cross sections could not reveal origin of failure within the ECs
- No failure found at component/via interconnect
- PTHs at terminals also examined, but no defect found


White paper available

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www.cpm.org/scv/

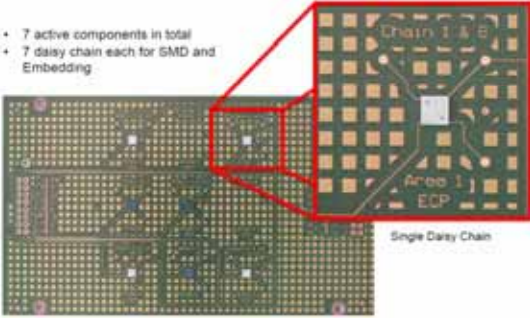
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## ECP® Reliability

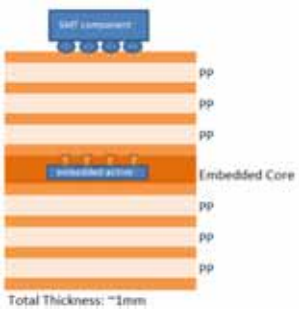


### Reliability test board for embedded actives – Technology Qualification

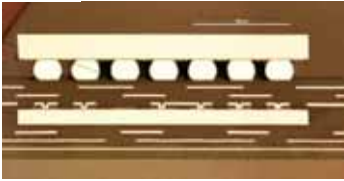
- 7 active components in total
- 7 daisy chain each for SMD and Embedding



Single Daisy Chain



Total Thickness: ~1mm




7x7 pin Daisy Chain component with copper RDL

White paper available

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## ECP® Reliability Results



### Reliability test board for embedded actives - Results

□ Drop Test per JEDEC JESD22-B111  
1500g/0,5ms

**Drop Test – Defect Modes (SMD)**




Start	Test Failure	SMD							ECP						
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
1															
2															
3															
4															
5															
6	✖														
7															
8															
9															
10															

- Earliest recorded drop failure for SMD was at 792 drops
- 3 out of 7 daisy chains survived 1000 drops
- Daisy chain 4 exhibited the lowest drop survivability
- There were solder cracks observed near the SMD component on all 4 failures
- No failure detected for embedded component daisy chains

White paper available

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## ECP® Reliability Results



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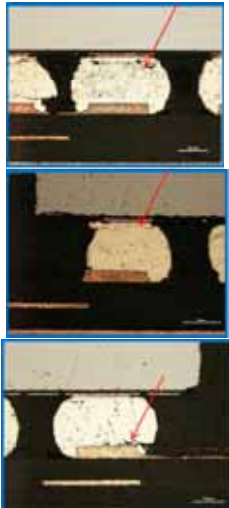
### Reliability test board for embedded actives – Results

- Temperature Cycle Test per JEDEC JESD22-A104  
-40°C/+125°C


Sample ID	Card	Structure No.	failed at cycle	Surface/Embedded
ITE2000_18_s04	18	4	684	5
ITE2000_20_s06	20	6	764	5
ITE2000_16_s06	16	6	786	5
ITE2000_15_s06	15	6	803	5
ITE2000_20_s04	20	4	818	5
ITE2000_11_s06	11	6	835	5
ITE2000_14_s04	14	4	853	5
ITE2000_19_s04	19	4	900	5
ITE2000_13_s04	15	4	999	5

White paper available

#### Failure modes



White paper available
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## Application Examples

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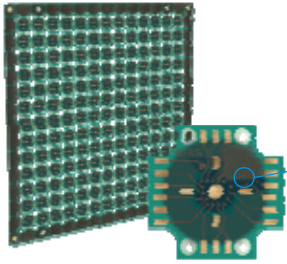
**Trends in the Electronics Industry - *Module / Packages*** **AT&S**

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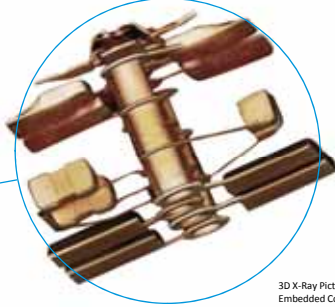
**Integration of Electronics in our daily lives - Technology meets Design**

**Module / Packages**

- Integration of new features in devices (Example: Sensors) – smallest packages and highest performance – ECP Technology opens up new possibilities



Picture: AT&S



3D X-Ray Picture of a Module with Embedded Components

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**Trends in the Electronics Industry - *Module / Packages*** **AT&S**

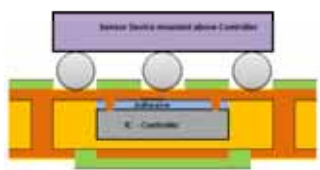
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**Flexibility due to modular design**

- Tightly spaced electronic devices
- Modular design to shorten time-to-market cycles

**Where ECP® is being used**

- Smartwatches
- Activity Trackers
- Heart rate monitors / pulse oximeters
- Sensors





5.5mm x 3.9mm x 1.2mm

Picture: AT&S

Optical Heart Rate Monitoring System with 1 embedded IC controller

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## Trends in the Electronics Industry - *Module / Packages*



### Flexibility due to modular design

- Customers require design flexibility
- Increasing density requires higher complexity of the circuit board
- Adoptions in design cause time- and cost intensive approval processes

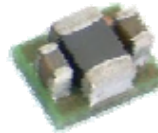


Picture: AT&S  
Engine Control Module:  
416 I/O Processor embedded

### Where ECP® is being used

- Connectivity modules (M2M communication)
- Power Modules
- Interface Modules
- Control units

2.3mm x 2.9mm x 1.0mm



DC/DC Converter with embedded active

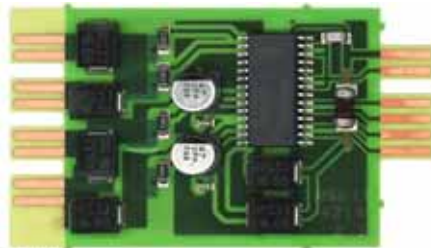
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## Trends in the Electronics Industry - *Power Modules*



### Steadily increasing demands for Power Management

- Every operational unit has to have a power supply
- Smaller energy sources require more efficient use of available capacity
- Thermal Management



Picture: AT&S  
Power Module: 4 MOSFETs embedded

### Where ECP® is being used

- Battery Management
- Power Modules
- Power MOSFETs



Picture: AT&S

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## Trends in the Electronics Industry - GaN / SiC





Market for advanced power modules

- Automotive
- Infrastructure
- Industrial


Technology shift coming – move to high efficiency semiconductor – GaN / SiC

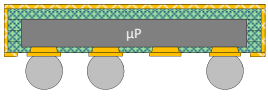
Packaging = Significant Value-Add



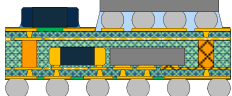
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## Further Application Examples

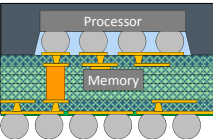




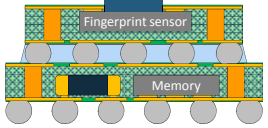
Active shielding - complete



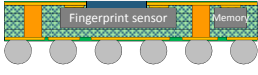
Active shielding - partial



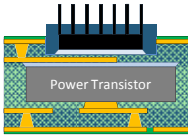
Data protection



3D Integration  
User authentication



Authentication



2.5DC Cavity integration

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## Standardization



- System-in-Package
  - ECP as Package
  - Standard qualification process
    - AEC Q100, JESD-22, MIL-STD-883...
- System-in-Board
  - ECP as Substrate
  - No standard in place yet
  - AT&S working with IPC Committee
    - Embedding-specific standard (IPC-7092)








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## Technology Outlook



### Further development of ECP®

- We are developing our ECP® technology further in terms of
  - Embedded die size (beyond 10 x 10 mm)
  - Embedded die thickness (less than 100µm)
  - Embedded passive component thickness (01005, 0201, 0402, 0803,...)
  - Wider height combination range for embedded components (active and passive)
  - Material selection (wider variety of Cu foils and prepregs)
  - Flexibility of build up concepts




Source: Fraunhofer IZM





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## AT&S ECP® Technology

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### Summary


- Key benefits of ECP®
  - Miniaturization
  - Improved Electrical Performance
  - Improved Mechanical Performance
  - Enhanced Thermal Management
  - Embedded component / no additional housing required
  - Security / Anti-tamper
  - Shielding
  
- ECP® has been in volume production at AT&S for several years (>200 Mio units in the field today)
- ECP® can be combined with various substrate buildups
- We can support product development, production and even take over part of the supply chain, if required
- We possess the necessary IP Portfolio for supporting your projects



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## AT&S – first choice for advanced applications

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