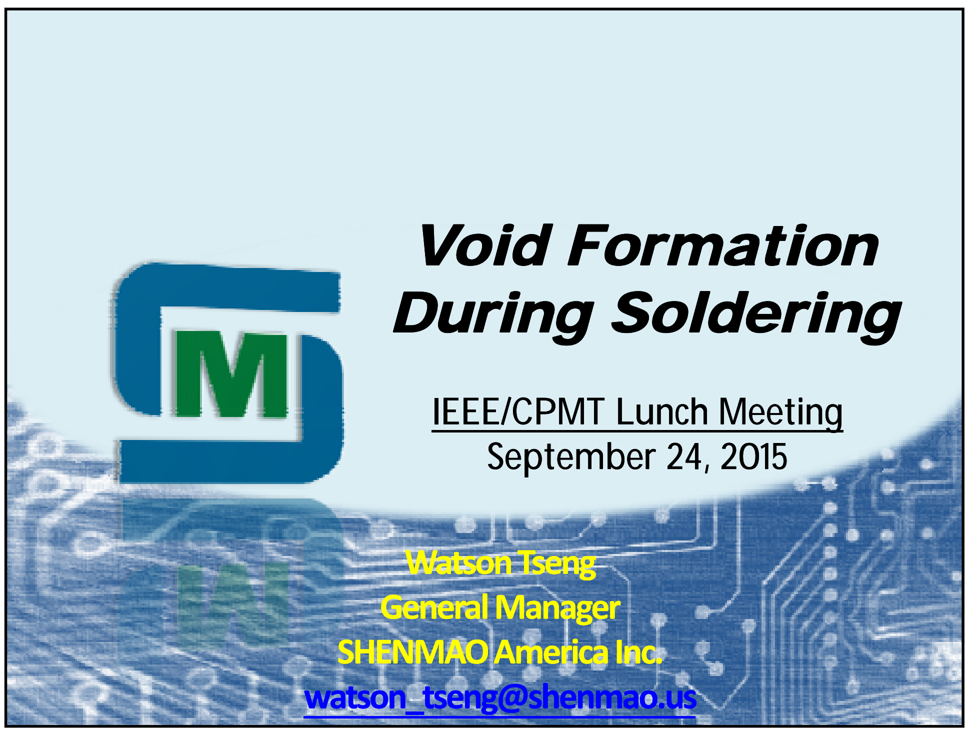

Overview

- Two Main Issues in Assembly
- Something About Voids
- Industrial Standards
- Factor Analysis for Void Formation
  - * Surface Finish
  - * Voids from PCB Design
  - * Voids from Component
  - * Voids from Solder Paste
  - * Voids from Process
- Voids in Bumping Process
- Conclusion

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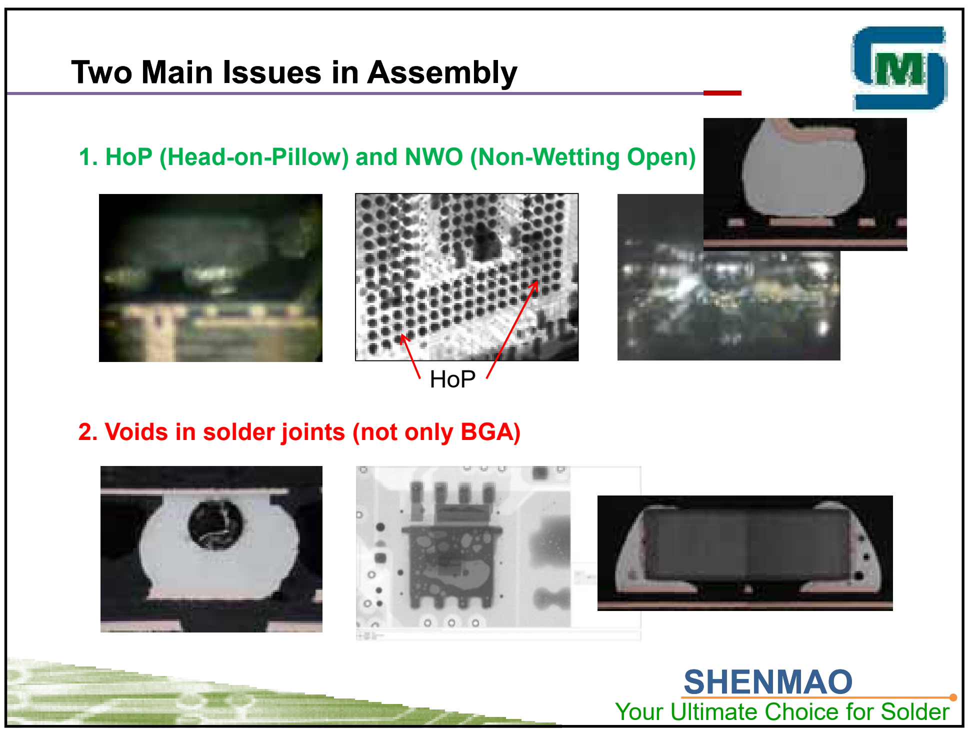
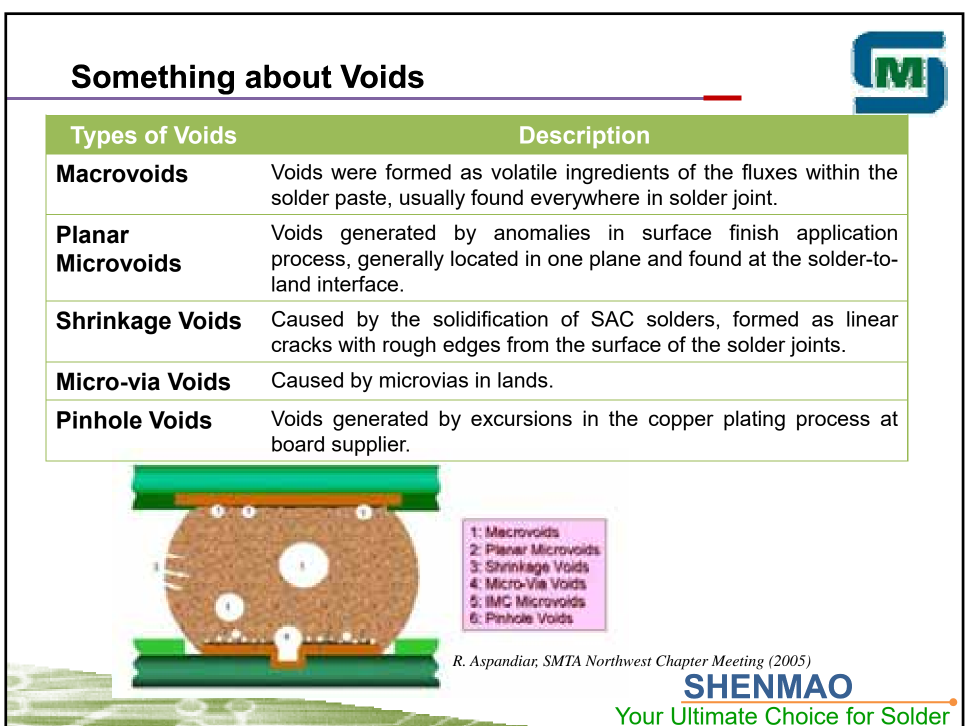
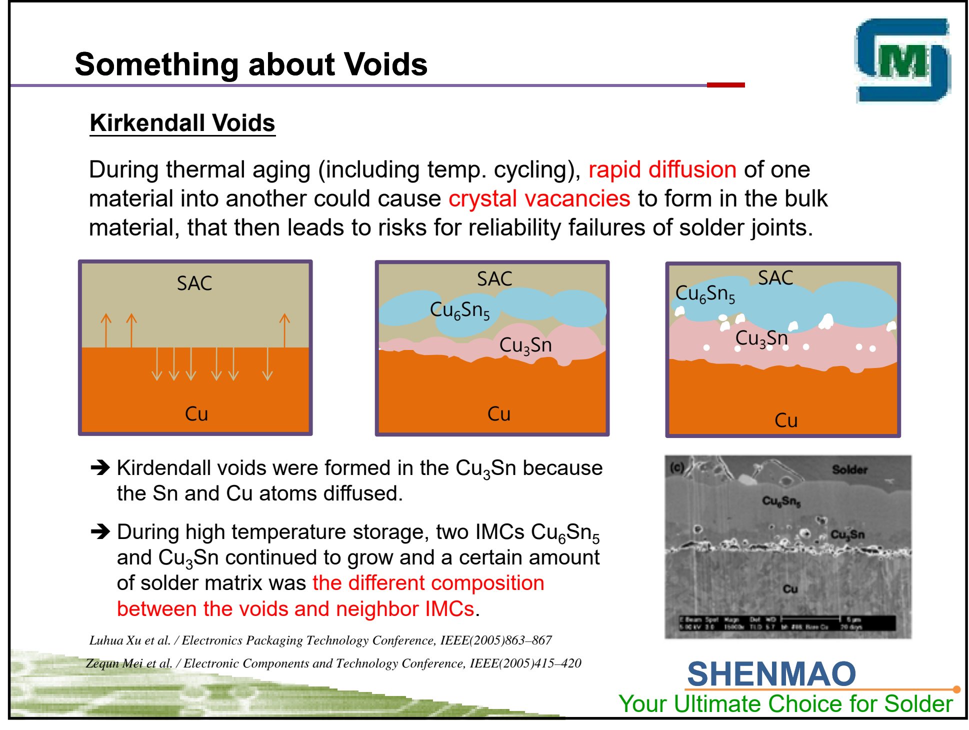




Types of Voids	Description
Macrovoids	Voids were formed as volatile ingredients of the fluxes within the solder paste, usually found everywhere in solder joint.
Planar Microvoids	Voids generated by anomalies in surface finish application process, generally located in one plane and found at the solder-to-land interface.
Shrinkage Voids	Caused by the solidification of SAC solders, formed as linear cracks with rough edges from the surface of the solder joints.
Micro-via Voids	Caused by microvias in lands.
Pinhole Voids	Voids generated by excursions in the copper plating process at board supplier.


Something about Voids
Kirkendall Voids
During thermal aging (including temp. cycling), rapid diffusion of one material into another could cause crystal vacancies to form in the bulk material, that then leads to risks for reliability failures of solder joints.
SAC
Cu
SAC
Cu6Sn5
Cu3Sn
Cu
SAC
Cu6Sn5
Cu3Sn
Cu
➔ Kirdendall voids were formed in the Cu3Sn because the Sn and Cu atoms diffused.
➔ During high temperature storage, two IMCs Cu6Sn5 and Cu3Sn continued to grow and a certain amount of solder matrix was the different composition between the voids and neighbor IMCs.
Luhua Xu et al. / Electronics Packaging Technology Conference, IEEE(2005)863–867
Zequn Mei et al. / Electronic Components and Technology Conference, IEEE(2005)415–420
(c)
Solder
Cu6Sn5
Cu3Sn
Cu
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Something about Voids
Why don't we like void?
❖ Poor Heat Transfer Rate
❖ Poor Current Carrying Capability
❖ Long-term Reliability Concern
❖ Squeezed Short
❖ Bump Height Uniformity
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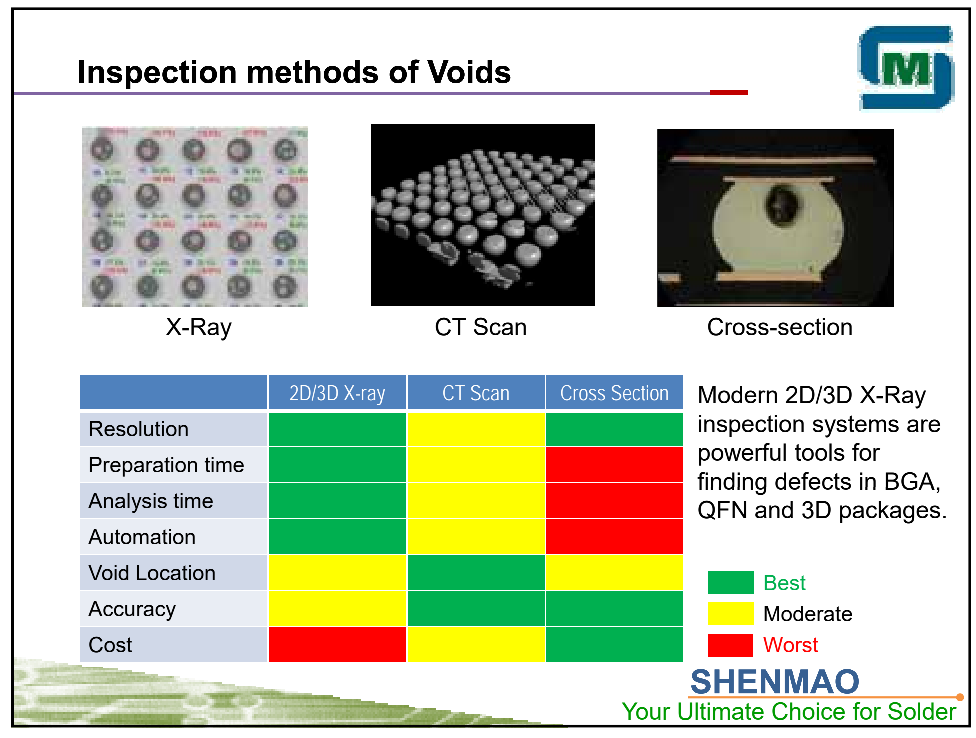
Inspection methods of Voids
X-Ray
CT Scan
Cross-section
2D/3D X-ray
CT Scan
Cross Section
Resolution
Preparation time
Analysis time
Automation
Void Location
Accuracy
Cost
Modern 2D/3D X-Ray inspection systems are powerful tools for finding defects in BGA, QFN and 3D packages.
Best
Moderate
Worst
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Inspection methods of Voids
Voiding Inspection Systems in SHENMAO Lab
SMT System
Wafer Bumping System
Dage 7600NT
Printer
Wafer printer
Reflow oven
Reflow oven
X-ray inspection
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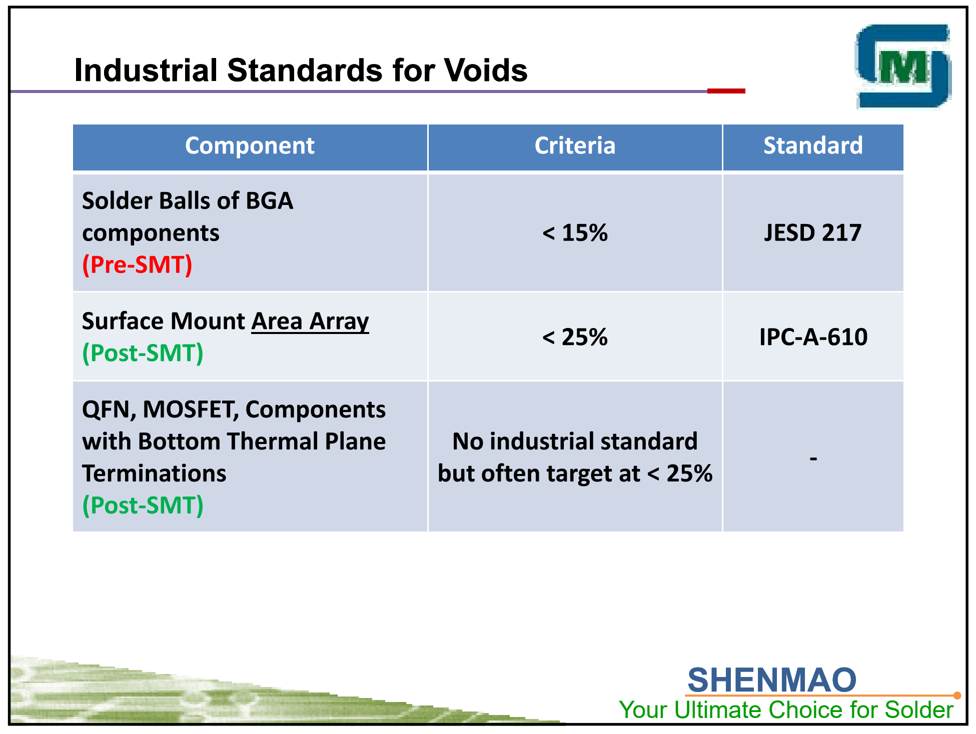
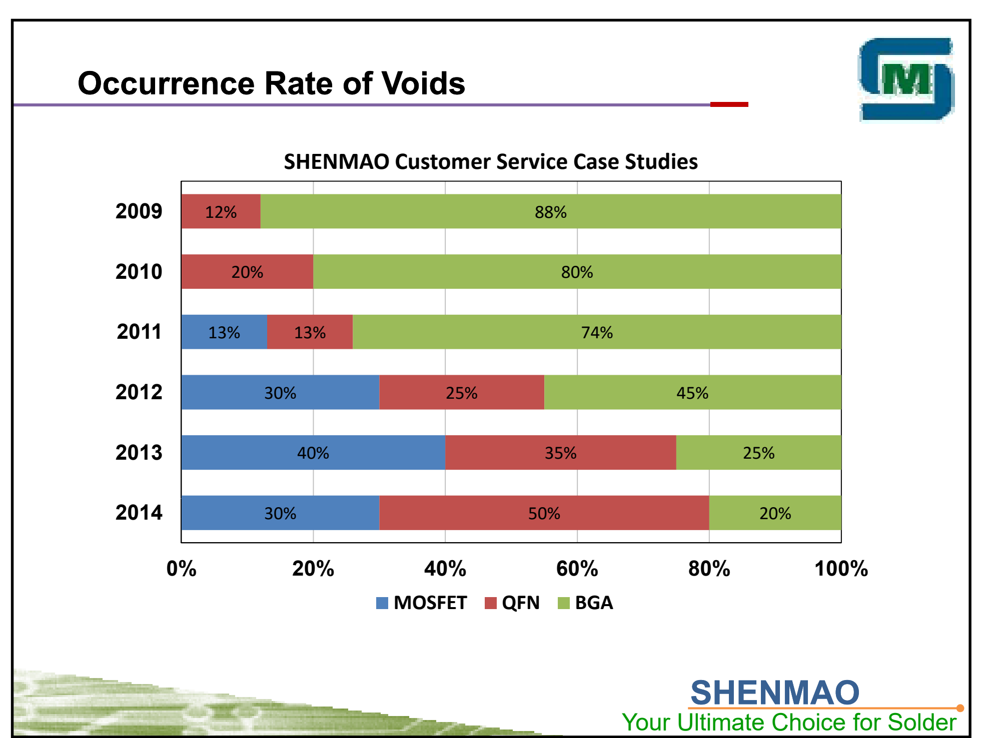
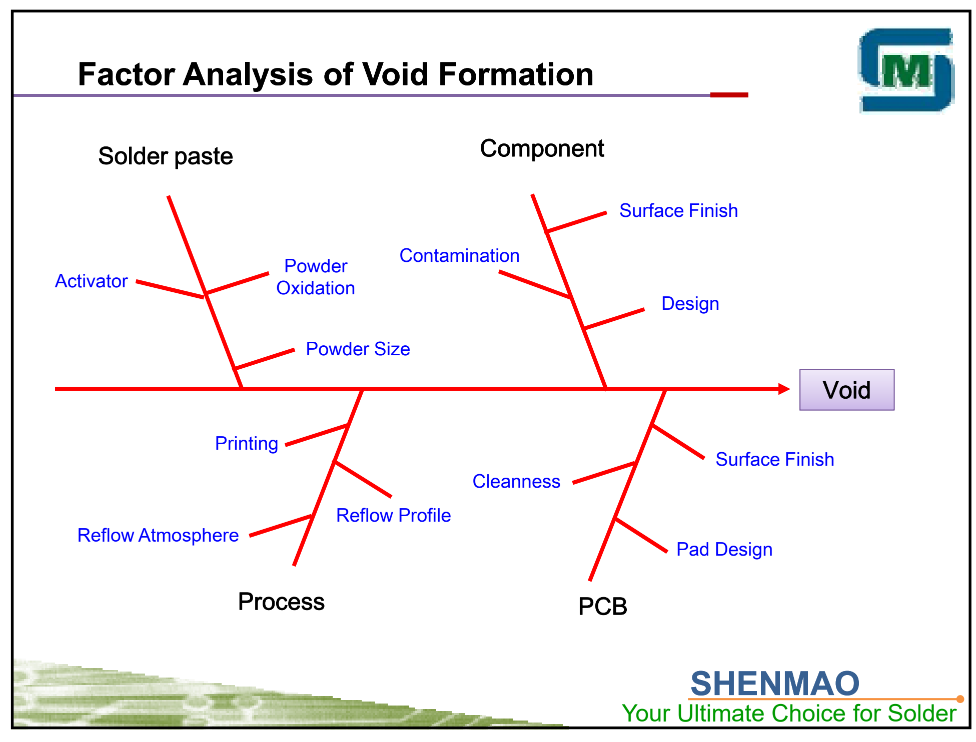


Component	Criteria	Standard
Solder Balls of BGA components (Pre-SMT)	< 15%	JESD 217
Surface Mount Area Array (Post-SMT)	< 25%	IPC-A-610
QFN, MOSFET, Components with Bottom Thermal Plane Terminations (Post-SMT)	No industrial standard but often target at < 25%	-




Factor Analysis of Void Formation
Solder paste
Component
Activator
Powder Oxidation
Powder Size
Contamination
Surface Finish
Design
Void
Printing
Reflow Profile
Reflow Atmosphere
Process
Cleanness
Surface Finish
Pad Design
PCB
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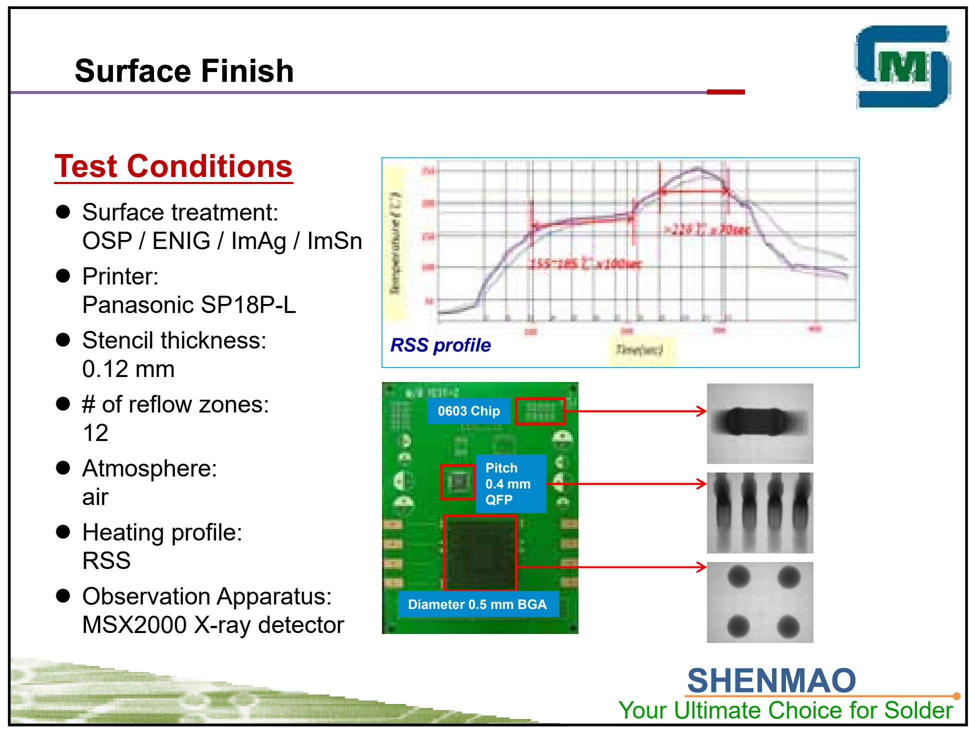
Surface Finish
Test Conditions
Surface treatment: OSP / ENIG / ImAg / ImSn
Printer: Panasonic SP18P-L
Stencil thickness: 0.12 mm
# of reflow zones: 12
Atmosphere: air
Heating profile: RSS
Observation Apparatus: MSX2000 X-ray detector
RSS profile
0603 Chip
Pitch 0.4 mm QFP
Diameter 0.5 mm BGA
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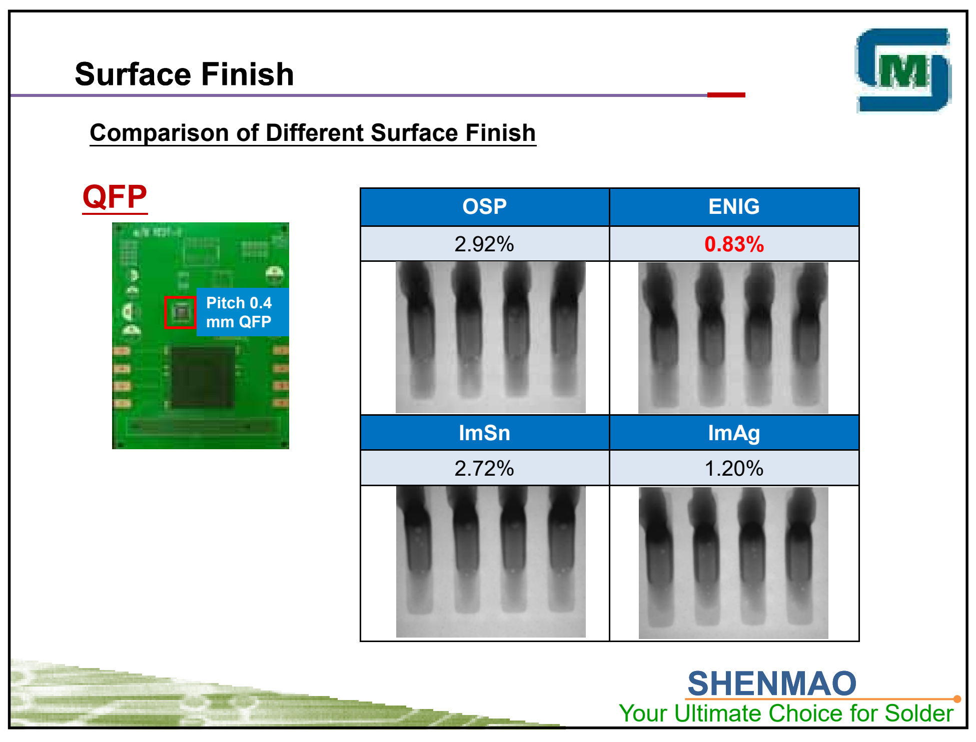
Surface Finish
Comparison of Different Surface Finish
QFP
Pitch 0.4 mm QFP
OSP
ENIG
2.92%
0.83%
ImSn
ImAg
2.72%
1.20%
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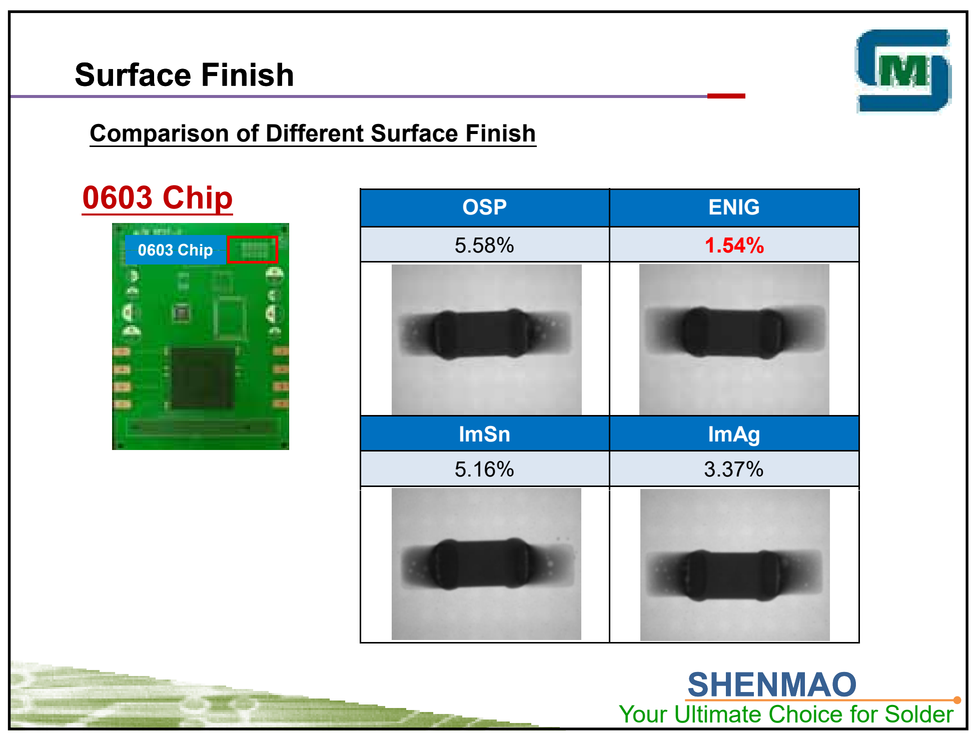
Surface Finish
Comparison of Different Surface Finish
0603 Chip
0603 Chip
OSP
ENIG
5.58%
1.54%
ImSn
ImAg
5.16%
3.37%
SHENMAO
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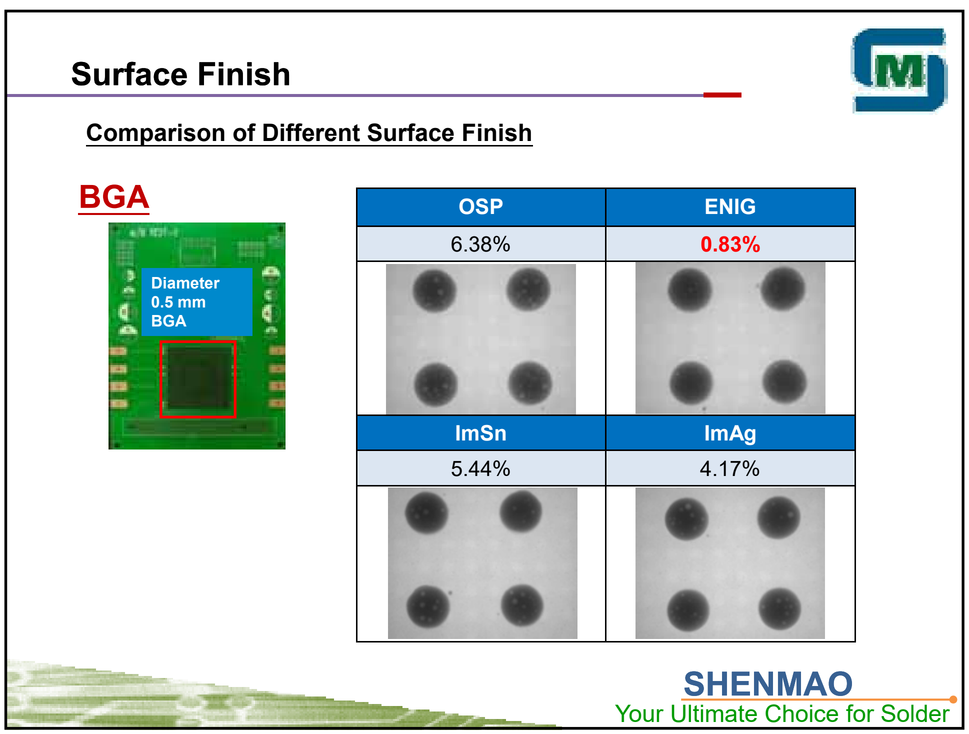
Surface Finish
Comparison of Different Surface Finish
BGA
Diameter 0.5 mm BGA
OSP
ENIG
6.38%
0.83%
ImSn
ImAg
5.44%
4.17%
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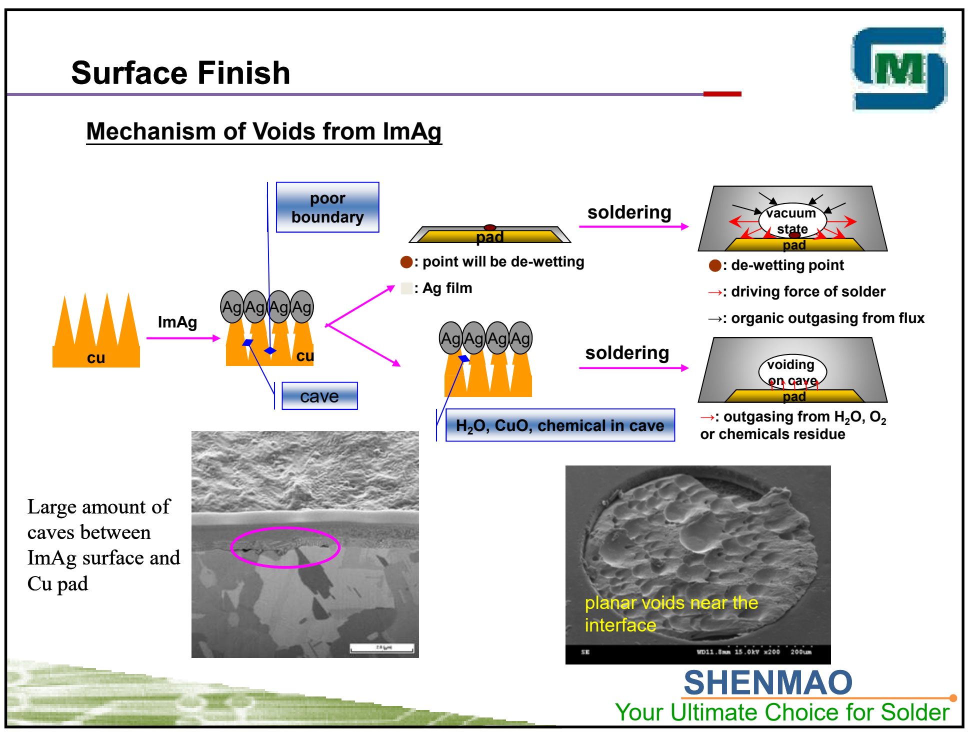
Surface Finish
Mechanism of Voids from ImAg
poor boundary
pad
: point will be de-wetting
: Ag film
soldering
vacuum state
pad
: de-wetting point
→: driving force of solder
→: organic outgasing from flux
cu
ImAg
Ag Ag Ag Ag
cu
cave
soldering
voiding on cave
pad
H2O, CuO, chemical in cave
→: outgasing from H2O, O2 or chemicals residue
Large amount of caves between ImAg surface and Cu pad
planar voids near the interface
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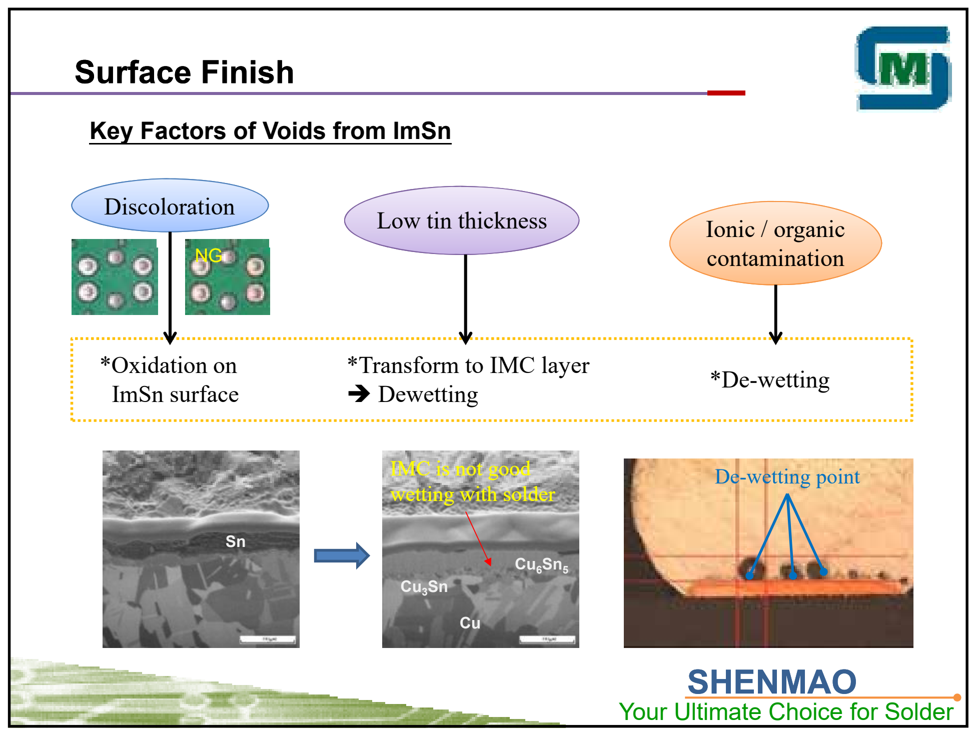
Surface Finish
Key Factors of Voids from ImSn
Discoloration
NG
Low tin thickness
Ionic / organic contamination
*Oxidation on ImSn surface
*Transform to IMC layer ➔ Dewetting
*De-wetting
Sn
IMC is not good wetting with solder
Cu6Sn5
Cu3Sn
Cu
De-wetting point
SHENMAO
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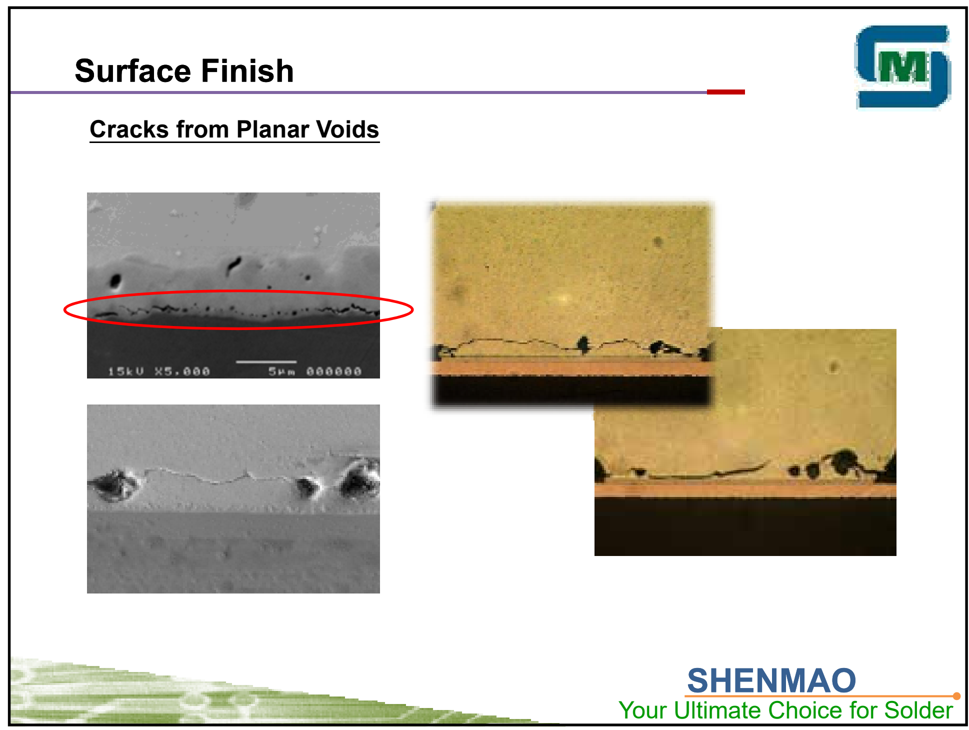
Surface Finish
Cracks from Planar Voids
15kV X5,000 5μm 000000
SHENMAO
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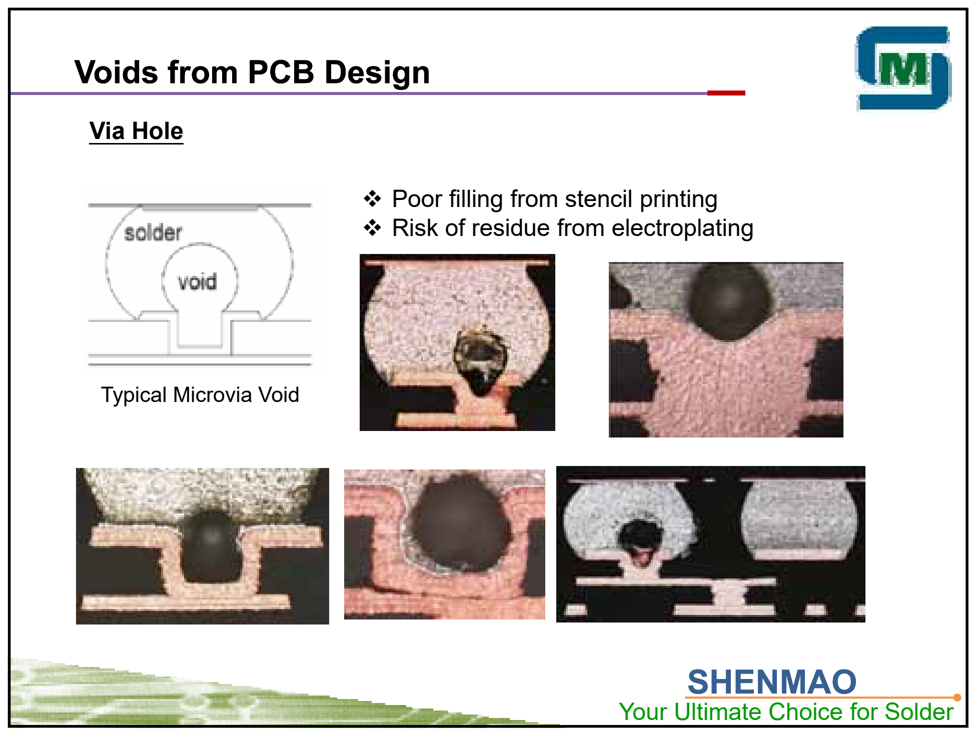
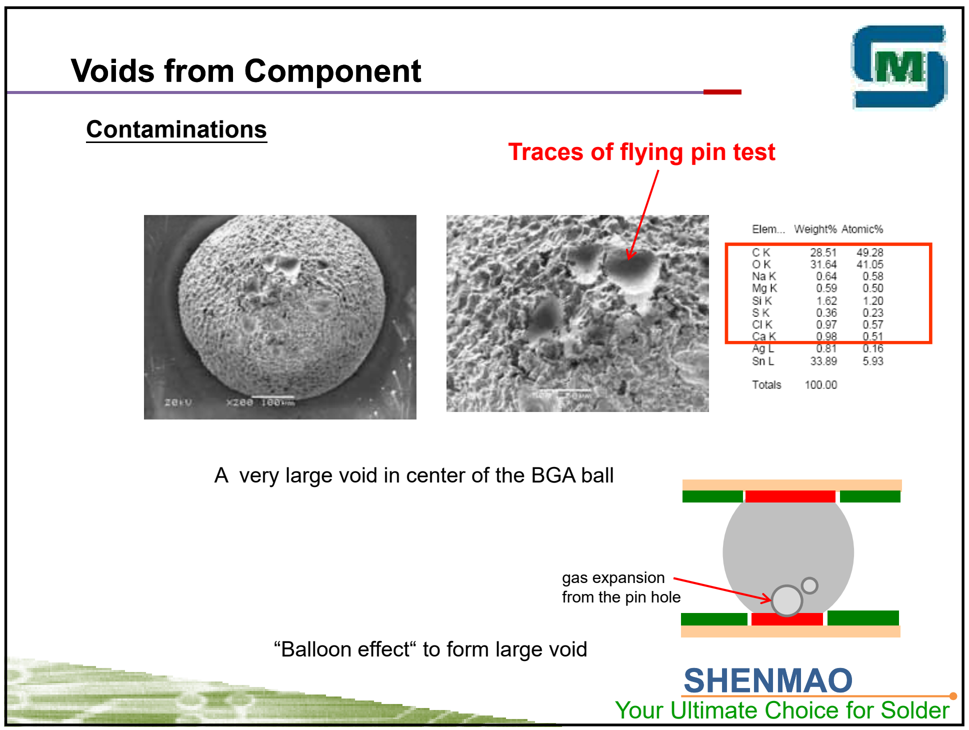
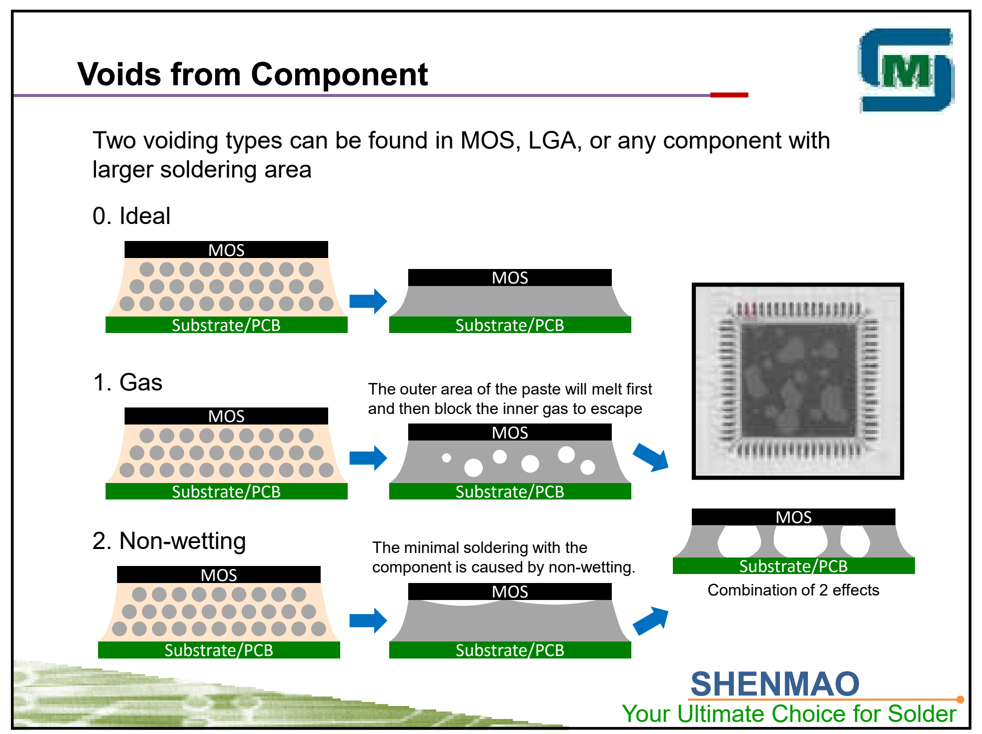




Elem...	Weight%	Atomic%
C K	28.51	49.28
O K	31.64	41.05
Na K	0.64	0.58
Mg K	0.59	0.50
Si K	1.62	1.20
S K	0.36	0.23
Cl K	0.97	0.57
Ca K	0.98	0.51
Ag L	0.81	0.16
Sn L	33.89	5.93
Totals	100.00	


Voids from Component
Two voiding types can be found in MOS, LGA, or any component with larger soldering area
0. Ideal
MOS
Substrate/PCB
MOS
Substrate/PCB
1. Gas
MOS
Substrate/PCB
The outer area of the paste will melt first and then block the inner gas to escape
MOS
Substrate/PCB
2. Non-wetting
MOS
Substrate/PCB
The minimal soldering with the component is caused by non-wetting.
MOS
Substrate/PCB
MOS
Substrate/PCB
Combination of 2 effects
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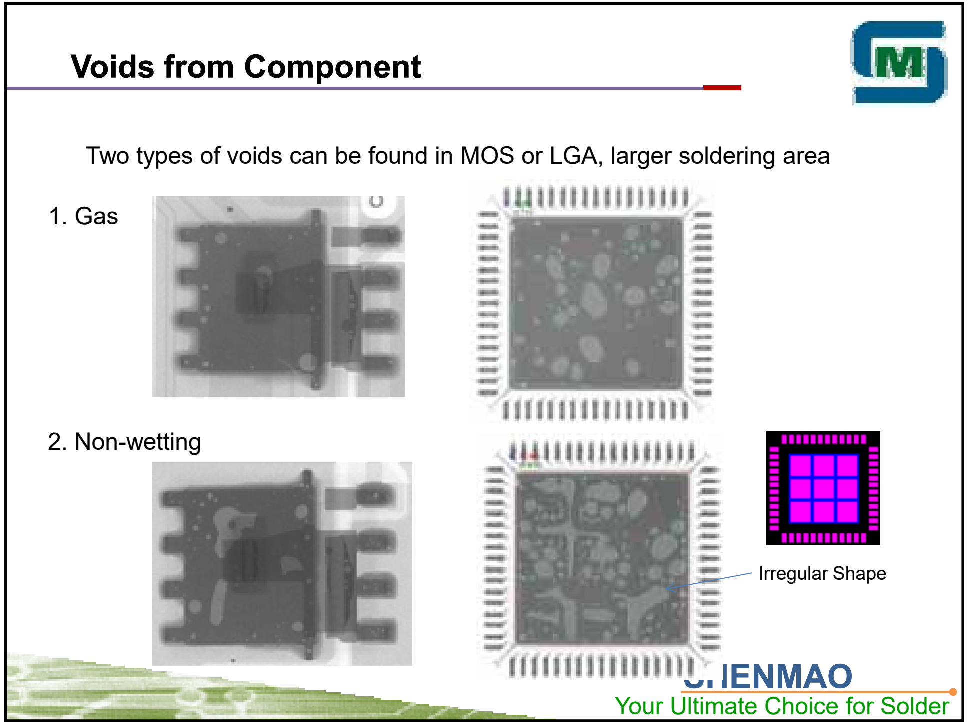
Voids from Component
Two types of voids can be found in MOS or LGA, larger soldering area
1. Gas
2. Non-wetting
Irregular Shape
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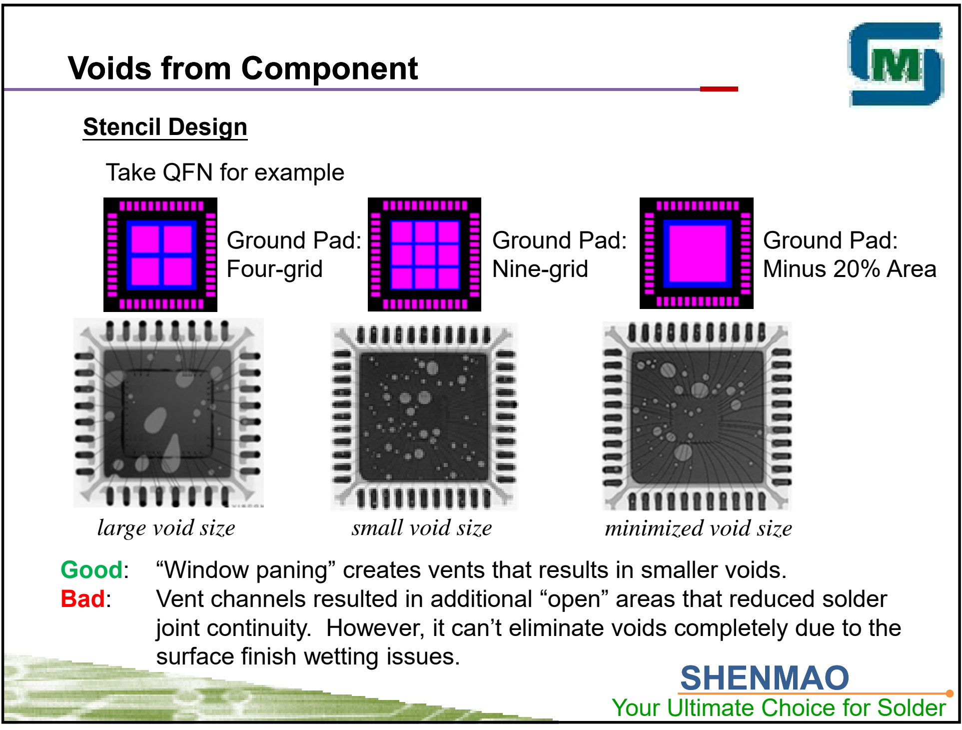

Voids from Solder Paste

Solder paste plays an important role in contribution of void.

- High volume of flux → High volume of gas generated
- Large surface area from solder powder

  → Rapid chemical reaction in reflow

Water soluble solder pastes tend to cause larger void than no-clean ones.

- Different chemical compound in flux
- Moisture absorption

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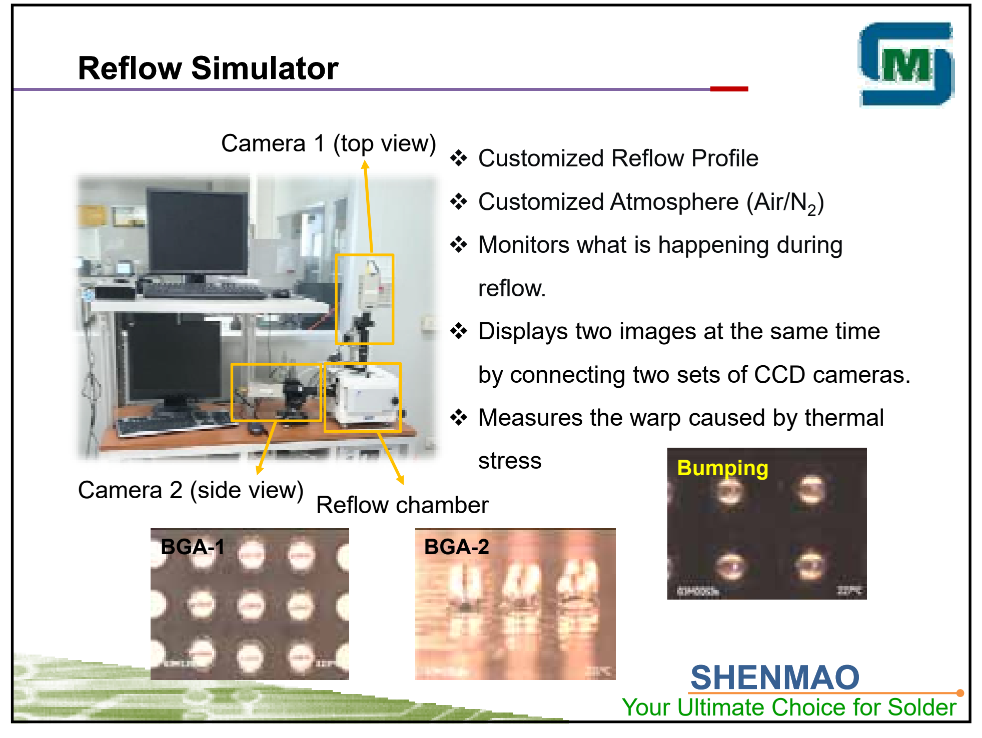
Reflow Simulator
Camera 1 (top view)
Camera 2 (side view)
Reflow chamber
❖ Customized Reflow Profile
❖ Customized Atmosphere (Air/N2)
❖ Monitors what is happening during reflow.
❖ Displays two images at the same time by connecting two sets of CCD cameras.
❖ Measures the warp caused by thermal stress
Bumping
BGA-1
BGA-2
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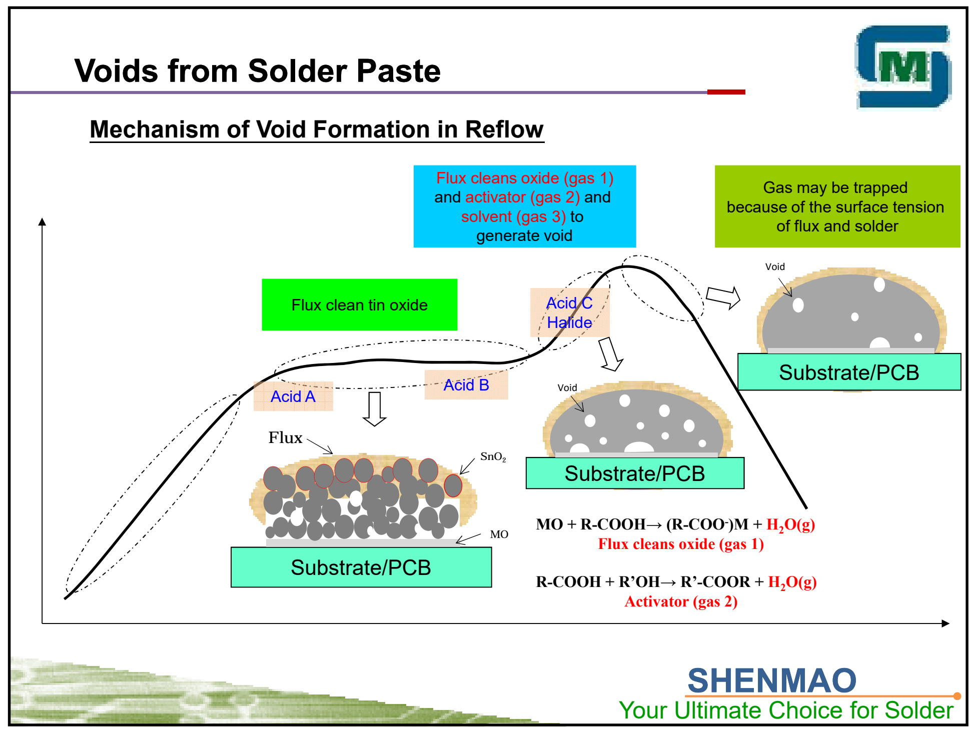
Voids from Solder Paste
Mechanism of Void Formation in Reflow
Flux cleans oxide (gas 1) and activator (gas 2) and solvent (gas 3) to generate void
Gas may be trapped because of the surface tension of flux and solder
Flux clean tin oxide
Acid C
Halide
Acid A
Acid B
Flux
SnO2
MO
Void
Substrate/PCB
Substrate/PCB
Substrate/PCB
MO + R-COOH→ (R-COO-)M + H2O(g)
Flux cleans oxide (gas 1)
R-COOH + R'OH→ R'-COOR + H2O(g)
Activator (gas 2)
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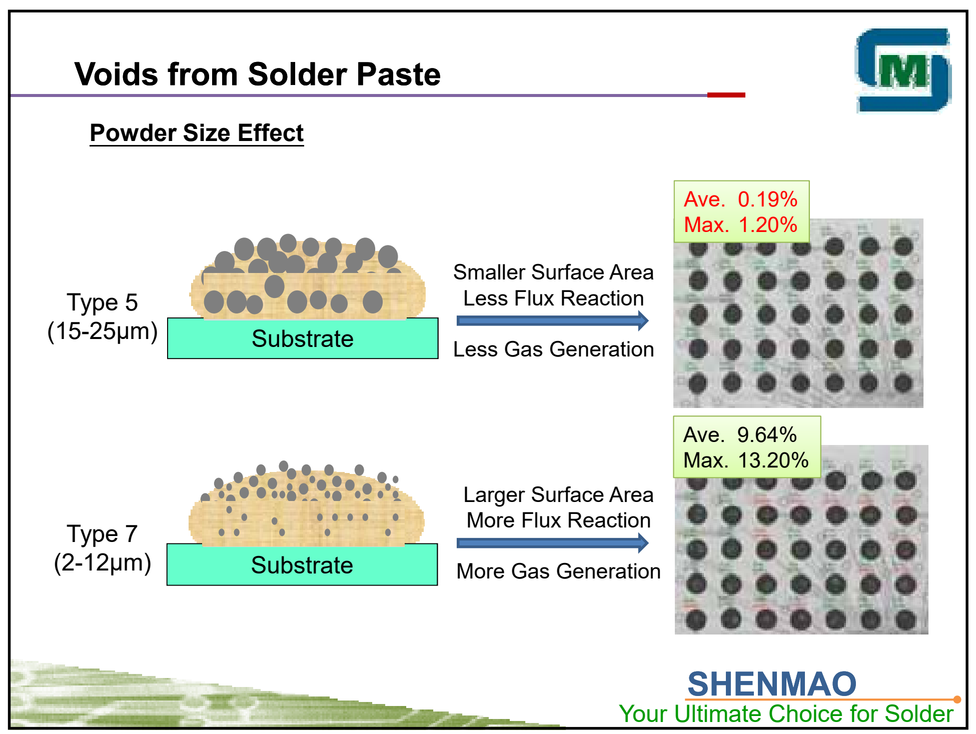
Voids from Solder Paste
Powder Size Effect
Type 5
(15-25µm)
Substrate
Smaller Surface Area
Less Flux Reaction
Less Gas Generation
Ave. 0.19%
Max. 1.20%
Type 7
(2-12µm)
Substrate
Larger Surface Area
More Flux Reaction
More Gas Generation
Ave. 9.64%
Max. 13.20%
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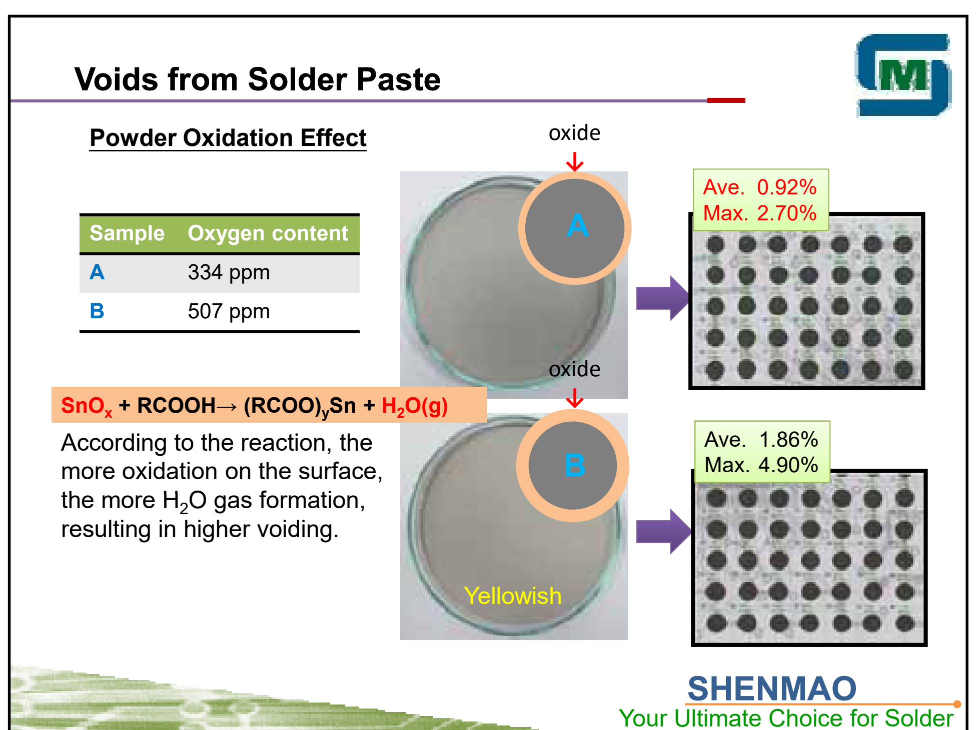
Voids from Solder Paste
Powder Oxidation Effect
Sample Oxygen content
A 334 ppm
B 507 ppm
SnO_x + RCOOH→ $(RCOO)_y$Sn + H_2O(g)
According to the reaction, the more oxidation on the surface, the more H_2O gas formation, resulting in higher voiding.
oxide
A
oxide
B
Yellowish
Ave. 0.92%
Max. 2.70%
Ave. 1.86%
Max. 4.90%
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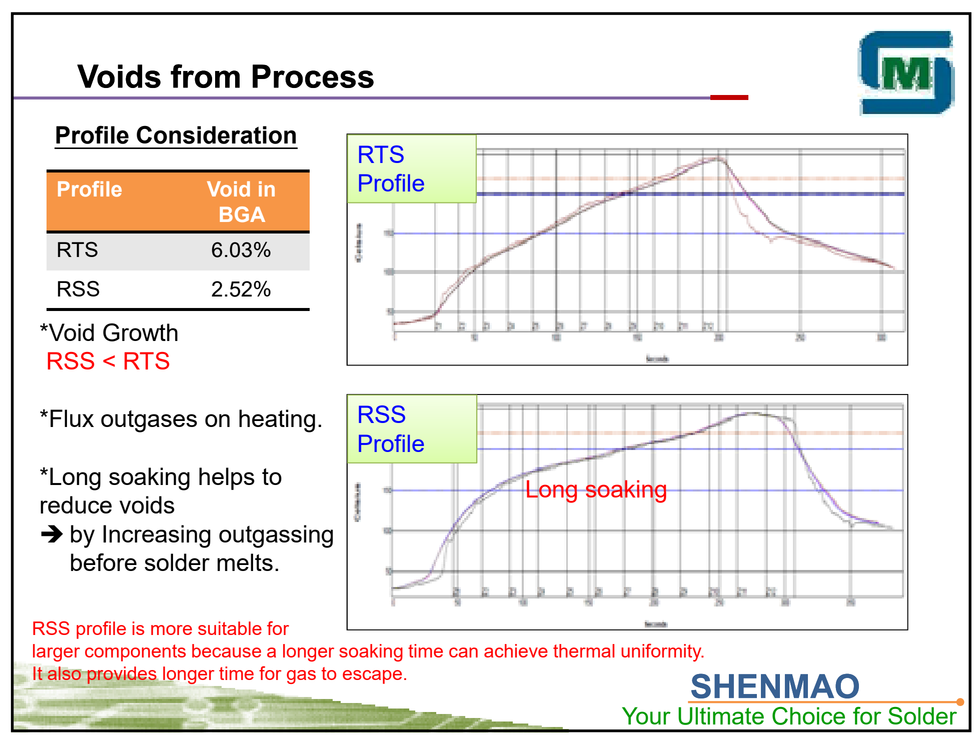
Voids from Process
Profile Consideration
Profile	Void in BGA
RTS	6.03%
RSS	2.52%
*Void Growth
RSS < RTS
*Flux outgases on heating.
*Long soaking helps to reduce voids
➔ by Increasing outgassing before solder melts.
RTS Profile
RSS Profile
Long soaking
RSS profile is more suitable for larger components because a longer soaking time can achieve thermal uniformity.
It also provides longer time for gas to escape.
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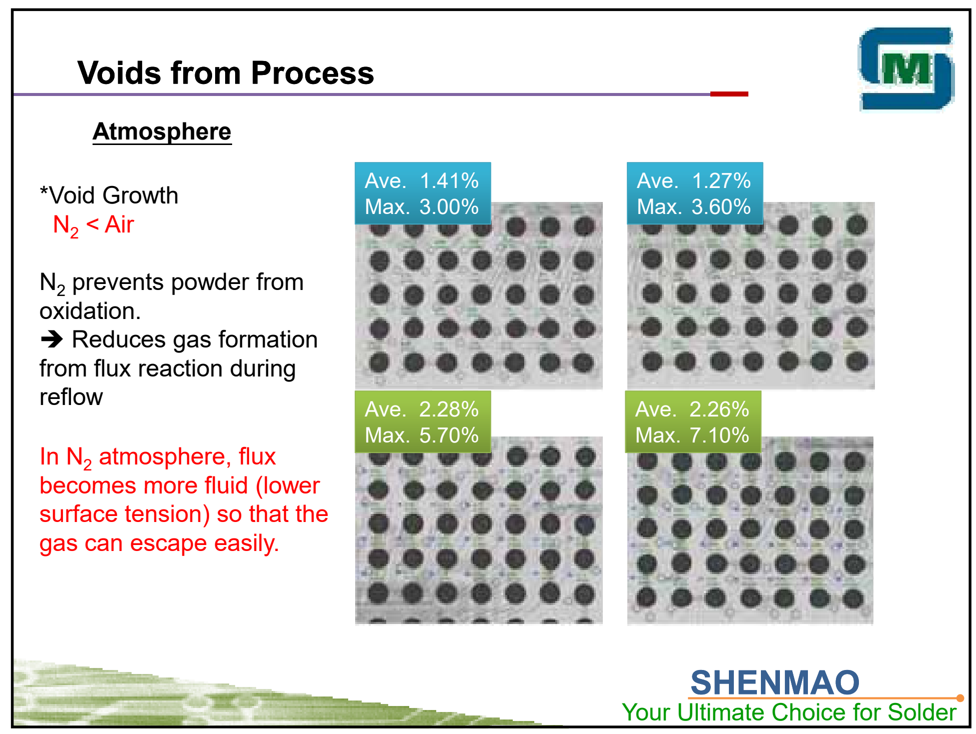
Voids from Process
Atmosphere
*Void Growth
N2 < Air
N2 prevents powder from oxidation.
➔ Reduces gas formation from flux reaction during reflow
In N2 atmosphere, flux becomes more fluid (lower surface tension) so that the gas can escape easily.
Ave. 1.41%
Max. 3.00%
Ave. 1.27%
Max. 3.60%
Ave. 2.28%
Max. 5.70%
Ave. 2.26%
Max. 7.10%
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Voids from Process

Vacuum Reflow

- **Gas evacuates from molten solder easily**
- Cycle time is 30-60 sec or longer (in-line reflow oven)
- Costs much more than conventional reflow oven
- Minor risk of splash of flux and solder ball
- Minor risk of small sized component shift

Fluxless Reflow (in Formic Acid Atmosphere)

- **No Flux ≈ No Gas Generation**
- Cycle time
- Limited cleaning and reduction ability
- Solder balls need to be fixed in (ball attach / bumping / pre-solder) process

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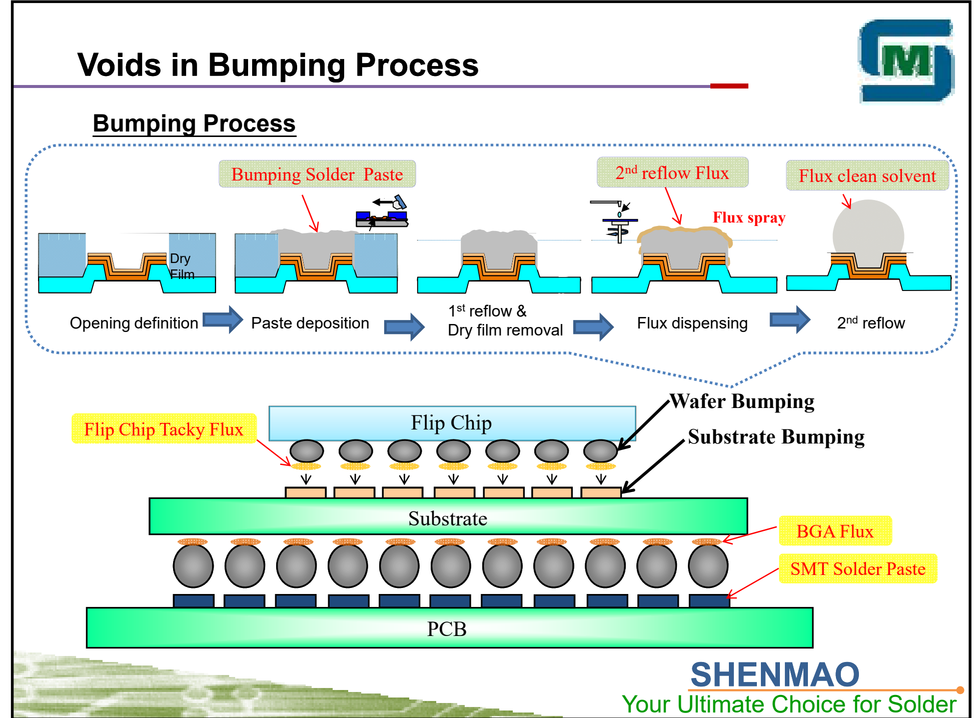
Voids in Bumping Process

Bumping Process



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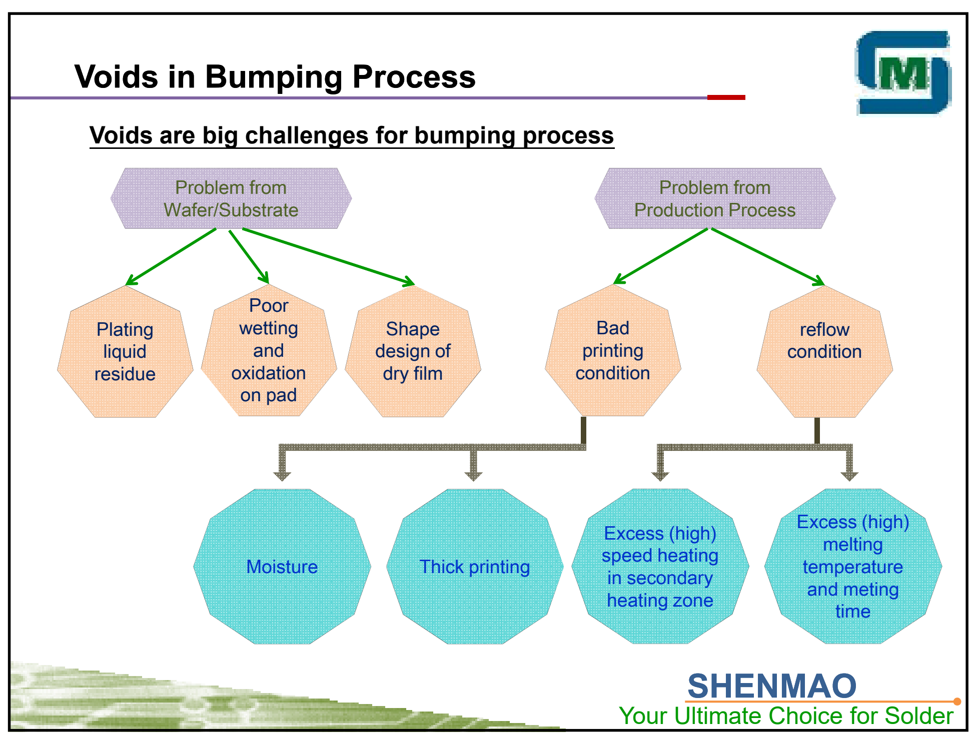
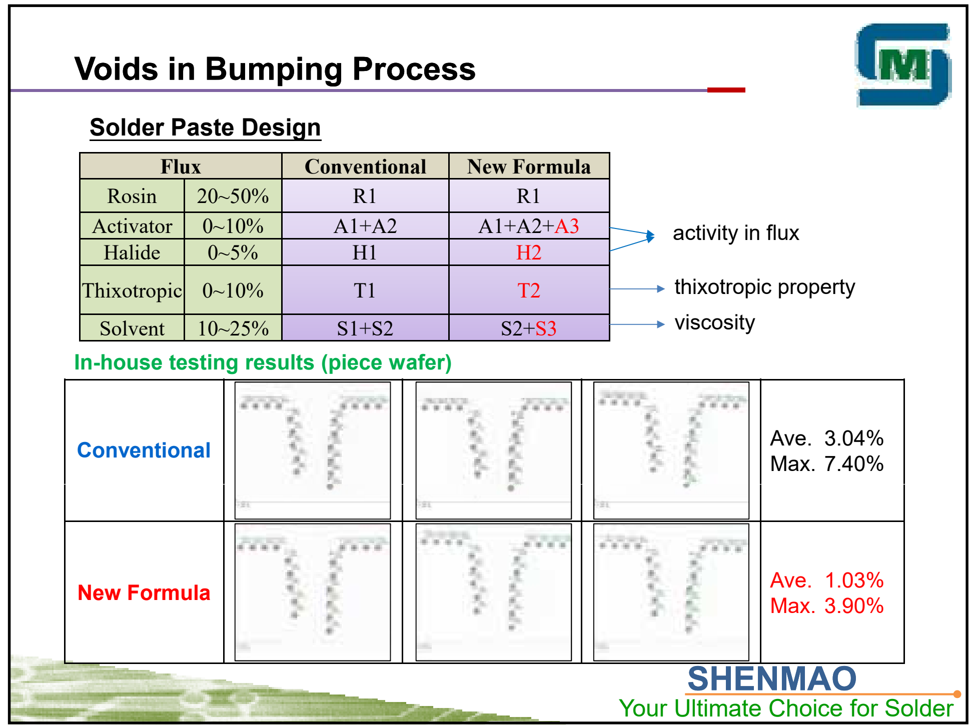
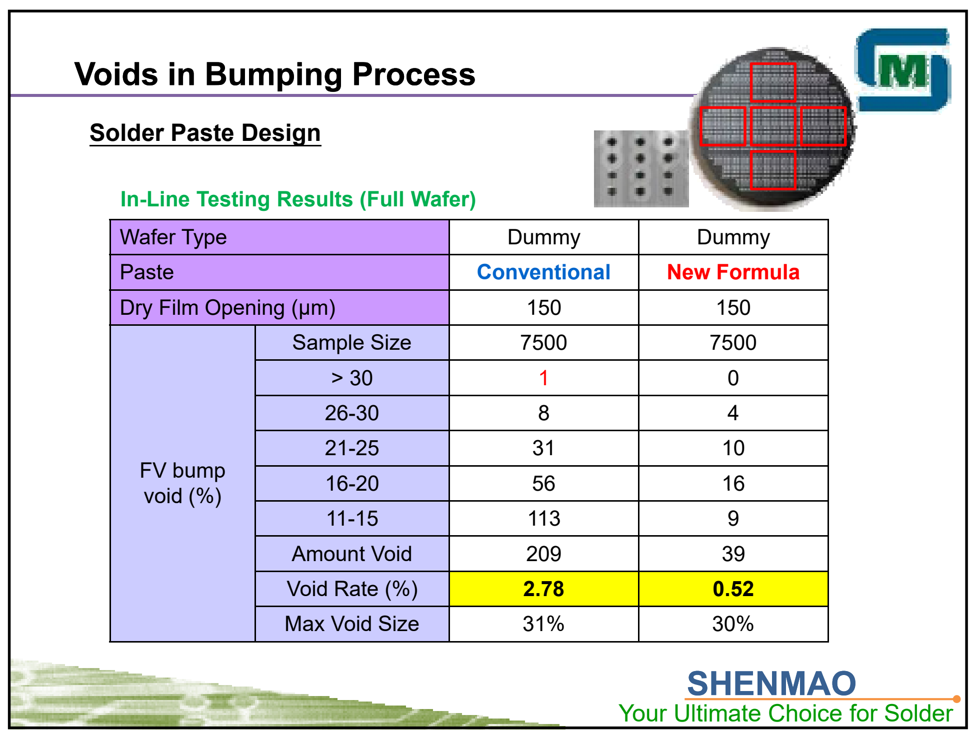




Flux		Conventional	New Formula
Rosin	20~50%	R1	R1
Activator	0~10%	A1+A2	A1+A2+A3
Halide	0~5%	H1	H2
Thixotropic	0~10%	T1	T2
Solvent	10~25%	S1+S2	S2+S3

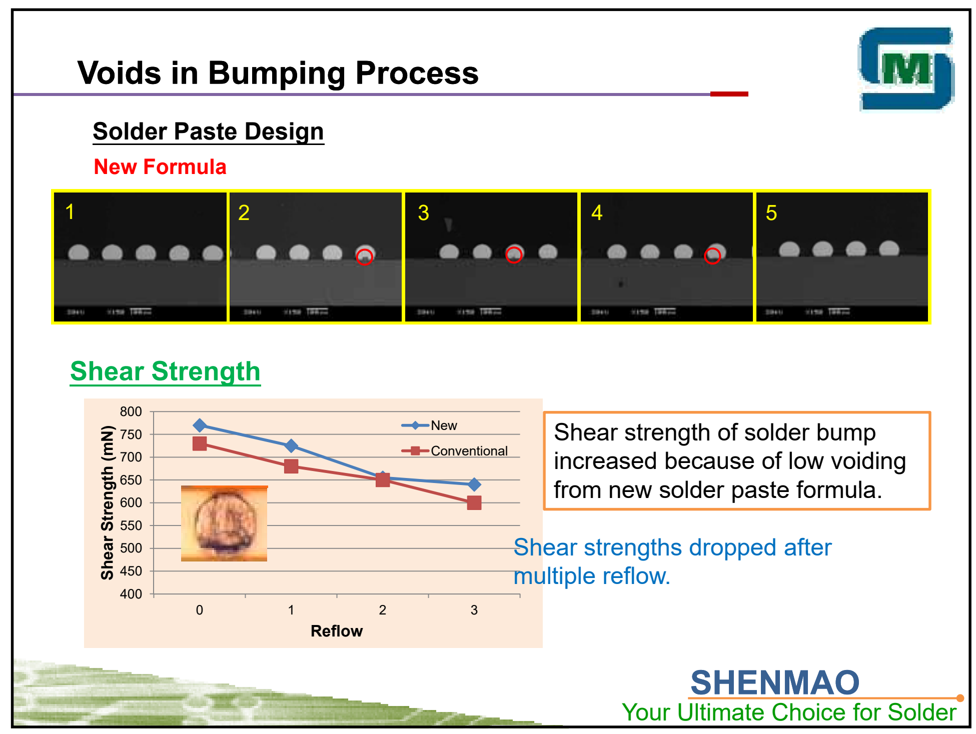


Voids in Bumping Process

Solder Paste Design

In-Line Testing Results (Full Wafer)

Wafer Type		Dummy	Dummy
Paste		Conventional	New Formula
Dry Film Opening (µm)		150	150
FV bump void (%)	Sample Size	7500	7500
	> 30	1	0
	26-30	8	4
	21-25	31	10
	16-20	56	16
	11-15	113	9
	Amount Void	209	39
	Void Rate (%)	**2.78**	**0.52**
	Max Void Size	31%	30%



Conclusion

Design

1. **Select a suitable surface finish.**
2. **Choose right solder powder size.**
3. **Avoid microvia.**
4. **Design stencil aperture properly for large ground pad.**

Process

1. **Control the quality of incoming component and PCB. Low cost is not always the best!**
2. **Discuss with solder paste manufacturer for best reflow profile. Or try different soldering paste.**
3. **Use Nitrogen reflow or Vacuum reflow if possible.**

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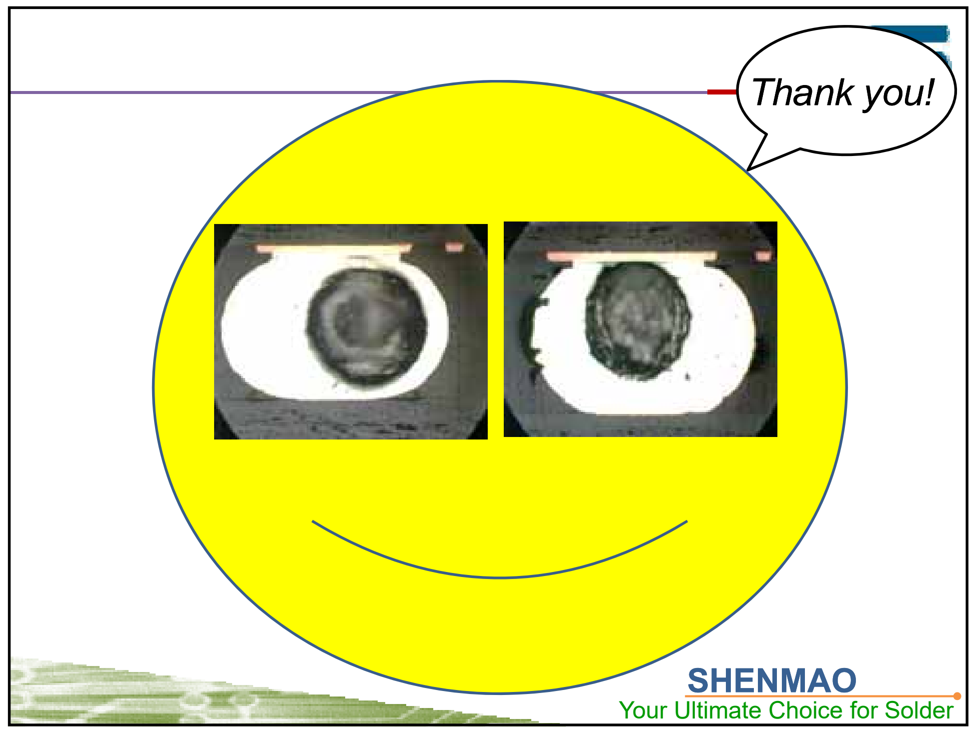

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