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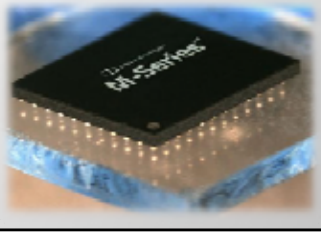
Chips Face-up Panelization Approach For Fan-out Packaging

Oct. 15, 2015

B. Rogers, D. Sanchez, C. Bishop, C. Sandstrom,
C. Scanlan, T. Olson



REV A

Background on FOWLP

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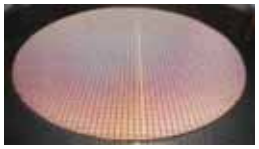
Fan-Out Wafer Level Packaging

- Chips embedded in molded panel
- IOs fanned in and out over mold surface using polymer and RDL buildup layers



Conventional fan-out

Benefits

- WLCSP-type packaging for chips with high IO count
- Excellent electrical properties and performance
- Smallest possible package form factor
- No custom substrate required
- Multi-chip and SIP applications

Challenges

Reliability, Yield, Cost

First Generation eWLB

Brunnbauer, M. et. al., "Embedded Wafer Level Ball Grid Array (eWLB)," *Electronics Packaging Technology Conference 8th Proceedings*, Dec. 2006.

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Chips Face-up FOWLP

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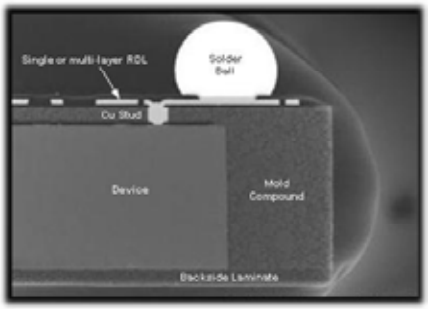

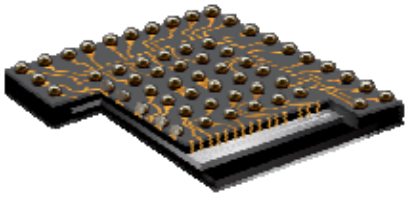

- Front surface of die protected by mold compound
- Cu studs provide current pathways
- Planar surface supports high density RDL
- Adaptive Patterning addresses die shift

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Benefits of Face-up Approach

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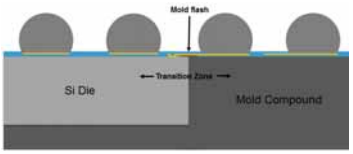
Challenges with exposed die in conventional structure

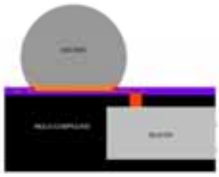
- Mold flash
- Protruding metal from chip singulation
- Polymer or RDL cracking at silicon-mold transition
- Silicon die has poor CTE match to PCB



Conventional fan-out structure

Chips Face-up FOWLP

- Rugged package with encased die
- No discontinuity at die edge
- Improved BLR performance



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Chips Face-up Process Flow

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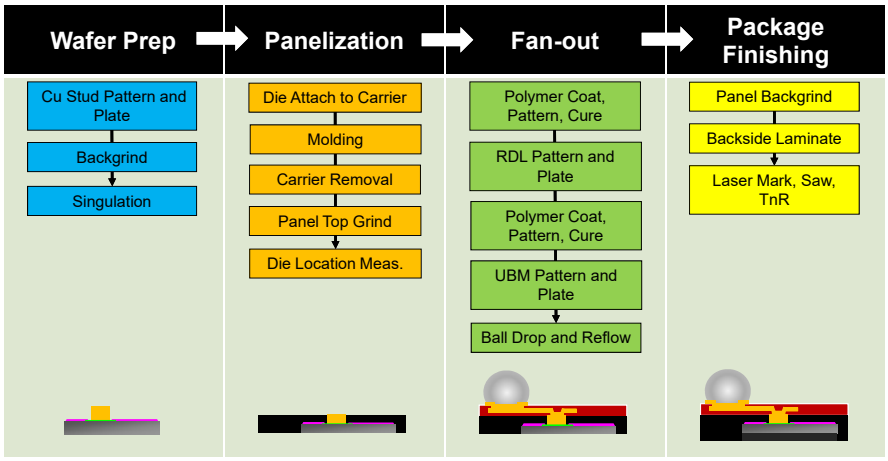

Wafer Prep – Cu Studs

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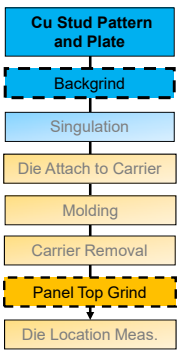


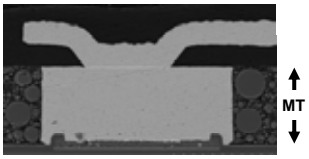
Low cost Cu stud fabrication

- Dry film plating template
- High speed Cu plating
- Minimize Cu stud target height

Cu stud target height = f (MT, BGT, TGT, CSU)

where MT = Final mold thickness target
BGT = Backgrind tolerance
TGT = Panel top grind tolerance
CSU = Cu stud plating non-uniformity

Cu studs on bond pads



Low contact resistance
Good thermal performance

Wafer Prep – Backgrind and Singulation

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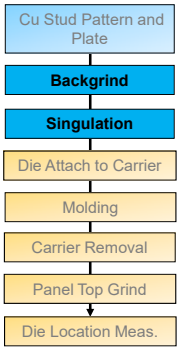
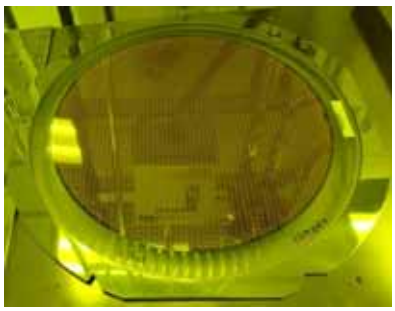


Backgrind

Optimize silicon thickness for panel warpage control

Singulation

Standard laser groove and wafer saw



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Panelization – Die Attach

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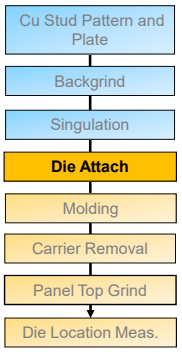
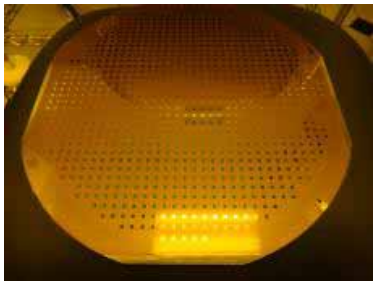


Chips placed face-up on release tape & carrier
Placement accuracy can affect overlay, yield
Serial process -> significant costs



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Panelization – Die Attach

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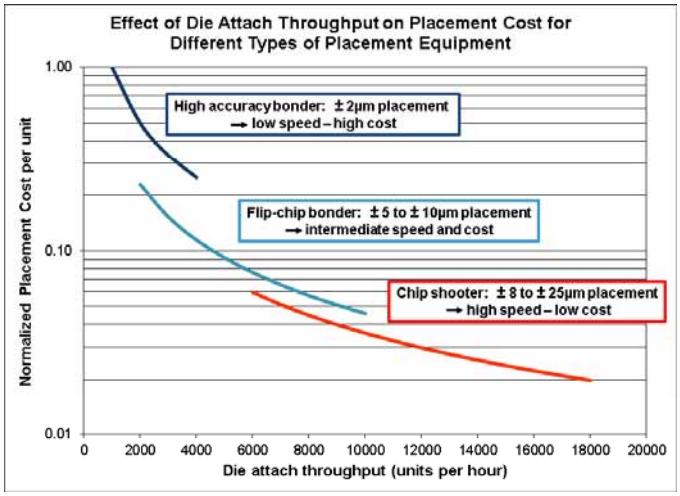

Chip shooter + Adaptive Patterning
⟶ High speed, high yield, low costs

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Panelization – Molding

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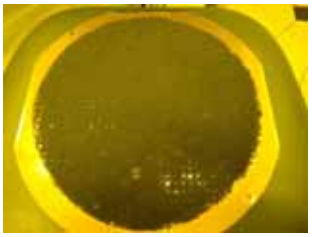
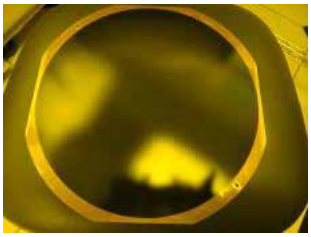
- Cu Stud Pattern and Plate
- Backgrind
- Singulation
- Die Attach to Carrier
- **Molding**
- Carrier Removal
- Panel Top Grind
- Die Location Meas.

Requirements:

High silica filled mold compound
No surface voids or incomplete molding
Good adhesion of die to release tape





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Panelization – Molding

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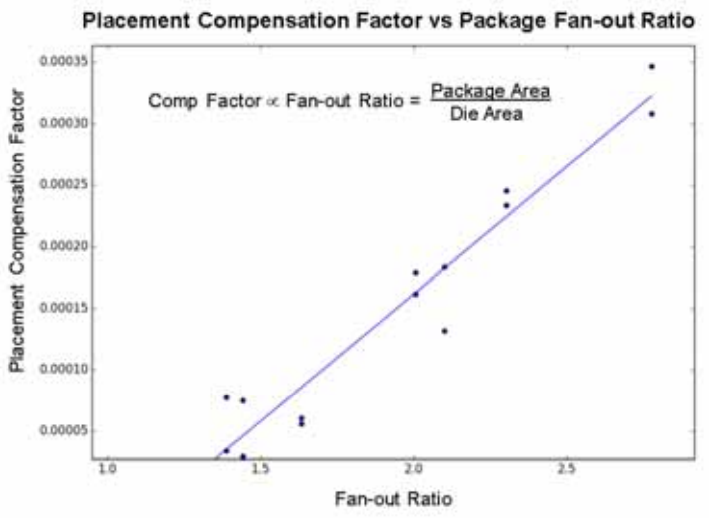

Placement pitch = nominal pitch · (1 + comp factor)

Pitch increased to account for shrinkage during molding

Panelization – Carrier Removal, Top Grind

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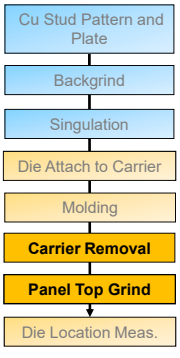
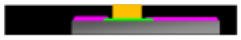


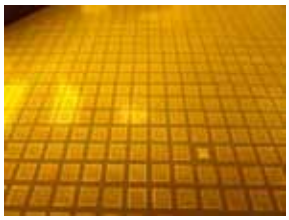
Carrier removal



Panel top grind

Reveal Cu studs and set frontside mold thickness

Mold thickness tolerance = f (BGT, TGT)



Panelization – Die Location Measurement

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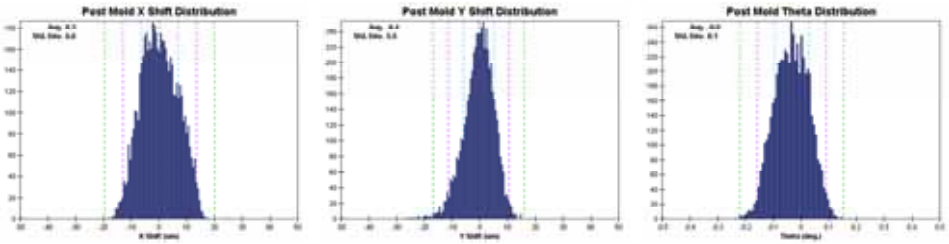
Optical scanner used to determine position and rotation of every die on the panel



Measured X, Y, and angle shifts
3mm X 3mm package on a 300mm panel
Control ~ ± 20um in X and Y, ± 0.2 degrees in theta

Adaptive Patterning

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Customization of design on each package to match actual die location

Process Flow

Inspect Cu stud pattern to determine true position and rotation of each die

↓

Import and optimize die position data in Adaptive Patterning software

↓

Generate adaptive via and RDL patterns for each unit on the panel

↓

Export physical layout of the whole panel for each layer

↓

Expose on lithography system which dynamically implements the unique design per panel

Adaptive Patterning Methods

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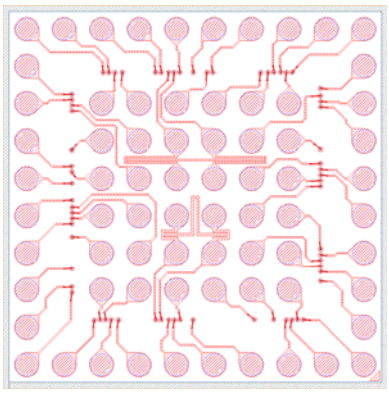
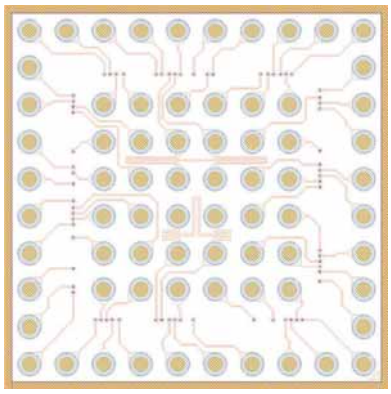
Adaptive Routing

Dynamically adapts RDL routing to accurately align to true die position



Adaptive Alignment

Aligns the entire RDL layer to true die position within the unit



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Adaptive Routing

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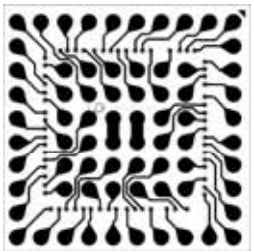
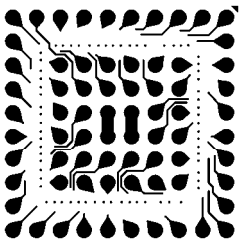
Dynamically adapts Via1 and a portion of RDL pattern of each individual package to align to the true position of each die

Via2, UBM and BGA pattern fixed with respect to package edge

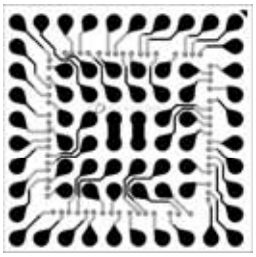
1) Create a nominal fan-out RDL design



2) Omit a small portion of the RDL design near the die pads (prestratum)



3) Complete the design after measuring the true position of each chip



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Effectiveness of Adaptive Routing

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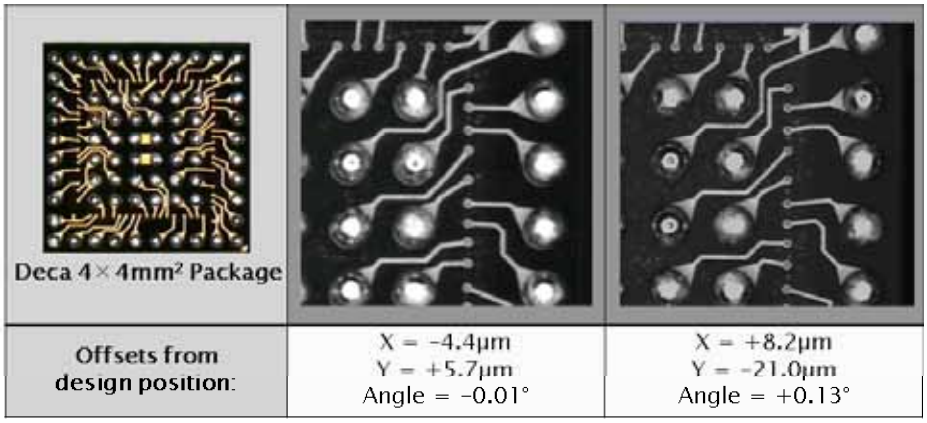

Minimal adjustment in RDL trace lengths, typically 10 to 20µm

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Adaptive Alignment

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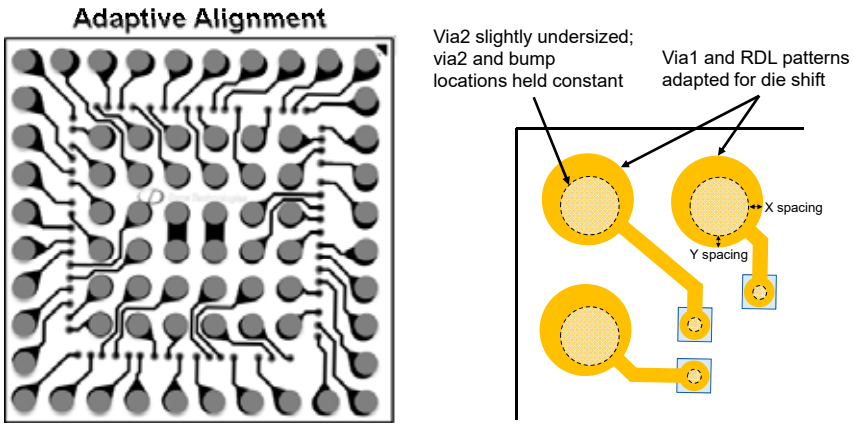
Entire RDL layer and Via1 shift to match die shift; misalignment is effectively moved to the UBM stack

Via2, UBM and BGA patterns remain fixed with respect to package edge



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Post Mold Yield with Adaptive Alignment

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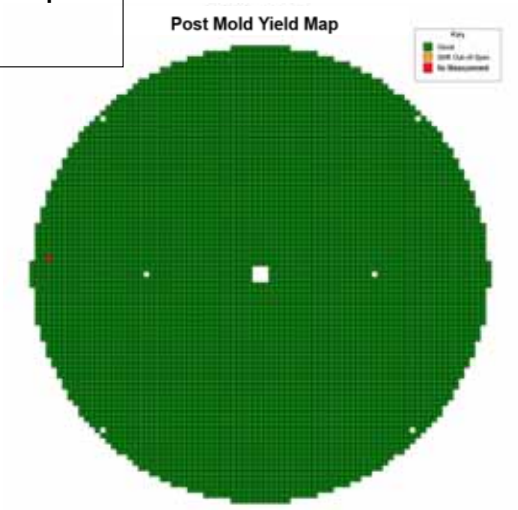
3mm X 3mm package in 300mm panel
± 20um shifts in X and Y,
± 0.2 degrees in theta



- Adaptive Alignment enabled 99.98% overlay yield

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Dual Die Module Example

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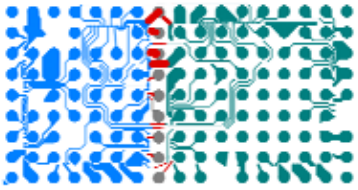
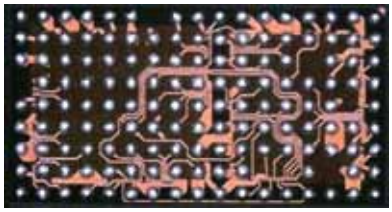
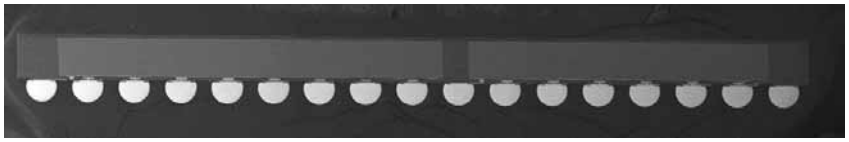
Two die, 4.5 mm x 8.5 mm M-Series package
3.6 x 4.1 mm & 3.5 x 3.17mm devices
Utilizes multi-mode Adaptive Patterning™
  Adaptive alignment over each die
  Adaptive routing on die-to-die connections



Adaptive Patterning™ Simulation





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Fan-out

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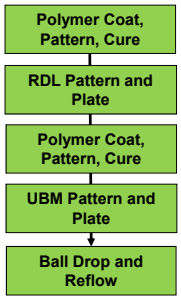
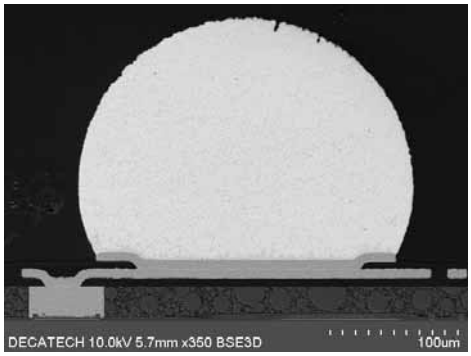


Conventional build-up: polymer 1, RDL, polymer 2, UBM layers + ball drop and reflow

Unique Adaptive Patterning design files facilitate good overlay to chips and Cu studs

Planar mold surface supports high density RDL wiring

Mold layer provides good inductor performance



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Package Finishing

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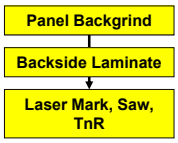
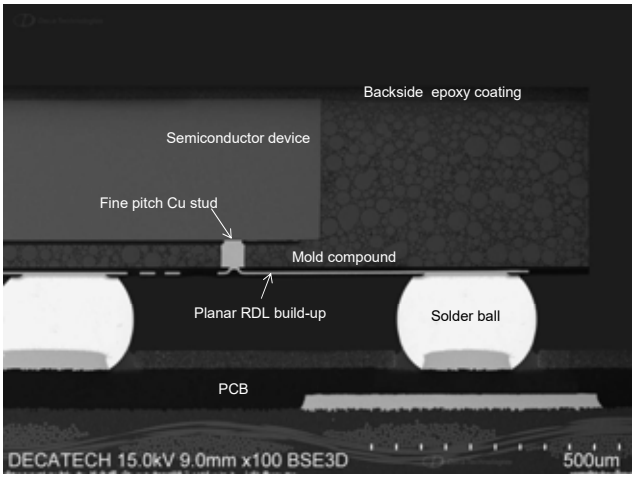


Package finishing used to complete part

Optional backside laminate for fully encased structure



Fully assembled M-Series part

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BLR on 8x8mm Full Array TV

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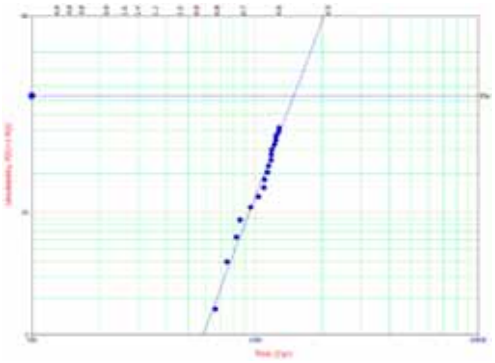
Passed BLR requirements at 8mm X 8mm body size

Test Vehicle	Testing Status	Drop Results	Cycling Results
Full Array 8X8 mm^2	Completed 1500 cycles and 1000 drops	No failures to 256 drops	First failure at 665 cycles

TC Results



Deca internal TV:
8x8mm full array

Testing of larger body sizes currently underway

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FOWLP Cost Challenge

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Conventional approach utilizes wafer fab equipment for build up layers

New approach: Use of solar-based processes

Solar processes applicable to FOWLP

- Patterned polymer
- Sputtered barriers and seed layers
- Electroplated metals
- Thin, warped wafer handling

6" solar wafers

Solar-like wafer and panel flow line created for FOWLP processing

- Low capital investment
- High throughput: > 100 wafers or panels per hour for wafer prep and fan-out processes

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FOWLP Manufacturing Formats

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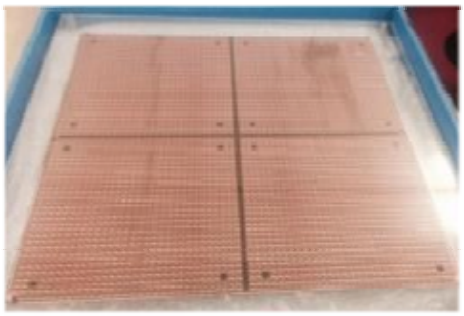
Currently 300mm round, with large panel in development

Initial production

300mm round

Large Panel Future Production



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Summary

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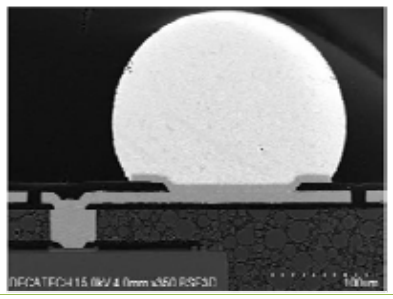
Advantages of chips face-up approach with Adaptive Patterning:

1) Low contact resistance to Al pads
2) Low chip attach costs
3) High yields through mold and Via1 overlay
4) Tight ground rules
5) Fully protected die edge
6) Planar surface for fine pitch RDL
7) Good RF performance
8) Robust BLR

Challenges:

Minimizing wafer prep costs
Control of grind tolerances



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Thank You