FO-WLP: Drivers for a Disruptive Technology

E. Jan Vardaman, President and Founder

Outline

- Industry trends
- WLP products and drivers
  - Fan-in WLP
  - FO-WLP
- FO-WLP Suppliers
- FO-WLP Variations
- Conclusions
Industry Trends 2016: A Few Observations....

- Industry is in an unprecedented “era of change” as our industry matures
  - Trend in mergers and acquisitions will continue this year
  - This year will be a “strange” year
- PC industry unit volumes remain flat
- Despite IoT “hype” mobile devices such as smartphones still driving unit volumes in semiconductor industry
- Thin products are driving thin package solutions
  - Must meet steep ramp with high volume
- Trend in WLP use for mobile products such as smartphones continues
  - Conventional WLP
  - FO-WLP
- Growth in the use of flip chip packages continues, with quest for lower cost solutions
- Wire bond still workhorse of industry, but higher growth rates in FC and WLP
- Moore’s Law proving more difficult to maintain
  - Next technology nodes become more expensive
  - Rely on semiconductor packaging to achieve lower system cost
  - Driving multi-die and system-in-package (SIP) solutions
- The road ahead requires new developments to lower packaging cost
  - Adoption of new technologies to achieve cost/performance trade-off

Drivers for WLP

- Major applications for WLP......
  - Smartphones (highest volume application)
  - Digital cameras and camcorders
  - Laptops and tablets
  - Medical
  - Automotive
  - Wearable electronics such as watch
- WLP meets system packaging needs
  - Small form factor
  - Need for low profile packages
  - Lower cost (less material)
- Form Factor is key
  - Low profile
  - Limited space on PCB

Source: TPSS.
It’s Not Just iPhones with Lots of WLPs......

- **Samsung smartphones with WLPs**
  - 6 years ago, no WLPs
  - Galaxy 6S has 13 WLPs on main board
- **Japanese domestic smartphones**
  - Sony Xperia Z4 has 13 WLPs
  - Sharp Aquos Zeta has 13 WLPs
- **China handset makers increasingly using WLPs**
  - Huawei Asend G620S has 4 WLPs
  - ZTE Goophone has 3 WLPs
  - Even low-end OPPO Joy has one....
- **On average 5 to 7 WLPs per smartphone and the numbers continue to increase......**

Conventional WLP Applications

- **Conventional WLPs for many device types (analog, digital, sensor, discrete)**
  - Power management IC (PMIC)
  - Audio CODEC
  - RF
  - IPD, ESD protection, filter
  - LED driver
  - Electronic compass
  - Controller
  - MOSFET
  - CMOS image sensors
  - Ambient light sensors
  - EEPROM
- **CAGR of almost 9% from 2014 to 2019**
- **Conventional WLPs trends**
  - Highest I/O count 309 (Fujitsu power management IC)
  - Largest body size in HVM Qualcomm PMIC 6.5 mm x 6.5 mm x 0.71 mm, 0.4mm pitch
  - Increasing number of 0.4mm pitch parts, some 0.35mm pitch
  - Fine pitch parts need high-density PCB to route signals
Chip:
Daisy Chain Test Vehicle
Size: 5 mm x 5 mm
Thickness 450 µm

Package:
Size: 8 mm x 8 mm
Balls: 300 µm dia.
196 I/Os
0.5mm pitch

Source: Infineon.
Fan-In and Fan-Out WLP Compared

Conventional WLP (Fan-In)
- Solder ball
- UBM (Under Bump Metallurgy)
- RDL (Al,Cu)
- Si Chip

Fan-Out WLP (package footprint larger than die)
- Solder ball
- Cu-RDL
- Si Chip
- EMC

Source: STATS ChipPAC

Drivers for FO-WLP

- Smaller form factor, lower profile package: similar to conventional WLP in profile (can be ≤0.4 mm)
- Thinner than flip chip package (no substrate)
  - Can enable a low-profile PoP solution as large as 15mm x 15mm body
- Support increased I/O density
  - Fine L/S (10/10µm)
  - Roadmaps for <5/5µm L/S, future 2/2µm L/S
- Allows use of WLP with advanced semiconductor technology nodes with die shrinks
  - With increased I/O and smaller die can’t “fan-in” using conventional WLP
  - Smaller diameter balls and ball pitch ≤0.3mm board level reliability issues (Qualcomm studies)
- Split die package or multi-die package/SiP
  - Multiple die in package possible
  - Die fabricated from different technology nodes can be assembled in a single package
  - Can integrate passives
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance

Source: STATS ChipPAC.
Multi-Die/SiP FO-WLP Solution

- 2 Layer-RDL Interconnection
- 2 Active Die + 10 Passives 0201 SMD

After Molding
After Pick & Place
After Thin Film Processing, Solder Ball Attach and Singulation

Source: Nanium

Applications for FO-WLP

- Baseband processors (in production many years)
- RF transceivers
- Power management integrated circuits (PMIC)
- Connectivity
- Radar module for automotive
- Near field communication (NFC)
- Audio CODEC
- Security devices
- Microcontrollers
- Memory
- NAND memory controllers
- RF-MEMS
- Application processors (future)

Source: NXP.
Source: TPSS.
Source: Nanium.
Application Processor Packaging Trends

- Thinner package and smaller footprint
  - Today 1.0mm height requirement
  - Future ≤0.8 mm
- 3D IC with TSV provides the ultimate in package height reduction, but continues to be pushed out
- Silicon interposers too expensive for many mobile products
- PoP in high-end smartphones
  - Option 1: Continue with FC on thin substrate
  - Option 2: Embedded AP in bottom laminate substrate
  - Option 3: Fan-out WLP with application processor as bottom package
  - Option 4: Some new format (SWIFT, NTI, etc.)
- FO-WLP AP in bottom PoP
  - Low profile
  - High routing density
  - System integration with competitive cost

Potential RF, PMIC, and AP, Migration to FO-WLP

Source: TPSS.


**FO-WLP Projections**

- Early products included baseband processor (Infineon Wireless Division)
- Device types include RF such as Bluetooth, NFC, GPS, PMIC, automotive radar, connectivity modules, future application processors from TSMC and others
- Many multi-die products in future
- Projecting a CAGR of 87% in unit shipments from 2015 to 2020

Source: TechSearch International, Inc.

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**Why is FO-WLP A Disruptive Technology?**

- **No substrate**
  - Thin-film metallization used for substrate (can go below 5μm L/S)
  - No traditional laminate substrate
  - No underfill
  - Most application processors had been using laminate substrate with flip chip bump interconnect
  - Removes substrate supplier as design partner

- **Infrastructure changes**
  - All packaging can take place at the foundry
  - Assembly can also take place at OSAT but uses a non-traditional OSAT assembly line
  - Requires iC/package co-design

Source: Nanium.
FO-WLP Suppliers Status

- Amkor Technology redeploying FO-WLP with new 300mm line (eWLB) in K4
- ADL Engineering 200mm pilot line in Taiwan
- ASE license for Infineon’s eWLB with 300mm in Taiwan, also offers “chip last” panel version
- Deca Technologies (300mm “panel” format)
- NANIUM (300mm wafer) license for Infineon’s eWLB
- NEPES (300mm line in Korea)
- PowerTech Technology (300mm line future, R&D on panel)
- SPI (300mm wafer)
- STS Semiconductor and Telecommunications (300mm production line in qualification)
- STATS ChipPAC (300mm wafer) purchased by JCET, license for Infineon’s eWLB
- Samsung (internal production expected)
- TSMC (300mm wafer InFO process)
- All China OSATs will offer versions in future
- YOUR NAME HERE

Infineon/IMC eWLB Process Flow

1. Lamination of double sided adhesive foil to a mold carrier
2. Pick & Place of (FE-good tested) chips onto the mold carrier
3. Compression Molding of Reconstituted Wafer
4. De-bonding of molded wafer from carrier
5. Application of dielectric, structuring and curing

Source: Infineon/IMC
Infineon/IMC eWLB Process Flow (Con.)

6. Application of Seed Layer; Application of Plating resist and structuring

7. Application of thick copper redistribution, removal of plating resist and seed layer

8. Application of solder stop, structuring of landing pad for solder ball

9. Soldering of preformed ball onto landing pad (UBM) of RDL Separation

Source: Infineon/IMC

RCP Process Flow

Die place onto carrier tape face down prior to encapsulation.

Mold frame removed, panel separated from carrier, ready to de-tape

Panel cross-section after build up process and bump applied

Source: NEPES
Deca Technologies M-Series Basic Process Flow

Wafer Prep  Panelization  Wafer Fab  Package Finish

Cu Stud Pattern and Plate

Singulation
Molding & Cure
Die Attach to Carrier
Carrier Removal
Panel Front Grind
Die Location Mears.

Polymer Coat, Pattern, Cure
RDL Pattern and Plate
Polymer Coat, Pattern, Cure
UBM Pattern and Plate
Ball Prep and Reflow

Panel Backgrind
Backside Chaffing
Laser Mark, Saw, TrnR

Soldering Graphic

Alternatives to Reconstituted Wafer FO-WLP

- Amkor’s SWIFT
- ASE’s chip last
- Conventional flip chip
- SPIL’s NTI
- Molded Interconnect Substrate (MIS)
- Embedded die solution/panel processing

Source: Amkor.
Source: ASE.
Source: TDK.
Source: SPIL.
**Amkor’s SWIFT™**

- **Target Markets**
  - Mobile, Networking
  - BB, AP, Logic + Memory, Deconstructed SoC
- **Utilizes Existing Bump and Assembly Capability**
  - Polymer based
  - Flexible
    - Multi-die and large die capability
    - Large package body capability
  - Advanced die integration
    - Stepper capability down to 2μm line/space
    - Die shift / orthogonal rotation elimination
    - Down to 30μm in-line copper pillar pitch
  - 3D capability
    - Package stack capability using Cu pillars or TMV

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**Fan Out Chip Last Panel vs Wafer Utilization**

Panel Size: 510x410 mm (209,100mm²) X 2
Strip Size: 240x76.2 mm (X21)
Strip Array: 34x13 => 442 ea

Wafer size: 300mm (70,686mm²)

**6:1 Area**

Source: ASE.
**ASE’s Chip’s Last Package**

- **Uses low-cost coreless substrate**
  - Fine pitch capable (15 L/S today, 12μm L/S development)
  - Manufactured in double panel format
  - Assembled in strip format
  - Multi-die and passives possible
  - Can be bottom PoP
- **Thin package (<375 μm)**
- **High current and thermal handling capabilities**
  - Due to thicker Cu (15-20 μm)
- **Uses existing FC infrastructure**
  - Flip chip with Cu pillar mounted on coreless substrate
  - Mass reflow and molded underfill

**Source:** ASE

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**Molded Interconnect Substrate: Poor Man’s FO-WLP**

- **Leadframe-based technology**
- **MIS-BGA offered by JCET (owns APS), SPIL, Carsem**
- **MediaTek in production for several years with MIS-BGA**
- **Versions offered by other OSATs called routable QFN**

**Source:** JCET
MIS Process Flow

- Providing a carrier
- Forming a trace layer
- Forming a via layer
- Forming a dielectric layer over the trace and via layer
- Removing part of the dielectric layer to expose the via layer
- Removing the carrier to expose the trace layer

Source: APS.

- Leadframe supplied by leadframe maker using special process
- Limited number of leadframe suppliers capable of supplying

Embedded Active Package Solutions

- ASE Embedded Electronics (new JV company with TDK)
- AT&S
- DNP
- General Electric
- Infineon
- Microsemi
- Schweizer
- Shinko Electric
- Taiyo Yuden
- TDK
- Texas Instruments
- Unimicron

Source: Chipworks

Source: TDK.

Source: TI.
Conclusions

- Mobile products require low profile packages that meet performance needs
  - Fan-in WLP
  - FO-WLP
- Shrinking technology nodes => shrinking die => less area for I/O (if pitch does not shrink)
  - Drives migration from Fan-In to Fan-Out WLP
- Single and multi-die packages with FO-WLP
- FO-WLP is a disruptive technology
  - Introduction with have impact similar to Intel’s introduction of Cu pillar bump
- Demand for low-cost packaging solutions drives adoption of new package designs and formats
  - New chip last packages?
  - MIS on modified leadframe?
  - Panel-level processing?
- In the year of the Monkey, one must be swift and agile........

Thank you!

TechSearch International, Inc.
4801 Spicewood Springs Road, Suite 150
Austin, Texas 78759 USA
+1.512.372.8987
tsi@techsearchinc.com

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