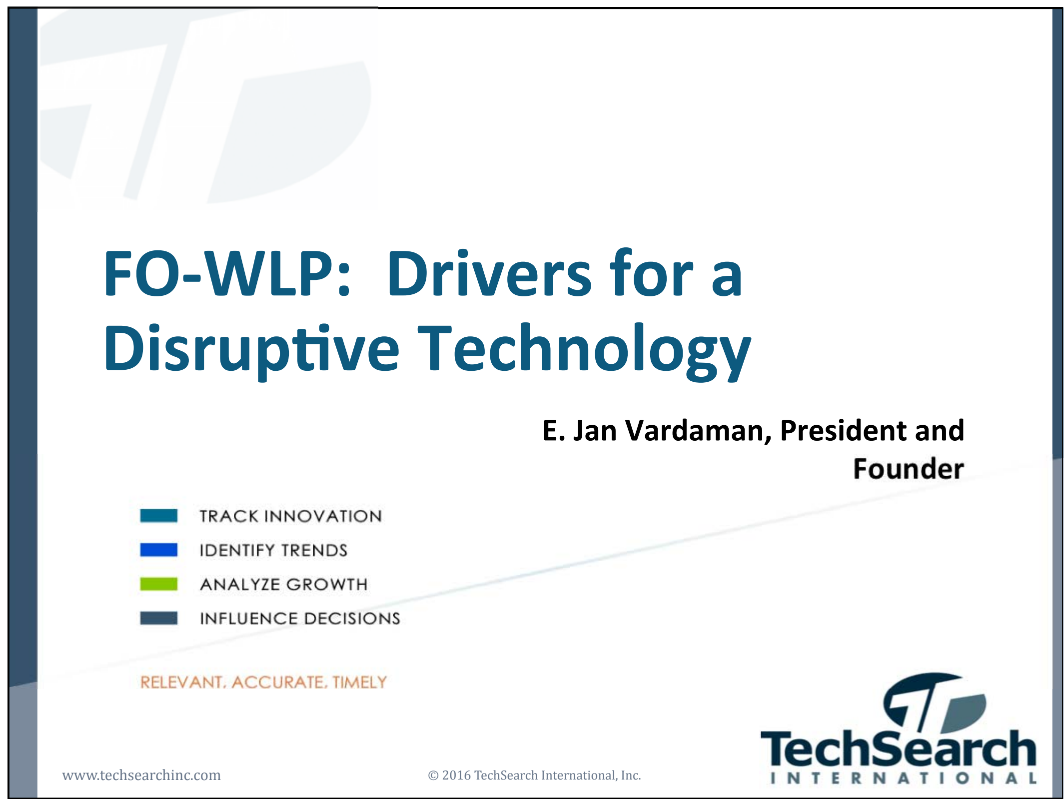
FO-WLP: Drivers for a Disruptive Technology
E. Jan Vardaman, President and Founder
TRACK INNOVATION
IDENTIFY TRENDS
ANALYZE GROWTH
INFLUENCE DECISIONS
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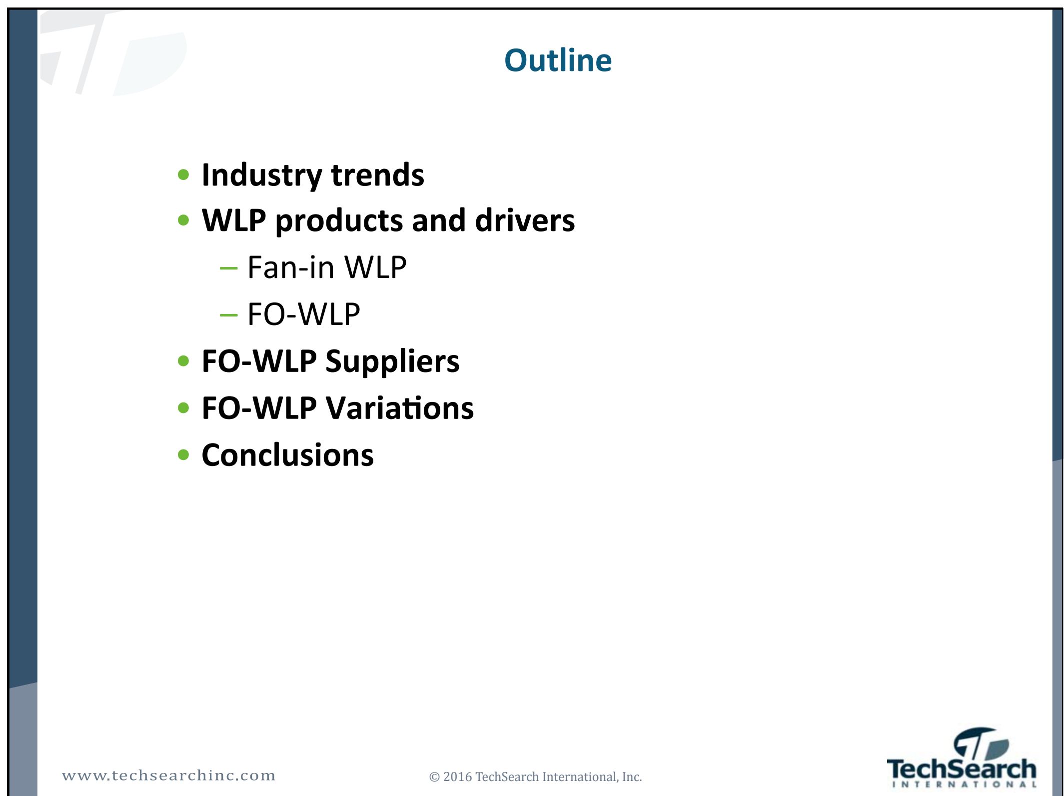
Outline
Industry trends
WLP products and drivers
– Fan-in WLP
– FO-WLP
FO-WLP Suppliers
FO-WLP Variations
Conclusions
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## Industry Trends 2016: A Few Observations….

- **Industry is in an unprecedented "era of change" as our industry matures**
  - Trend in mergers and acquisitions will continue this year
  - This year will be a "strange" year
- **PC industry unit volumes remain flat**
- **Despite IoT "hype" mobile devices such as smartphones still driving unit volumes in semiconductor industry**
- **Thin products are driving thin package solutions**
  - Must meet steep ramp with high volume
- **Trend in WLP use for mobile products such as smartphones continues**
  - Conventional WLP
  - FO-WLP
- **Growth in the use of flip chip packages continues, with quest for lower cost solutions**
- **Wire bond still workhorse of industry, but higher growth rates in FC and WLP**
- **Moore's Law proving more difficult to maintain**
  - Next technology nodes become more expensive
  - Rely on semiconductor packaging to achieve lower system cost
  - Driving multi-die and system-in-package (SiP) solutions
- **The road ahead requires new developments to lower packaging cost**
  - Adoption of new technologies to achieve cost/performance trade-off

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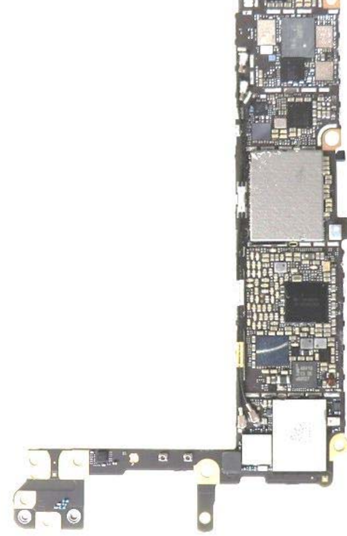
## Drivers for WLP

- **Major applications for WLP……**
  - Smartphones (highest volume application)
  - Digital cameras and camcorders
  - Laptops and tablets
  - Medical
  - Automotive
  - Wearable electronics such as watch
- **WLP meets system packaging needs**
  - Small form factor
  - Need for low profile packages
  - Lower cost (less material)
- **Form Factor is key**
  - Low profile
  - Limited space on PCB



Source: TPSS.

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## It's Not Just iPhones with Lots of WLPs……

- **Samsung smartphones with WLPs**
  - 6 years ago, no WLPs
  - Galaxy 6S has 13 WLPs on main board
- **Japanese domestic smartphones**
  - Sony Xperia Z4 has 13 WLPs
  - Sharp Aquos Zeta has 13 WLPs
- **China handset makers increasingly using WLPs**
  - Huawei Asend G620S has 4 WLPs
  - ZTE Goophone has 3 WLPs
  - Even low-end OPPO Joy has one….
- **On average 5 to 7 WLPs per smartphone and the numbers continue to increase……**

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## Conventional WLP Applications

- **Conventional WLPs for many device types (analog, digital, sensor, discrete)**
  - Power management IC (PMIC)
  - Audio CODEC
  - RF
  - IPD, ESD protection, filter
  - LED driver
  - Electronic compass
  - Controller
  - MOSFET
  - CMOS image sensors
  - Ambient light sensors
  - EEPROM
- **CAGR of almost 9% from 2014 to 2019**
- **Conventional WLPs trends**
  - Highest I/O count 309 (Fujitsu power management IC)
  - Largest body size in HVM Qualcomm PMIC 6.5 mm x 6.5 mmx 0.71 mm, 0.4mm pitch
  - Increasing number of 0.4mm pitch parts, some 0.35mm pitch
  - Fine pitch parts need high-density PCB to route signals

Source: ASE.


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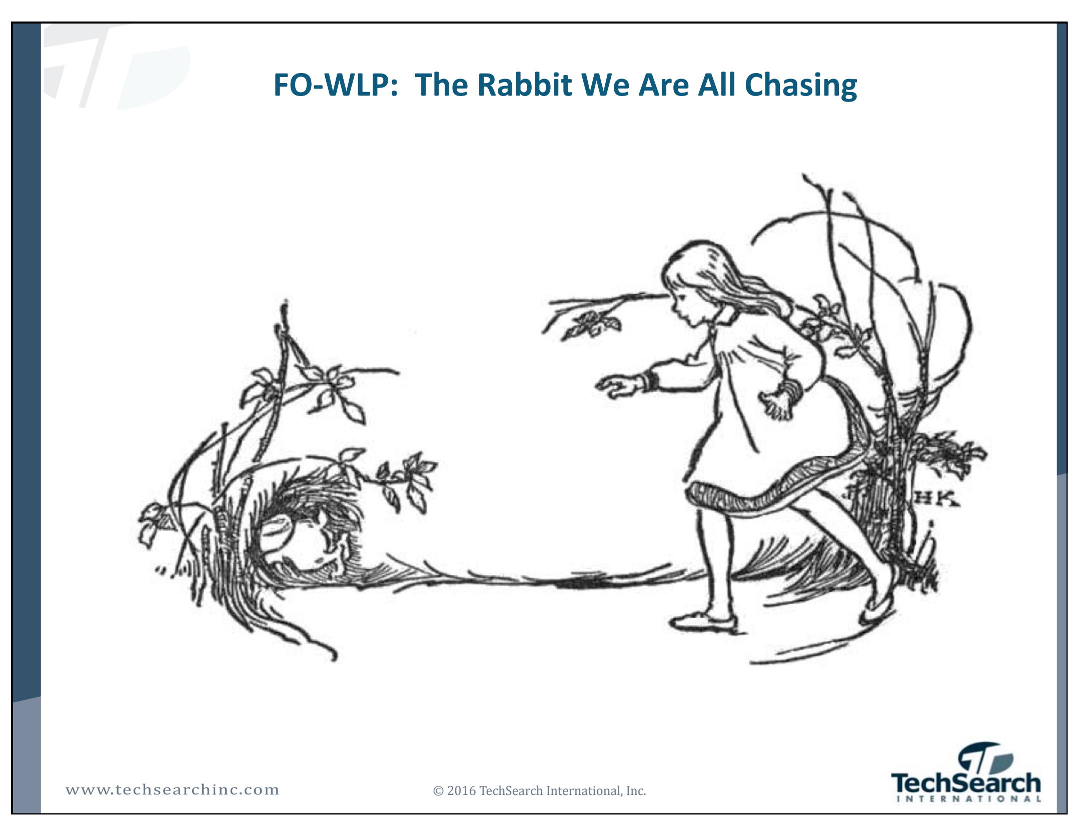
FO-WLP: The Rabbit We Are All Chasing
HK
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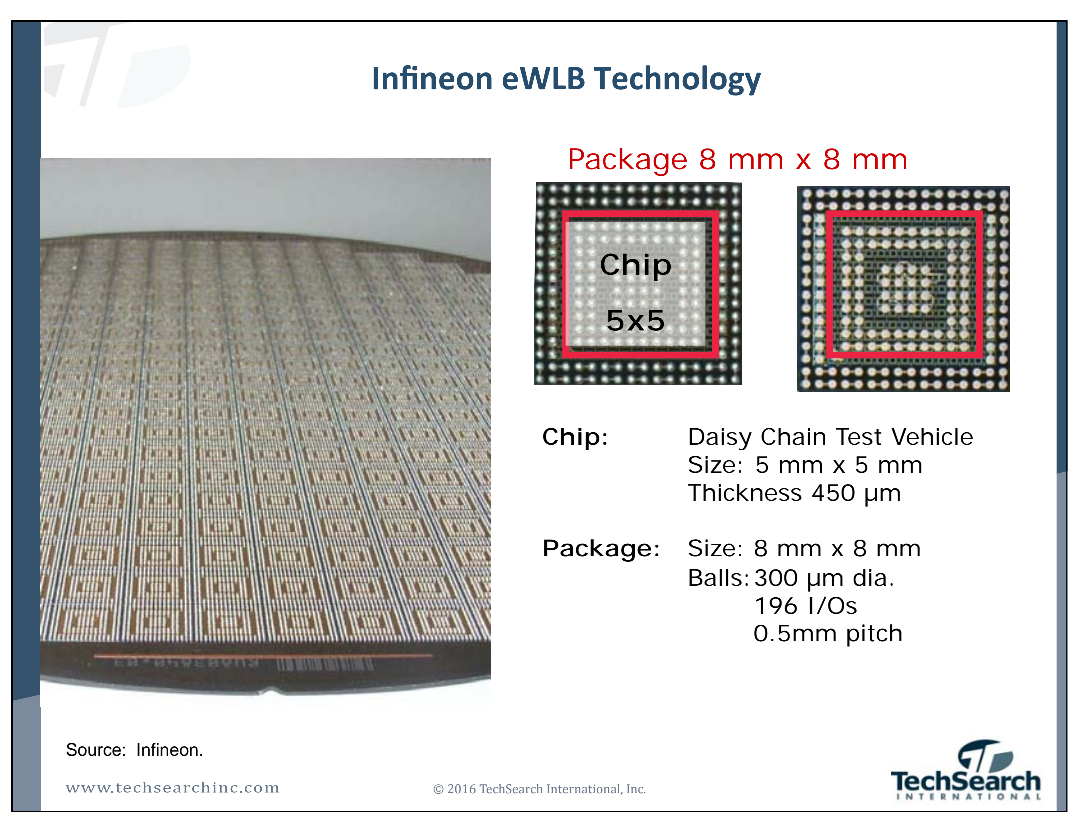
Infineon eWLB Technology
Package 8 mm x 8 mm
Chip
5x5
Chip: Daisy Chain Test Vehicle
Size: 5 mm x 5 mm
Thickness 450 µm
Package: Size: 8 mm x 8 mm
Balls: 300 µm dia.
196 I/Os
0.5mm pitch
Source: Infineon.
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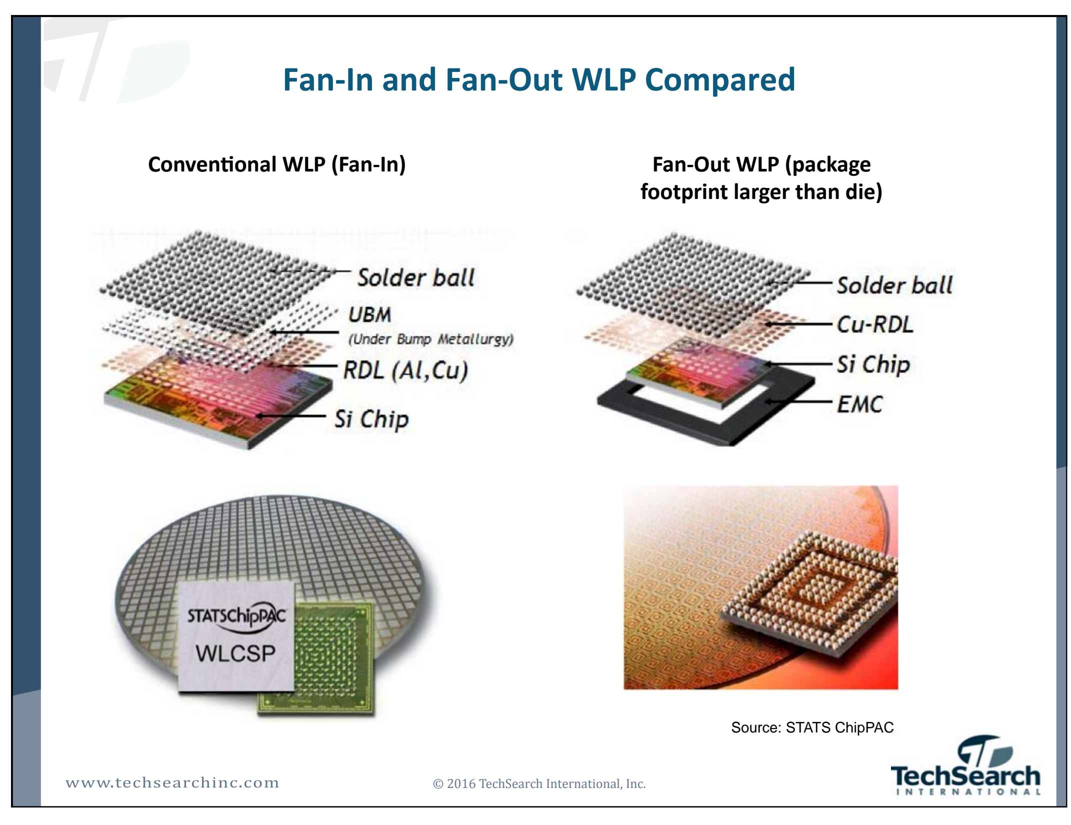
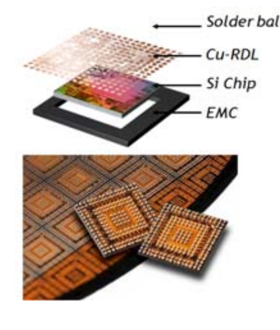



## Drivers for FO-WLP

- **Smaller form factor, lower profile package: similar to conventional WLP in profile (can be ≤0.4 mm)**
- **Thinner than flip chip package (no substrate)**
  - Can enable a low-profile PoP solution as large as 15mm x 15mm body
- **Support increased I/O density**
  - Fine L/S (10/10µm)
  - Roadmaps for <5/5µm L/S, future 2/2µm L/S
- **Allows use of WLP with advanced semiconductor technology nodes with die shrinks**
  - With increased I/O and smaller die can't "fan-in" using conventional WLP
  - Smaller diameter balls and ball pitch ≤0.3mm board level reliability issues (Qualcomm studies)
- **Split die package or multi-die package/SiP**
  - Multiple die in package possible
  - Die fabricated from different technology nodes can be assembled in a single package
  - Can integrate passives
- **Excellent electrical and thermal performance**
- **Excellent high temperature warpage performance**



Source: STATS ChipPAC.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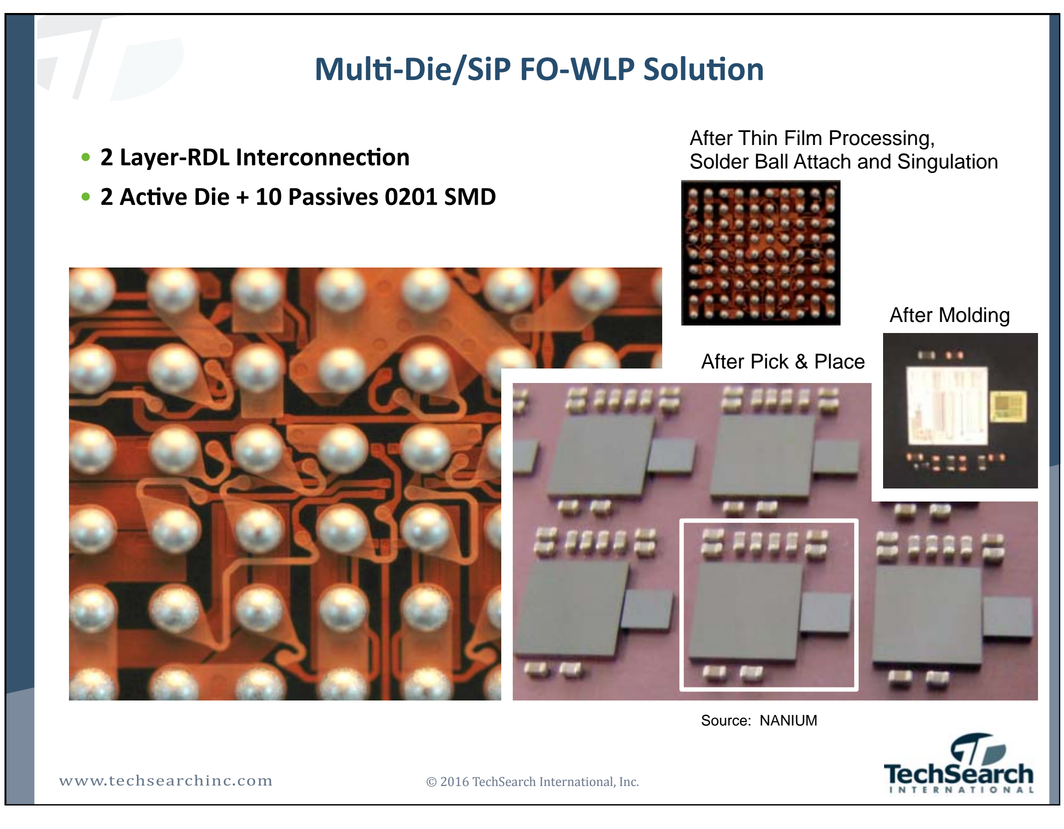

Multi-Die/SiP FO-WLP Solution
2 Layer-RDL Interconnection
2 Active Die + 10 Passives 0201 SMD
After Thin Film Processing, Solder Ball Attach and Singulation
After Molding
After Pick & Place
Source: NANIUM
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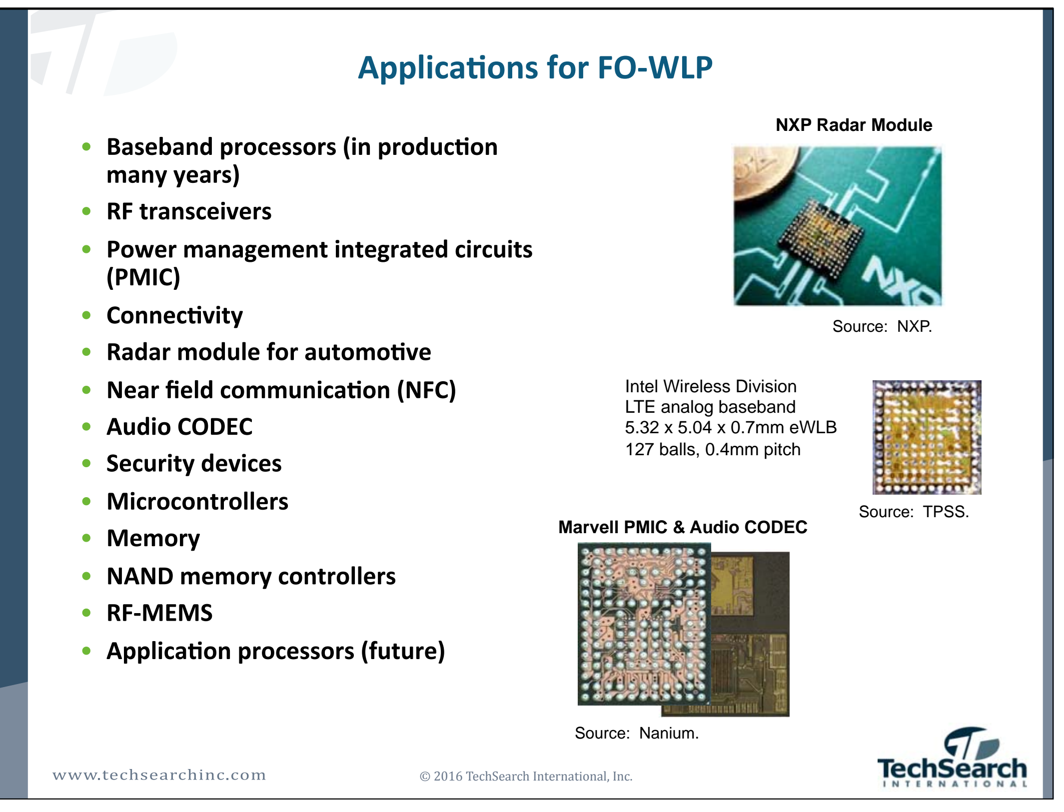

Applications for FO-WLP
Baseband processors (in production many years)
RF transceivers
Power management integrated circuits (PMIC)
Connectivity
Radar module for automotive
Near field communication (NFC)
Audio CODEC
Security devices
Microcontrollers
Memory
NAND memory controllers
RF-MEMS
Application processors (future)
NXP Radar Module
Source: NXP.
Intel Wireless Division
LTE analog baseband
5.32 x 5.04 x 0.7mm eWLB
127 balls, 0.4mm pitch
Source: TPSS.
Marvell PMIC & Audio CODEC
Source: Nanium.
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## Application Processor Packaging Trends

- **Thinner package and smaller footprint**
  - Today 1.0mm height requirement
  - Future ≤0.8 mm
- **3D IC with TSV provides the ultimate in package height reduction, but continues to be pushed out**
- **Silicon interposers too expensive for many mobile products**
- **PoP in high-end smartphones**
  - Option 1: Continue with FC on thin substrate
  - Option 2: Embedded AP in bottom laminate substrate
  - Option 3: Fan-out WLP with application processor as bottom package
  - Option 4: Some new format (SWIFT, NTI, etc.)
- **FO-WLP AP in bottom PoP**
  - Low profile
  - High routing density
  - System integration with competitive cost

Today's PoP (1.0mm)

FO-WLP as Bottom PoP (<0.8mm)

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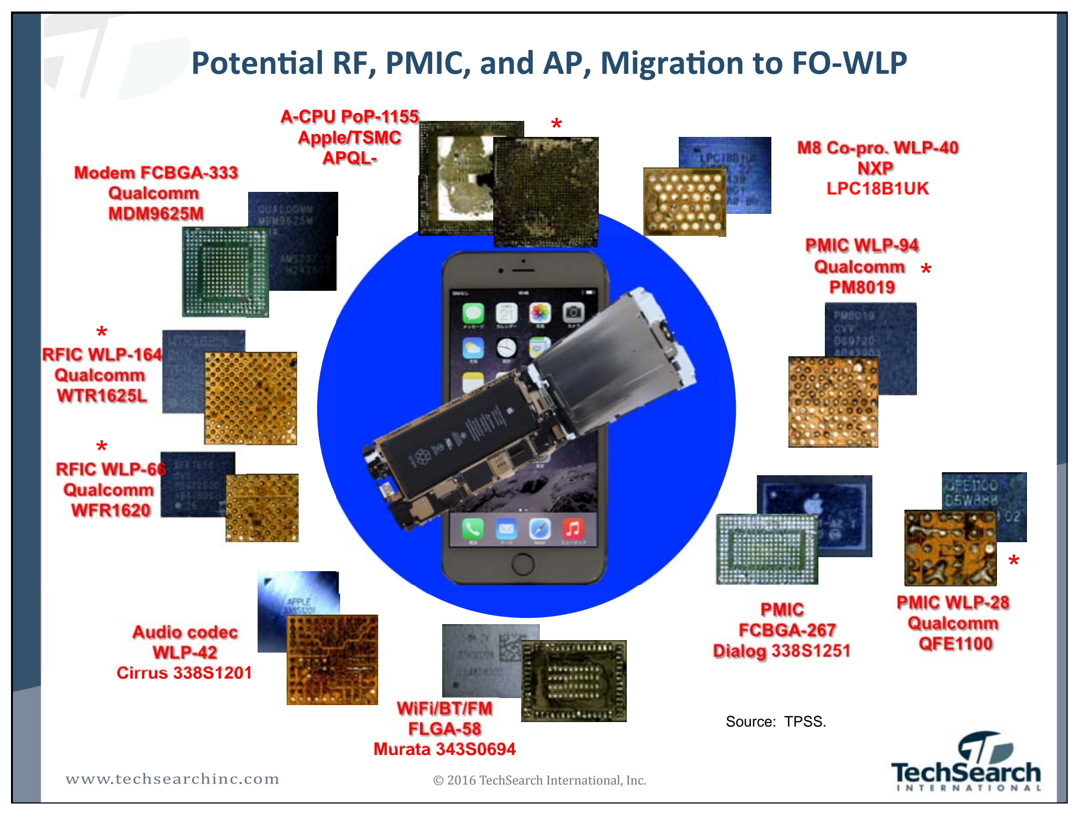
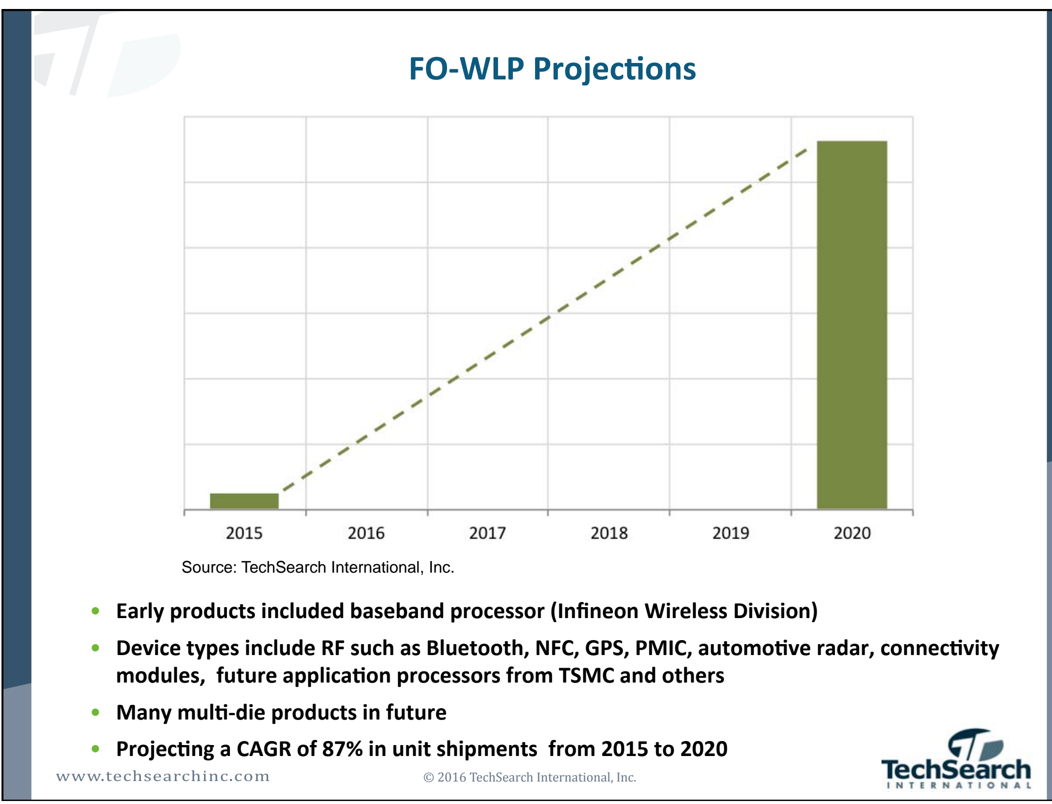
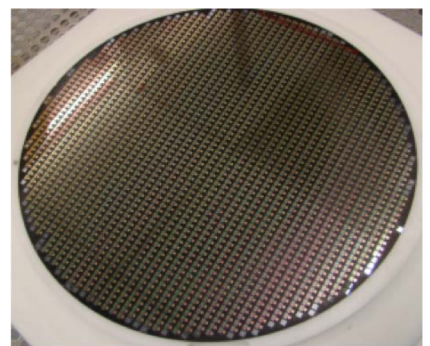





## Why is FO-WLP A Disruptive Technology?

- **No substrate**
  - Thin-film metallization used for substrate (can go below 5µm L/S)
  - No traditional laminate substrate
  - No underfill
  - Most application processors had been using laminate substrate with flip chip bump interconnect
  - Removes substrate supplier as design partner
- **Infrastructure changes**
  - All packaging can take place at the foundry
  - Assembly can also take place at OSAT but uses a non-traditional OSAT assembly line
  - Requires IC/package co-design



Source: Nanium.



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## FO-WLP Suppliers Status

- Amkor Technology redeploying FO-WLP with new 300mm line (eWLB) in K4
- ADL Engineering 200mm pilot line in Taiwan
- ASE license for Infineon's eWLB with 300mm in Taiwan, also offers "chip last" panel version
- Deca Technologies (300mm "panel" format)
- NANIUM (300mm wafer) license for Infineon's eWLB
- NEPES (300mm line in Korea)
- PowerTech Technology (300mm line future, R&D on panel)
- SPIL (300mm wafer)
- STS Semiconductor and Telecommunications (300mm production line in qualification)
- STATS ChipPAC (300mm wafer) purchased by JCET, license for Infineon's eWLB
- Samsung (internal production expected)
- TSMC (300mm wafer InFO process)
- All China OSATs will offer versions in future
- YOUR NAME HERE


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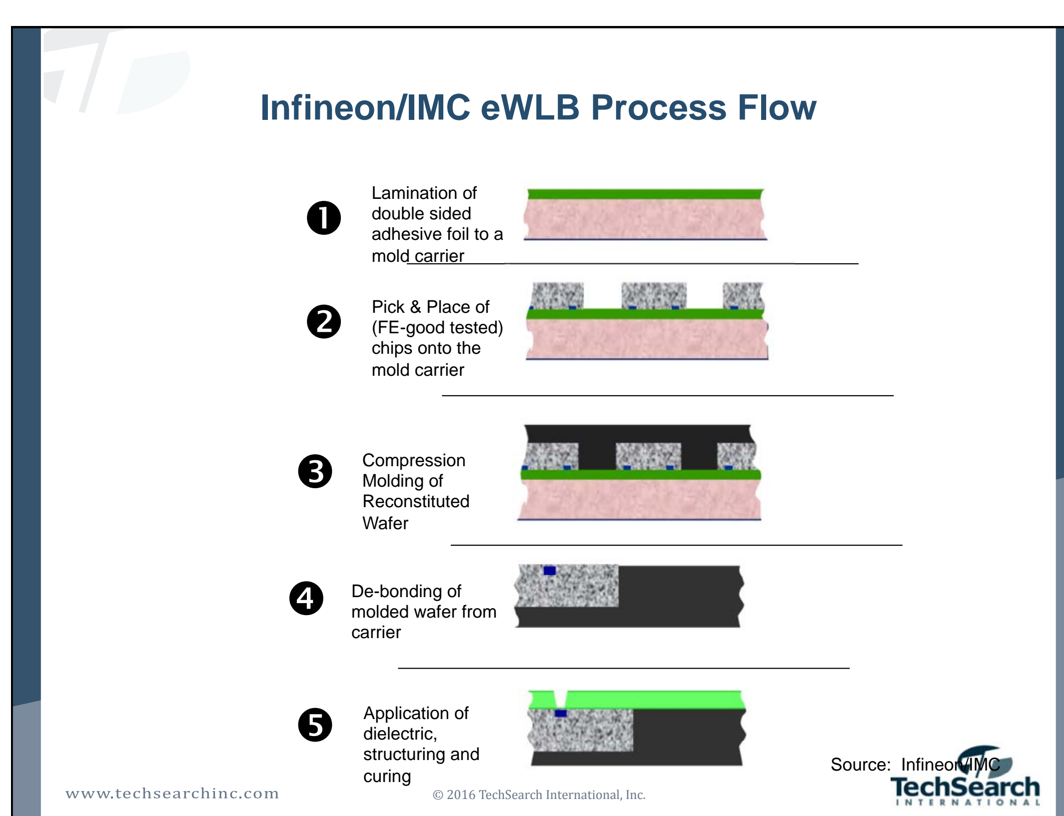

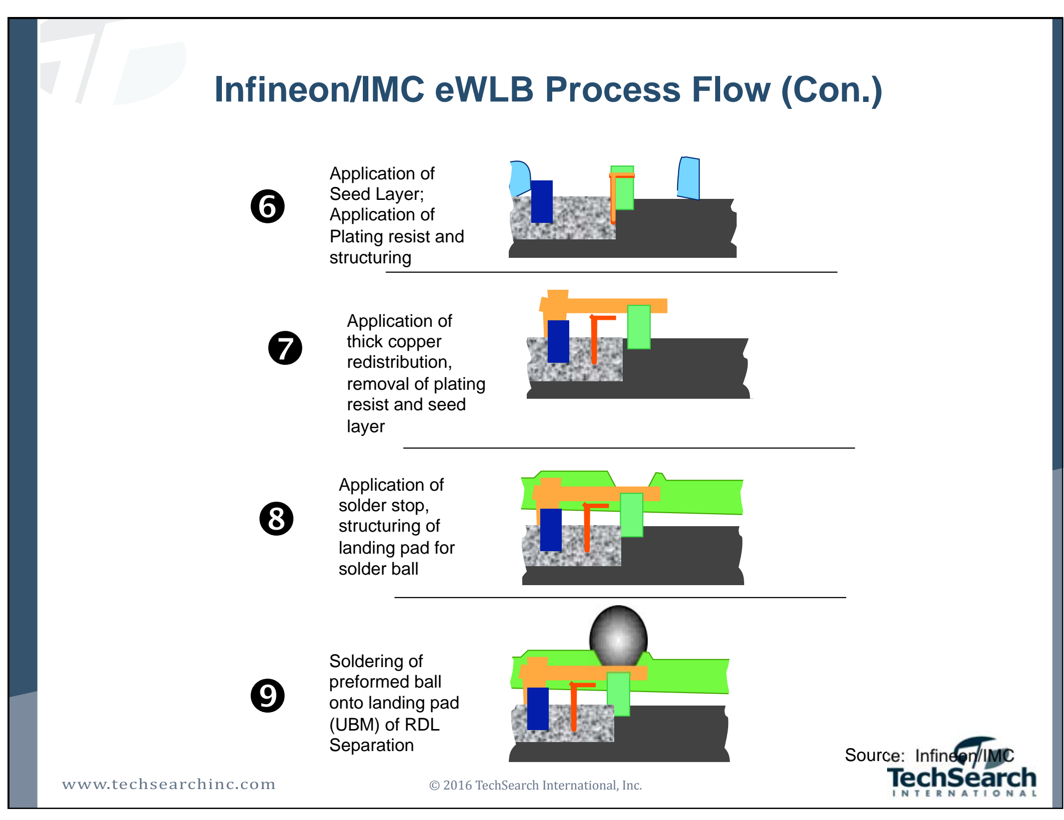
Infineon/IMC eWLB Process Flow (Con.)
6
Application of Seed Layer; Application of Plating resist and structuring
7
Application of thick copper redistribution, removal of plating resist and seed layer
8
Application of solder stop, structuring of landing pad for solder ball
9
Soldering of preformed ball onto landing pad (UBM) of RDL Separation
Source: Infineon/IMC
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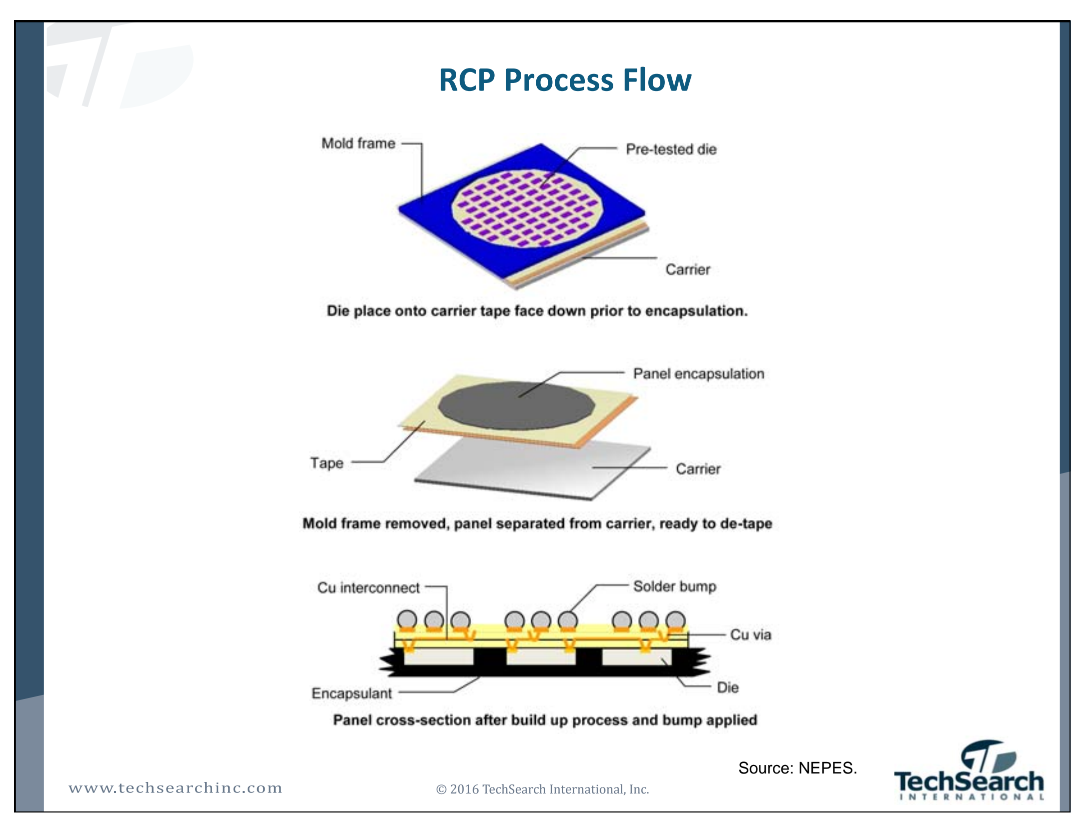
RCP Process Flow
Mold frame
Pre-tested die
Carrier
Die place onto carrier tape face down prior to encapsulation.
Panel encapsulation
Tape
Carrier
Mold frame removed, panel separated from carrier, ready to de-tape
Cu interconnect
Solder bump
Cu via
Die
Encapsulant
Panel cross-section after build up process and bump applied
Source: NEPES.
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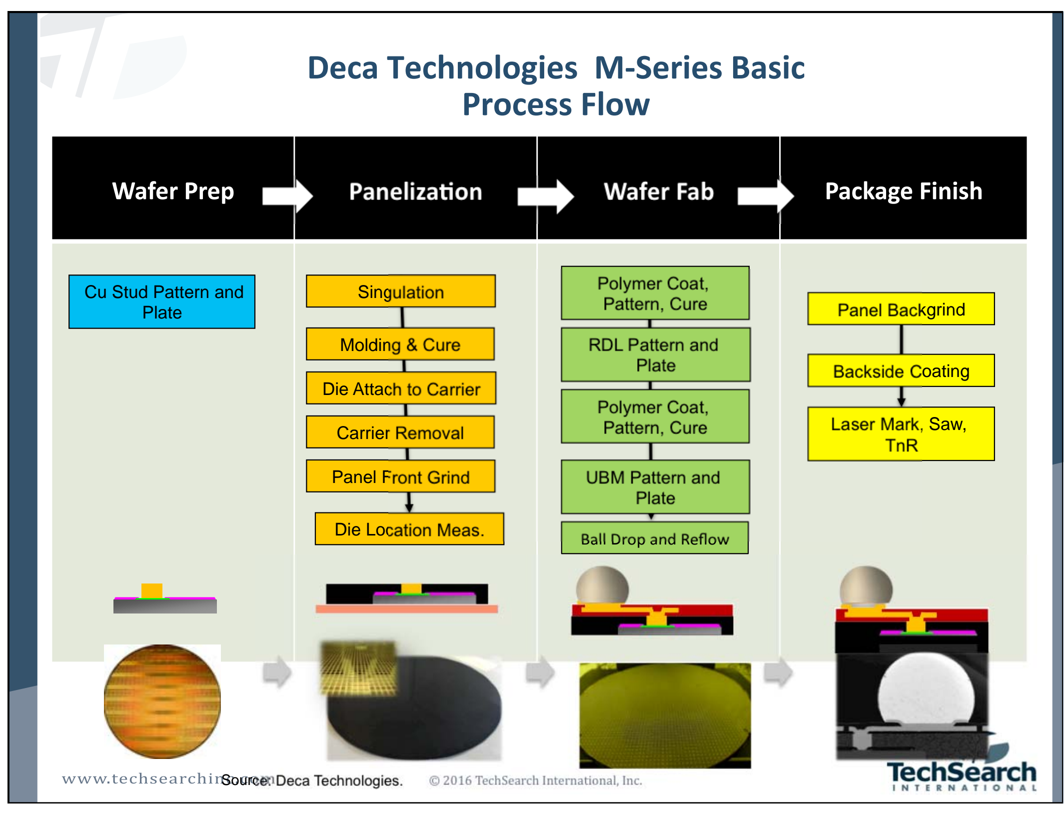
Deca Technologies M-Series Basic Process Flow
Wafer Prep
Panelization
Wafer Fab
Package Finish
Cu Stud Pattern and Plate
Singulation
Molding & Cure
Die Attach to Carrier
Carrier Removal
Panel Front Grind
Die Location Meas.
Polymer Coat, Pattern, Cure
RDL Pattern and Plate
Polymer Coat, Pattern, Cure
UBM Pattern and Plate
Ball Drop and Reflow
Panel Backgrind
Backside Coating
Laser Mark, Saw, TnR
Source: Deca Technologies.
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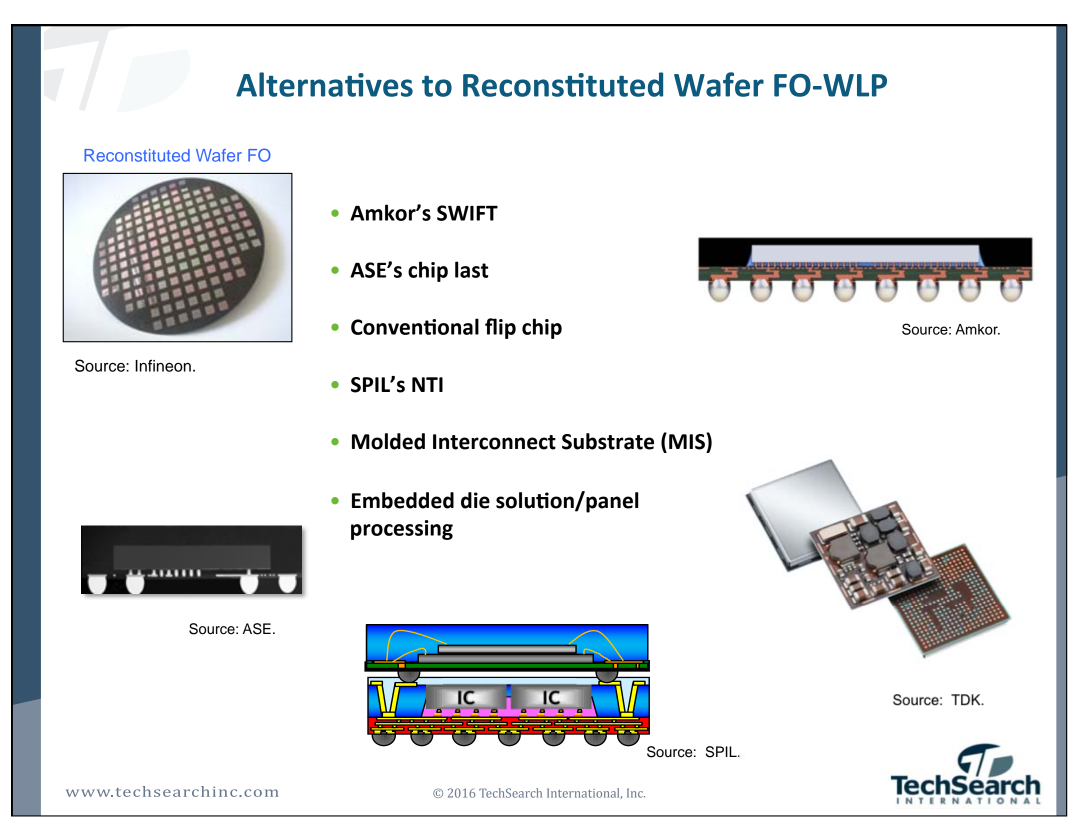
Alternatives to Reconstituted Wafer FO-WLP
Reconstituted Wafer FO
Source: Infineon.
Amkor's SWIFT
ASE's chip last
Conventional flip chip
SPIL's NTI
Molded Interconnect Substrate (MIS)
Embedded die solution/panel processing
Source: Amkor.
Source: ASE.
IC
IC
Source: SPIL.
Source: TDK.
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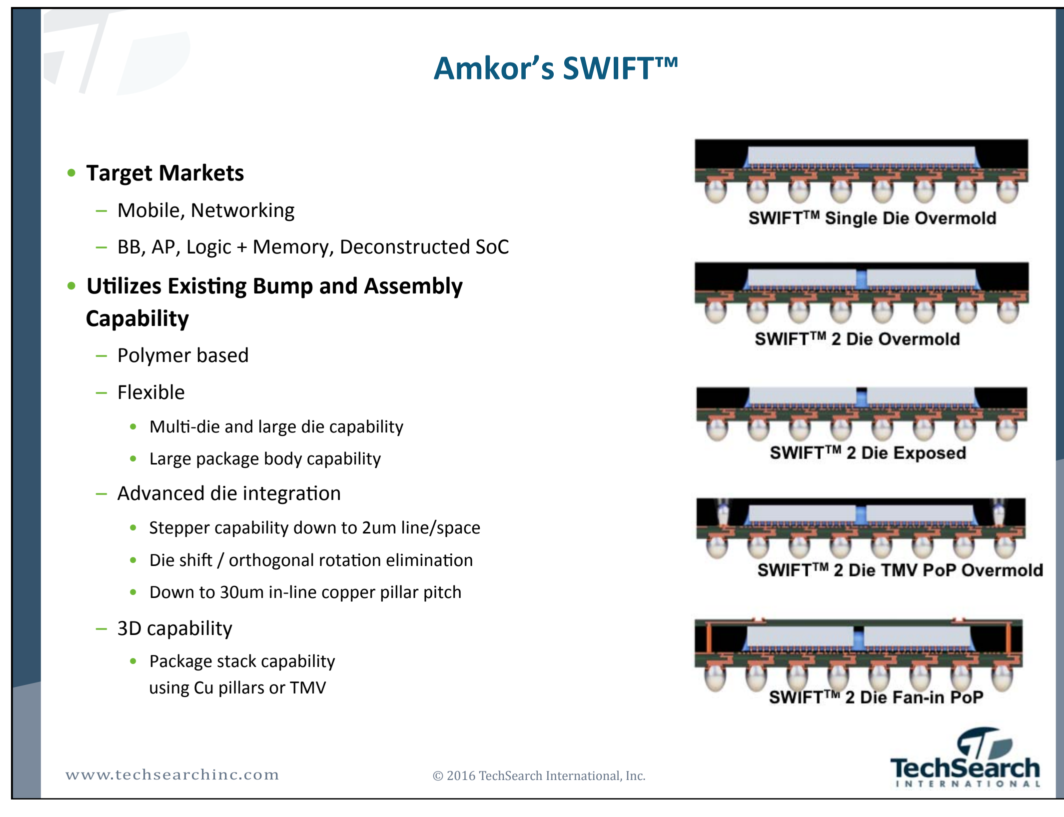
Amkor's SWIFT™
Target Markets
Mobile, Networking
BB, AP, Logic + Memory, Deconstructed SoC
Utilizes Existing Bump and Assembly Capability
Polymer based
Flexible
Multi-die and large die capability
Large package body capability
Advanced die integration
Stepper capability down to 2um line/space
Die shift / orthogonal rotation elimination
Down to 30um in-line copper pillar pitch
3D capability
Package stack capability using Cu pillars or TMV
SWIFT™ Single Die Overmold
SWIFT™ 2 Die Overmold
SWIFT™ 2 Die Exposed
SWIFT™ 2 Die TMV PoP Overmold
SWIFT™ 2 Die Fan-in PoP
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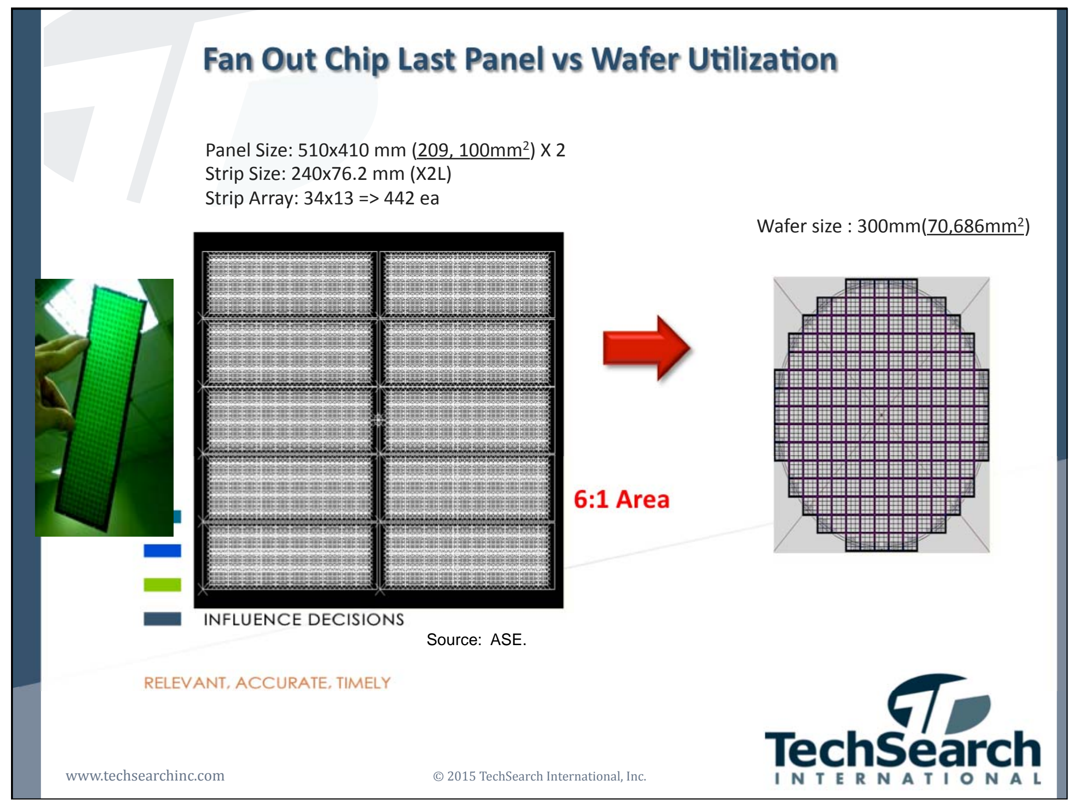
Fan Out Chip Last Panel vs Wafer Utilization
Panel Size: 510x410 mm (209, 100mm²) X 2
Strip Size: 240x76.2 mm (X2L)
Strip Array: 34x13 => 442 ea
Wafer size : 300mm(70,686mm²)
6:1 Area
INFLUENCE DECISIONS
Source: ASE.
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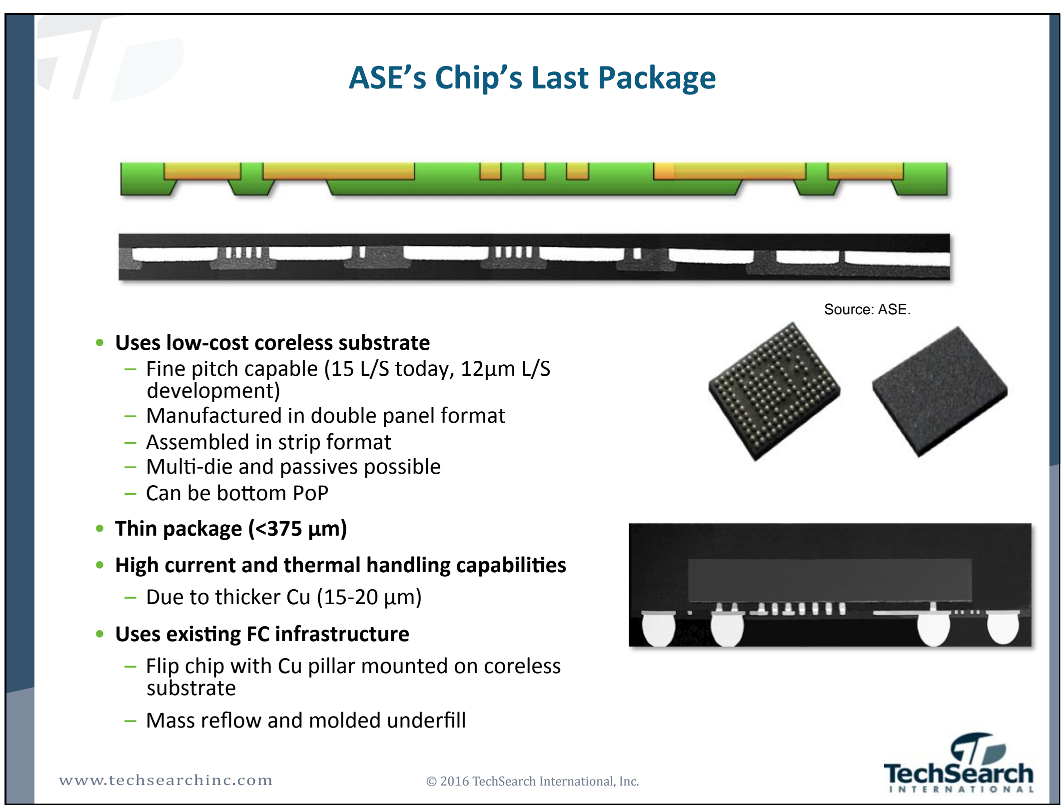
ASE's Chip's Last Package
Source: ASE.
Uses low-cost coreless substrate
Fine pitch capable (15 L/S today, 12µm L/S development)
Manufactured in double panel format
Assembled in strip format
Multi-die and passives possible
Can be bottom PoP
Thin package (<375 µm)
High current and thermal handling capabilities
Due to thicker Cu (15-20 µm)
Uses existing FC infrastructure
Flip chip with Cu pillar mounted on coreless substrate
Mass reflow and molded underfill
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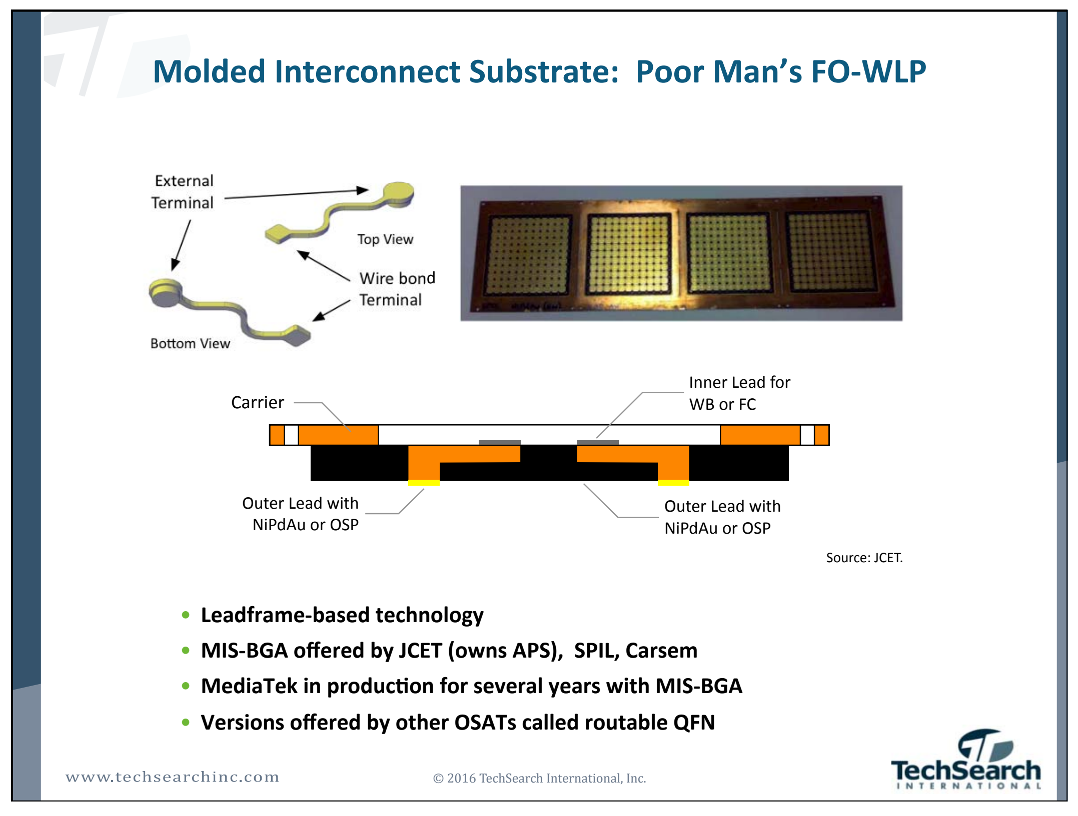
Molded Interconnect Substrate: Poor Man's FO-WLP
External Terminal
Top View
Wire bond Terminal
Bottom View
Carrier
Inner Lead for WB or FC
Outer Lead with NiPdAu or OSP
Outer Lead with NiPdAu or OSP
Source: JCET.
Leadframe-based technology
MIS-BGA offered by JCET (owns APS), SPIL, Carsem
MediaTek in production for several years with MIS-BGA
Versions offered by other OSATs called routable QFN
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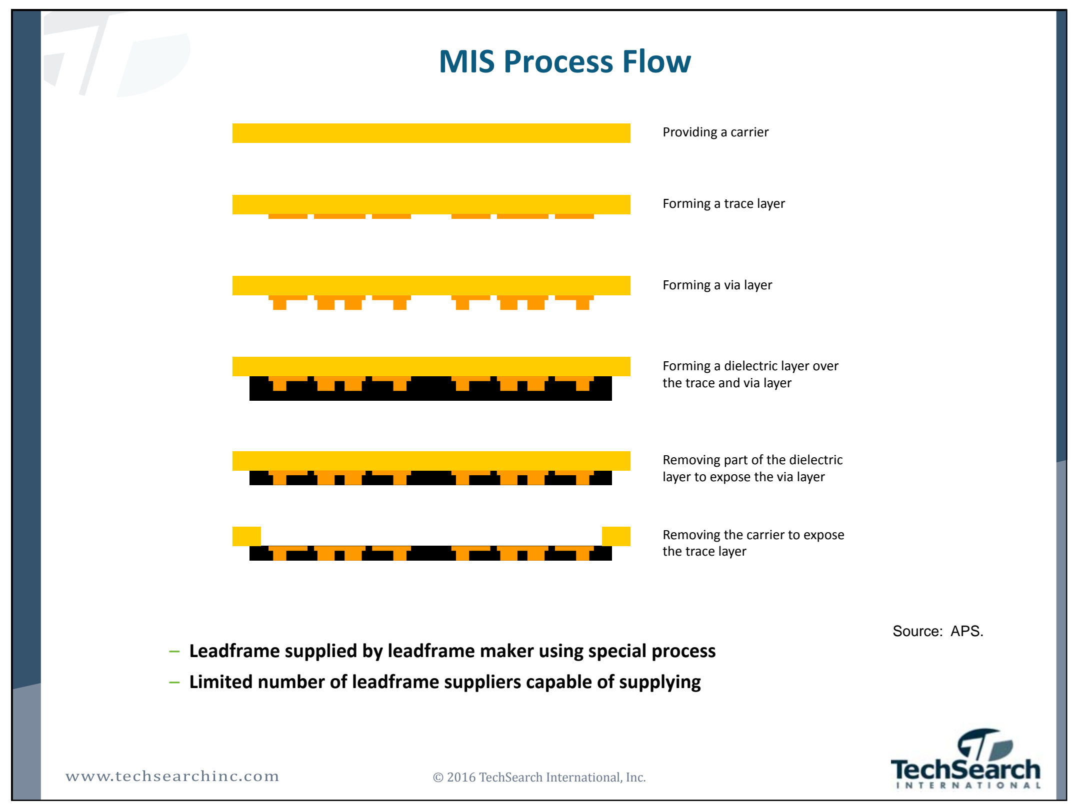
MIS Process Flow
Providing a carrier
Forming a trace layer
Forming a via layer
Forming a dielectric layer over the trace and via layer
Removing part of the dielectric layer to expose the via layer
Removing the carrier to expose the trace layer
Source: APS.
– Leadframe supplied by leadframe maker using special process
– Limited number of leadframe suppliers capable of supplying
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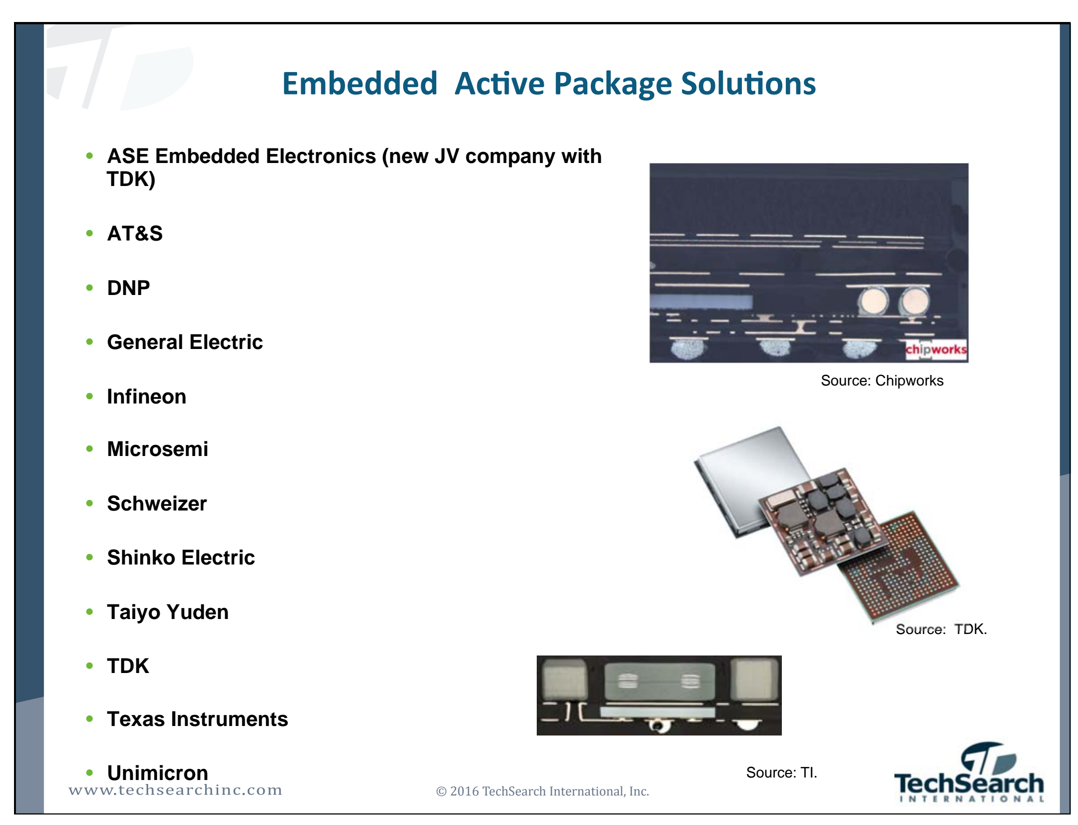
Embedded Active Package Solutions
• ASE Embedded Electronics (new JV company with TDK)
• AT&S
• DNP
• General Electric
• Infineon
• Microsemi
• Schweizer
• Shinko Electric
• Taiyo Yuden
• TDK
• Texas Instruments
• Unimicron
chipworks
Source: Chipworks
Source: TDK.
Source: TI.
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## Conclusions

- **Mobile products require low profile packages that meet performance needs**
  - Fan-in WLP
  - FO-WLP
- **Shrinking technology nodes => shrinking die => less area for I/O (if pitch does not shrink )**
  - Drives migration from Fan-In to Fan-Out WLP
- **Single and multi-die packages with FO-WLP**
- **FO-WLP is a disruptive technology**
  - Introduction with have impact similar to Intel's introduction of Cu pillar bump
- **Demand for low-cost packaging solutions drives adoption of new package designs and formats**
  - New chip last packages?
  - MIS on modified leadframe?
  - Panel-level processing?
- **In the year of the Monkey, one must be swift and agile……..**

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