Emerging IC Packaging Platforms for ICT Systems

- IEEE CPMT Chapter Lunch Meeting

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Outline

- Evolution of Internet
- The Promise of Internet of Everything (IoE)
- Technology Challenges and Potential Solutions
  - System Requirements and Key Drivers
  - Component Technology Innovation
  - Emerging IC Packaging Technology Platforms
- Summary

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Evolution of Internet /
The Promise of Internet of
Everything (IoE)

Moore's Law & Internet: A Historical Perspective

A persevering prediction
Number of transistors in CPU*
Log scale

MOORE'S LAW DEFINED

1960 70 80 90 2000 10 14
Source: Intel   *Central processing unit
Economist.com

Internet Hosts

Stage 1 DARPA Experiment, operation
Stage 2 Enterprise Internets, R&A scaling
Stage 3 Universality

1995-NSFNet ceases, non-USA nets >50%

1990-ARPANet ceases

1989-first public commercial Internets created

1986-NSFNet created

Jan 1983-ARPANet adopts TCP/IP, first real Internet begins

ARPANet

1968 1973 1979 1984 1990 1995 2001

Cisco VNI Forecast, 2014 – 2019

The world's population, number of households, and workforce are growing moderately, but the rate of connectivity is growing faster

www.cisco.com/go/vni

Growth of the Internet of Things (IoT)

Source: Cisco IBSG projections, UN Economic & Social Affairs http://www.un.org/esa/population/publications/longrange2/WorldPop2300final.pdf

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Metcalfe's Law – The Magic of Interconnections

The Systemic Value of Compatibly Communicating Devices Grows as the Square of Their Number:

Cost $\cong$ N

Critical Mass Crossover

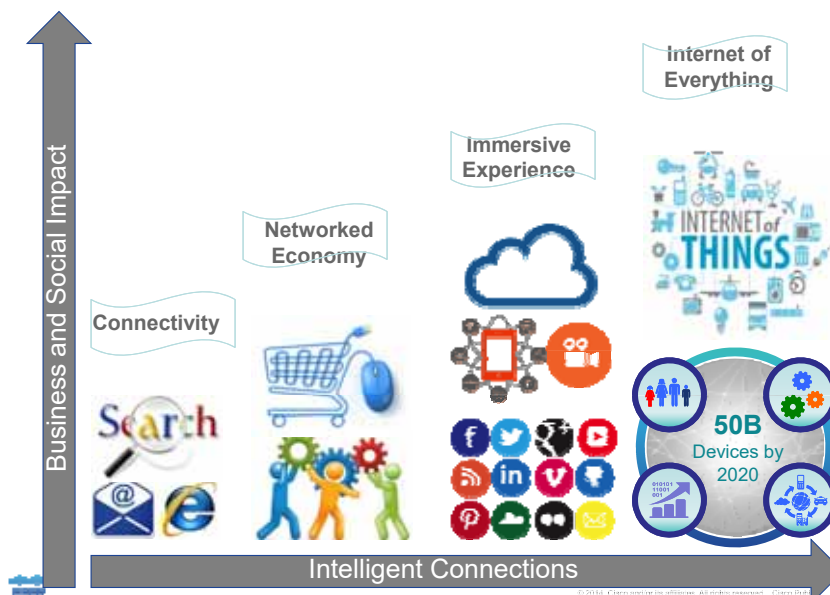Value $\cong$ N²

Dollars

$

N

Devices
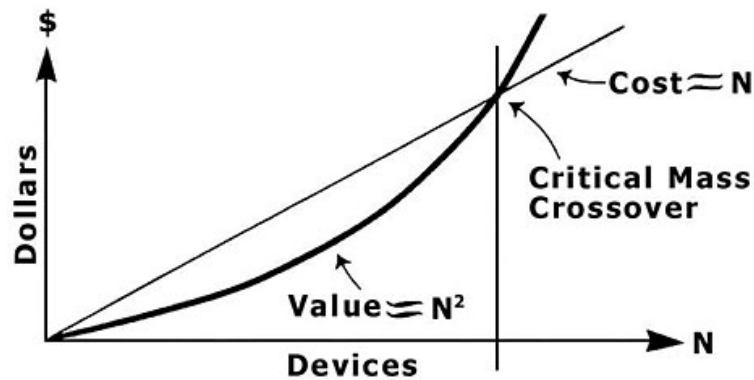
Bob Metcalfe

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## Evolution of Internet – Business Perspective

Business and Social Impact

Internet of Everything

Immersive Experience

Networked Economy

Connectivity

Search

INTERNET of THINGS

50B Devices by 2020

Intelligent Connections

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## Internet of Everything: Key Drivers

Process Manufacturing	Transportation + Logistics	Discrete Manufacturing	Utilities
Real-Time	Scale	Smart Data/ Analytics	Security
Government/ Smart Cities	Healthcare	Retail	Finance

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Technology Challenges – System Requirements and Key Drivers

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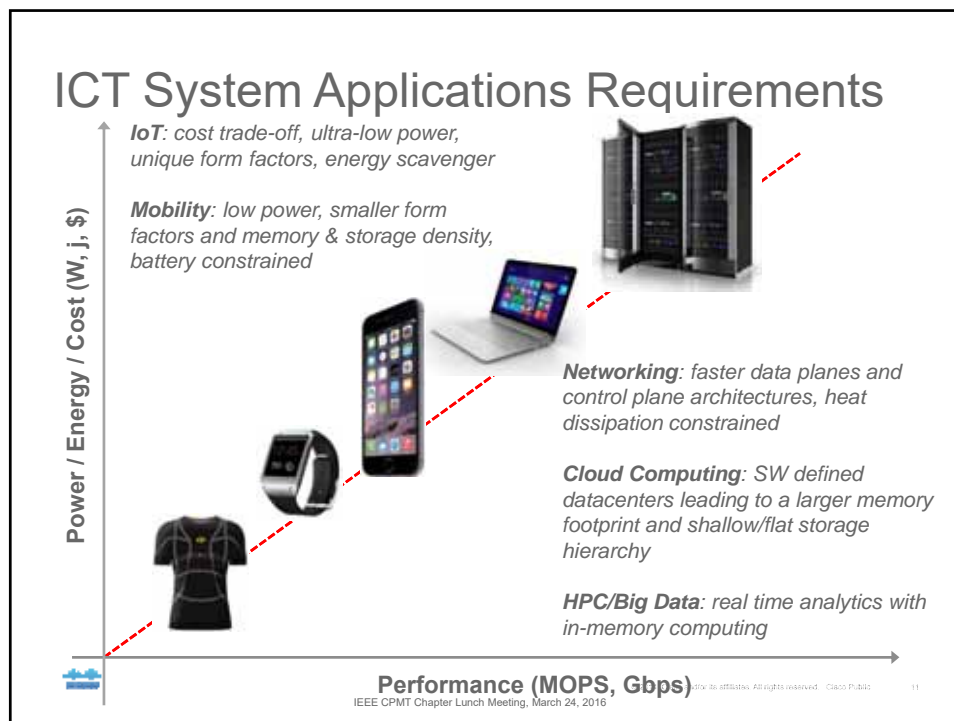
Technology Node Scaling

Cost per transistor may start to rise
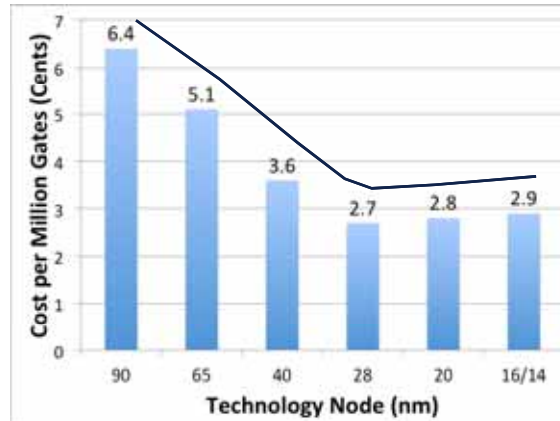
Recently announced **7nm** test chip produced by IBM Research Alliance

Source: IBM, Broadcom

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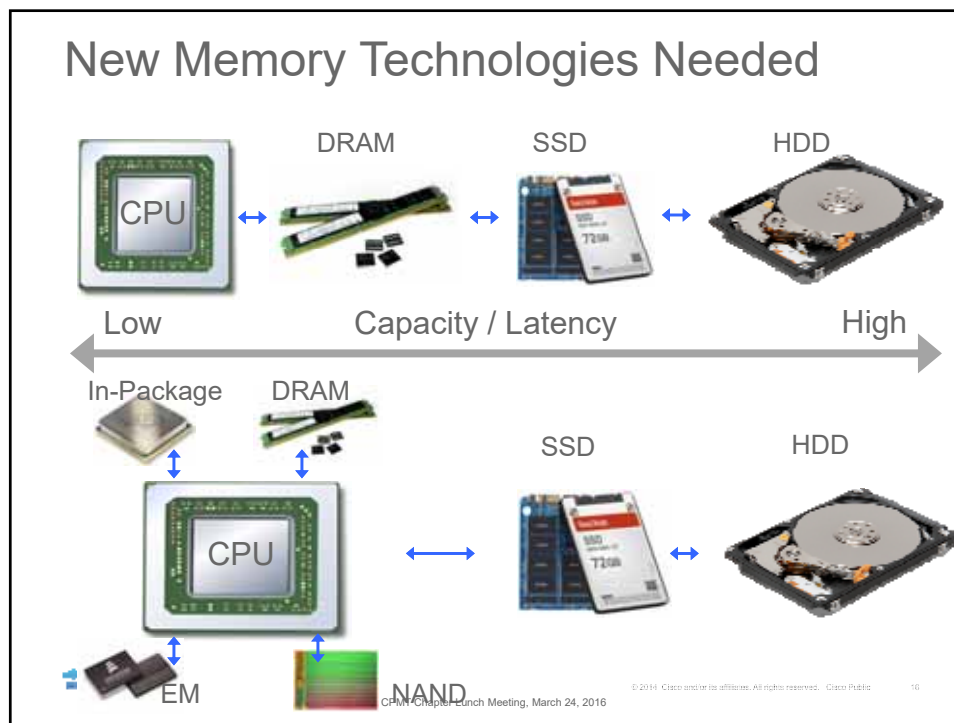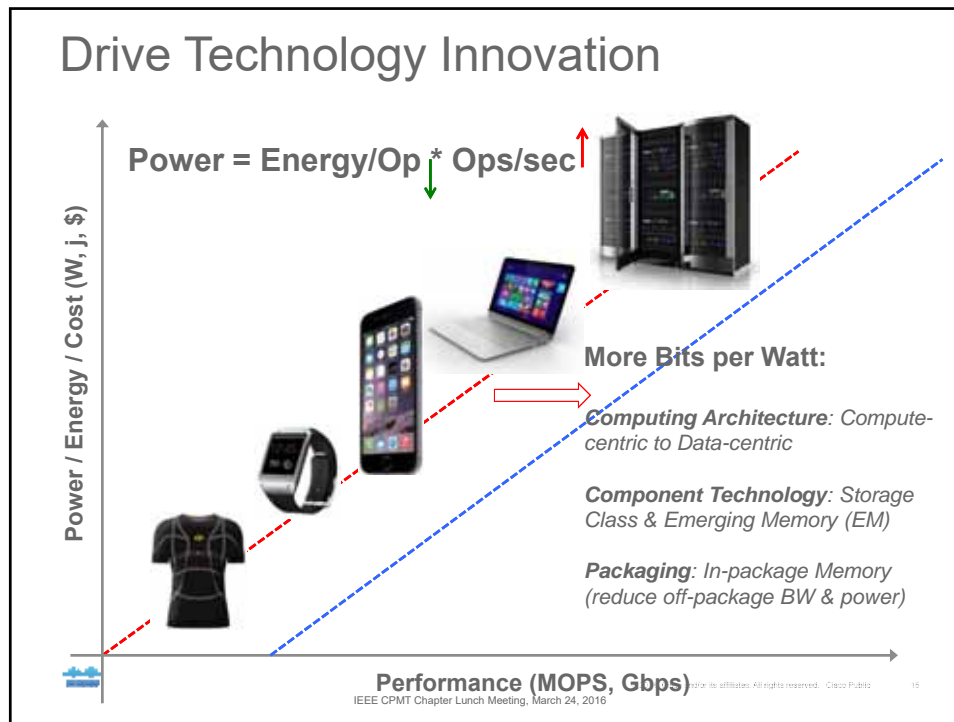However, economics will likely be the key challenges to continued technology node scaling.

Potential Solutions:

- Component Technology Innovation
*- Emerging IC Packaging Technology Platforms*

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Drive Technology Innovation

Power = Energy/Op * Ops/sec

Power / Energy / Cost (W, j, $) (vertical axis)

More Bits per Watt:

Computing Architecture: Compute-centric to Data-centric

Component Technology: Storage Class & Emerging Memory (EM)

Packaging: In-package Memory (reduce off-package BW & power)

Performance (MOPS, Gbps)

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New Memory Technologies Needed

CPU ↔ DRAM ↔ SSD ↔ HDD

Low — Capacity / Latency — High

In-Package   DRAM

CPU ↔ SSD ↔ HDD

EM   NAND

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Emerging Memory (EM) Technologies

Floating Gate 3D NAND (March 2015)

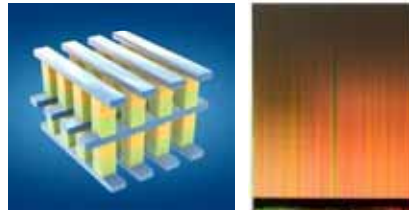**3D XPoint NVM (July 2015)**
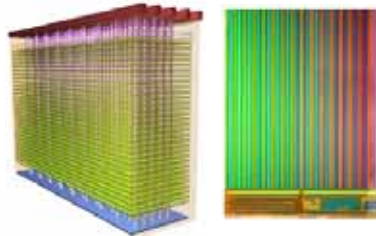
- 3X high capacity than existing NAND technologies
- Enables >10TB in a standard 2.5" SSD
- Scaling for the next decade

- 1st new memory technology in 25+ years
- 1000X faster than NAND
- 1000X endurance of NAND
- 10X denser than conventional memory
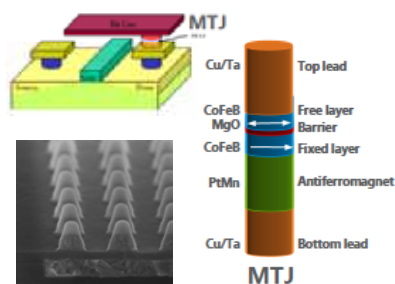
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Source: Micron
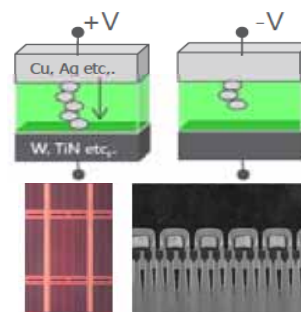

Future Memory Technologies

Spin Torque Memory

Resistive Memory

- Potential long-term DRAM replacement
- Early application as a high-speed cache
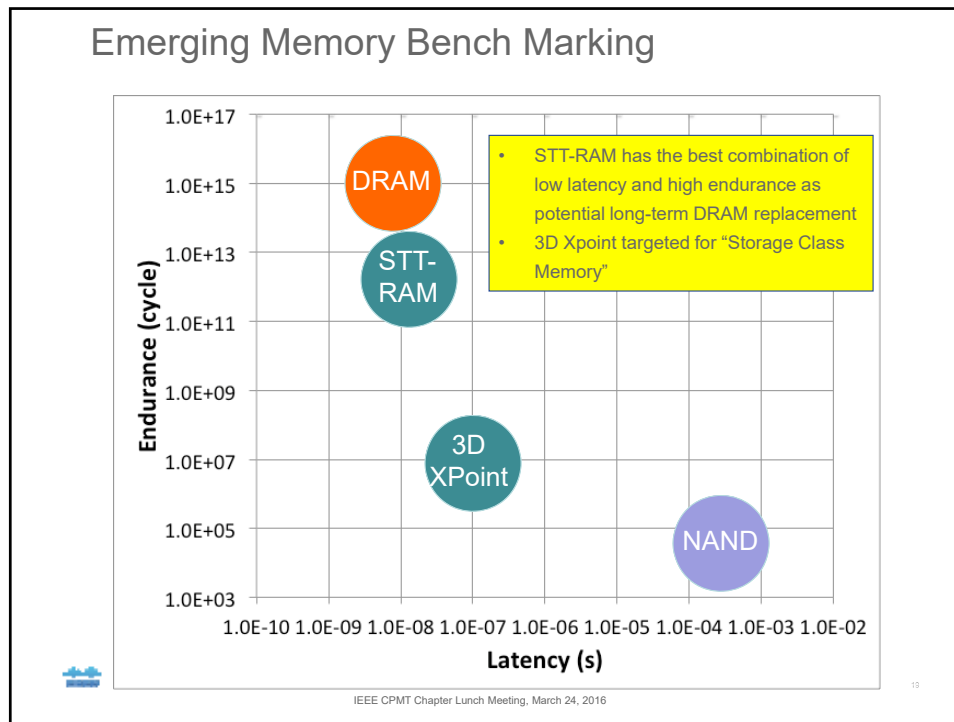- Based on electron spin at atomic level

- Flash replacement beyond 10nm
- NVM
- High-speed, low power, CMOS compatible

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Source: Micron, IMEC

Emerging Memory Bench Marking

- STT-RAM has the best combination of low latency and high endurance as potential long-term DRAM replacement
- 3D Xpoint targeted for "Storage Class Memory"

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In-Package Memory *integrating* with CPU

High Bandwidth Memory (HBM)

- High BW
- Saving on energy/bit vs GDDR5
- In-Package integration with CPU
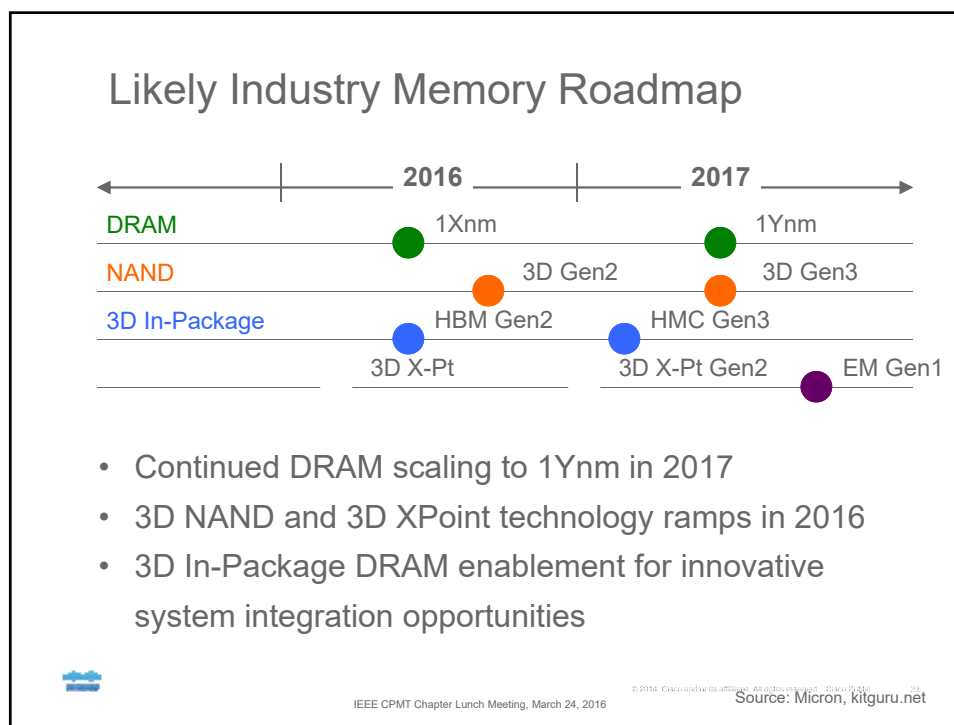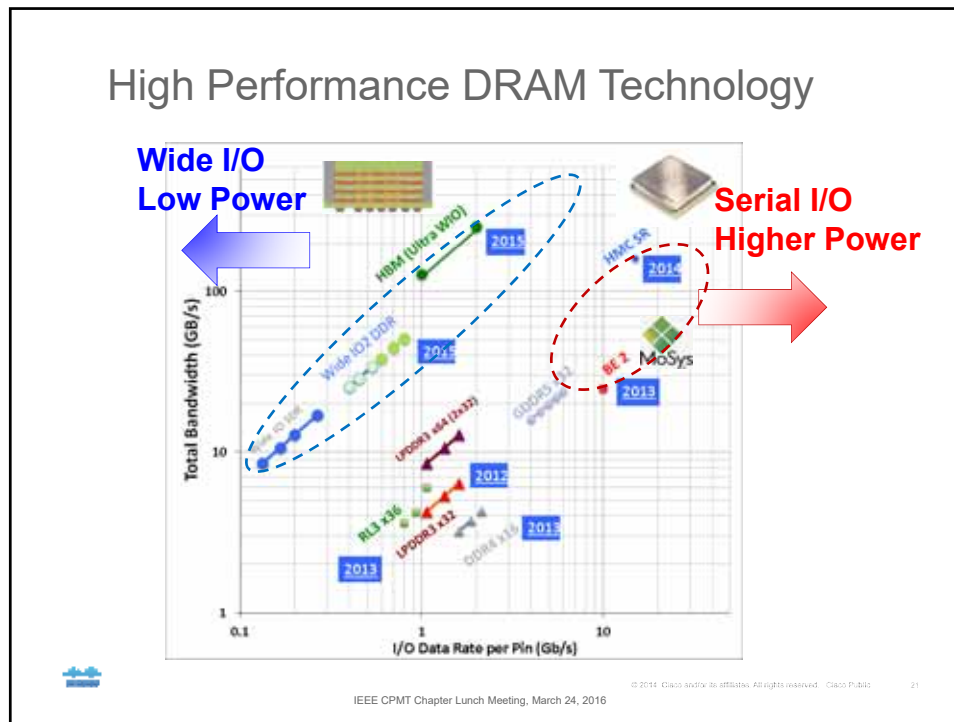- JEDEC standard

Source: SK Hynix, AMD

Hybrid Memory Cube (HMC)

- High BW
- Saving on energy/bit vs DDR3
- Easy of System Integration
- High-speed serial I/O

Source: Micron, Juniper

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High Performance DRAM Technology

Wide I/O Low Power

Serial I/O Higher Power

Likely Industry Memory Roadmap

	2016		2017	
DRAM	1Xnm		1Ynm	
NAND		3D Gen2	3D Gen3	
3D In-Package	HBM Gen2		HMC Gen3	
	3D X-Pt		3D X-Pt Gen2	EM Gen1

- Continued DRAM scaling to 1Ynm in 2017
- 3D NAND and 3D XPoint technology ramps in 2016
- 3D In-Package DRAM enablement for innovative system integration opportunities

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Source: Micron, kitguru.net

Emerging Packaging Tech Platform

	FC-MCP	Si Interposer	Embedded Si Interposer	Organic Interposer	3D IC
Dielectric Properties	Good	Lossy	Lossy	Good	Lossy
Feature Dimensions	Down to ~ 10um L/S	BEOL interconnects	BEOL interconnects	Down to ~ 5um L/S	BEOL interconnects
CTE Mismatch	Mod. High	Excellent	Mod. High	Mod. High	Excellent
Cost	Moderate	Moderate	TBD	Moderate	High
Availability / Supply Chain	Available	Available	Development	Development	Development

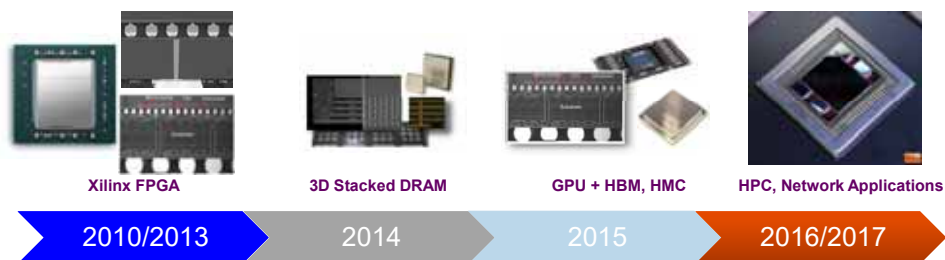**From Substrate Based to Wafer Level System Integration**

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2.5D / 3D IC Landscape

Xilinx FPGA   **3D Stacked DRAM**   **GPU + HBM, HMC**   **HPC, Network Applications**

2010/2013	2014	2015	2016/2017

- FPGA (28nm TSMC)
- Logic + Logic Partition
- TSMC CoWoS (2.5D)

- 3D Stacked DRAM
- HMC (Serial I/O, Micron)
- HBM (Wide-I/O, JEDEC)
- 3DS DDR4 (128GB DIMM)

- GPU + HBM Integration
- HBM and HMC Qualification
- Network Applications

- GPU + HBM Production
- CPU + HBM Production
- NPU + HBM Production
- Heterogeneous Integration

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Summary

- Realization of the promise of Internet of Everything relies on next generations of computing, networking and storage systems.

- Silicon performance advancement alone may not get us there as (2D) technology node scaling is becoming more costly.

- New computing architectures, emerging memory components through 3D /volume scaling and 3D IC packaging technologies will be key in future system enablement.

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