PURPOSES

To present the recent advances and new trends in the following semiconductor packaging technologies:

- Fan-Out Wafer/Panel-Level Packaging
- 3D IC Integration with TSVs
- 2.5D IC Integration/TSV-less Interposers
Fan-Out Wafer/Panel-Level Packaging

(1) PATENTS IMPACTING THE SEMICONDUCTOR PACKAGING

(2) FAN-OUT WAVER/PANEL-LEVEL PACKAGING FORMATIONS
   (A) Chip-First (Die-Down)
   (B) Chip-First (Die-Up)
   (C) Chip-Last (RDL-First)

(3) RDL FABRICATIONS
   (A) Polymer Method
   (B) PCB/LDI Method
   (C) Cu Damascene Method

(4) TSMC InFO-WLP and InFO-PoP vs. Samsung ePoP

(5) WAFER vs. PANEL CARRIER

(6) NOTES ON DIRECTRIC AND EPOXY MOLD COMPOUND

(7) SEMICONDUCTOR and PACKAGING FOR IoTs (SiP)

(8) WAFER-LEVEL SYSTEM-in-PACKAGE (WLSiP)

(9) PACKAGE-FREE LED (EMBEDDED LED CSP)

(10) SUMMARY

Typical PCB Assemblies in Electronic Products
Patents Impacting the Semiconductor Packaging

(Even there are many important patents such as flip chip and TSV, however I think the following 4 impact the semiconductor packaging the most.)

- Lead-Frame
- Organic Substrate with Solder Balls
- Fan-In Wafer Level Packaging
- Fan-Out Wafer Level Packaging

The first lead-frame patent!

Lau, CSR, 19(6), 2015
Chip Circuitry Fan-Out by Lead-Frame

Chip Circuitry is Fanned-Out by Lead-Frame to PCB.

Gold Wires
Silicon Chip
Lead-Frame
Through-hole Lead
J-Lead
PCB
Gull-wing Lead

United States Patent
Lin et al.

Patent Number: 5,216,278
Date of Patent: Jun. 1, 1993

Related U.S. Application Data

Solder Bumped Pad Array Carriers", Proceedings of
the Intern'l Engineering Packaging Soc., pp. 264-274,
E. Stephans, "Pinless Module Connector", IBM Tech.

Primary Examiner—Andrew J. James
Assistant Examiner—Carl Whitehead, Jr.
Attorney, Agent, or Firm—Jasper W. Dockrey

ABSTRACT
A semiconductor device (10) having first and second
wiring layers (30, 33) on opposite surfaces of a carrier
substrate (12) interconnected through vias (32) formed
in the carrier substrate (12) electrically coupling an
 electronic component (18) to a mounting substrate
 through compliant solder balls (26) displaced away
 from via (33), the semiconductor device (10) character-
 ized by a standard size carrier substrate (12) having high

Lead-Frame is replaced by package substrate and solder balls to fan-out the chip circuitry to PCB.
The circuitry of Chip is Fan-Out Through Substrate and Solder Balls

1993, AMKOR led OSATs to license this technology from Motorola.

BGA (ball grid array) era began!

Chip: 4 to 625mm²
Solder ball: ranging from 10s to 1000s
Pitch: ranging from 0.5, 0.65, 0.8, 1, to 1.27mm
PBGA package size: range from 10mmx10mm, to as large as 55mmx55mm

Lau, CSR, 19(6), 2015

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Fan-in WLP (WLCSP) to eliminate package substrate and underfill.

Lau, CSR, 19(6), 2015
Wafer-Level Chip Size Packages (WLCSP)

In the past 15 years, WLCSP has been used mainly for low pin-counts (≤ 200) with pitch ranges from 0.5, 0.4, 0.35, and 0.3mm, small die size (≤ 6mm x 6mm), low-cost, low-end, low-profile, and high-volume applications.

Semiconductor ICs such as the electrostatic discharge / electromagnetic interference protection, radio frequency (RF) filtering, power management, power amplifiers, surface acoustic wave / bulk acoustic wave filters, DC/DC converters, light-emitting diodes, battery and display driver, audio/video codecs and amplifiers, logic gates, electrically erasable programmable read-only memory (EEPROM), microcontrollers, Bluetooth + frequency modulation (FM) + Wi-Fi combos, global positioning system (GPS), baseband, and radio frequency transceivers have been packaged with various WLCSPs for various electronic products such as cell-phones, smartphones and tablets, and wearables.

For internet of things (IoTs), the CMOS image sensors and MEMS sensors will also be packaged with WLCSPs.

Chip 2001, AMKOR led OSATs and Foundries to license this technology from Flip Chip Technologies.

2001, AMKOR led OSATs and Foundries to license this technology from Flip Chip Technologies.

WLP (wafer-level packaging) era began!

Chip

Metal wire (RDL)

Metal pad

Over Mold Encapsulant

Dielectric

Solder Ball

PCB

Solder Mask (Polyimide)

RDLs to fan-out the circuitry beyond the chip edges without using a lead-frame or substrate.

United States Patent

Pitcher et al.

Patent No.: US 6,727,576 B2

Date of Patent: Apr. 27, 2004

References Cited

U.S. PATENT DOCUMENTS

6,537,846 B2 * 3,2009 Camarote et al. ...... 488/46

* cited by examiner

Primary Examiner—David Nidols

Assistant Examiner—Mai-Bing Tran

(74) Attorney, Agent, or Firm—Fish & Richardson

(72) Assignee: Infineon Technologies AG, Munich

* Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(71) Appl. No.: 10/014,400

(22) Filed: Oct. 31, 2000
What is claimed is:

1. A semiconductor structure, comprising:
   a semiconductor chip having an edge and a surface;
   a contact pad disposed on the surface of the semiconductor chip; and
   a conductive layer disposed on the surface of the semiconductor chip and in contact with the contact pad, the conductive layer having a portion that extends beyond the edge of the semiconductor chip.

2. The structure of claim 1, wherein the conductive layer comprises a metal line.

3. The semiconductor structure of claim 1, wherein the chip comprises a device.

4. The semiconductor structure of claim 3, wherein the device comprises an integrated circuit.

5. The semiconductor structure of claim 3, wherein the device comprises a micro-electromechanical device.

6. The semiconductor structure of claim 1, further comprising:
   a front layer, having a first portion disposed on the surface of the semiconductor chip, and a second portion extending beyond the edge of the semiconductor chip, the conductive layer being disposed on the front layer.

7. The semiconductor structure of claim 6, wherein the front layer is a dielectric layer.

8. The semiconductor structure of claim 6, wherein the front layer is compliant.

9. The semiconductor structure of claim 6, wherein the front layer includes a bump.

10. The semiconductor structure of claim 6, wherein the second portion of the front layer extends beyond an edge of a second semiconductor chip.

11. A semiconductor structure, comprising:
    a semiconductor chip having a surface and an edge;
    a contact pad disposed on the surface of the semiconductor chip; and
    a front layer, having a first portion disposed on the surface of the semiconductor chip, and a second portion extending beyond the edge of the chip.

12. The semiconductor structure of claim 11, wherein the second portion of the front layer extends beyond an edge of a second semiconductor chip.

13. The semiconductor structure of claim 11, further comprising:
    a conductive layer disposed on the surface of the semiconductor chip, the conductive layer having a portion that extends beyond the edge of the semiconductor chip.

14. The semiconductor structure of claim 11, wherein the front layer is a dielectric layer.

15. The semiconductor structure of claim 11, wherein the front layer is compliant.

16. The semiconductor structure of claim 11, wherein the front layer includes a bump.
Advantages of Fan-Out Wafer/Panel Level Packaging over FCPBGA

(1) lower cost  
(2) lower profile  
(3) eliminating the substrate  
(4) eliminating the wafer bumping  
(5) eliminating the flip chip reflow  
(6) eliminating the flux cleaning  
(7) eliminating the underfill  
(8) better electrical performance  
(9) better thermal performance  
(10) easier to go for system-in-package (SiP) and 3D IC packaging

Lau, CSR, 19(6), 2015

Advantages of Fan-Out Wafer/Panel Level Packaging over Fan-In Wafer Level Packaging

(1) the use of known good die (KGD)  
(2) better wafer-level yield  
(3) using the best of silicon  
(4) multichip  
(5) embedded integrated passive devices  
(6) more than one RDL  
(7) higher pin counts (or die shrink)  
(8) better thermal performance  
(9) easier to go for SiP and 3D IC packaging  
(10) higher PCB level reliability.

Lau, CSR, 19(6), 2015
Chip-First (Die-Up) Chip-First (Die-Down)

Most of the fan-out wafer/panel-level packages in manufacturing today use either one of these formations for portable, mobile, and wearable products.

The reconfigured carrier is neither wafer or panel!

Lau, et al., CSR 20(3), 2016

FOW/PLP Formation: Chip-First (Die-Down)

Lau, et al., CSR 20(3), 2016
TSMC’s InFO (Integrated Fan-Out) WLP for Apple’s A10 Application Processor Chip-Frist (Die-Up)
FIG. 11 also shows a more detailed view of the die 104 and the wiring layer 108, in accordance with some embodiments. The view of the die 104 and wiring layer 108 are exemplary; alternatively, the die 104 and wiring layer 108 may comprise other configurations, layouts and/or designs. In the embodiment shown, the die 104 includes a substrate 124 comprising silicon or other semiconductive materials. Insulating layers 126a and 126b may comprise passivation layers disposed on the substrate 124. Contact pads 128 of the die 104 may be formed over conductive features of the substrate such as metal pads 127, plugs, vias, or conductive lines to make electrical contact with electrical components of the substrate 124, which are not shown.

Lau, CSR, 19(6), 2015

FOW/PLP Formation: Chip-First (Die-Up)

Test for KGD

Device Wafer

2-side tape

Temporary (wafer or panel) carrier

Die face-up

KGD

KGD

KGD

Over mold the reconfigured carrier

EMC

Backgrind the over-mold to expose the contact pad

Contact pad

Solder balls

RDLs

Build RDLs on contact pads and mount solder balls

Remove carrier and tape and then dice the molded wafer or panel into individual packages

KGD

KGD

KGD

Lau, et al., CSR 20(3), 2016
Forecast Fan-Out Wafer-Level Packaging (FOWLP) Revenues ($M)

Key Components in iPhone 6 Plus

- **AP chipset PoP** (A9 + 2GB LPDDR4)
- **iPhone 6S/6S Plus**
- **2GB LPDDR4**
- **150µm-pitch staggered C4 bumps**
- **2-2-2 build-up substrate**
- **A9 application processor fabricated by 14/16nm Fin-FET process technology**
- **Lau, CSR, 19(6), 2015**
TSMC’s InFO_PoP

Conventional PoP for Application Processor (AP) chipset

Eliminated wafer bumping, solder reflow, flux cleaning, underfilling, and package substrate. Lower Profile!

Samsung’s ePoP
SK Hynix’s MLC (Multi Level Cell) 128Gb (Gigabit) or 8GB (Gigabyte) NAND Flash in iPhone

Samsung’s Application Processor Chip-Set and Memory chip-Set

On February 17, 2015, Samsung announced that their Exynos 7 Octa application processor (AP) has been in production using their 14nm FinFET technology process (the first in the world for AP.)
Samsung’s Next Generation High-End Smartphones

A 40% saving!

Embedded Fan-Out Panel Wafer-Level Packaging (FOPLP)
Wafer vs. Panel

For fan-out wafer/panel packaging, why use panel leads to lower cost?

- Because the RDLs of the panel are fabricated by PCB/LDI technology and P&P of dies and passives are by SMT equipment.
- Since the area of panel is larger than that of wafer, thus more packages can be made.

It should be noted that, fan-out panel wafer level packaging is applied to low-end, low-performance, low pin-count, and small devices. The line width/spacing of the RDLs are >10µm.
IZM Fan-Out Panel-Level Packaging Integration line

Placement → Accuracy → Molding → Lamination → Laser Drilling

Mech. Drilling → Cu Plating → Imaging → Etching

- ASM Siplace CA3
- Mahr OMS 600/IMPEX proX3
- WL: Towa up to 8" PL: APIC up to 16"x24"
- Lauffer/Bürkle
- Siemens Microbeam/Schmoll Picodrill with HYPER RAPID 50

Schmoll MX1 → Ramgraber automatic plating line → Orbotech Paragon Ultra 200 → Schmid

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Process for Panel RDLs by PCB and Laser Direct Imaging

- Lamination of a RCC on the reconfigured panel
- Drilling
- Cu plating to fill the hole and connect to the pad
- Laser direct imaging
- Passivation

Cu etching

- Strip photoresist
- Repeat all the processes to get RDL2
- Repeat all the processes to get Cu contact pads, spin coat solder mask, and mount solder balls

Al or Cu Pad → KGD → EMC

Lau, et al., CSR 20(3), 2016
The geometry, material, process, equipment, and application of fan-out wafer/panel-level packaging

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<tr>
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</thead>
<tbody>
<tr>
<td>High-end</td>
<td>&lt; 2 - 5µm</td>
<td>≤ 2µm</td>
<td>SiO₂ (1µm)</td>
<td>Stepper</td>
<td>Cu damascene, Semi. Equip., High-Precision P&amp;P</td>
</tr>
<tr>
<td></td>
<td>5 - 10µm</td>
<td>≥ 3µm</td>
<td>Polymers (4 - 8µm)</td>
<td>Mask aligner or Stepper</td>
<td>Cu plating, Packaging Equip., Ordinary P&amp;P</td>
</tr>
<tr>
<td>Low-end</td>
<td>&gt; 10µm</td>
<td>≥ 5µm</td>
<td>Resin (15 - 30µm)</td>
<td>Laser direct imaging</td>
<td>PCB Cu plating, PCB Equip., SMT P&amp;P</td>
</tr>
</tbody>
</table>

**Chip-Last (RDL-First)**

For very high-density and high-performance applications, e.g., high-end servers, computers, and networking.

The reconfigured carrier is wafer!
Chip-Last (RDL-First)
Fan-Out Wafer-Level Packaging (FOWLP)

Since 2006, NEC Electronics Corporation (now Renesas Electronics Corporation) has been developing a novel SMAFTI (SMArt chip connection with FeedThrough Interposer) packaging technology for:

- inter-chip wide-band data transfer
- 3D stacked memory integrated on a logic devices
- system in wafer-level package (SiWLP) (2010)
- and “RDL-first” fan-out wafer-level packaging (2011)

The FTI (feedthrough interposer) of SMAFTI is a film with ultra-fine line width and spacing RDLs. The dielectric of the FTI is usually SiO₂ or polymer and the conductor wiring of the RDLs is Cu.

The FTI not only supports the RDLs underneath within the chip, it also supports beyond the edges of the chip.

Area array solder balls are mounted at the bottom-side of the FTI which are to be connected to the PCB. Epoxy mold compound (EMC) is used to embed the chip and support the RDLs and solder balls.

In 2015, Amkor announced a very similar technology called “SWIFT™” (silicon wafer integrated fan-out technology).  

Lau, et al., CSR 20(3), 2016

A 3D Stacked Memory Integrated on a Logic Device Using SMAFTI Technology

NEC Electronics, Oki Electric Industry, and Elpida Memory
1120 Shimokuzawa, Sagamihara, Kanagawa 229-1198, Japan
Chip-last with face-down (die-down) or “RDL-first” FOWLP

This is very different from the chip-first FOWLP.

First of all, this only works on wafer carrier.

Also, comparing to chip-first, RDL-first FOWLP requires:
- building up the RDLs on a bare silicon wafer (the FTI),
- performing the wafer bumping,
- performing the fluxing, chip-to-wafer bonding, and cleaning,
- performing the underfill dispensing and curing.

Each of these tasks is a huge task and requires additional materials, process, equipment, manufacturing floor space, and personal effort.

Thus, comparing to chip-first FOWLP, chip-last (RDL-first) FOWLP incurs very high cost and has more chances to have higher yield losses. It can only be afforded by very-high density and performance applications such as high-end servers and computers.

Lau, et al., CSR 20(3), 2016
Wafer Bumping Process Flow

(1) Redef. Passivation
(2) Sputter Ti/Cu
(3) Spin Resist
(4) Patterning
(5) ECD Cu, Solder
(6) Strip Resist
(7) Etch Cu/Ti
(8) Flux, Reflow

C4 (controlled collapsed chip connection) bump

C2 (chip connection) bump

Process flow of RDLs by Dual Cu damascene method

Si wafer
SiO₂
SiO₂ by PECVD
Photoresist
Spin coat Photoresist
Stepper, Litho.
RIE of SiO₂
Stepper, Litho.

RIE of SiO₂
Strip resist
TiCu
Cu
Sputter Ti/Cu and Electroplate Cu
Solder
RDL1
RDL2
RDL0
Contact Pad
DL0
DL1
DL2
DL3
RDL0
RDL1
RDL2

CMP the overburden Cu and Ti/Cu
Repeat the processes to get RDL2 and contact pad

Lau, et al., CSR 20(3), 2016
Typical SEM Image of RDLs Fabricated by Dual Cu Damascene Method

Removing Si-Wafer and Solder Ball Mounting

After the assembly, remove the Si wafer and mount solder balls

RDL3
RDL2
RDL1
Si wafer

Repeat the processes to get RDL2

RDL2
RDL1
V12
V23
Si wafer

Backgrind and then CMP the Si wafer, TiCu, and passivation

SiO₂ by PECVD

Spin coat photoresist

Lau, et al., CSR 20(3), 2016

Lau, et al., CSR 20(3), 2016
AMKOR’s SWIFT

SWIFT™
Silicon Wafer Integrated Fan-out Technology


AMKOR’s SWIFT
(Silicon Wafer Integrated Fan-out Technology)

Conventional Fan-out Technology

SWIFT
In 2012, GIT published a paper on chip-last fan-out (CLFO) package with embedded PMIC in ultra-thin laminate substrates.

In 2015, ASE proposed a low cost fan-out chip-last package (FOCLP) using a coreless panel substrate for low-end and low pin-count applications.

Strictly speaking, since they used the substrates and area-array solder balls to fan-out the circuitry from the chip to PCB, this cannot be considered the FOW/PLP.


Chip-Last Fan-out Package with Embedded Power ICs in Ultra-Thin Laminates

Nitesh Kumbhat*, Koushik Ramachandran, Fuhan Liu, Brent Wagner#, Venky Sundaram and Rao Tummala

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#Georgia Tech Research Institute, Georgia Institute of Technology, 445 9th St NW, Atlanta, GA 30332

*Phone: 404-385-0730 / Email: nitesh@gatech.edu
Low Cost Chip Last Fanout Package using Coreless Substrate

Scott Chen, Simon Wang, Coltrane Lee, John Hunt
ASE Group, Chung-Li, Taiwan ROC

NOTES ON DIELECTRIC MATERIALS

For the RDLs in Chip-First FOWLP with very fine line width/space, the dielectric layer (SiO$_2$) is fabricated by the low-temperature PECVD (<200°C) or SACVD (sub-atmosphere chemical vapor deposition) (170°C), which are less than the critical temperature (230°C) of the compression molded EMC.

For polymer dielectric layer, low curing temperature polymers such as BCB and PBO are required. For example, the curing temperature of DOW’s BCB is 200°C and for Sumitomo’s PBO, 220°C.

For low warpage and high reliability Chip-First and Chip-Last FOWLP, the Young’s modulus and elongation of the dielectric materials must be, respectively, low and high. For example, the Young’s modulus and elongation of DOW’s BCB are 2GPa and 28, while Sumitomo’s PBO, 2.7GPa and 55.
NOTES ON MOLDING MATERIALS

The molding of FOWLP is by the compression method with EMC.

For Chip-First FOWLP, the curing temperature of the EMC must be lower than the release temperature of the 2-side tape.

For Chip-First and Chip-Last FOWLP:

- There are at least two forms of EMC, namely liquid and solid. The advantages of liquid EMC are better handling, good flowability, fewer voids, better fill, and less flow marks. The advantages of solid EMC are less cure shrinkage, better stand-off, and less die drift.
- High filler content (>85%) EMC will shorten the time in mold, lower the mold shrinkage, and reduce the mold warpage.
- Uniform filler distribution and filler size of the EMC will reduce flow marks/fill and enhance flowability.

<table>
<thead>
<tr>
<th></th>
<th>Filler content (wt%)</th>
<th>Maximum filler size (µm)</th>
<th>Mold condition (m/°C)</th>
<th>Post cure (h/°C)</th>
<th>Tg (°C)</th>
<th>Bending stiffness (GP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sumitomo (solid)</td>
<td>90</td>
<td>55</td>
<td>7/125</td>
<td>1/150</td>
<td>170</td>
<td>30</td>
</tr>
<tr>
<td>Nagase (liquid)</td>
<td>89</td>
<td>75</td>
<td>10/125</td>
<td>1/150</td>
<td>165</td>
<td>22</td>
</tr>
</tbody>
</table>

Lau, et al., CSR 20(3), 2016

NOTES ON EQUIPMENT

Pick and Place (P&P)

- SMT/chip shooter P&P for large-pitch KGDs and thus large line width/spacing RDLs, e.g., Universal, Panasonic, and ASM.
- High precision P&P for fine-pitch KGDs and thus fine line width/spacing RDLs, e.g., Toray, Datacon, and ASM.

RDLs

- The seed/adhesion layer by PVD, e.g., Applied Materials, SPTS (now Orbotech) and NEXX.
- The dielectric layer by PECVD, e.g., Applied Materials, Lam Research, and Tokyo Electron.
- The conductor wiring by ECD, e.g., Semitool (now Applied Materials), Novellus (now Lam Research), and NEXX.

Molding

Compression with EMC, e.g., Yamada, TOWA, and ASM.

Solder Ball Mounting

The equipment suppliers are, e.g., Shibuya, PacTech, and ASM.

Packaging Handling

Inspection, test, and laser marking are, e.g., DISCO, Kulicke & Soffa, and ASM.

Lau, et al., CSR 20(3), 2016
Internet of Things (IoTs)

Semiconductor Drivers for IoTs

- Cost, Cost, Cost
- Ultra Low Power (long battery life)
- Small Form Factor (miniaturization)
- Low Heat Dissipation for wearables (touch to the skin)
- Security
Semiconductor and Packaging for IoTs

Potential semiconductors for IoTs are:

- Sensors
- Microcontroller unit (MCU)
- Power management IC (PMIC)
- CMOS image sensor (CIS)
- Memory/Embedded flash
- Micro-electromechanical system (MEMS)
- Fingerprint identification sensor (FIS)
- Radio frequency identification (RFID)/RFIC
- Global positioning system (GPS) IC
- Microprocessors to control the devices
- Digital signal processor (DSP) IC
- Wireless (e.g., Blue-tooth, Wi-Fi) connectivity IC
- Near field communication (NFC) IC
- Security for authentication and anti-counterfeiting IC

- Unlike smartphones, the process technologies don’t need to go down to 14nm and 0.18µm (at most 45nm) are more than adequate.
- Also, most semiconductors for IoTs don’t need 12” wafers and 8” wafers are enough!
- Furthermore, unlike NB and smartphones that have a very simple product platform and very large manufacturing volumes, the products associated with IoT applications will have more platforms, but smaller manufacturing volumes.
- The key is to integrate some of the above into a very small form factor SoC (System-on-Chip)/SiP (System-in-Package).
- Some of the simple SiP can be assembled by the SMT or wire bonding chip on board.

Lau, CSR, 19(3), 2015

Apple Watch

- The processor is integrated with the DRAM into a SoC.

- Apple then integrated the SoC, NAND flash, wireless connectivity chip, PMIC, sensors, and some special-purpose chips into a SiP called S1 for their Apple Watch.

Lau, CSR, 19(3), 2015
Intel’s Tiny Curie Module

The Intel Curie module can enable efficient and intelligent wearable solutions for a broad range of form factors – from rings, bags, bracelets, pendants, fitness trackers to even buttons.

The Intel Curie Module includes:

- The integration of the low-power 32-bitx86 processor with 80kB SRAM and 384kB flash into Intel Quark SE SoC.

- The integration of the Quark SE SoC MCU, low power DSP, Blue-tooth low energy wireless connectivity, PMIC, and a 6-axes combo sensor with accelerometer and gyroscope MEMS into a SiP (called Curie module) for wearable applications.

WLSiP
(Wafer-Level System-in-Package)
Basically, WLSiP use the fan-out wafer/panel-level packaging to build the SiP.

- WLSiP pick up the known-good dies (KGDs) and discrete and place them on a temporary carrier and then over mold the whole reconfigured wafer with epoxy molding compound (EMC).
- Remove the carrier and build the RDLs and mount the solder balls.
- Finally, dice the molded wafer with RDLs and solder balls into individual units.

There are many advantages of the WLSiP over the SiP. One of the biggest advantages is lower profile and lower cost by eliminating the organic substrate!
SUMMARY AND RECOMMENDATIONS

Out of the three methods in forming the FOWLP, chip-first with die-down is the most simple and low cost while chip-last (RDL-first) is the most complex and high cost. Chip-first with die-up requires slightly more process steps (and thus is slightly costly) than chip-first with die-down.

Chip-first FOWLP can perform more than what fan-in wafer-level packaging (WLP) can do. However, some of the things that PBGA (plastic ball grid array) package can do, but chip-first FOWLP cannot are: (1) larger die size \((\geq 12\text{mm} \times 12\text{mm})\) and (2) larger package size \((\geq 25\text{mm} \times 25\text{mm})\). This is due to the thermal expansion mismatch and warpage limitations of the chip-first FOWLP. In this case, chip-last (RDL-first) FOWLP can extend the application boundary to die size with the range of \(\leq 15\text{mm} \times 15\text{mm}\) and fan-out package size \((\leq 32\text{mm} \times 32\text{mm})\). With the heat spreader wafer option, the boundary can even be stretched to die size of \(<20\text{mm} \times 20\text{mm}\) and fan-out package size of \(<42\text{mm} \times 42\text{mm}\).

Chip-first FOWLP is just right for packaging semiconductor ICs such as baseband, RF/analog, PMIC, AP, low-end ASIC, CPUs (central processing units) and GPUs (graphics processing units) for portable, mobile, and wearable products. While chip-last (RDL-first) FOWLP is suitable for packaging the very high density and performance IC devices such as high-end CPUs, GPUs, ASIC, and FPGA (field programmable grid array) for high-end servers, computer, networking, and telecommunication products.
SUMMARY AND RECOMMENDATIONS

- Out of the three methods for fabricating the RDLs, PCB technology with LDI is the cheapest, while Cu damascene is the most expensive. The method used will depend on the Cu line width/spacing and thickness of the RDLs. Usually, if the line width/spacing and thickness are <5µm and ≤2µm respectively, then Cu damascene is the preferred option; if they are ≥5µm and ≥3µm, then use polymer with ECD; and for >10µm and ≥5µm, PCB with LDI should be used.

- For chip-first FOWLP, the choice of reconfigured wafer or panel depends on the Cu line width/spacing of RDLs. If it is >10µm, then use large (610mm x 457mm) panel, and combine with PCB/LDI and SMT P&P to increase throughput and to save cost.

- For chip-first FOWLP, the curing temperature of polymers for RDL’s dielectric layer should be less than the critical temperature (230°C) of the compression molded EMC.

- For chip-first FOWLP, the curing temperature of the EMC must be lower than the release temperature of the 2-side tape. For chip-first and chip-last FOWLP, high filler content EMC will shorten the time in mold, lower the mold shrinkage, and reduce the mold warpage. Uniform filler distribution and filler size of the EMC will reduce flow marks/fill and enhance flowability.

- WLSiP is a cost-effective way to build low-profile and low-cost SiPs.

- Embedded Wafer-level packaging is a low-cost and high throughput solution for package-free LED CSPs.

Lau, et al., CSR 20(3), 2016

3D IC Integration
3D IC Integration (The right thing to do!)

Said the 1965 Nobel Physics laureate, Richard Feynman at the Gakushuin University (Tokyo) in 1985:

“Another direction of improvement (of computing power) is to make physical machines three dimensional instead of all on a surface of a chip (2D). That can be done in stages instead of all at once – you can have several layers and then add many more layers as time goes on.”

TSVs straight through the same memory chips to:

- enlarge the memory capacity
- lower the power consumption
- increase the bandwidth
- lower the latency (enhance electrical performance)
- reduce the form factor

will be the major applications of 3D IC Integration!
Samsung Mass-Produces Industry's First TSV-based DDR4 DRAM

On November 26, 2015, Samsung start to produce the 128GB RDIMM (dual inline memory module) with 78 TSVs for each DRAM!

This is not a wide I/O device, nor does it contain a base logic die. It is just for memory capacity and low power consumption.

Micron’s First HMC Sample Shipped in the Last Week of September 2013

- The hybrid memory cube is a 4-DRAM (each one with 2000+ TSVs) on a logic controller (which size is slightly larger than the DRAMs) with TSVs
- The hybrid memory cube is on an organic package substrate.
- The TSV-DRAM is ~50-μm thick.
- The TSV-DRAM is with 20-μm (tall) Cu pillar + solder cap.
- The memory cube is assembled one DRAM at a time with thermal compression bonding.
- The heat dissipation is from 10W to 20W.
- TSV diameter ~ 5 to 6-μm.
- Volume production will be in next summer.
Intel’s “Knight’s Landing” with 8 HMC Fabricated by Micron (2015 production)

- 5X the bandwidth vs. GDDR5
- Up to 16GB
- One-third the footprint
- Half the energy per bit
- Managed memory stack for optimal levels of reliability, availability and serviceability

MCDRAM (Multi-Channel DRAM) is based on Micron’s HMC

Rik Myslewski, “Intel teams with Micron on next-gen many-core Xeon Phi with 3D DRAM Introduces new ‘fundamental building block of HPC systems’ with Intel Omni Scale Fabric”, Posted in HPC, June 2014.

High Bandwidth Memory (HBM) DRAM (Mainly for Graphic applications)
JEDEC Standard (JESD235), October 2013

HBM is designed to support bandwidth from 128GB/s to 256GB/s

Underfill is needed between the interposer and the organic substrate. Also, underfill is needed between the interposer and the GPU/CPU and the memory cube.
AMD's graph card made by Hynix's HBM, which is TCB of the NCF DRAM chips one by one

Wafer Bumping with Nonconductive Film (NCF) and FC bonding with NCF

Lau, et al., CSR, 19(5), 2015
Conventional Stepwise Process of Stacked Chips by Thermocompression Bonding (TCB)

It takes about 10 sec to cure the NCF and at the same time melt a solder and connect to an electrode on the substrate.

Toray's Collective TCB of Stacked Chips

Stage temperature = 80°C

1st step (3s): Bond-force = 50N
Temp. = 220-260°C
2nd step (7s): Bond-force = 70N
Temp. = 280°C

Peripheral portion
Area portion
SUMMARY

TSVs straight through the same DRAMs is the right way to:

◆ enlarge the memory capacity
◆ lower the power consumption
◆ increase the bandwidth
◆ lower the latency (enhance electrical performance)
◆ reduce the form factor

Unfortunately, due to the high-cost in making the TSVs and stacking the DRAMs, currently, it is used only for high-end servers, graphics and computers.

2.5D IC Integration and TSV-Less Interposers
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➢ ITRI’s TSV-less TSH
➢ Shinko’s TSV-less i-THOP

Xilinx/SPIL’s TSV-less SLIT
(Silicon-Less Interconnect Technology)
Xilinx/TSMC’s CoWoS

- Devices (Cannot see)
- Metal Contacts
- Metal Layers

Si Chip
- Micro Bump
- Cu Pillar
- Solder

4RDLs

Interposer

TSV and most interposer are eliminated! Only RDLs remained.

- Lower cost
- Better performance
- Lower profile

Package Substrate
- Solder Ball

Xilinx/SPIL’s SLIT

- Cu Pillar Solder
- C4/Contact via

4RDLs

- No entire TSV fabrication module
- No thin wafer handling technology
- No novel backside TSV revealing process
- No multiple inspection & metrology steps for TSV fabrication & backside TSV revealing steps.

Xilinx/SPIL IMAPS Oct 2014

TSV-Less Interconnect Technology

(a) RDLs build-up on a Si-wafer

(b) Chip to wafer bonding

(c) Underfilling

(d) Over molding the whole wafer
(e) Reinforced wafer and backgrind the Si-wafer

(f) Passivation, photoresist, mask, litho, etch passivation, sputter Ti/Cu, photoresist, mask, litho.

(g) Cu plating

(h) Strip photoresist, etch Ti/Cu, C4 bumping
Amkor’s TSV-less SLIM (Silicon-Less Integrated Module)

- Foundry BEOL layers retained
- Same CuP bond pads
- Same UBM and solder bump
- No TSV
- Much thinner

Amkor, 11th International Conference and Exhibition on Device Packaging, 2015.
Intel’s TSV-less EMIB
(Embedded Multi-Die Interconnect Bridge)
Heterogeneous Integration using Intel’s EMIB and Altera’s FPGA Technology

Intel’s Embedded Multi-die Interconnect Bridge (EMIB)

Embedded Multi-die Interconnect Bridge (EMIB)
A TSH interposer supporting chips with Cu pillars on its top-side and chips with solder bumps on its bottom-side

Underfill is needed between the TSH interposer and package substrate. Underfill may be needed between the TSH interposer and chips.

Lau et al., IEEE/CPMT Transactions, 2014
Shinko’s TSV-less i-THOP  
(Integrated Thin film High density Organic Package)
Shinko’s 2.5D IC Integration without TSVs

Chip-to-chip interconnection through 2µm width traces

Chip1

Chip2

40µm-pitch Pads

Thin Film (2 layers + FC Pad)

Conventional Build-up Substrate (1-2-2)

Shinko, ECTC 2014

Schematic image of the test chip

Min. 40µm-pitch

Cu-pillar + Ni + SnAg

Passivation Daisy Chain

Cu-OSP (Organic Solderability Preservation)

ENEPIG (Electro-less Ni/Pd/Au plating)

SEM image of test chip

40µm pitch flip chip bonding pads (25µm-diameter)

Shinko, ECTC 2014
Shinko’s 2.5D IC Integration without TSVs

SUMMARY
(2.5D IC Integration - Interposers)

- In general, interposers are for extremely high-I/O, high-performance, high-density, and fine-pitch semiconductor IC applications.

- In general, the build-up package substrates are more than adequate to support the semiconductor IC chips in high-end smartphones and an interposer is not necessary.

- TSVs are needed for 3D IC integration (to straight through the same DRAMs to increase the memory capacity, the bandwidth, and lower the power consumption.)

- TSVs are eliminated from the 2.5D IC integration (interposers) to save cost, enhance performance, and lower package profile, e.g., SLIT, EMIB, SLIM, i-THOP and TSH.
Thank you very much for your attention!