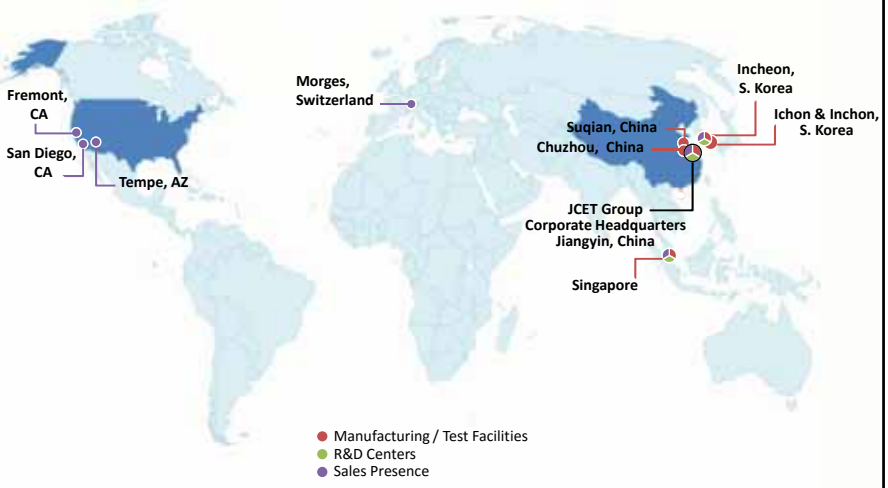

JCET
STATSChipPAC
Advanced Packaging Technologies for System Integration
Dr. Dongkai Shangguan
IEEE CPMT Distinguished Lecturer Program
April 2016


Our Business
JCET
STATSChipPAC
Silicon wafers from foundry
Full turnkey packaging and test solutions
RDL/IPD
Bump
Probe
Assembly
Final Test
Drop Ship
Customized solutions for a wide range of applications
2

JCET Global Footprint



3

Outline

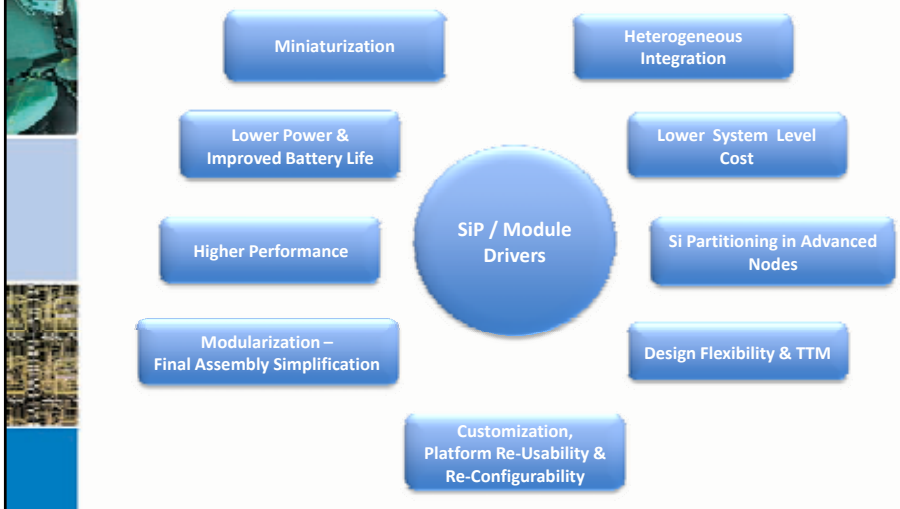
- Market Drivers for System Integration
- Process Technologies for SiP
- Technology Integration for SiP
- Summary

4

Market Drivers for System Integration

Drivers for System Integration

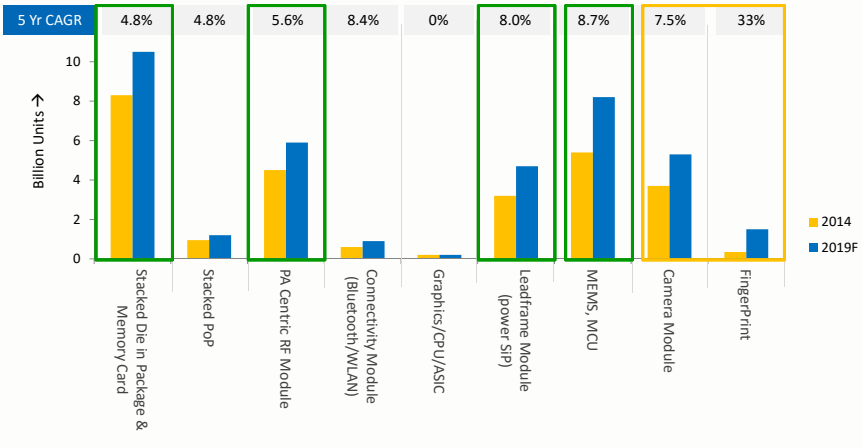
- Heterogeneous integration for optimized system solution
- Differentiation & specialization



6

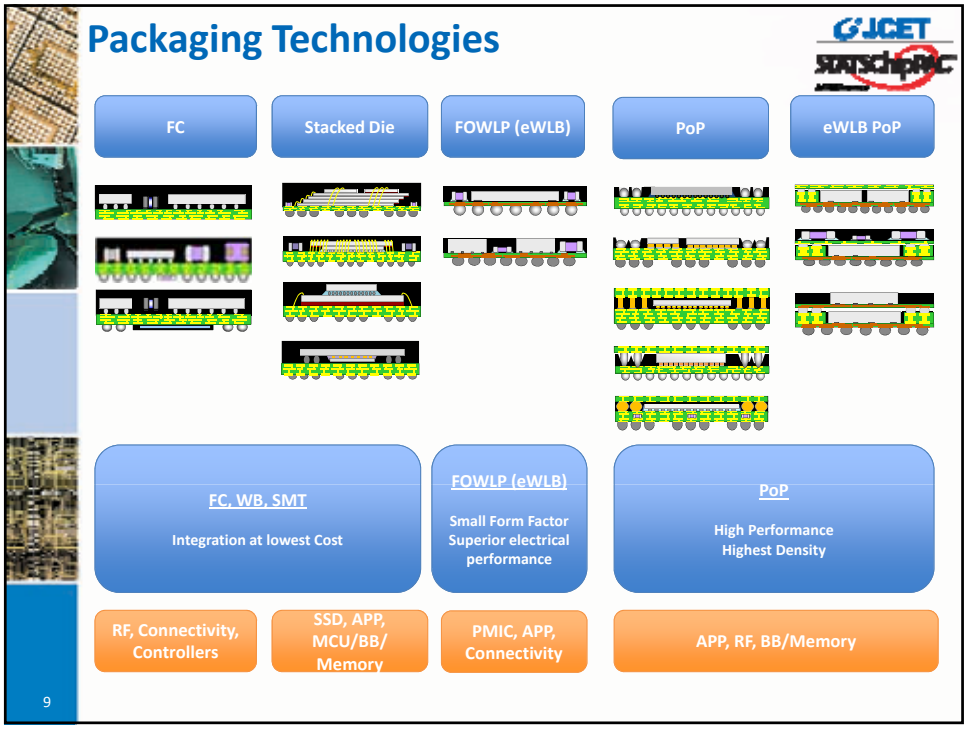
SiP Market

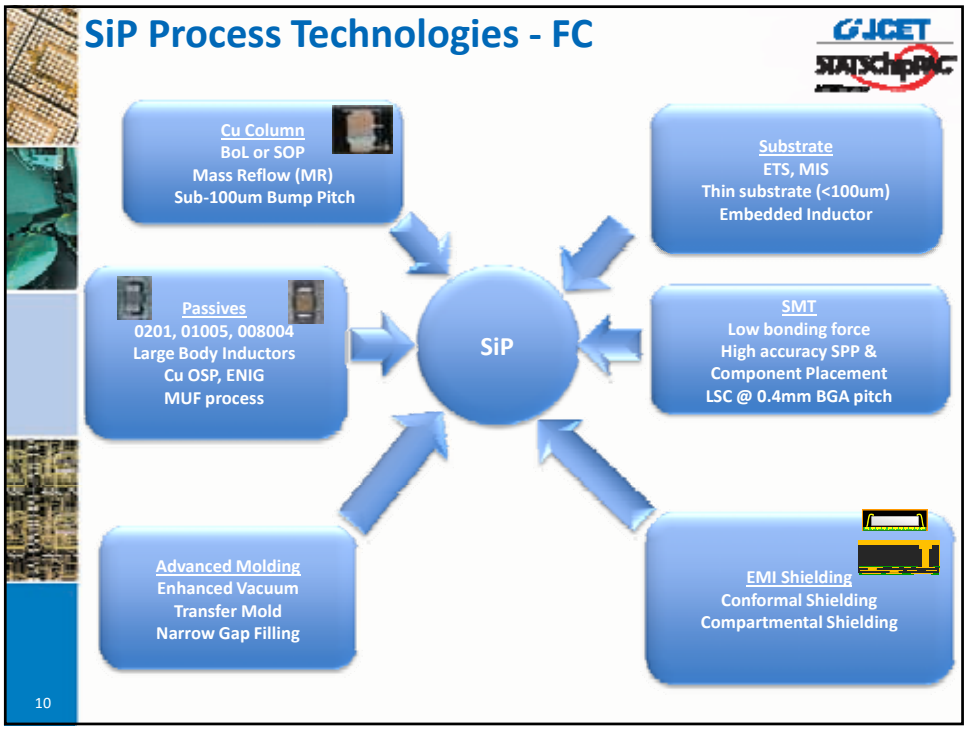
"opportunities for the global players to innovate in SiP and modules to take electronics share through integration" (Credit Suisse)

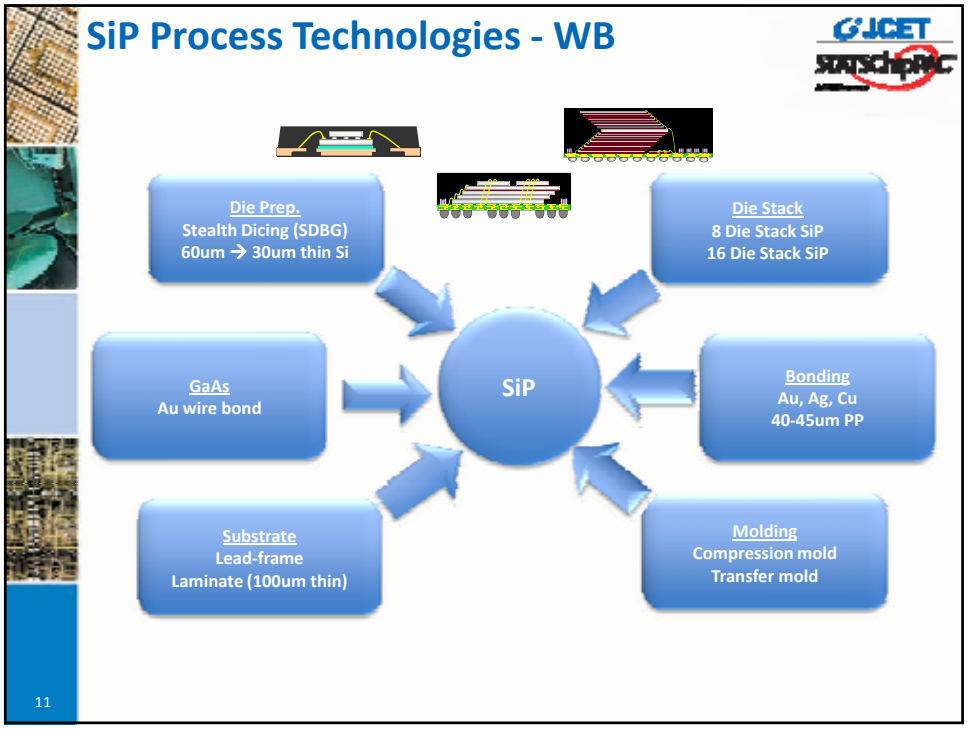


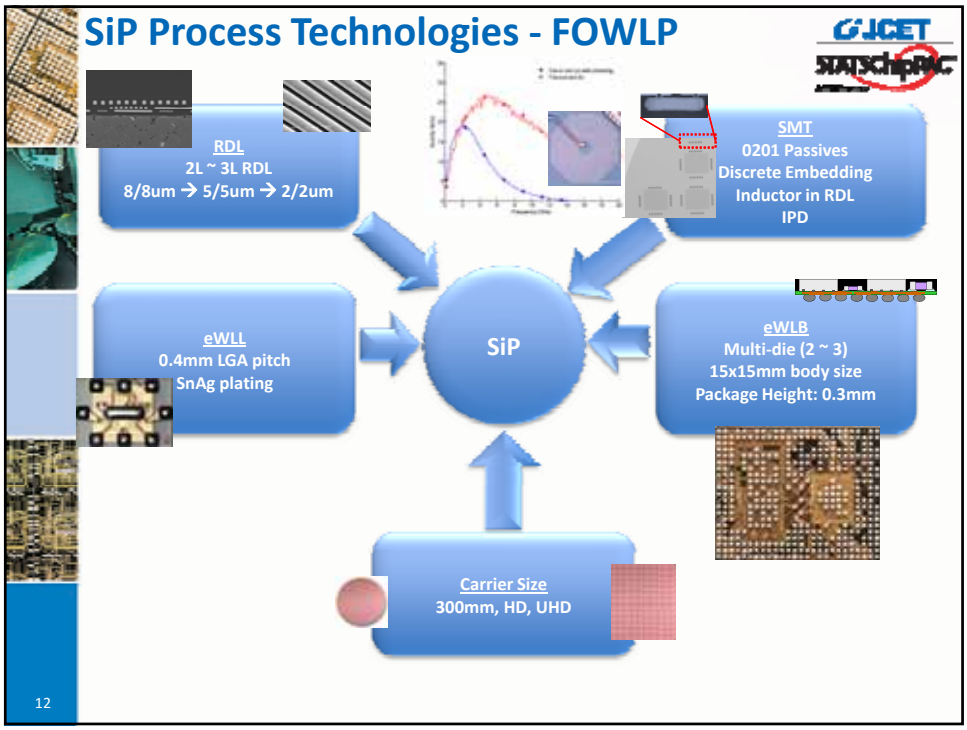
(Based on Prismark Data)

Process Technologies for SiP

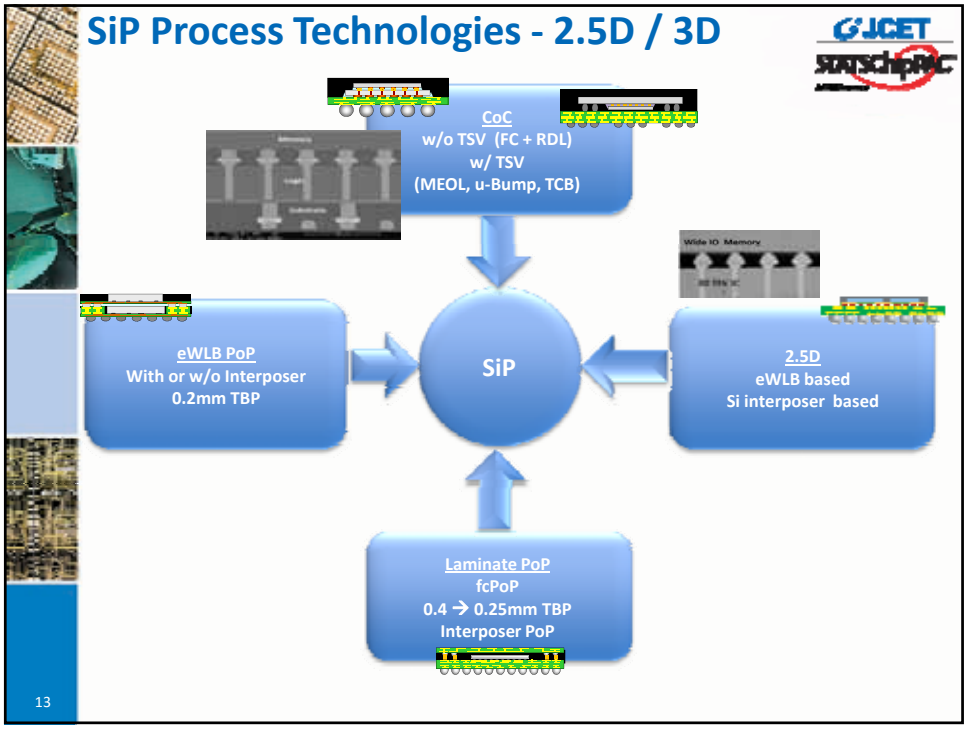

Packaging Technologies
JCET
STATSChipPAC
FC
Stacked Die
FOWLP (eWLB)
PoP
eWLB PoP
FC, WB, SMT
Integration at lowest Cost
FOWLP (eWLB)
Small Form Factor
Superior electrical performance
PoP
High Performance
Highest Density
RF, Connectivity, Controllers
SSD, APP, MCU/BB/ Memory
PMIC, APP, Connectivity
APP, RF, BB/Memory
9


SiP Process Technologies - FC
JCET
STATSChipPAC
Cu Column
BoL or SOP
Mass Reflow (MR)
Sub-100um Bump Pitch
Substrate
ETS, MIS
Thin substrate (<100um)
Embedded Inductor
Passives
0201, 01005, 008004
Large Body Inductors
Cu OSP, ENIG
MUF process
SiP
SMT
Low bonding force
High accuracy SPP &
Component Placement
LSC @ 0.4mm BGA pitch
Advanced Molding
Enhanced Vacuum
Transfer Mold
Narrow Gap Filling
EMI Shielding
Conformal Shielding
Compartmental Shielding
10


SiP Process Technologies - WB
JCET
STATSChipPAC
Die Prep.
Stealth Dicing (SDBG)
60um → 30um thin Si
Die Stack
8 Die Stack SiP
16 Die Stack SiP
GaAs
Au wire bond
SiP
Bonding
Au, Ag, Cu
40-45um PP
Substrate
Lead-frame
Laminate (100um thin)
Molding
Compression mold
Transfer mold
11


SiP Process Technologies - FOWLP
JCET
STATSChipPAC
RDL
2L ~ 3L RDL
8/8um → 5/5um → 2/2um
SMT
0201 Passives
Discrete Embedding
Inductor in RDL
IPD
eWLL
0.4mm LGA pitch
SnAg plating
SiP
eWLB
Multi-die (2 ~ 3)
15x15mm body size
Package Height: 0.3mm
Carrier Size
300mm, HD, UHD
12

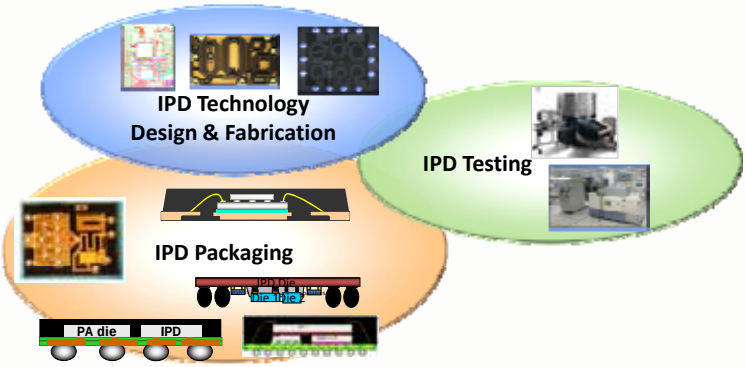
SiP Process Technologies - 2.5D / 3D



13

IPD Package Solutions

- Customized IPDs for integration in SiP
- Stand-alone IPDs – Baluns, Filters, Diplexers, etc.



14

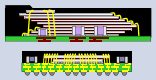
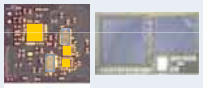
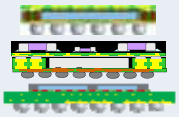
Technology Integration for SiP

Packaging Technology Trends

Market Segment	Drivers	Technology Trends
Networking & Servers	➢ Ever increasing bandwidth requirements for Cloud Computing & Data (~ IoT)	➢ Mainstream to stay with High Density FC technology ➢ 2.5D/3D adoption for high end applications
Mobile Processors	➢ Bandwidth ➢ Performance ➢ Form Factor	➢ FOWLP / Interposer PoP - Premium segment / High end ➢ Wide scale adoption of PoP - Mid~ Hi-end ➢ fcFBGA - Tablets
Mobile Chipset / Peripheral	➢ Integration to reduce total system cost, shorten design time, reduce FF ➢ Plug & play solutions ➢ SiP proliferation	➢ Increased SiP components for integration of various components (power, sensors, controllers, memory, RF) ➢ Increased WLCSP & FOWLP ➢ Low cost substrate
IoT / WE	➢ Low power MCU, Sensors & Connectivity ➢ Low cost ➢ Small FF	➢ Continued use of low cost package tech ➢ Higher integration to meet the FF & cost targets ➢ FOWLP-PoP adoption for MEMS / Logic ➢ Low cost substrates (MIS, ETS, SMS, ...)

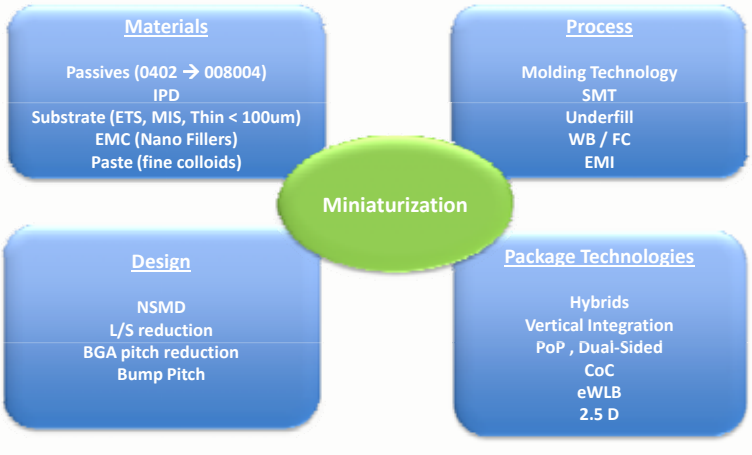
16

SiP Module Configurations & Applications

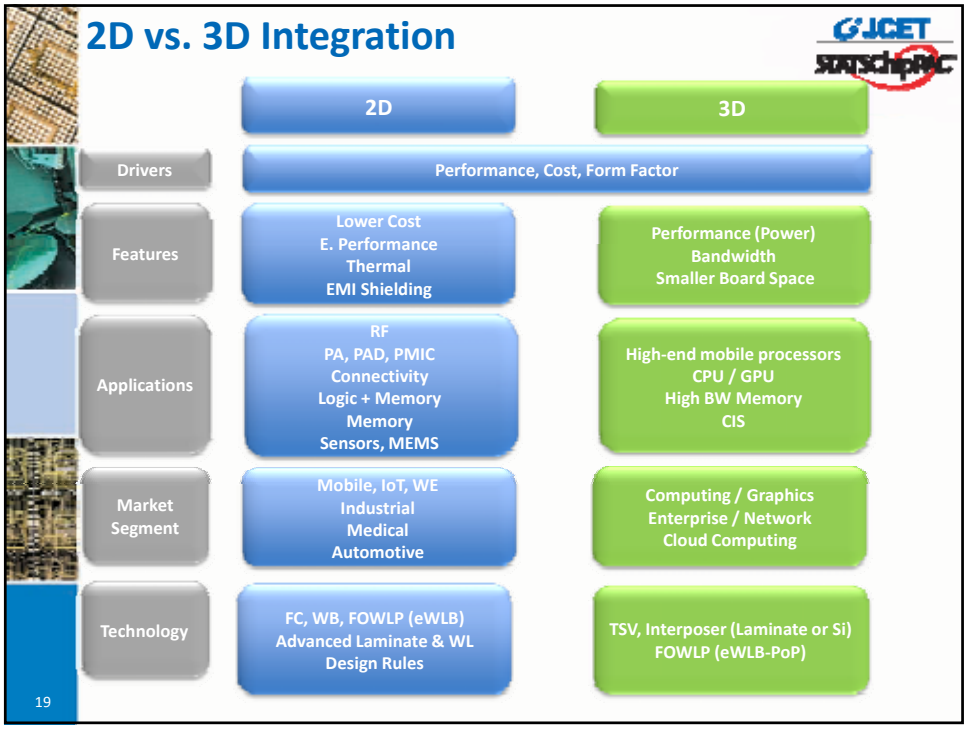
SiP Package Types		Features	Applications
Stacked Die Module		• LGA/BGA • Thin Stacked Die • Passives	• SSD (Removable & Embedded) • BB/AP Processors (WE)
Substrate Module		• LGA/BGA • Bare Die or Over-Mold • IPDs, Passives • Cu OSP + LF Solder	• Filters • PA Modules • Connectivity Combo Modules
fcFBGA SiP		• Passives, WLCSP, Packaged Components • Coreless or cored substrates	• Controller Modules • PA/PAD Modules • RF FEM
Hybrid (FC+WB) SiP			
FOWLP (eWLB) SiP		• Multi-die embedded • 10/10 → 5/5um L/S • Passives Integration • 5x5~ 12x12mm Body Size	• Connectivity • PMIC, CODEC • PA Modules • AP processor+ Memory • RF MEMS
eWLB-PoP & 2.5D SiP		• eWLB-PoP (eBAR) • 0.4 → 0.2mm stacking pitch	• High-end AP Processors • CPU/GPU • High bandwidth

17

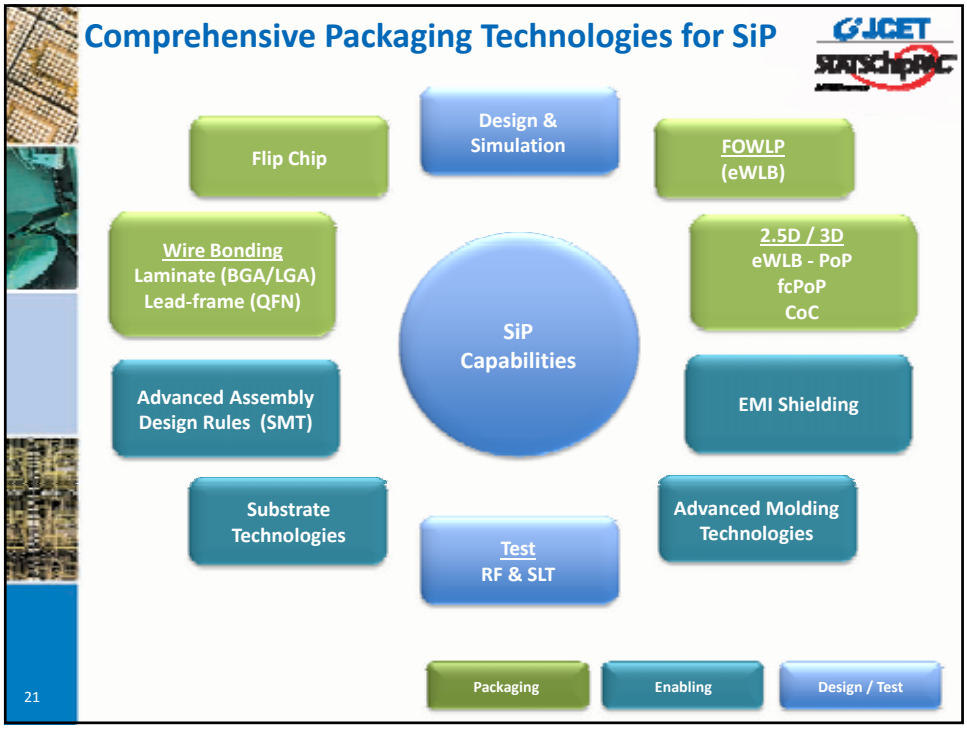
Miniaturization

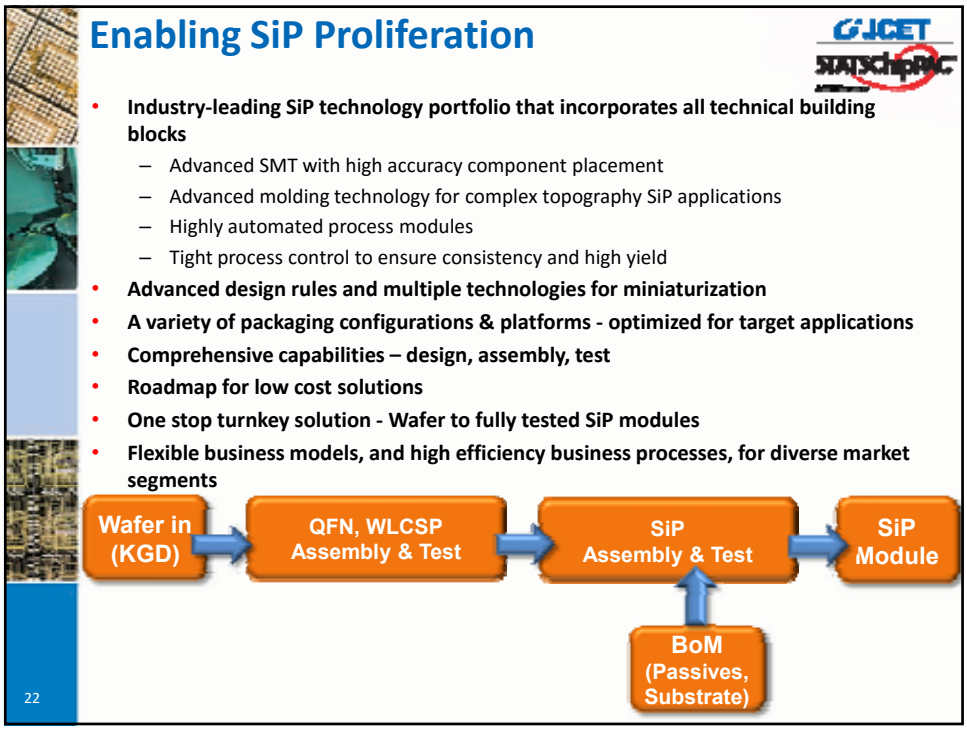


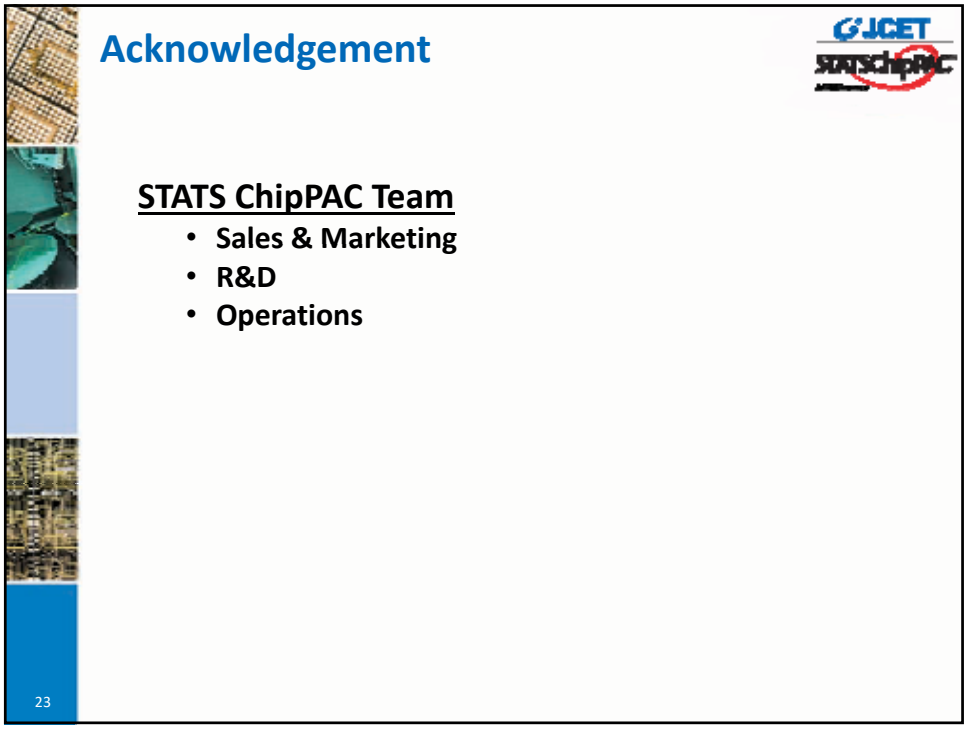
18

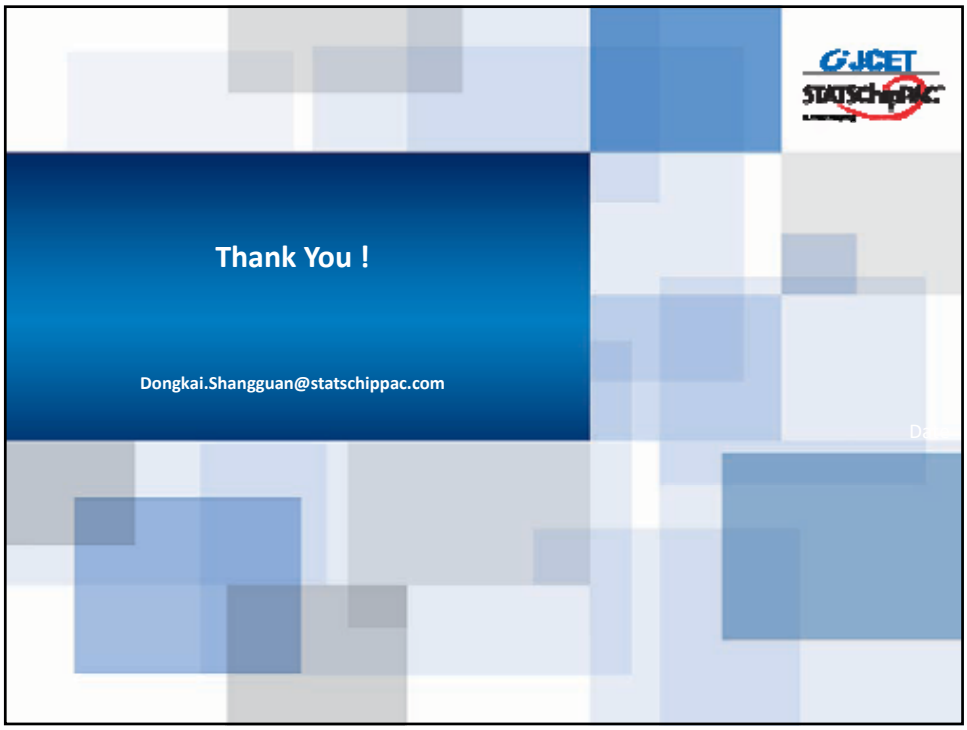

2D vs. 3D Integration
2D
3D
Drivers
Performance, Cost, Form Factor
Features
Lower Cost
E. Performance
Thermal
EMI Shielding
Performance (Power)
Bandwidth
Smaller Board Space
Applications
RF
PA, PAD, PMIC
Connectivity
Logic + Memory
Memory
Sensors, MEMS
High-end mobile processors
CPU / GPU
High BW Memory
CIS
Market Segment
Mobile, IoT, WE
Industrial
Medical
Automotive
Computing / Graphics
Enterprise / Network
Cloud Computing
Technology
FC, WB, FOWLP (eWLB)
Advanced Laminate & WL
Design Rules
TSV, Interposer (Laminate or Si)
FOWLP (eWLB-PoP)
19


Summary


Comprehensive Packaging Technologies for SiP
JCET
STATSCHIPPAC
Flip Chip
Design & Simulation
FOWLP (eWLB)
Wire Bonding
Laminate (BGA/LGA)
Lead-frame (QFN)
SiP Capabilities
2.5D / 3D
eWLB - PoP
fcPoP
CoC
Advanced Assembly Design Rules (SMT)
EMI Shielding
Substrate Technologies
Test
RF & SLT
Advanced Molding Technologies
Packaging
Enabling
Design / Test
21


Enabling SiP Proliferation
JCET
STATSCHIPPAC
• Industry-leading SiP technology portfolio that incorporates all technical building blocks
– Advanced SMT with high accuracy component placement
– Advanced molding technology for complex topography SiP applications
– Highly automated process modules
– Tight process control to ensure consistency and high yield
• Advanced design rules and multiple technologies for miniaturization
• A variety of packaging configurations & platforms - optimized for target applications
• Comprehensive capabilities – design, assembly, test
• Roadmap for low cost solutions
• One stop turnkey solution - Wafer to fully tested SiP modules
• Flexible business models, and high efficiency business processes, for diverse market segments
Wafer in (KGD)
QFN, WLCSP Assembly & Test
SiP Assembly & Test
SiP Module
BoM (Passives, Substrate)
22


Acknowledgement
STATS ChipPAC Team
• Sales & Marketing
• R&D
• Operations
23


Thank You !
Dongkai.Shangguan@statschippac.com