Presented to the Santa Clara Valley Chapter,
IEEE CPMT Society
Tuesday, November 22, 2016

WAFER LEVEL PROCESS FORMATION OF A POLYMER ISOLATED CHIP SCALE PACKAGE

Outline

- Small Silicon CSP device
- Assembly Issue
- Polymer Isolation Process Module
- Experimental Results
- Conclusion
- Q & A

0201/01005 Silicon CSP

- 2 Lead Chip Scale Package 0201/01005 sized devices
- 100% of the CSP area is the silicon
- Using a 01005 sized CSP device occupies less board area compared to the same sized die built in a plastic molded package

Small CSP package

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01005

0201

01005 sized CSP

- More than Two Thousand 01005 parts able to fit on top of a dime
- Dime thicker than six 01005 parts

Dime Diameter: 17.91 mm
Dime Thickness: 1.35 mm

ASSEMBLY SHORT ISSUE

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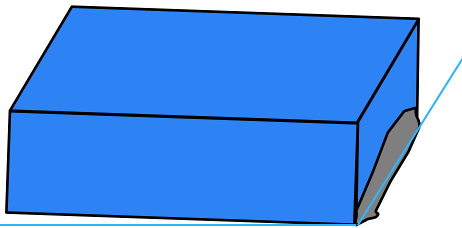
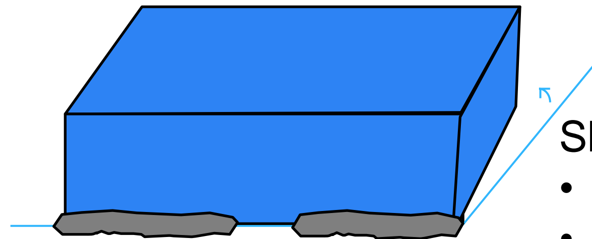
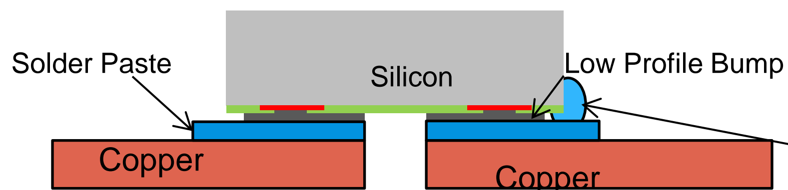

Solder Bridge on the CSP end
(CSP tilted at the end)


Solder Bridge on CSP side
(CSP tilted to one side)

Short/Leakage contributing factors
- Short Bump Height (Low Profile)
- Solder Paste Proximity to CSP Edge
- Solder Stencil to Pad Alignment
- CSP placement accuracy and tilt



Excess Solder (Short between bare silicon die sidewall and the PCB pad)

SOLDER SHORT ISSUE

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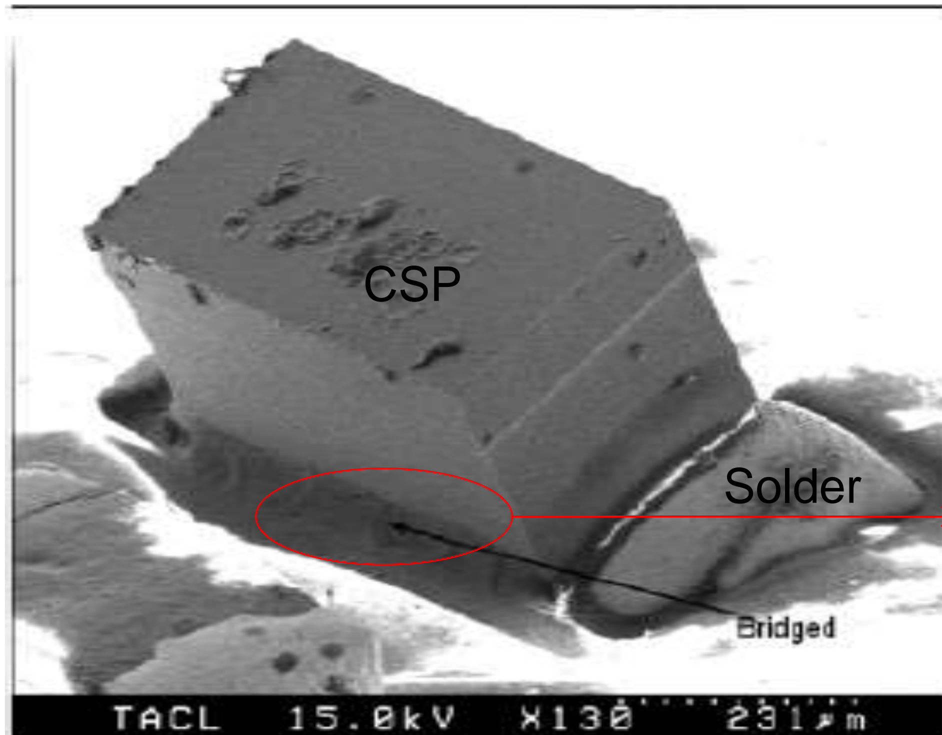
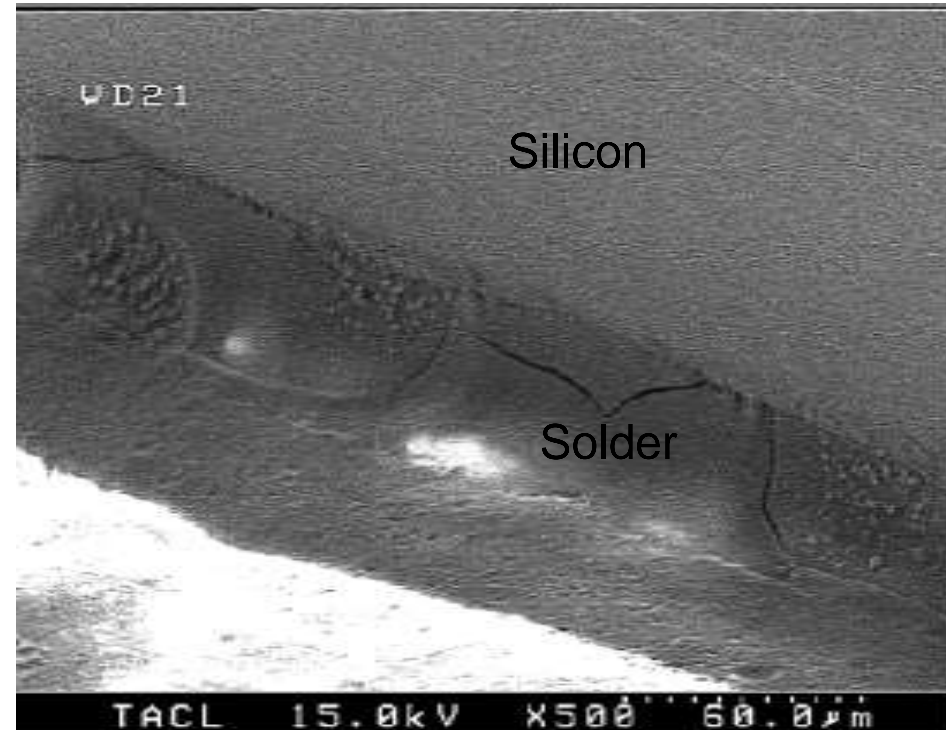


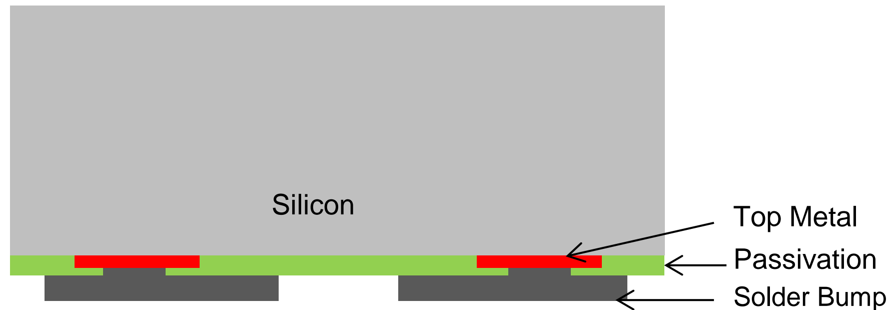
0201 CSP Tilt
(Sidewall Bridging)



Close up image
Of sidewall Solder Bridging

Short causes assembly rework and added cost

5-Side Polymer Isolation

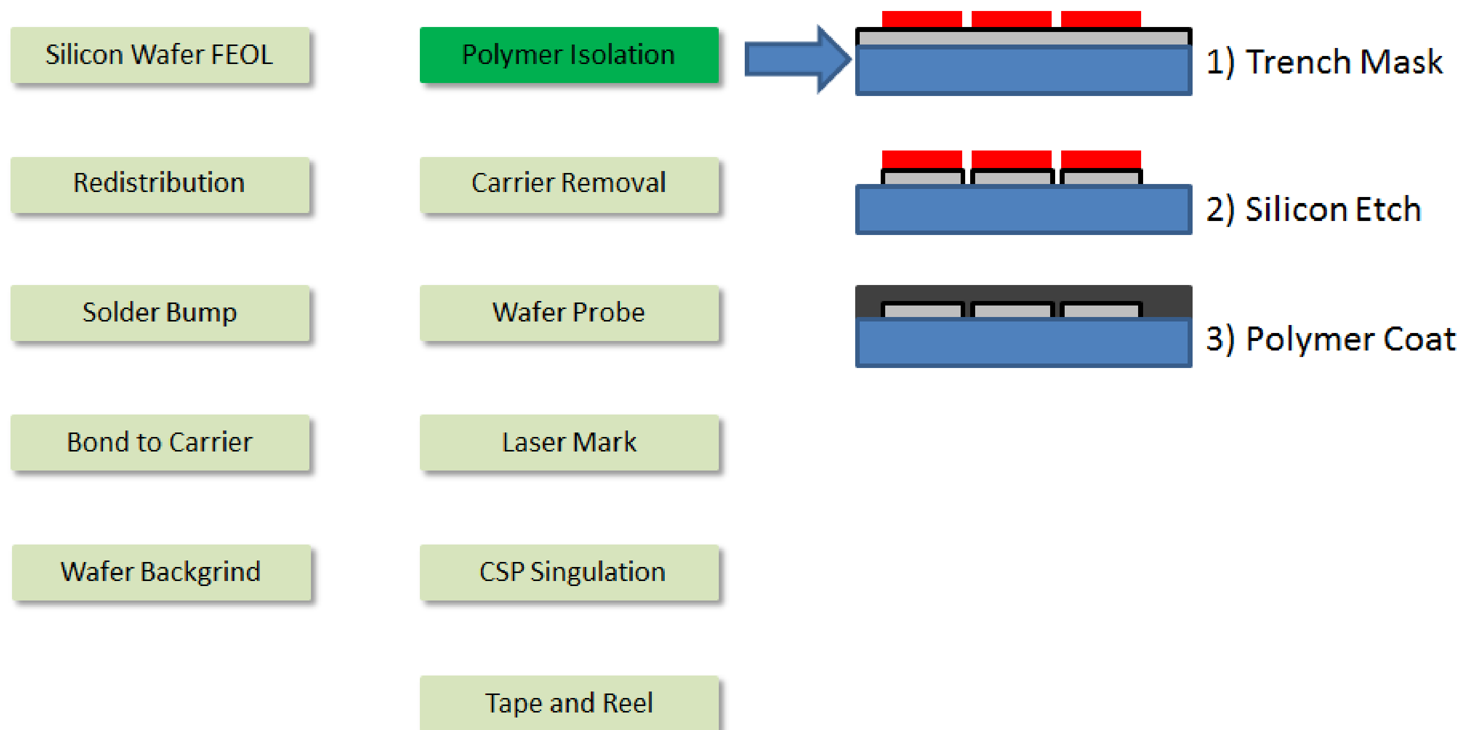


Conventional Bare Silicon CSP

5-Side Polymer Isolated CSP

- About 70% of a 0201/01005 CSP area is available for silicon circuits
- Area lost due from the saw street region
- Silicon removed from the saw street & replaced with a polymer
- No lost in silicon real estate area with the addition of the polymer isolation
- Polymer Isolation on silicon sidewall prevents the assembly short issue
- Polymer on the backside prevents short to the silicon backside

PROCESS FLOW



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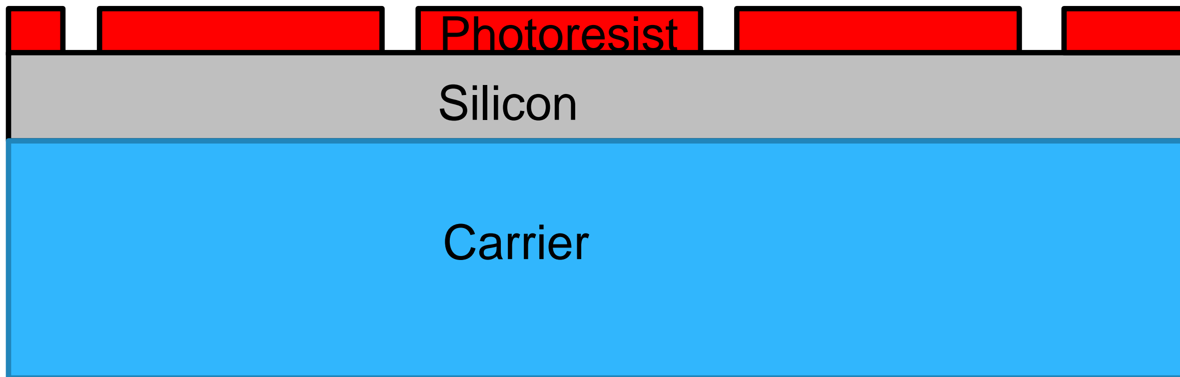
Process Flow (Brief)

1) Mount Wafer to Carrier Substrate
2) Silicon Wafer Backgrind

Process Flow (Brief)



3) Scribe line Silicon Trench Mask

Process Flow (Brief)

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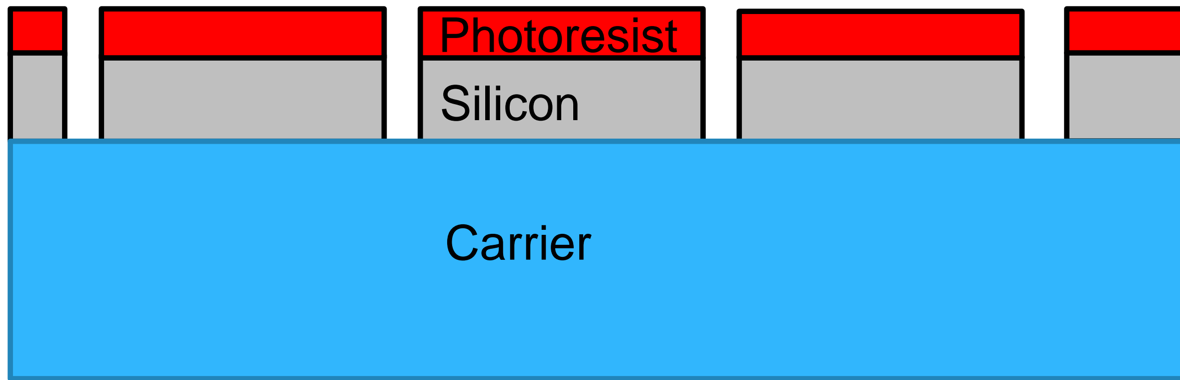
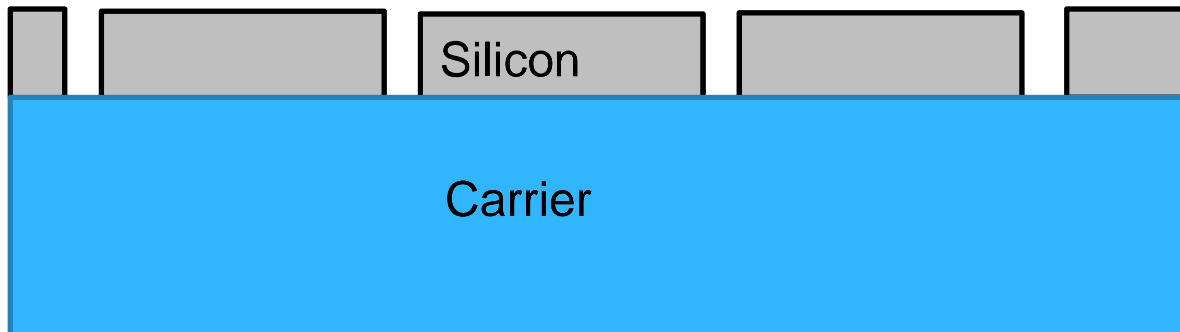
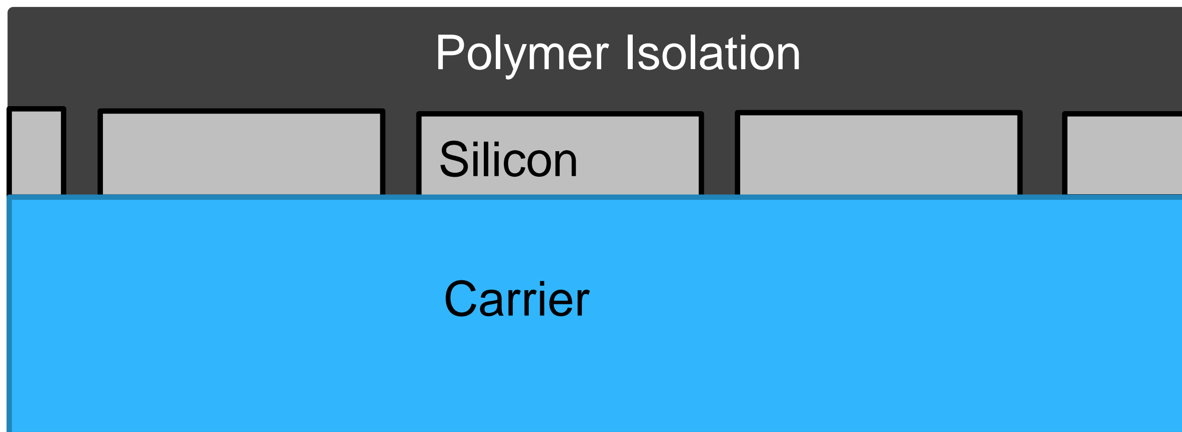


4) Silicon Trench Etch
Suitable for products that have Test Structures and Dummy Fill in the Scribe Line region.



5) Resist Clean

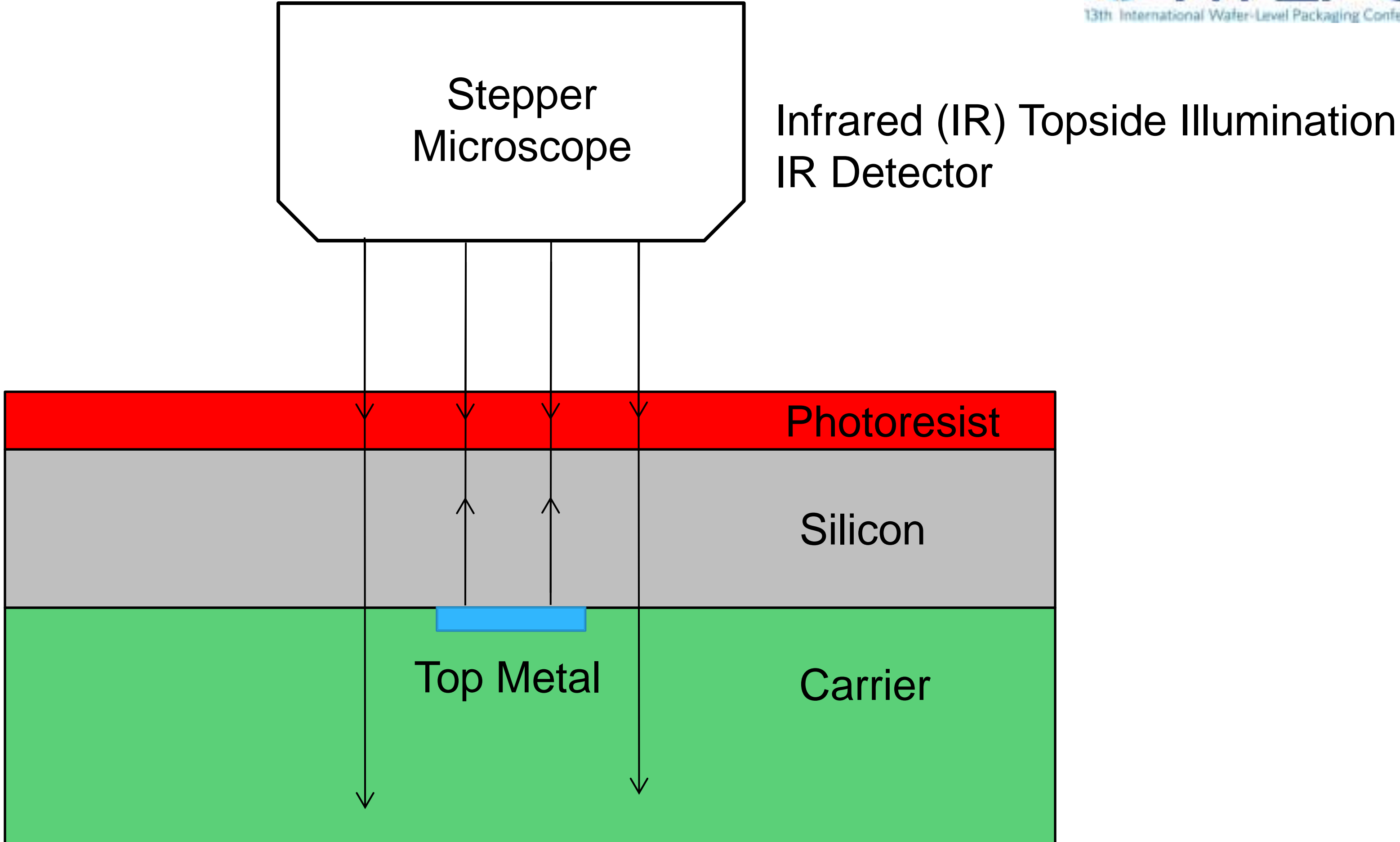
Process Flow (Brief)



6)Polymer Coat & Cure

Final Probe done after carrier removal
Screens out dies damaged from defects at Silicon Etch Module

BACKSIDE ALIGNMENT



Silicon Etch Alignment

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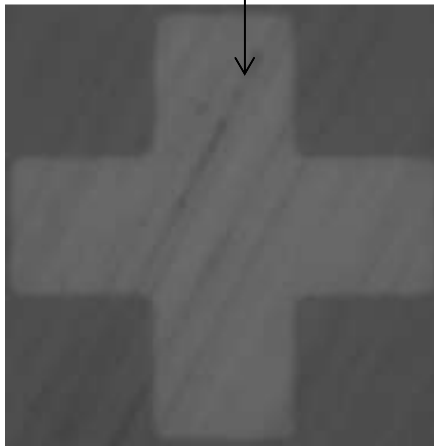
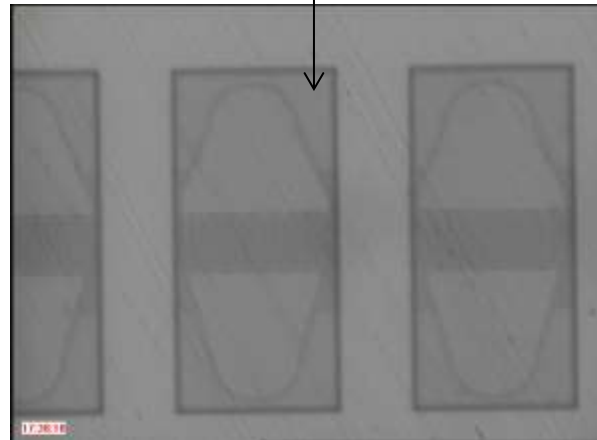
Top Metal



Alignment Feature
IR Camera
(Stepper)

Photoresist

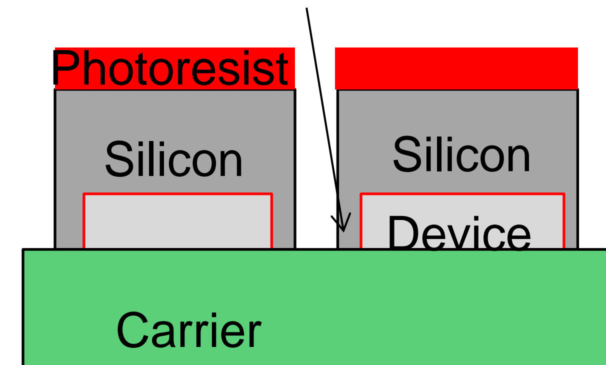


- Develop Inspection (IR Scope)

Check Pattern Alignment
Product & Misalignment Structure

- CD Measure

Silicon Etch Space to
Front side active Silicon Devices
(7.5 um)
Alignment is important



After Silicon Plasma Etch

- Wafer Probe done after Silicon Plasma Etch Module
- Reject dies that may be Damaged from the silicon etch

Cross Sections

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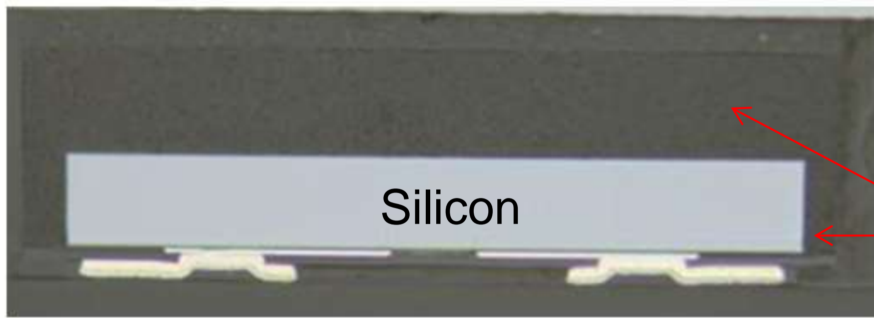
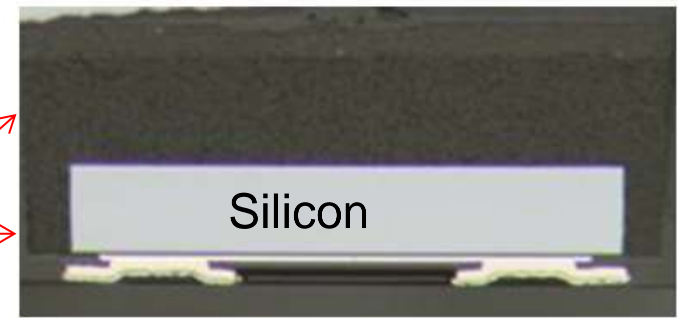


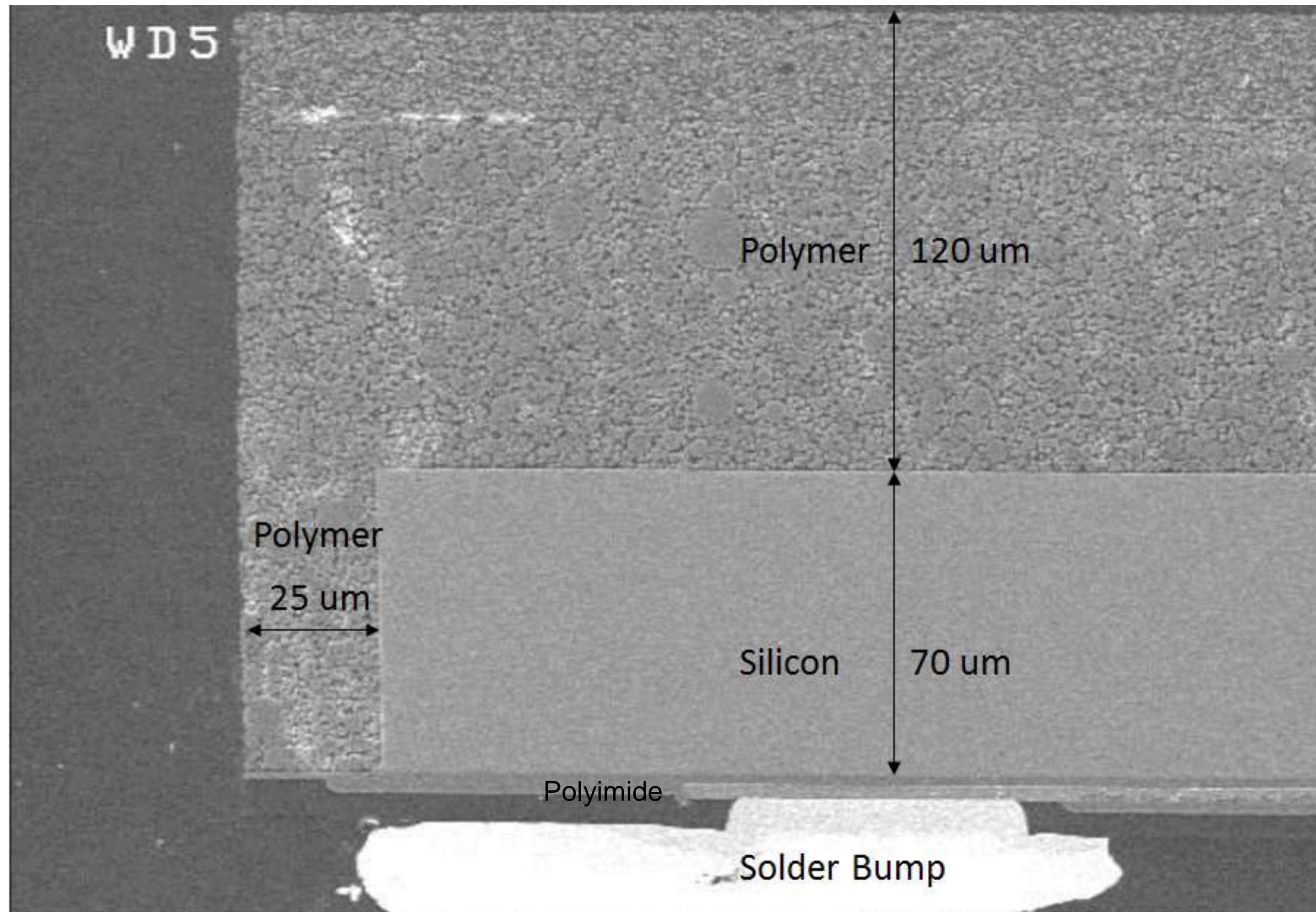
Polymer



0201 Sized Polymer Isolated CSP
(0.200 mm Thick)

01005 Sized Polymer Isolated CSP
(0.170 mm Thick)

SEM Cross Section



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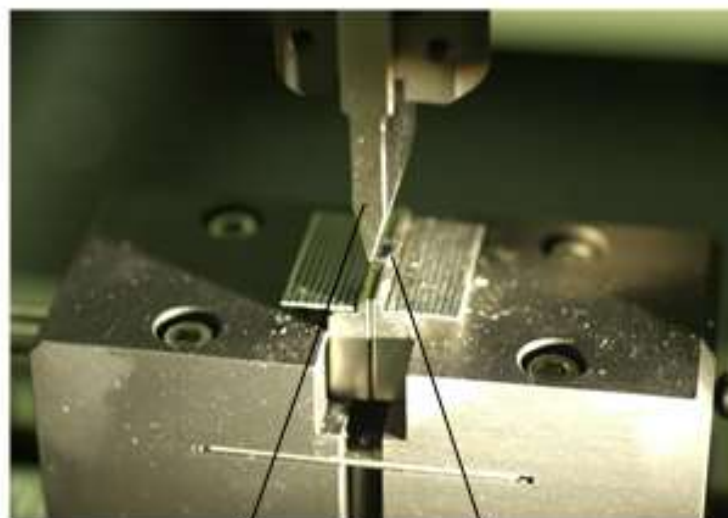
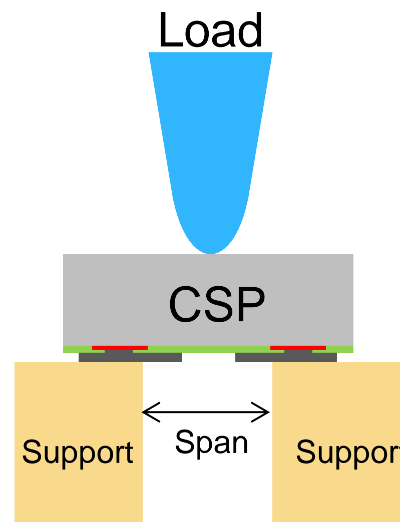
Experimental Results
Mechanical Strength
Reliability

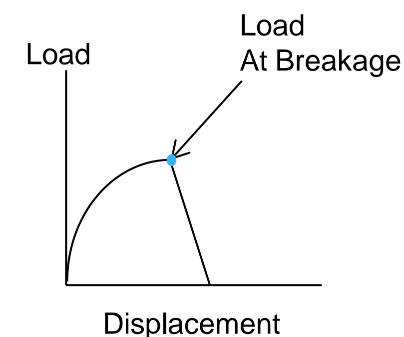
Mechanical Strength
3 Point Bend Test Setup



Setup

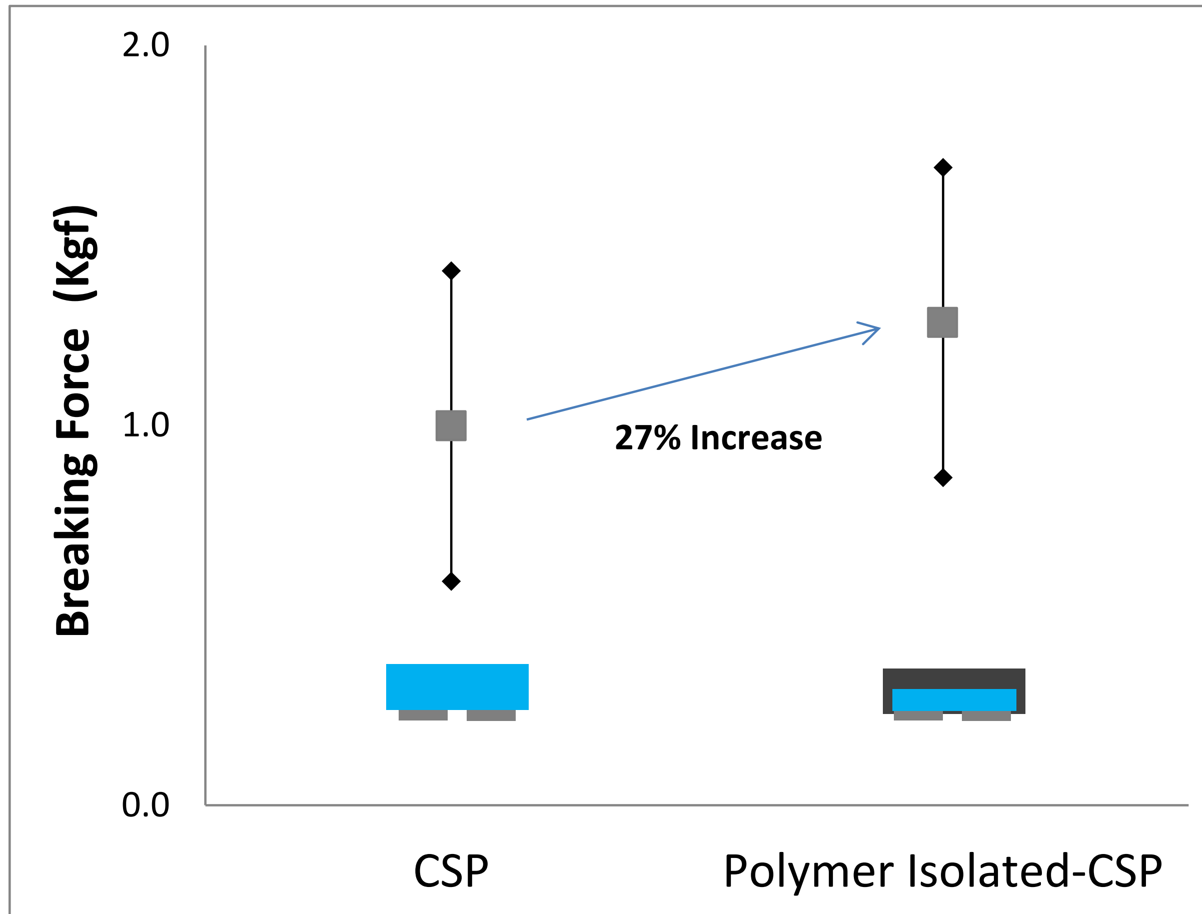


Setup
Cross Section



Force (Load) vs Displacement Curve (Example)

Mechanical Strength



CSP Thickness:
Bare Silicon: 270 um
Polymer Isolated: 200 um

Mechanical Strength
Silicon Fracture Stress

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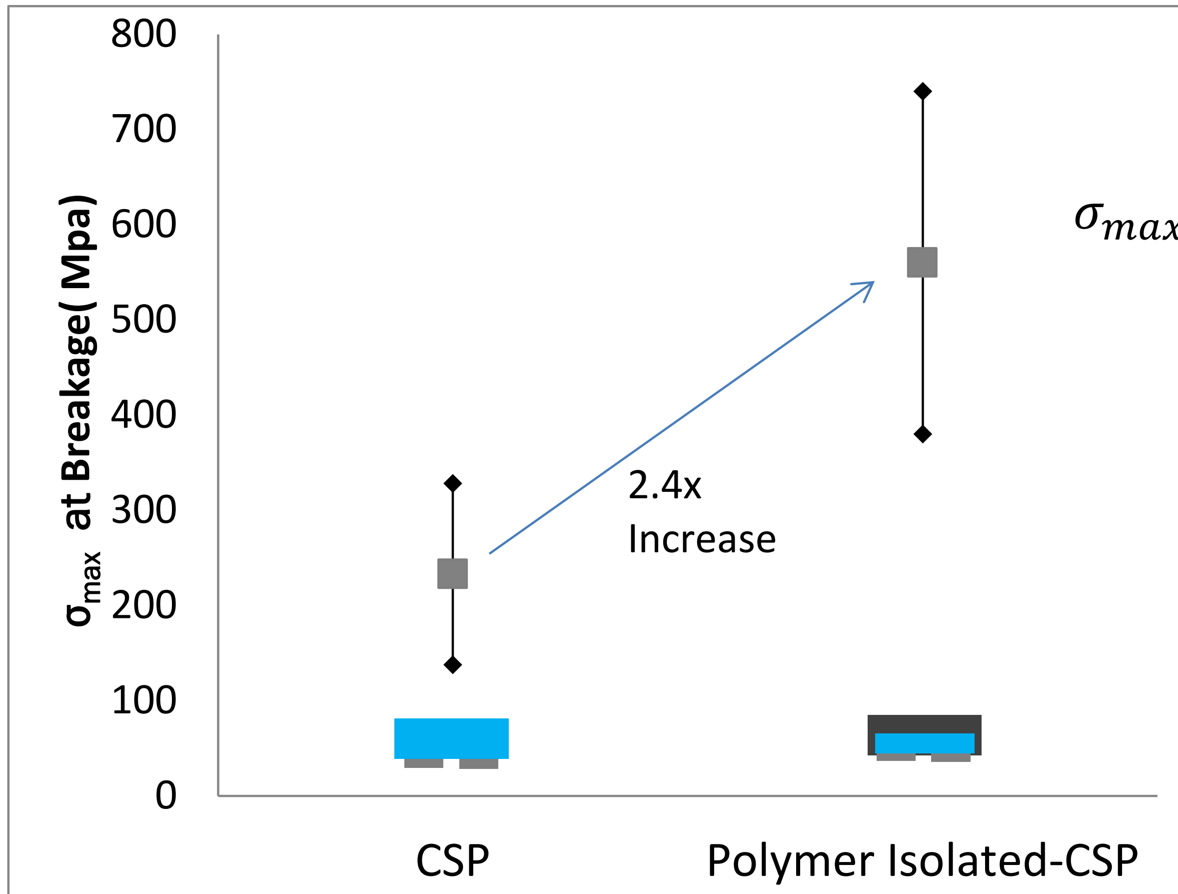

$$\sigma_{max} = \frac{3 \times F_{break} \times L_{span}}{2 \times W \times T^2}$$

Silicon Fracture Stress Increase

- Poly Isolation
- Plasma Etch Silicon Street

Plasma Silicon Etch Scribe

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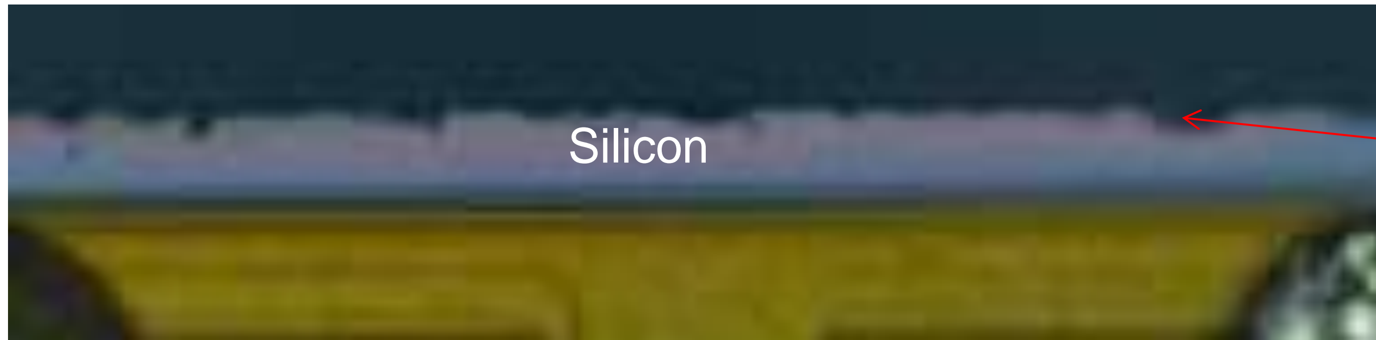
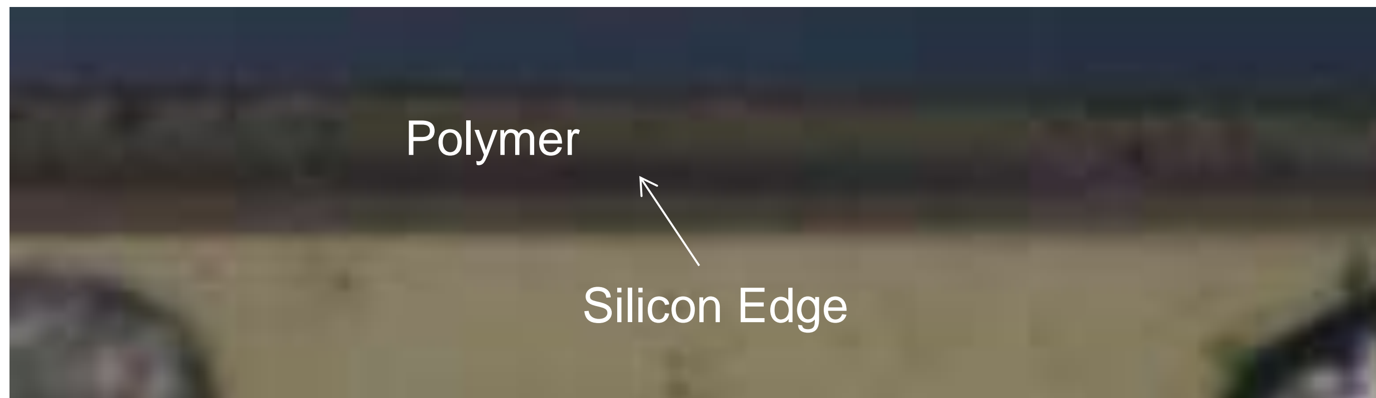


Traditional Mechanical Dicing Saw



Polymer Isolated CSP With Plasma Silicon Etch

Board Level Reliability

Board Level Test	Condition	Read Point	Rej/ sample size
Board Assembly Yield	Mount on Board & Test	Test After Mount	0/1180
Highly Accelerated Stress Test (HAST)	Temp= +130°C, RH=85%,18.8 psig, biased	96 hr	0/270
Temperature Cycle	T = -65°C to 150°C	1000 cycles	0/270

Polymer Intact After HAST

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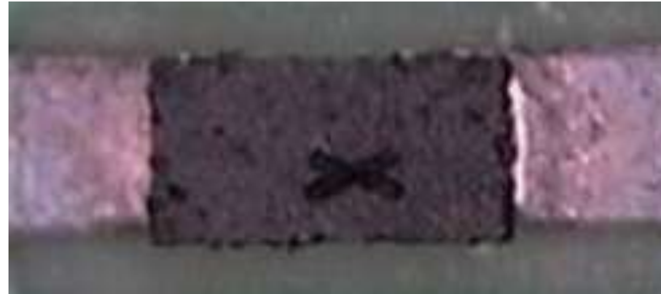
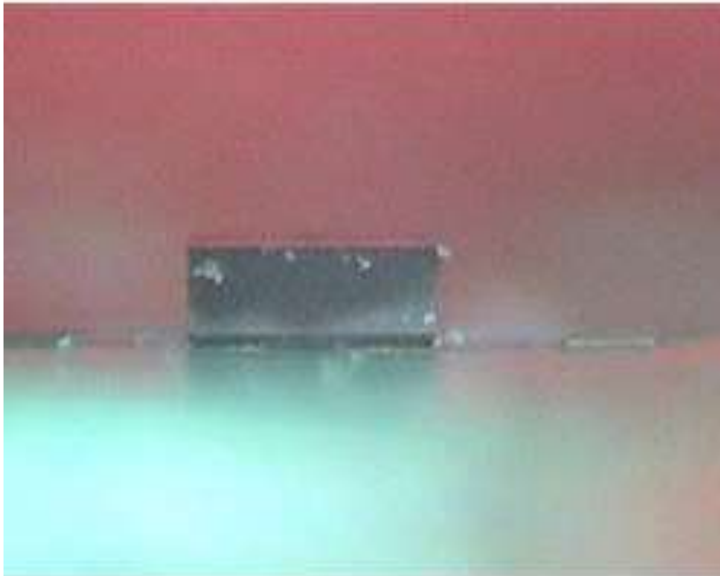
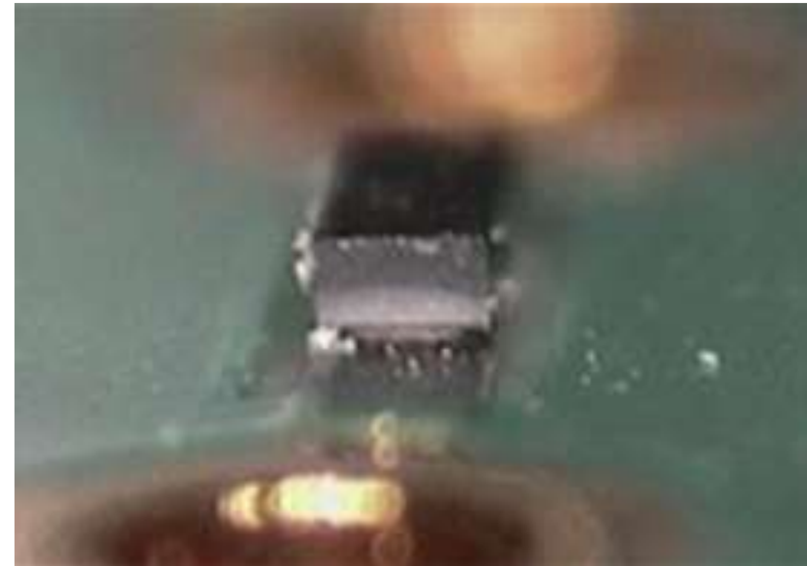


Top View



Side View



End View

X-Ray Image

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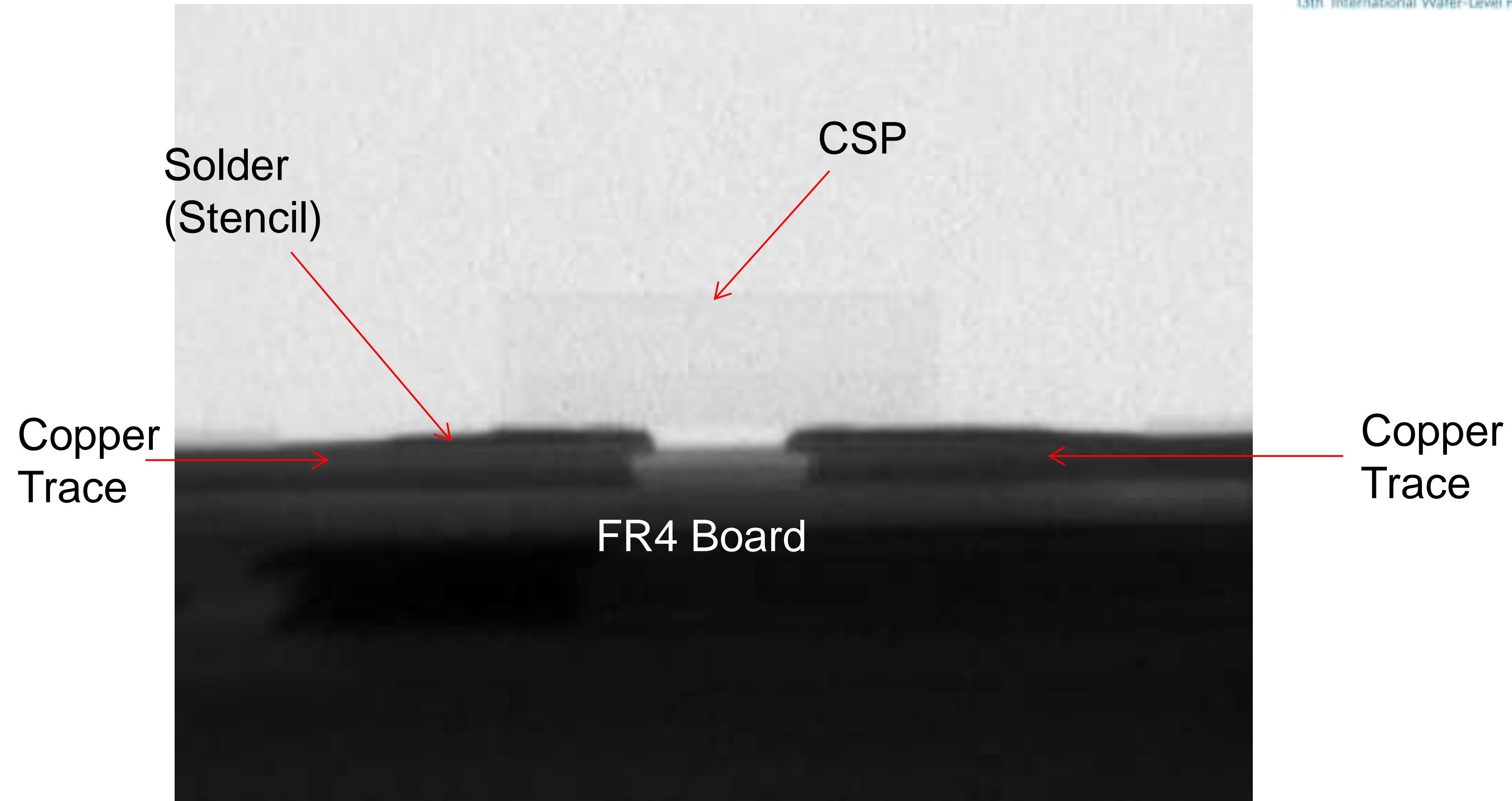

Black & White X-Ray of CSP after HAST Reliability

X-Ray Image

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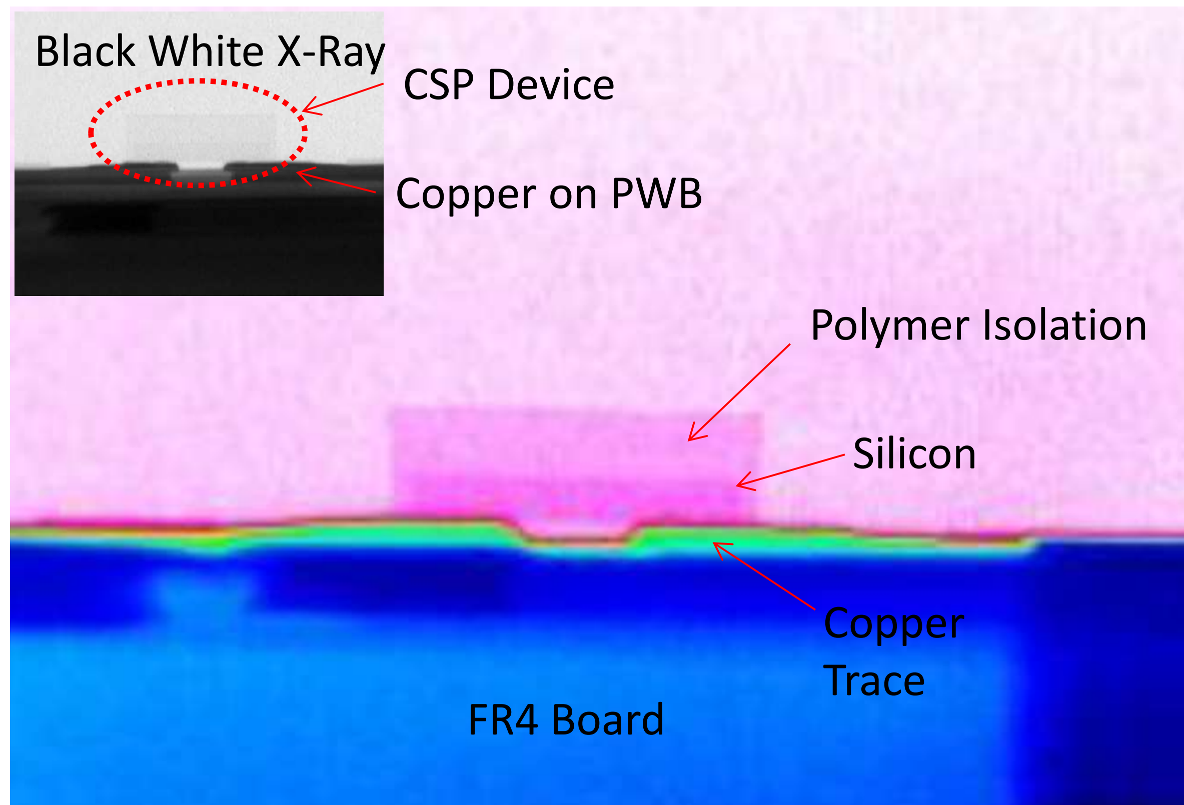

Black & White/Color X-Ray of CSP after HAST Reliability

Polymer Sidewall Isolation

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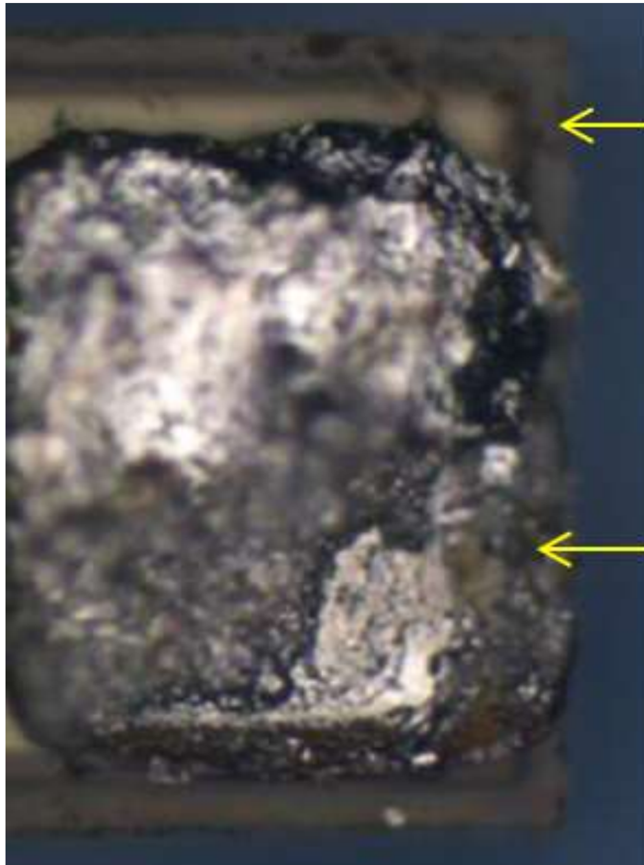

Polymer
Sidewall Isolation

Solder

No Leakage to substrate due to Polymer Isolation on sidewalls
Even if solder extends to the scribe and along the sidewall

CONCLUSION

A 5-side polymer 0201/01005 CSP requires the bulk silicon to be thinned down to maintain the low profile final package thickness.

- Thinner silicon decreases the mechanical strength
- Improve silicon strength with silicon plasma etch instead of mechanical diamond saw

Polymer Isolated 0201/01005 sized CSP key points:

- Polymer Sidewall Isolation eliminates assembly solder shorts to the silicon
- Wafer Level Polymer Process Module integrated into standard CSP Flow
- Carrier provides mechanical support during polymer formation module after the wafer is thinned to <100um
- Backside Silicon Street Etch suitable for scribe lines that contain test structures and dummy fill
- 27% better mechanical strength than typical bare silicon CSP (Silicon Plasma Etch and polymer isolation)
- Industrial Temp Cycle Performance (> 1000 cycles 150C to -65C)
- Polymer Isolation still intact after HAST (96 hr)
- Qualified for Production

Thank You!

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