Ten Years of Robustness Validation Applied to Power Electronics Components

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Ten Years of Robustness Validation Applied to Power Electronics Components

1. Introduction
2. Robustness Validation Process
   - Handbooks, Standards
   - Robustness Margin
   - Mission Profile
3. Qualification of Power Modules
4. Qualification of DC Link Capacitors
5. End of Life Tests
   - Accelerated Mechanical Fatigue Testing
   - Cosmic Ray Testing
6. Advanced Technologies
   - Thick wire copper bonding
   - Planar Interconnects
   - Embedded Power Electronics
7. Conclusions
8. References
The Basic Question

Have I passed my qualification tests according to the standard?

Is our product "sufficiently reliable" in the application?

Fit for use

Fit for standard

Robustness Validation Process

The new 'test to fail' qualification approach (instead of a 'test-to-pass'), is a paradigm shift from 'Fit for Standard' to 'Fit for Application'.

Robustness Validation generates knowledge on the relevant component failure mechanisms that may occur at the boundaries of the specification limits.

Therefore Components could be designed with known robustness margins combined with cost and time saving potentials.

60 companies formed a task force to settle a new comprehensive Qualification method:
- ZVEI
- SAE
- AEC
- JSAE
RV is a knowledge-based approach:
- Knowledge of the conditions of use (mission profile)
- Knowledge of the failure mechanisms and failure modes
- Knowledge of acceleration models for the failure mechanisms

**Definition Robustness Validation** is a process to demonstrate that a product
- performs its intended function(s) with sufficient robustness margin
- under a defined mission profile for its specified lifetime.
Robustness Margin

- Time at end of expectation
- Degradation

Customer Application

Robustness curve at Time 0

Mission Profile

- Mission profiles should be generated down the supply chain in an interactive way.

Mission Profile Components:
- car
- system
- module
- component

requirements
freeze of specification
freeze of design

generation of mission profile
A Mission Profile is a simplified representation of relevant conditions to which the Device/Component production population will be exposed in all of their intended application throughout the full life cycle of the component.

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Qualification of Components for E-Mobility

ZVEI-ECPE Team Power Electronics

LV324  LV324/ Lifetime  DC-Link Film C

OEMs
5 German carmakers

1st Tier B
3 German Subsystem suppliers

2nd Tier B
3 – Power Modules/6 – DC-Link

→ Harmonisation with JEITA is in progress

IEEE CPMT/SVC April 27, 2017

Power Module Qualification

LV324 Qualification of Power Electronics Modules for Use in Motor Vehicle Components
General Requirements, Test Conditions and Tests

Scope
This document defines requirements, test conditions and tests for validating properties, including the service life, of power electronics modules for use in components of motor vehicles up to 3.5 t. The described tests concern the qualification of components at module level but not the qualification of semiconductor chips or production processes.

Overview
The tests described in the following serve to validate the properties and service life of power electronics modules for use in the automotive industry. The defined tests are based on the currently known failure mechanisms and the motor vehicle-specific application profiles of power modules.
**Power Module Tests**

<table>
<thead>
<tr>
<th>QM module test</th>
<th>(Determination of the electrical and mechanical parameters after the individual qualification tests)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate parameters</td>
<td></td>
</tr>
<tr>
<td>Rated and reverse currents</td>
<td></td>
</tr>
<tr>
<td>Forward voltages</td>
<td></td>
</tr>
<tr>
<td>X-ray, scanning acoustic microscopy (SAM)</td>
<td></td>
</tr>
<tr>
<td>IPI VI/OMA</td>
<td></td>
</tr>
</tbody>
</table>

**Characterizing module tests**

- QC-01 Determination of parasitic stray inductance (Lp)
- QC-02 Determination of thermal resistance (Rth value)
- QC-03 Determination of short-circuit resistance
- QC-04 Insulation test
- QC-05 Determination of mechanical data

**Power Module Tests**

**Environmental tests**

- QE-01 Thermal shock (TST)
- QE-02 Contactability (CO)
- QE-03 Vibration (V)
- QE-04 Mechanical shock (MS)

**Life tests**

- QL-01 Power cycle (PCsec)
- QL-02 Power cycle (PCmin)
- QL-03 High temperature storage (HTS)
- QL-04 Low temperature storage (LTS)
- QL-05 High temperature reverse bias (HTRB)
- QL-06 High temperature gate bias (HTGB)
- QL-07 High humidity high temperature reverse bias (H3TRB)

- Final test to record the electrical parameters of all DUTs
- Conversion of the test results into reliability data
Power Module Tests

4.1.4 Chip-near interconnect technology
Chip upper side connection design and design of chip lower side connection with the substrate.
Examples:
Chip upper side: bond wire, ribbon bond, copper clip, sintering technology
Chip lower side: chip soldering, sintering technology, diffusion soldering

4.1.5 Chip-remote interconnect technology
Connection design which does not directly include the chip. A distinction shall be made between interconnect technology for electrical and thermal interfaces. Due to the design, chip-remote interconnect technology may be both electrical and thermal.
Examples:
Electrical interfaces: design of load and auxiliary contact connection
Thermal interface: system soldering between substrate and base plate (modules with base plate) or interface between module and cooling system (modules without base plate)

Power cycling reliability of IGBT4

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PCsec Test Conditions

Table 11: Limit values for test parameters PCsec

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load current on-time ( t_{ON} )</td>
<td>&lt; 5 s</td>
</tr>
<tr>
<td>Load current level ( I_{L} )</td>
<td>&gt; 0.85 ( t_{ON} ) a, b</td>
</tr>
<tr>
<td>Gate-voltage ( U_{G} )</td>
<td>Typically 15 V c</td>
</tr>
</tbody>
</table>

a The load current level of > 0.85 \( t_{ON} \) shall only be selected for one sample point.
b A value < 0.85 \( t_{ON} \) can be selected for the second and further sample points to enable a suitable temperature increase difference to be set.
c The gate-voltage for the IGBT and MOSFET test can (e.g. if contact current densities become too high) be less than 15 V if the desired temperature increase cannot be implemented with on-times of \( t_{ON} < 5 \) s due to the module's thermal properties. However, it shall always be guaranteed that the switch is permanently operated in the saturated range. In such cases, the gate-voltage which is used shall be accordingly adapted once at the start of the test and shall be documented in each case.

<table>
<thead>
<tr>
<th>Forward voltage</th>
<th>IGBT: ( U_{CE,sat} )</th>
<th>MOSFET: ( U_{DS} )</th>
<th>Diode: ( U_{F} )</th>
<th>5 % a</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increase in virtual junction temperature swing</td>
<td>( \Delta T_{Vj} )</td>
<td>+ 20%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Failure Criteria

Life Time Model/ Reliability Curve

Lifetime Models for a certain IGBT module technology showing the impact of power cycle \( t_{on} \) times at a given aspect ratio of the bond loop.
PCT with Different Control Strategies

1. Constant timing
2. Constant $\Delta T_{\text{baseplate}}$
3. Constant power dissipation
4. Constant $\Delta T_{\text{junction}}$

Failure criteria

Temperature [°C]

Cycle count

Source: U. Scheuermann, ESREF 2010

Calculation of life time from the given mission profile

Electrical characteristics
$V_{\text{DC}}, I_{\text{rms}}, E_{\text{loss}}, P_{\text{total}}$

Motor + drive control
$V_{\text{DC}}, \text{phase current, } m, \cos \varphi, f_{\text{TH}}$

Mission profile

Loss Calculation

Loss profile
$Z_{\text{loss}}, Z_{\text{on}}, Z_{\text{on saturation}}, \text{IGBT / diode}$

Cooling conditions

Thermal simulation

Temperature Profile
$T_{\text{real}}, \text{IGBT / diode / solder}$

Climatic conditions
$T_{\text{ambient}}$

Calculation of $\Delta T$ occurrence

Cycle numbers with different $\Delta T$

Life-time modeling
$T_{\text{ambient}}$ dependence

Life time
Consumption per year

M. Thoben/ Infineon
Consolidated Results after Rainflow Counting

Estimation of Lifetime

Calculation of lifetime based on mission profile
Overview of calculation steps

Mission Profile
Power loss model
Temperature profile
Power cycling / thermal cycling
Lifetime model

Delta T
Time
Number

Supplier A 2K
Supplier B 2K
Supplier C 2K corr.
Supplier D
Supplier E
1. The process is good for any drive cycle

2. The weakest parts in a power module are normally the bond wires, substrate solder and chip solder. This is due to the differences in the Coefficient of Thermal Expansion CTE

3. A translation has to be made from the vehicles mission profile down to the device/interconnect level

Finally the robustness margin can be estimated using a lifetime model/ reliability curve from the module manufacturer
**Typical Types of Capacitors for DC-link Applications**

Performance comparisons of the 3 types of capacitors

<table>
<thead>
<tr>
<th>Relative Performance</th>
<th>Al-Caps</th>
<th>MPPF-Caps</th>
<th>MLCC-Caps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superior</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intermediate</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inferior</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Dominant failure modes and critical stressors**

<table>
<thead>
<tr>
<th></th>
<th>Al-Caps</th>
<th>MPPF-Caps</th>
<th>MLCC-Caps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dominant failure modes</td>
<td>open circuit</td>
<td>open circuit</td>
<td>short circuit</td>
</tr>
<tr>
<td>Most critical stressors</td>
<td>$T_s, V_c, l_c$</td>
<td>$T_s, V_c, humidity$</td>
<td>$T_s, V_c, vibration/shock$</td>
</tr>
<tr>
<td>Self-healing capability</td>
<td>moderate</td>
<td>good</td>
<td>no</td>
</tr>
</tbody>
</table>

Al-Caps: Aluminium electrolytic capacitors
MPPF-Caps: Metallized Polypropylene Film Capacitors
MLCC-Caps: Multilayer Ceramic Capacitors
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Reliability Analysis of Wire Bonds in Semiconductor Packages

B. Czerny *, A. Mazloum-Nejadari b, G. Khatibi c

* Christian Doppler Laboratory for Lifetime and Reliability of Interfaces in Complex Multi-Material Electronics, CTA, TU Wien, Vienna, Austria
b Institute of Informatics, TU Wien
c Institute of Informatics, TU Vienna

ECPE Workshop, Thermal and Reliability Modelling and Simulation of Power Electronics Components and Systems
Fuerth/Nuremberg, Germany

Bond Wire Lift-off Failure in Power Modules

Investigating the thermo-mechanical fatigue of 400μm Al bond wire interconnects with respect to bond wire lift-off failure
Time consuming PC as a standard testing method for bond wire lift-off failure
Developing a mechanical testing method for fast fatigue qualification for wire bond lift-off failure
- Can accelerated mechanical testing provide similar fatigue failure?
- Is there a influence due to the accelerated testing frequency?
- Can the results be compared to standard testing methods?
Accelerated Mechanical Fatigue Interconnect Testing Setup (AMFIT)

- Mechanically exciting bond wire near interface in bonding direction
- Gripping bond wire ~200μm above bonding surface
- Small static tensile load preventing rebonding and grinding
- Symmetric linear cyclic displacement of 200 nm – 800 nm (LDV controlled)
- LCF to VHCF results possible due to variable testing frequency 20Hz – 10kHz

Bond Wire Lift-off Failure

- Crack propagation in the wire material along the grain boundaries between recrystallised fine and coarse grains near the interface
- Fine microstructure (~1 μm) at the bonding interface
- PC and AMFIT same failure modes
Three Major Trends and Consequences for Testing

1. **Operation at higher temperatures**

   For 600V IGBTs a $T_J = 200 \degree C$ and for WBG devices $T_J > 200 \degree C$ is feasible in future. Packages are a bottleneck.

   → Test equipment has to be adapted to higher temperatures

2. **Higher reliability requirements**

   This means longer test times

   → More accelerated tests are required

3. **Multiple stress tests**

   → Physical models and simulations are needed
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PC Results of Infineon’s XT samples

Failure Mechanism after Power Cycling

With baseplate

Without baseplate
Reliability Results of Danfoss Bond Buffer Technology

J. Rudzko, M. Becker, R. Eisele, M. Puech, F. Osterwald

ECPE Workshop "Intelligent Reliability Testing"
2-3 December 2014, Nuremberg, Germany

Combination of Sinter Technology and Cu Wire Bonding Leads to DBB Technology

- Cu – wire on bond buffer sintered die
- Al – wire soldered die
- wire lift off
- solder degradation and wire lift off

technology improvements
Processing Steps for DBB Technology

1700V power module

Common manufacturing steps

Power cycling reliability @ $\Delta T = 100K$

Test parameter:
- $\Delta T = 100K$
- $T_{min} = 20^\circ C$
- $P = \text{const}$
- $t_{min} = 35$
- $t_{max} = 108$

3 millions of cycles
Case Study: Ultra Low Inductance Power Module Packaging

Peter Beckedahl
Sven Bülow
Andreas Kaul
Martin Röblitz
Matthias Spang

Funded by BMBF LES2 Call

HHK – High frequency, High current Components for use in medical equipment and megawatt class PV inverters

Outstanding power cycling capability
Factor of 20 better reliability than standard technology
### Commutation Stray Inductance Simulation

| Inner commutation loop stray inductance only | ~1.3nH |
| Main terminals contribute with additional | ~14.5nH |

### Top IGBT Components
- **w/o Terminals Bondwire First SKiN 3D SKiN**
- **TOP IGBT**:
  - 5.27nH
  - 3.48nH
  - 1.19nH
- **BOT IGBT**:
  - 5.17nH
  - 3.44nH
  - 1.39nH

### Performance Comparison - Water Cooling

<table>
<thead>
<tr>
<th>3 Phase Motor Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF = 0.85</td>
</tr>
<tr>
<td>50 °C Water</td>
</tr>
<tr>
<td>Tj(_{\text{max}}) = 150 °C</td>
</tr>
</tbody>
</table>

**HHK SiC Module**
- **versus 62mm Module**
- **SKM400GB12T4**

### Switching Frequency (kHz)

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>AC Output Cu (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>50</td>
</tr>
<tr>
<td>13</td>
<td>100</td>
</tr>
<tr>
<td>20</td>
<td>150</td>
</tr>
<tr>
<td>27</td>
<td>200</td>
</tr>
<tr>
<td>40</td>
<td>250</td>
</tr>
<tr>
<td>47</td>
<td>300</td>
</tr>
<tr>
<td>53</td>
<td>350</td>
</tr>
<tr>
<td>60</td>
<td>400</td>
</tr>
</tbody>
</table>

### 3x Output Current at 15kHz with HHK SiC

<table>
<thead>
<tr>
<th>HMK Module</th>
<th>62mm Module</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chips</td>
<td>SiC MOSFET</td>
<td>Si-IGBT T4</td>
</tr>
<tr>
<td>Chip area per switch</td>
<td>200mm(^2)</td>
<td>400mm(^2)</td>
</tr>
<tr>
<td>Power</td>
<td>0.045W/K(\text{W}^\text{2})</td>
<td>0.100W/K(\text{W}^\text{2})</td>
</tr>
<tr>
<td>V(<em>{\text{r}})/V(</em>{\text{c}}) at 400A</td>
<td>2.7V</td>
<td>1.8V</td>
</tr>
<tr>
<td>Switch Loss Transistor</td>
<td>15.5mJ</td>
<td>75mJ</td>
</tr>
<tr>
<td>Switch Loss Diode</td>
<td>6mJ</td>
<td>30mJ</td>
</tr>
</tbody>
</table>
A new high current, ultra low inductance full SiC power module has been presented.

- **A commutation stray inductance of about 1nH is possible due to**
  - Use of dual side flex foil for high current DC+ and DC- interface
  - Long strip lines of DC+ and DC- interface with overlapping, matching potentials on module and DC-Link
  - No screw holes within the main current path which would require large creepage distances around the overlapping potentials

- **Excellent electrical performance**
  - Switching speed of up to 70kA/μs do not cause critical over voltages
  - No oscillations between parallel chips
  - Acceptable low package resistance
500 W Pedelec demonstrator

- Embedding technology for power core
  - Power core is building block for power modules
  - Surface embedded components for power modules
  - Reduction of thermal and electrical resistance and inductance

- Copper filled slots
- Double sided thin copper (5 μm)
- Full area back side copper interconnection
- Copper inlay

Novel Bridge and Classical Bridge Build-up

- Classic Bridge Build-up
- Novel embedded Bridge Build-up

Power Core sandwiched between full sized bottom IMS and small top side IMS
The Robustness Validation Process is a “test-to-fail” approach. The methodology is based on three key components:

- Knowledge of the conditions of use (mission profile)
- Knowledge of the failure mechanisms (physics-of-failure)
- Knowledge of accelerated models for the failure mechanisms needed to define and assess accelerated tests

For a given mission profile the robustness margin should be estimated and be a basis for a reliable design and product.

A ZVEI-ECPE has moderated two qualification specifications including the whole supply chain:

- For power modules
- For DC-Link Capacitors (in preparation)

A harmonization with JEITA regarding power module qualification is ongoing.

An other End-of-life tests was mentioned. The Accelerated mechanical fatigue testing

New technologies like thick-wire copper bonding and planar interconnects will disclose new failure mechanisms which require new lifetime models.

A major need are low inductive interconnects to make wide band gap power modules operation useful.
References/1

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Robustness Validation:
- AEC Q101 Rev D1, Sept 6 2013 "FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS" Appendix A7.3.3.3 Robustness Validation on Component Level http://www.aeccouncil.com/AECDocuments.html
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