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Ten Years of Robustness Validation Applied to Power Electronics Components

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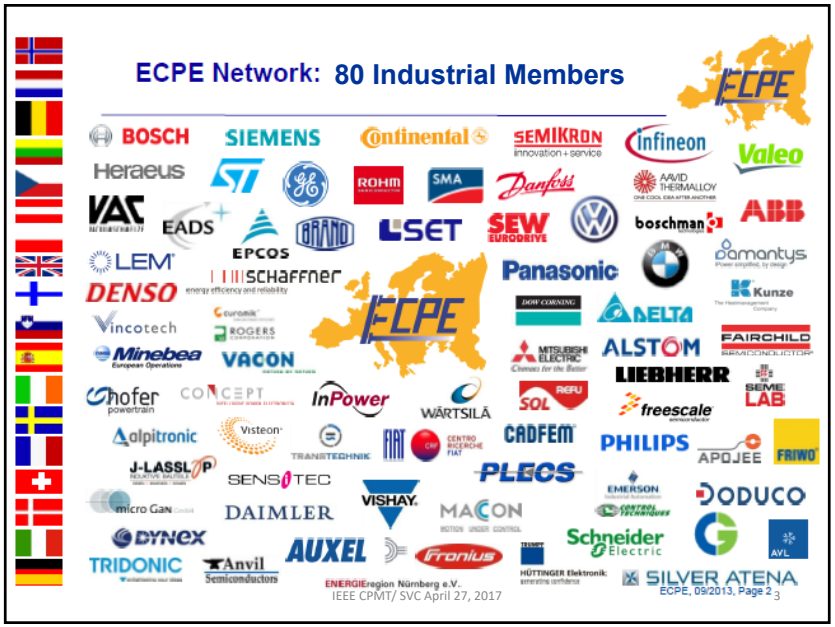

Ten Years of Robustness Validation Applied to Power Electronics Components

1. **Introduction**
2. **Robustness Validation Process**
   - Handbooks, Standards
   - Robustness Margin
   - Mission Profile
3. **Qualification of Power Modules**
4. **Qualification of DC Link Capacitors**
5. **End of Life Tests**
   - Accelerated Mechanical Fatigue Testing
   - Cosmic Ray Testing
6. **Advanced Technologies**
   - Thick wire copper bonding
   - Planar Interconnects
   - Embedded Power Electronics
7. **Conclusions**
8. **References**

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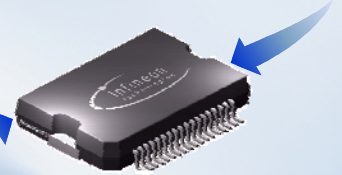
The Basic Question

Have I passed my qualification tests according to the standard?

Fit for use



Fit for standard

Is our product "sufficiently reliable" in the application?

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Robustness Validation Process

The new **'test to fail'** qualification approach (instead of a 'test-to-pass'), is a paradigm shift from **'Fit for Standard'** to **'Fit for Application'**.

Robustness Validation generates knowledge on the **relevant component failure mechanisms** that may occur at the boundaries of the specification limits.

Therefore Components could be designed with known **robustness margins** combined with cost and time saving potentials.

60 companies formed a task force to settle a new comprehensive Qualification method :

- ZVEI
- SAE
- AEC
- JSAE

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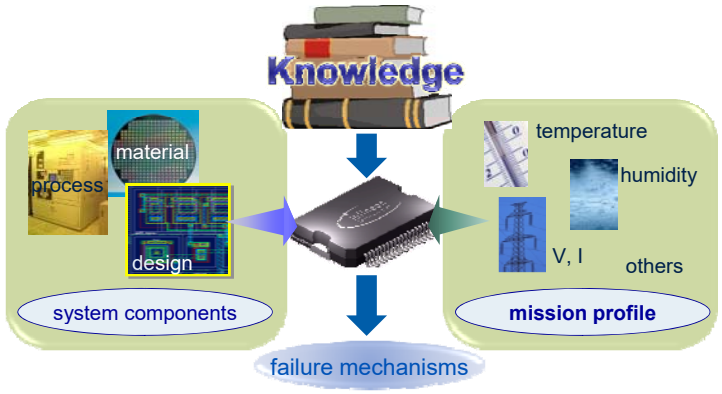
RV – A Knowledge-Based Approach



RV is a knowledge-based approach:

- Knowledge of the conditions of use (mission profile)
- Knowledge of the failure mechanisms and failure modes
- Knowledge of acceleration models for the failure mechanisms

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Definition Robustness Validation

Robustness Validation is a process to demonstrate that a product

- performs its intended function(s) with sufficient **robustness margin**
- under a defined **mission profile** for its specified lifetime.

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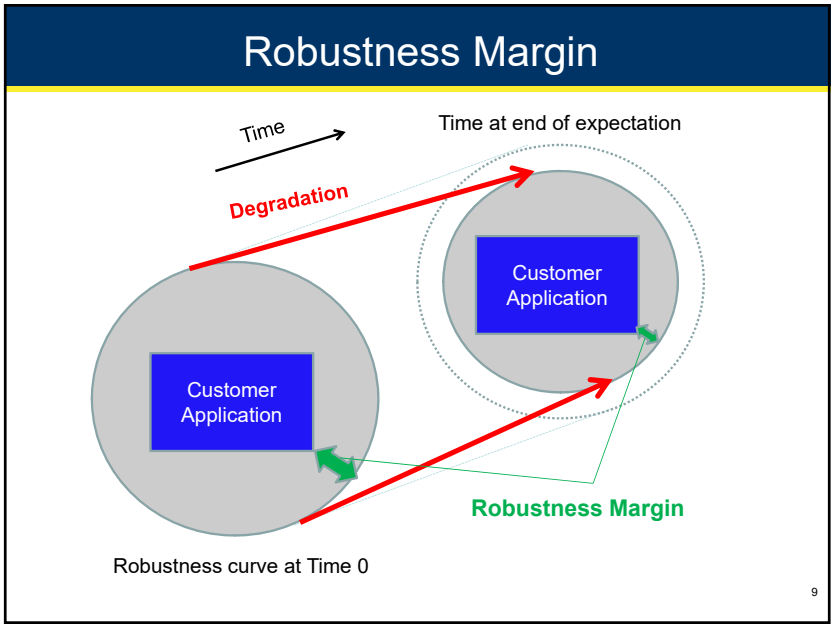
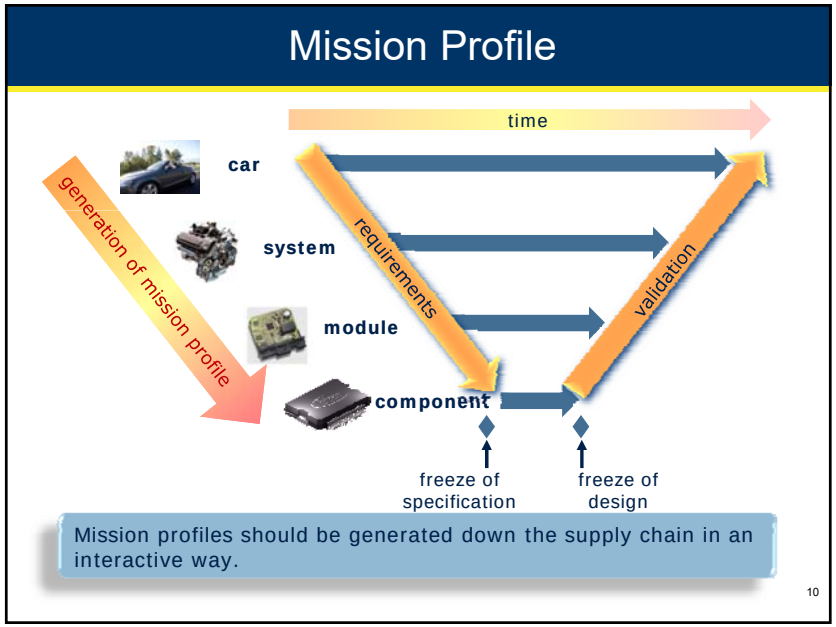

Robustness Margin
Time
Time at end of expectation
Degradation
Customer Application
Customer Application
Robustness Margin
Robustness curve at Time 0
9


Mission Profile
time
car
system
module
component
generation of mission profile
requirements
validation
freeze of specification
freeze of design
Mission profiles should be generated down the supply chain in an interactive way.
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Mission Profile

A Mission Profile is a simplified representation of **relevant conditions** to which the Device/ Component production population will be **exposed** in all of their **intended application** throughout the **full life cycle of the component**.

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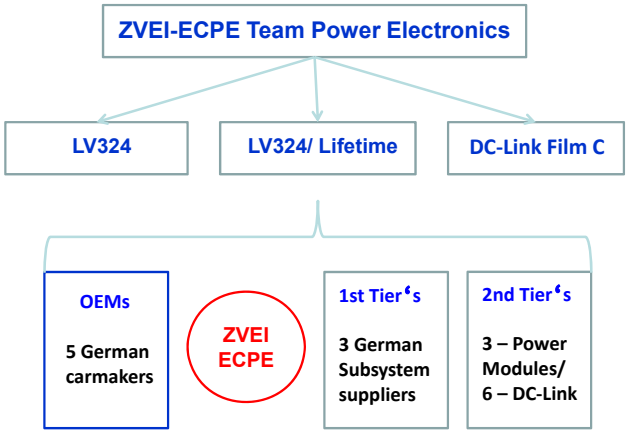
Qualification of Components for E-Mobility



→ **Harmonisation with JEITA is in progress**

IEEE CPMT/ SVC April 27, 2017

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Power Module Qualification

LV324 Qualification of Power Electronics Modules for Use in Motor Vehicle Components

General Requirements, Test Conditions and Tests

Scope

This document defines requirements, test conditions and tests for validating properties, including the service life, of power electronics modules for use in components of motor vehicles up to 3,5 t.

The **described tests concern the qualification of components at module level** but not the qualification of semiconductor chips or production processes.

Overview

The tests described in the following serve to validate the properties and service life of power electronics modules for use in the automotive industry.

The defined tests are based on the currently known failure mechanisms and the motor vehicle-specific application profiles of power modules.

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Power Module Tests

QM module test
(Determination of the electrical and mechanical parameters after the individual qualification tests)

- Gate parameters
- Rated and reverse currents
- Forward voltages
- X-ray, scanning acoustic microscopy (SAM)
- IPI VI/OMA

Characterizing module tests

- QC-01 Determination of parasitic stray inductance (Lp)
- QC-02 Determination of thermal resistance (Rth value)
- QC-03 Determination of short-circuit resistance
- QC-04 Insulation test
- QC-05 Determination of mechanical data

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Power Module Tests

Environmental tests

- QE-01 Thermal shock (TST)
- QE-02 Contactability (CO)
- QE-03 Vibration (V)
- QE-04 Mechanical shock (MS)

Life tests

- QL-01 Power cycle (PCsec)
- QL-02 Power cycle (PCmin)
- QL-03 High temperature storage (HTS)
- QL-04 Low temperature storage (LTS)
- QL-05 High temperature reverse bias (HTRB)
- QL-06 High temperature gate bias (HTGB)
- QL-07 High humidity high temperature reverse bias (H3TRB)

- **Final test to record the electrical parameters of all DUTs**
- **Conversion of the test results into reliability data**

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Power Module Testmatrix

LV 324 06.02.2014

	Minimum Number of Readouts @	End Of Line Test [c] (according to 6.1.2-6.1.8)	SAM System / Chip solder	Correlation [a] $U_{GE,th}/U_{GE,th}$	Correlation [a] $t_{D(on)}$ / $t_{D(on)}$	Correlation [a] $t_{D(off)}$ / $t_{D(off)}$	Correlation [a] U_{CE} / U_{DS}	Correlation [a] V_F	Correlation [a,b] R_{th}	Short Circuit Test	Dynamic Test (Double Pulse)	Isolation Test [b]	Mechanical Data	Optional IPI VI / OMA
QC-01 .. QC-05	1: Start of test 2: End of test	1	1	1,2	1,2	1,2	1,2	1,2	1,2			1,2		1,2
QE-01 TST	1: 0c 2: 500c 3: 1000c	1-3	3	1-3	1-3	1-3	1-3	1-3	1,3	1-3	1-3	1-3		1,3
QE-02 CO	1: Start of test 2: End of test													1,2
QE-03 V	1: Start of test 2: End of test	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2		1,2
QE-04 MS	1: Start of test 2: End of test	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2		1,2
QL-01 PC_{sec}	1: 0c 2: End of life	1,2 (opt)	2	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2		1,2
QL-02 PC_{min}	1: 0c 2: End of life	1,2 (opt)	2	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2		1,2
QL-03 HTS	1: 0h 2: 1000h	1-2		1-2	1-2	1-2	1-2	1-2		1-2	1-2	1-2		1,2
QL-04 LTS	1: 0h 2: 1000h	1-2		1-2	1-2	1-2	1-2	1-2		1-2	1-2	1-2		1,2
QL-05 HTRB	1: 0h 2: 1000h	1-2		1-2	1-2	1-2	1-2	1-2		1-2	1-2	1-2		1,2
QL-06 HTGB	1: 0h 2: 1000h	1-2		1-2	1-2	1-2	1-2	1-2		1-2	1-2	1-2		1,2
QL-07 H^3TRB	1: 0h 2: 1000h	1-2		1-2	1-2	1-2	1-2	1-2		1-2	1-2	1-2		1,2
Testersamples	1: 0h												1	

Correlation - Für die Korrelationen werden die 25°C Messwerte der charakteristischen Daten zum angegebenen Messzeitpunkt mit den Warten der Eingangsmessung verglichen. Dabei sind die für die Korrelation verwendeten Werte entsprechend zu dokumentieren und maximale prozentuale Angaben von den erwarteten Abweichungen anzugeben.
ISO Test - Beim Iso Test wird die Isolationsfähigkeit des Module gemäß Serienendtest-Spezifikation geprüft.
Ein definiertes Hoch- bzw. Herunterfahren vor/nach Belastungen ist entsprechend der Vorgabe im Kapitel Modultest sicher zu stellen.

Tabelle 8: Prüfungsabhängige Modultests

Part of Power Module Test Matrix

Thermal Shock

Contactability

Vibration

	Minimum Number of Readouts @	End Of Line Test [c] (according to 6.1.2-6.1.8)	SAM System / Chip solder	Correlation [a] $U_{GE,th}/U_{GS,th}$
QC-01 .. QC-05	1: Start of test 2: End of test	1	1	1,2
QE-01 TST	1: 0c 2: 500c 3: 1000c	1-3	3	1-3
QE-02 CO	1: Start of test 2: End of test			
QE-03 V	1: Start of test 2: End of test	1,2		1,2

$U_{GE,th}$ Gate-Emitter-Threshold Voltage
$U_{GS,th}$ Gate-Source-Threshold Voltage

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Power Module Tests

4.1.4 Chip-near interconnect technology

Chip upper side connection design and design of chip lower side connection with the substrate.

Examples:

Chip upper side: bond wire, ribbon bond, copper clip, sintering technology Chip lower side: chip soldering, sintering technology, diffusion soldering

4.1.5 Chip-remote interconnect technology

Connection design which does not directly include the chip. A distinction shall be made between interconnect technology for electrical and thermal interfaces. Due to the design, chip-remote interconnect technology may be both electrical and thermal.

Examples:

Electrical interfaces: design of load and auxiliary contact connection

Thermal interface: system soldering between substrate and base plate (modules with base plate) or interface between module and cooling system (modules without base plate)

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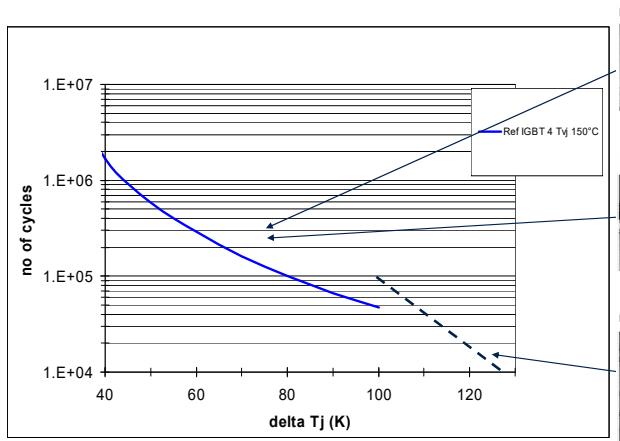
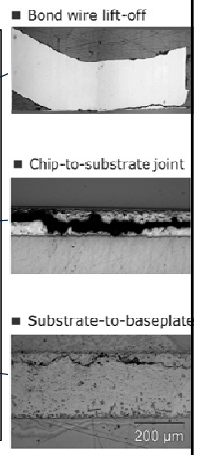
Power cycling reliability of IGBT4





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PCsec Test Conditions

Table 11: Limit values for test parameters PC_{sec}

Parameter		Value
Load current on-time	t_{ON}	< 5 s
Load current level	I_L	> 0.85·I_{CN} [a, b]
Gate-voltage	U_G	Typically 15 V [c]

[a] The load current level of > 0.85·I_{CN} shall only be selected for one sample point.
[b] A value < 0.85·I_{CN} can be selected for the second and further sample points to enable a suitable temperature increase difference to be set
[c] The gate-voltage for the IGBT and MOSFET test can (e.g. if contact current densities become too high) be less than 15 V if the desired temperature increase cannot be implemented with on-times of t_{ON} < 5 s due to the module's thermal properties. However, it shall always be guaranteed that the switch is permanently operated in the saturated range. In such cases, the gate-voltage which is used shall be accordingly adapted once at the start of the test and shall be documented in each case

Forward voltage	IGBT: UCE,sat MOSFET: UDS Diode: UF	+ 5 % a
Increase in virtual junction temperature swing	ΔTvj	+ 20%

Failure Criteria

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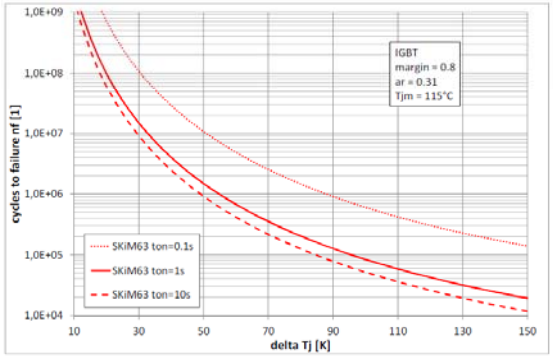
Life Time Model/ Reliability Curve



Semikron

Lifetime Models for a certain IGBT module technology showing the impact of power cycle **ton** times at a given **aspect ratio** of the bond loop

IEEE CPMT/ SVC April 27, 2017

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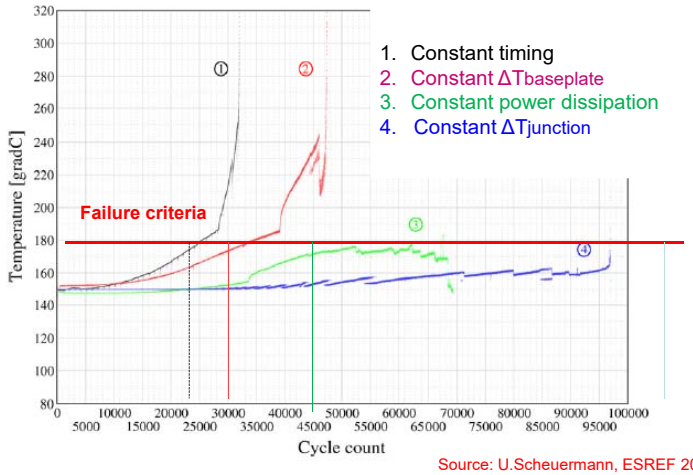
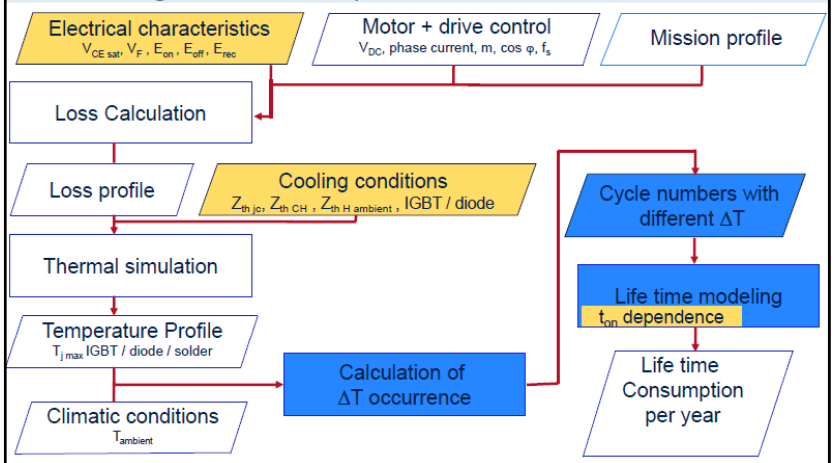
PCT with Different Control Strategies



1. Constant timing
2. Constant ΔTbaseplate
3. Constant power dissipation
4. Constant ΔTjunction

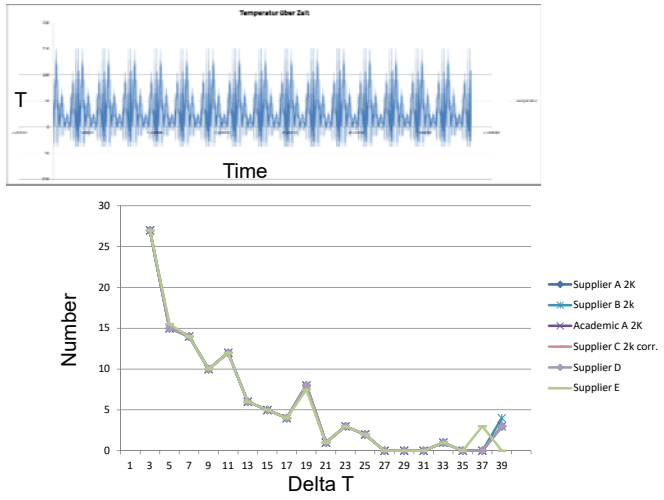
Source: U.Scheuermann, ESREF 2010

Calculation of life time from the given mission profile



M. Thoben/ Infineon

Consolidated Results after Rainflow Counting



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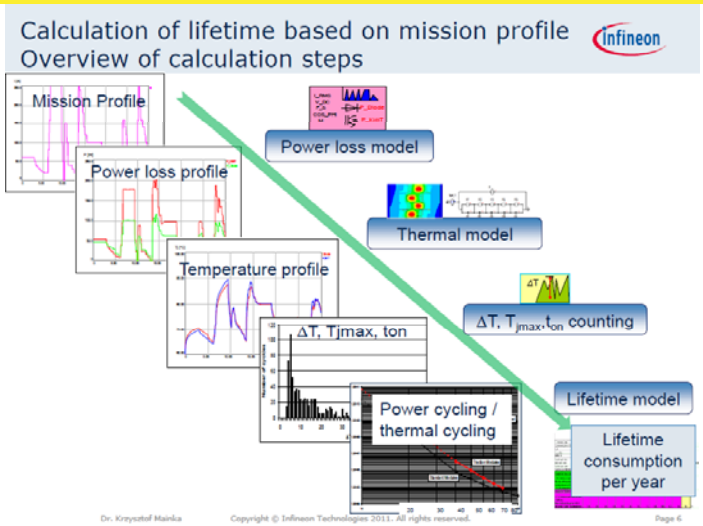
Estimation of Lifetime



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Estimating the Robustness Margin

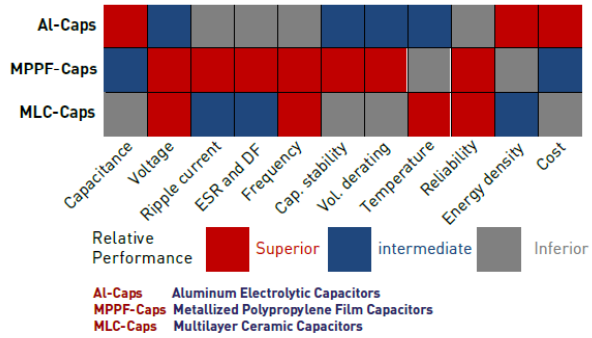
1. The process is good for any drive cycle
2. The weakest parts in a power module are normally the bond wires, substrate solder and chip solder. This is due to the differences in the Coefficient of Thermal Expansion CTE
3. A translation has to be made from the vehicles mission profile down to the device/interconnect level

Finally the robustness margin can be estimated using a lifetime model/ reliability curve from the module manufacturer

Ten Years of Robustness Validation Applied to Power Electronics Components

Typical Types of Capacitors for DC-link Applications

Performance comparisons of the 3 types of capacitors



Al-Caps Aluminum Electrolytic Capacitors
MPPF-Caps Metallized Polypropylene Film Capacitors
MLC-Caps Multilayer Ceramic Capacitors

Typical Types of Capacitors for DC-link Applications

Dominant failure modes and critical stressors

	Al-Caps	MPPF-Caps	MLCC-Caps
Dominant failure modes	wear out		
	open circuit	open circuit	short circuit
Most critical stressors	T_a, V_C, i_C	T_a, V_C, humidity	T_a, V_C, vibration/shock
Self-healing capability	moderate	good	no

Al-Caps Aluminium Electrolytic Capacitors
MPPF-Caps Metallized Polypropylene Film Capacitors
MLC-Caps Multilayer Ceramic Capacitors

Ageing of Film Capacitors

Electrical Ageing

- Field Strength
- Insulation Current
- Corona Discharging

Fatigue of Materials and Connection

- Vibrations, Shock
- Thermo- Mechanical Movements

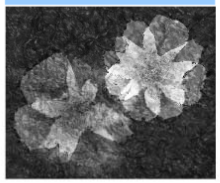
Corrosion, Oxidation

- Humidity
- High Temperatures
- Traces of Acids‘, Chloride etc.
- Contact Corrosion

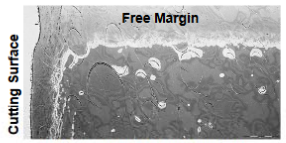
Overview on Reliability on Film Capacitors

TDK EPCOS

Self Healing

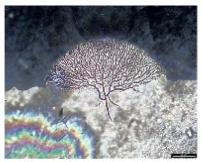


Clearings 200µm



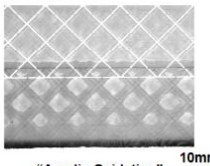
Degradation of the metallization due to corona discharging 100µm

Load: 40min 500V_{eff}

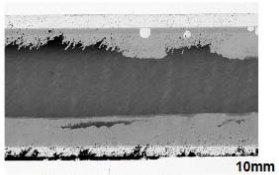


"Corona Treeing" 20µm

Corrosion, Oxidation



"Anodic Oxidation" 10mm



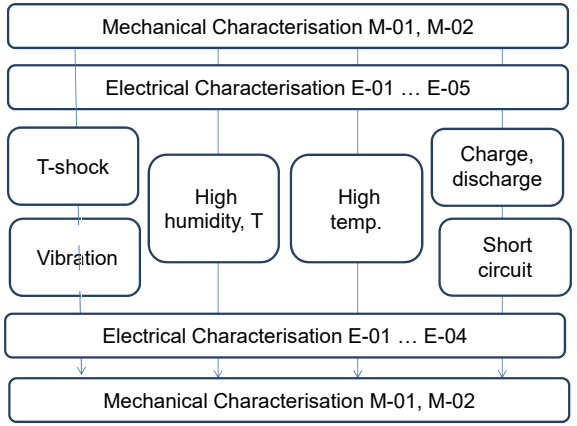
"Corroded Electrods" 10mm

Example 2) *Sensitive against Corrosion and Oxidation*

Dr. W. Grimm, 3-12-2014

DC-link film C: Testplan

6 capacitors are tested for each of the 4 groups



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Reliability Analysis of Wire Bonds in Semiconductor Packages

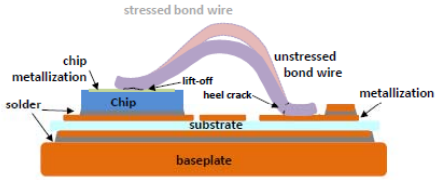
B. Czerny [a], A. Mazloum-Nejadari [b], G. Khatibi [a]

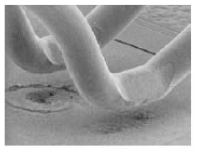
[a] Christian Doppler Laboratory for Lifetime and Reliability of Interfaces in Complex Multi-Material Electronics, CTA, TU Wien, Vienna, Austria
[b] Infineon AG, Neubiberg, Germany

ECPE Workshop „Thermal and Reliability Modelling and Simulation of Power Electronics Components and Systems"

Fuerth/Nuremberg, Germany
30. Nov. – 01. Dec. 2016

Bond Wire Lift-off Failure in Power Modules



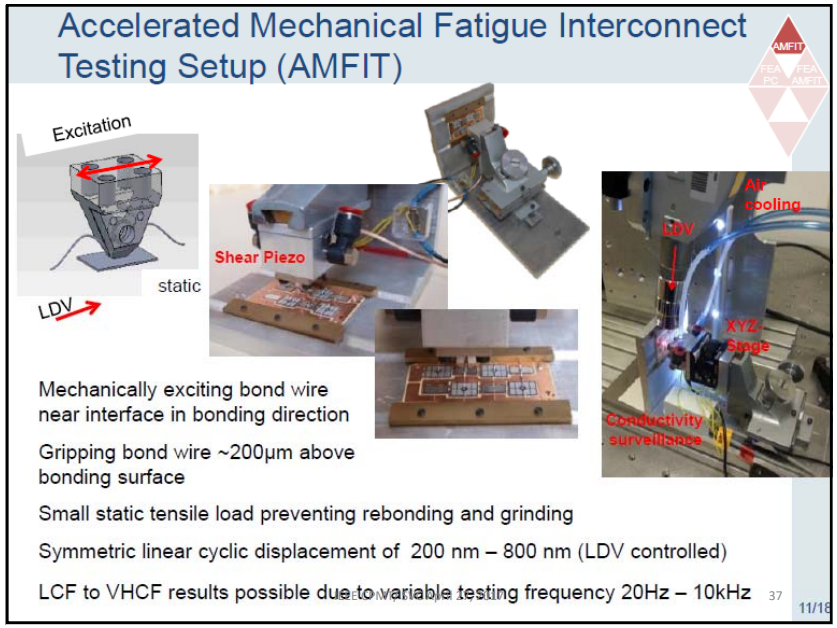


Investigating the thermo-mechanical fatigue of 400µm Al bond wire interconnects with respect to bond wire lift-off failure

Time consuming PC as a standard testing method for bond wire lift-off failure

Developing a mechanical testing method for fast fatigue qualification for wire bond lift-off failure

- Can accelerated mechanical testing provide similar fatigue failure?
- Is there a influence due to the accelerated testing frequency?
- Can the results be compare to standard testing methods?


Accelerated Mechanical Fatigue Interconnect Testing Setup (AMFIT)
Excitation
static
LDV
Shear Piezo
Air cooling
LDV
XYZ-Stage
Conductivity surveillance
Mechanically exciting bond wire near interface in bonding direction
Gripping bond wire ~200µm above bonding surface
Small static tensile load preventing rebonding and grinding
Symmetric linear cyclic displacement of 200 nm – 800 nm (LDV controlled)
LCF to VHCF results possible due to variable testing frequency 20Hz – 10kHz
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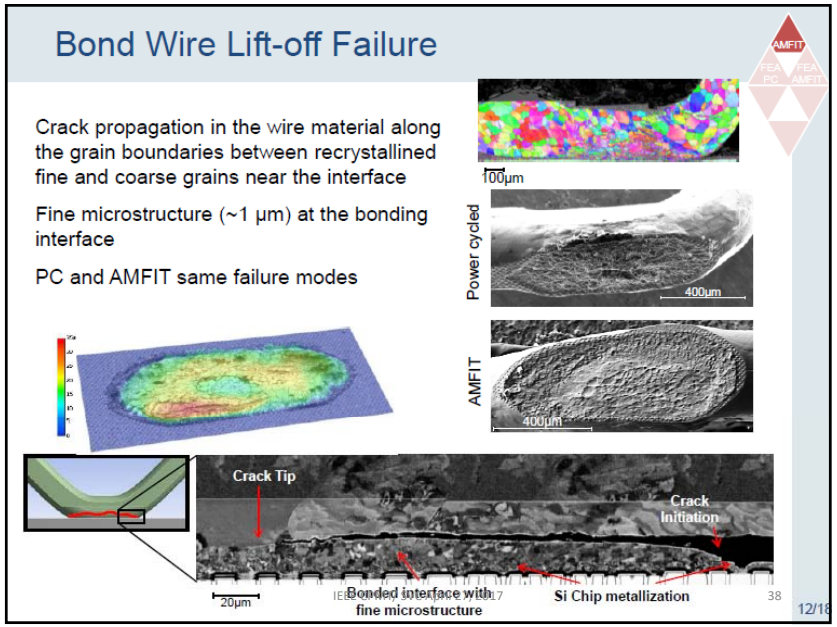
11/18


Bond Wire Lift-off Failure
Crack propagation in the wire material along the grain boundaries between recrystallined fine and coarse grains near the interface
Fine microstructure (~1 µm) at the bonding interface
PC and AMFIT same failure modes
100µm
Power cycled
400µm
AMFIT
400µm
Crack Tip
Crack Initiation
20µm
Bonded interface with fine microstructure
Si Chip metallization
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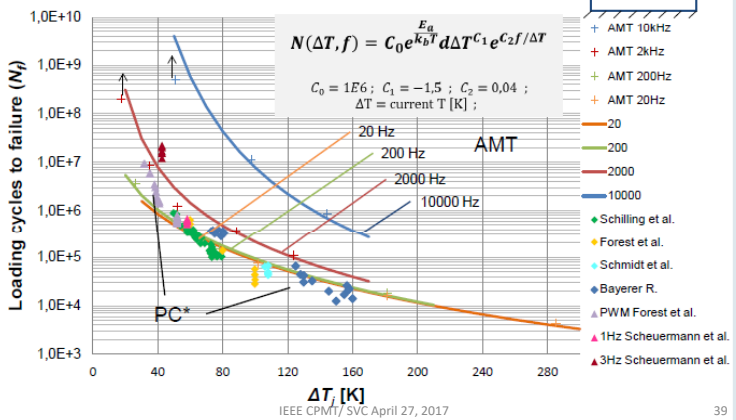
12/18

AMFIT Results as a function of ΔT_j

AMFIT fatigue results compared to PC test results

Frequency variation between 20Hz and 10kHz



Three Major Trends and Consequences for Testing

1. **Operation at higher temperatures**

For 600V IGBTs a Tj = 200 ° C and for WBG devices Tj > 200 ° C is feaseable in future. Packages are a bottleneck.

→ **Test equipment has to be adapted to higher temperatures**

2. **Higher reliability requirements**

This means longer test times

→ **More accelerated tests are required**

3. **Multiple stress tests**

→ **Physical models and simulations are needed**

Ten Years of Robustness Validation Applied to Power Electronics Components

1. **Introduction**
2. **Robustness Validation Process**
   - Handbooks, Standards
   - Robustness Margin
   - Mission Profile
3. **Qualification of Power Modules**
4. **Qualification of DC Link Capacitors**
5. **End of Life Tests**
   - Accelerated Mechanical Fatigue Testing
   - Cosmic Ray Testing
6. **Advanced Technologies**
   - Thick wire copper bonding
   - Ultra low inductance
   - Embedded Power Electronics
7. **Conclusions**
8. **References**

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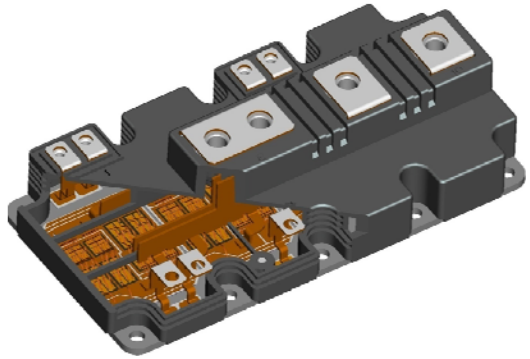
Thick Copper Wirebond Module



For copper bonding a copper chip metallization is needed

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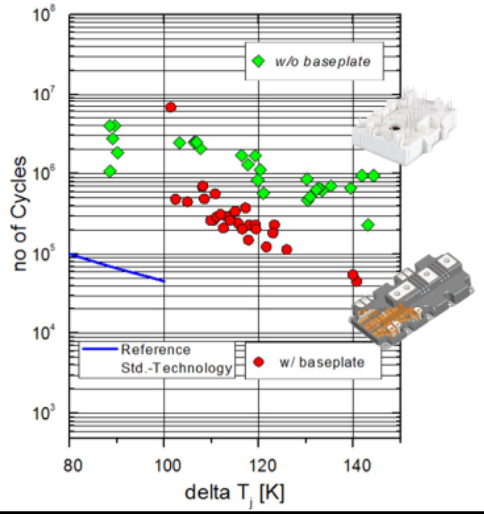
PC Results of Infineon's XT samples



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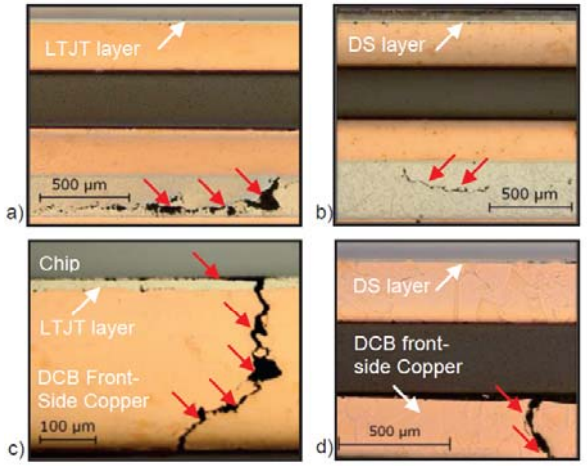
Failure Mechanism after Power Cycling



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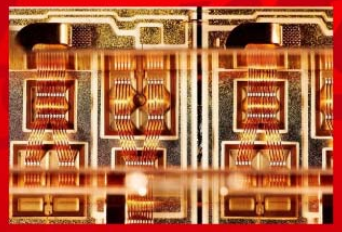
Reliability Results of Danfoss Bond Buffer Technology

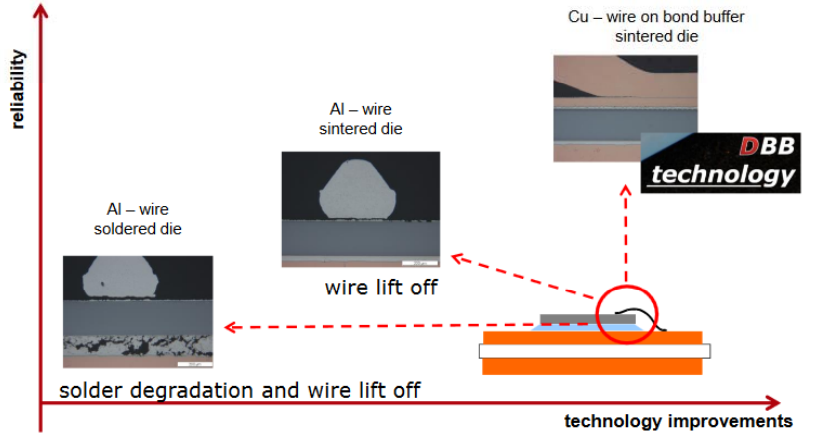
J. Rudzki, M. Becker, R. Eisele, M. Poech, F. Osterwald



Fraunhofer ISIT

ECPE Workshop "Intelligent Reliability Testing"
2-3 December 2014, Nuremberg, Germany 45

Combination of Sinter Technology and Cu Wire Bonding Leads to DBB Technology



6 | DSP Jacek Rudzki

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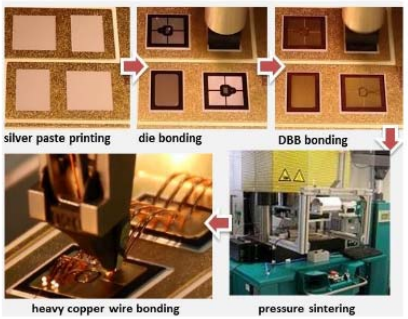
Processing Steps for DBB Technology



1700V power module

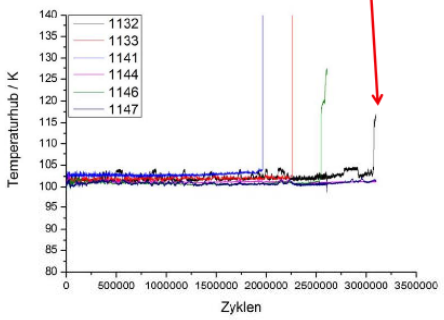
Common manufacturing steps

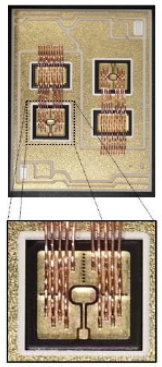
8 | DSP Jacek Rudzki ENGINEERING TOMORROW

Power cycling reliability @ ΔT=100K

Test parameter:
ΔT = 100K
T_{min} = 20°C
P = const
t_{on} = 1s
t_{off}= 10s

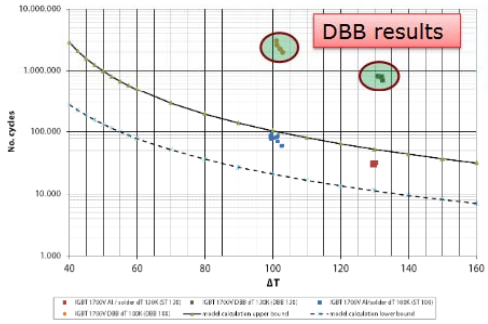
3 milions of cycles





13 | DSP Jacek Rudzki IEEE CPMT/ SVC April 27, 2017 ENGINEERING TOMORROW

Coffin Manson Diagramm - DBB Results



Type	DBB 130	DBB 100	ST 130	ST 100
ton [s]	1	1	1	1
toff [s]	10	10	10	10
Ipulse [A/cm²]	100	100	100	100
Tj,min [°C]	20	20	20	20
Tj,max [°C]	150	120	150	120
DT [K]	130	100	130	100
Tm [°C]	85	70	85	70

Outstandig power cycling capability
Factor of 20 better reliability than standard technology

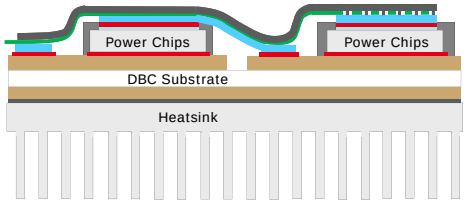
Case Study:

Ultra Low Inductance Power Module Packaging

Peter Beckedahl
Sven Bütow
Andreas Maul
Martin Röblitz
Matthias Spang

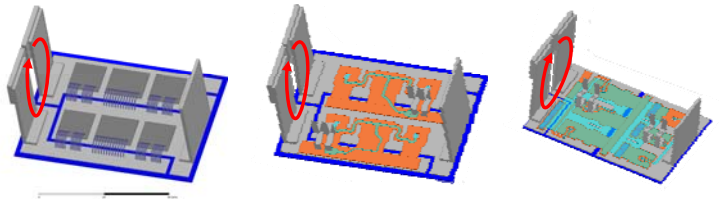
Funded by BMBF LES2 Call

„**HHK** – **H**igh frequency, **H**igh current **C**omponents for use in medical equipment and megawatt class PV inverters“



w/o Terminals	Bondwire	First SKiN	3D SKiN
TOP IGBT	5,27nH	3,48nH	1,19nH
BOT IGBT	5,17nH	3,44nH	1,39nH
Mean Value	5,22nH	3,46nH	1,29nH
Percent	100%	66%	25%

Inner commutation loop stray inductance only ~1,3nH
Main terminals contribute with additional ~14,5nH



Bondwire Design | First SKiN Design | 3D SKiN Design

FORMS.1014 / Rev. 06

3 Phase Motor Drive
PF = 0,85
50 °C Water
Tjmax = 150 °C

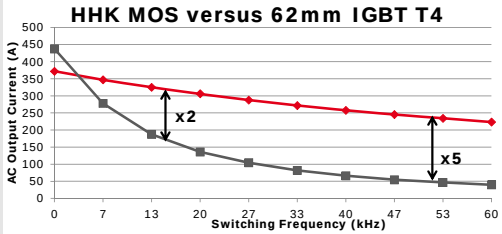
HHK SiC Module

versus

62mm Module SKM400GB12T4

2x output current at 15kHz with HHK SiC

5x output current at 50kHz with HHK SiC



	HHK Module	62mm Module	Comparison
Chips	SiC MOSFET	Si IGBT T4 CAL Diode	
Chip area per switch	200mm^2	400mm^2 200mm^2	33%
R_{THJ-S}	0,045K/W	0,100K/W 0,175K/W	25%
V_{DS} / V_{CE} at 400A	2,2V	1,8V	120%
Switch Loss Transistor	15,5mJ	75mJ	20%
Switch Loss Diode	6mJ	30mJ	20%

FORMS.1014 / Rev. 06

- **A new high current, ultra low inductance full SiC power module has been presented**

- **A commutation stray inductance of about 1nH is possible due to**
  - Use of dual side flex foil for high current DC+ and DC- interface
  - Long strip lines of DC+ and DC- interface with overlapping, matching potentials on module and DC-Link
  - No screw holes within the main current path which would require large creepage distances around the overlapping potentials

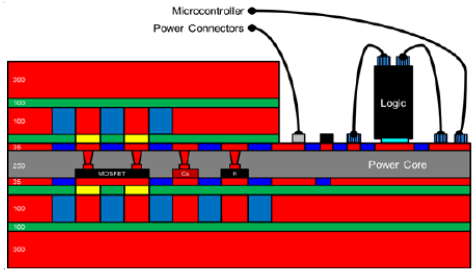
- **Excellent electrical performance**
  - Switching speed of up to 70kA/µs do not cause critical over voltages
  - No oscillations between parallel chips
  - Acceptable low package resistance

FORMS.1014 / Rev. 06

500 W Pedelec demonstrator

empower

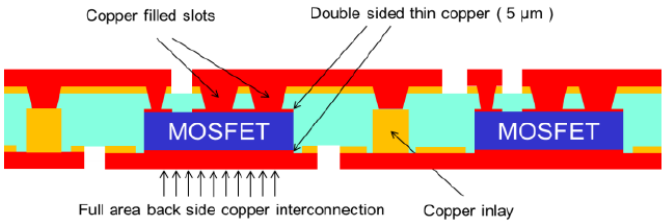
- Concept of power module
  - IMS + power core + silver sinter interconnections
  - IMS construction : 300 µm Cu / Thermal dielectric / 100 µm Cu
  - Full area bottom IMS
  - Smaller Top IMS : Access to high current connectors using exposed area



500 W Pedelec demonstrator

empower

- Embedding technology for power core
  - Power core is building block for power modules
  - Surface embedded components for power modules
  - Reduction of thermal and electrical resistance and inductance



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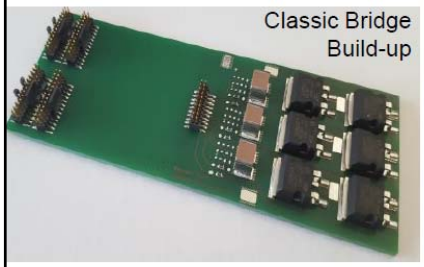
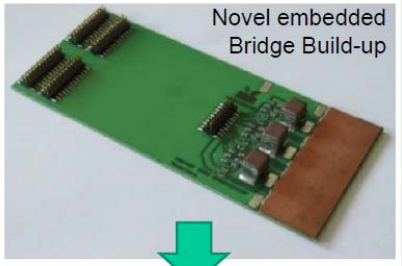
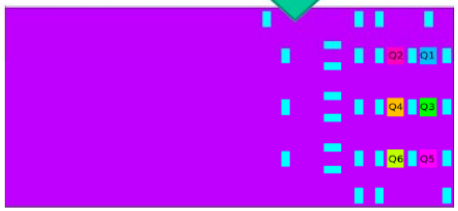
Novel Bridge and Classical Bridge Build-up

empower





Power Core sandwiched between full sized bottom IMS and small top side IMS



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Summary/ 1

- The Robustness Validation Process is a **"test-to-fail"** approach
- The methodology is based on three key components:
  i. Knowledge of the conditions of use (**mission profile**)
  ii. Knowledge of the failure mechanisms (**physics-of- failure**)
  iii. Knowledge of accelerated **models** for the failure mechanisms needed to define and assess **accelerated tests**
- For a given mission profile the **robustness margin** should be estimated and be a basis for a reliable design and product
- A ZVEI-ECPE has moderated **two qualification specifications** including the whole supply chain:
  i. For power modules
  ii. For DC-Link Capacitors (in preparation)
- A **harmonization with JEITA** regarding power module qualification is ongoing

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Summary/ 2

- **An other End-of-life tests was mentioned → The Accelerated mechanical fatigue testing**
- **New technologies like thick-wire copper bonding and planar interconnects will disclose new failure mechanisms which require new lifetime models**
- **A major need are low inductive inerconnects to make wide band gap power modules operation useful**

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