IEEE/EPS Chapter Lecture in the Silicon Valley Area

Fan-Out Wafer-Level Packaging for 3D IC Heterogeneous Integration

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PURPOSES/CONTENTS

To present the recent advances and trends in the following semiconductor packaging technologies:

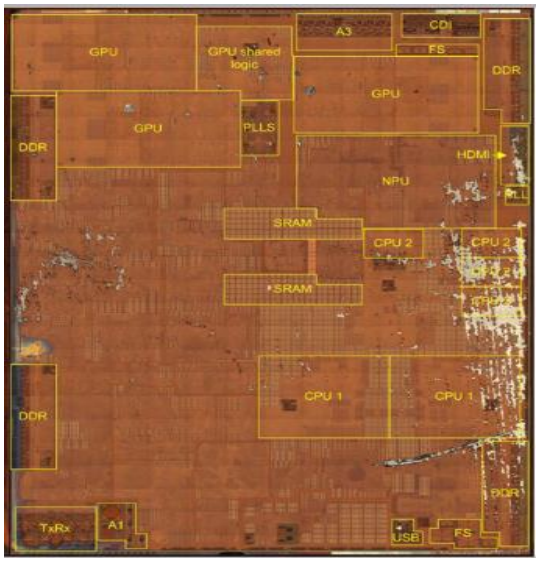
- **System-on-Chip (SoC)**
- **System-in-Package (SiP)**
- **Heterogeneous Integration**
- **Heterogeneous Integration on Organic Substrates**
- **Heterogeneous Integration on Silicon Substrates**
- **Heterogeneous Integration on RDLs**
- **FOWLP for 3D IC Heterogeneous Integration**
- **Trends in Heterogeneous Integration**

System-on-Chip (SoC)

- SoC integrates ICs with different functions into a single chip for the system or subsystem.
- Due to the drive of Moore's law, SoC has been very popular in the pass 10+ years.

A10

A11



Apple's application processor (A10) consists of:

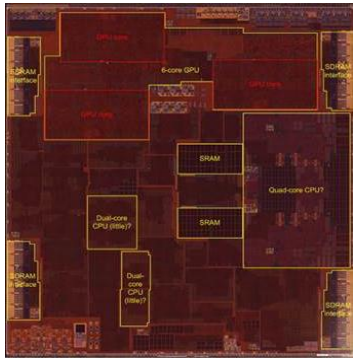
- A 6-core GPU (graphics processor unit)
- Two dual-core CPU (central processing unit)
- 2 blocks of SRAMs (static random access memory), etc.
- 16nm process technology
- Chip area ~ 125mm^2
- 3.3B transistors

A11 consists of:

- More functions, e.g., Neural Engine for Face ID
- Apple designed tri-core GPU
- 10nm process technology
- Chip area ~ 89.23 mm^2, a ~30% die shrink compared to the A10
- 4.3B transistors

Pop for the Mobile DRAMs and Application Processor of iPhone 7/7+

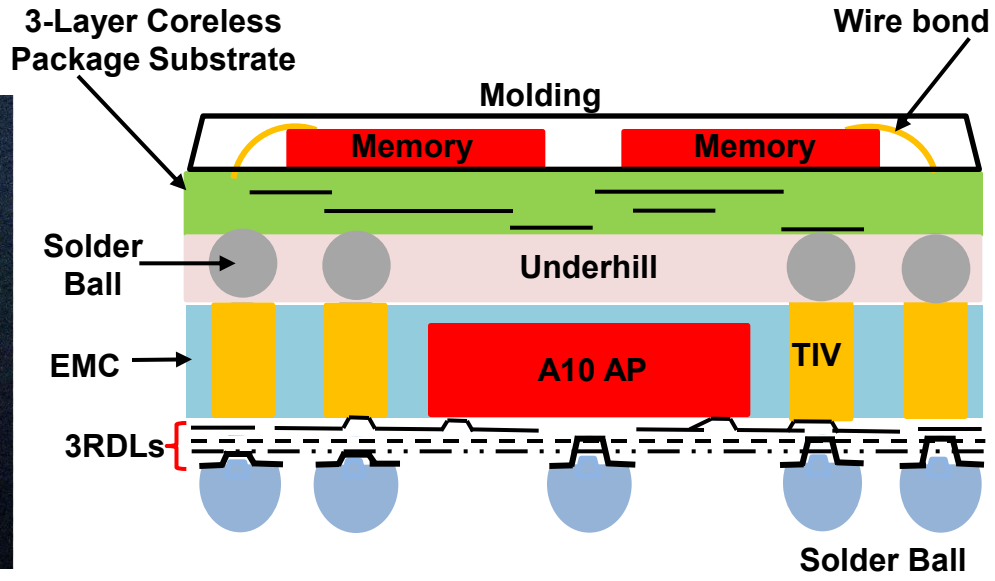
SoC

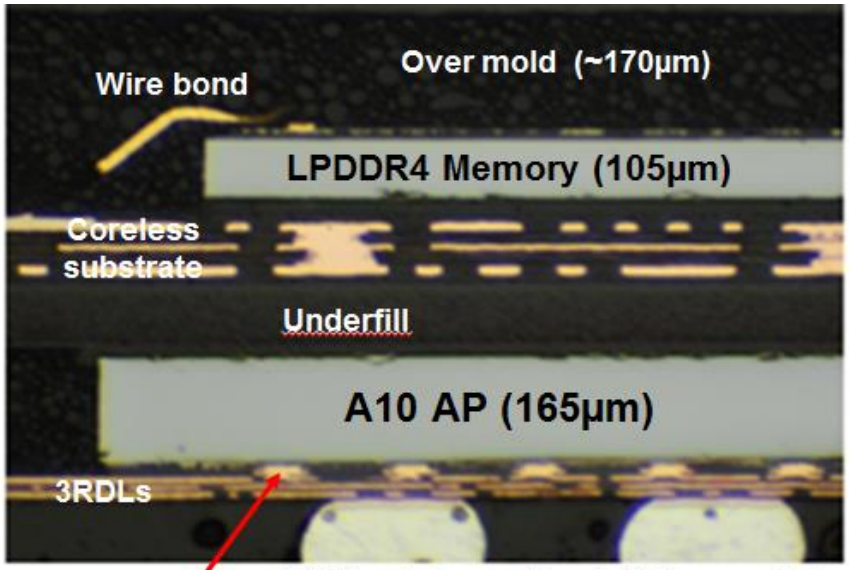


11.6mm x 10.8mm
x 165µm

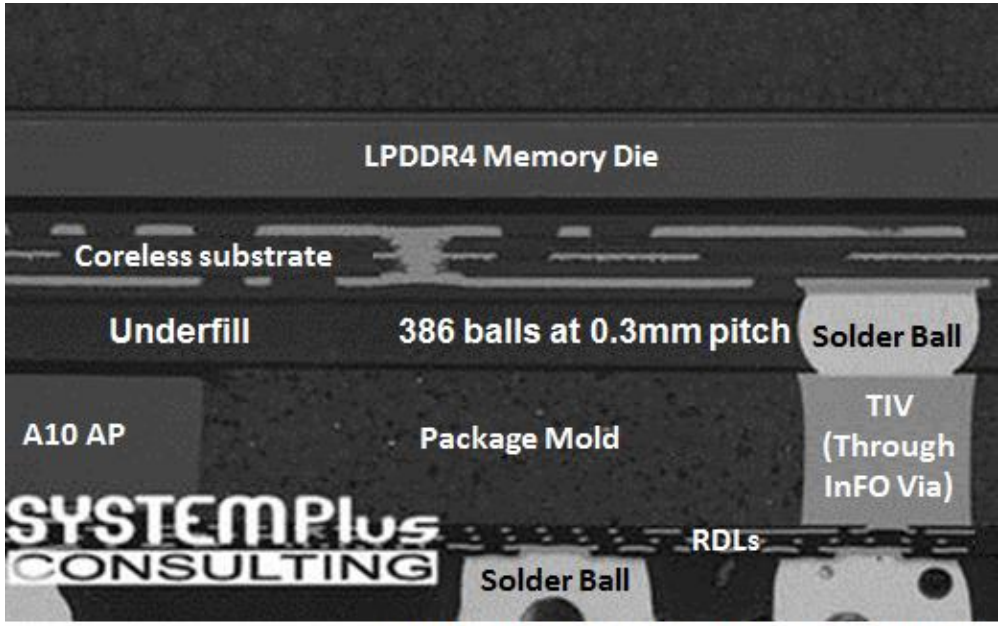
Pop

15.5mm x 14.4mm x 825µm





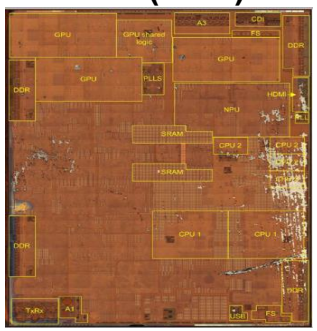
Binghamton University/Prismark



~1300 solder balls at 0.4mm pitch

Pop for the Mobile DRAMs and Application Processor of iPhone X/8/8+

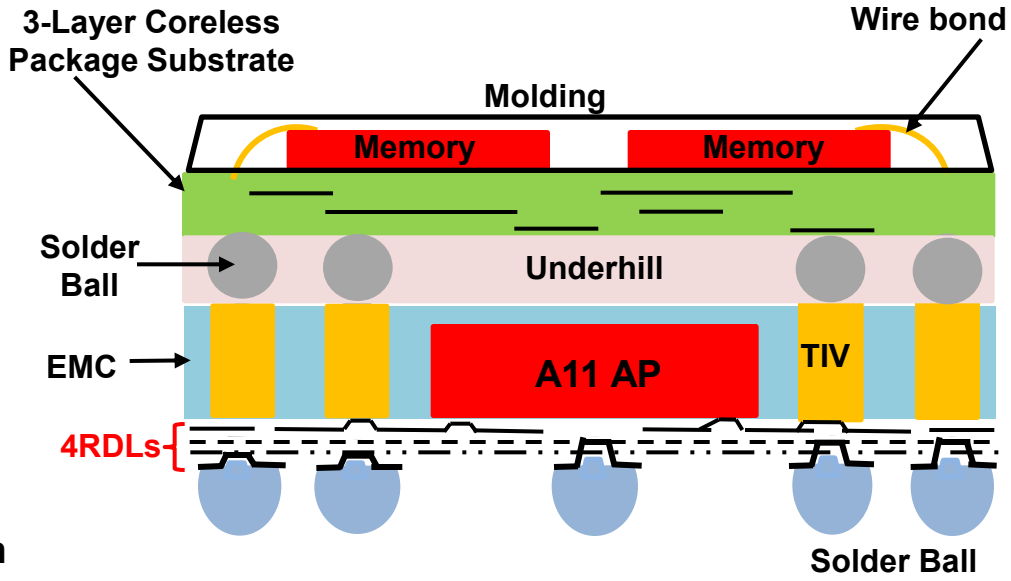
A11 (SoC)

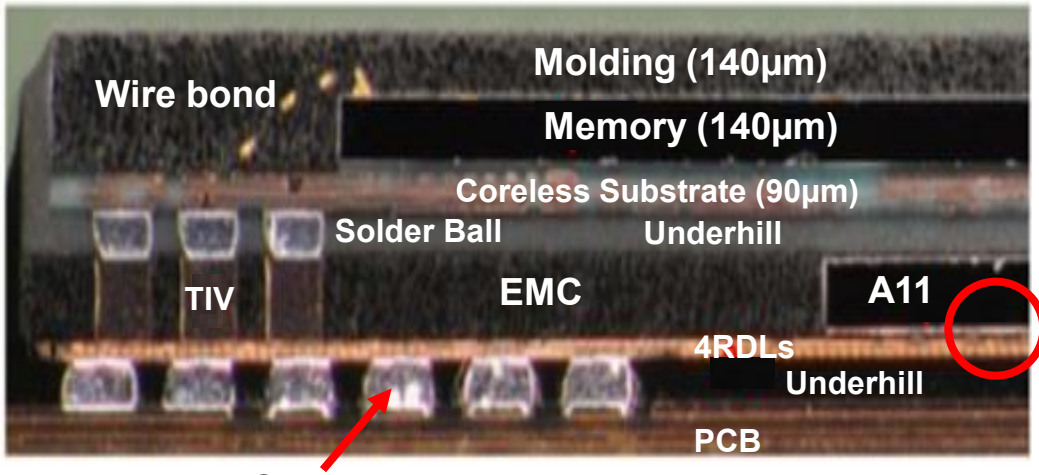


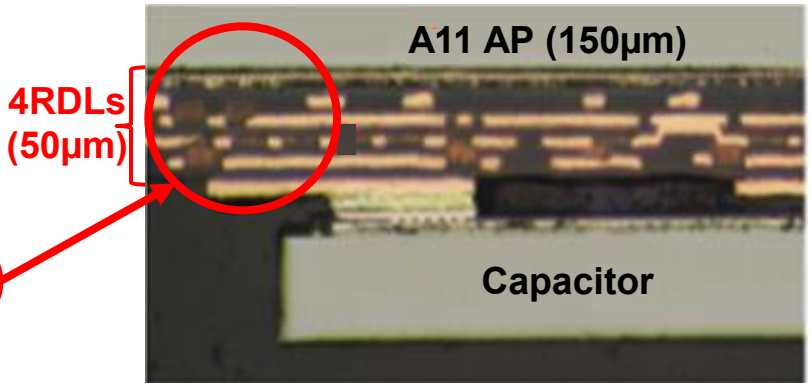
10mmx8.7mmx165μm

Pop

13.9mmx14.8mmx790mm







Modified from Prismark/Binghamton University

Heterogeneous Integration

What is Heterogeneous Integration?

Heterogeneous integration contrasts with SoC. Heterogeneous integration uses packaging technology to integrate dissimilar chips with different functions into a system or subsystem, rather than integrating all the functions into a single chip and go for finer feature size.

Why Heterogeneous Integration?

This is because of the end of the Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. Heterogeneous integration is going to take some of the market shares away from SoC.

What are Heterogeneous Integration for?

For the next five years, we will see more of a higher level of heterogeneous integration, whether it is for:

- **Time-to-market**
- **Performance**
- **Form factor**
- **Power consumption**
- **Cost**

System-in-Package (SiP)

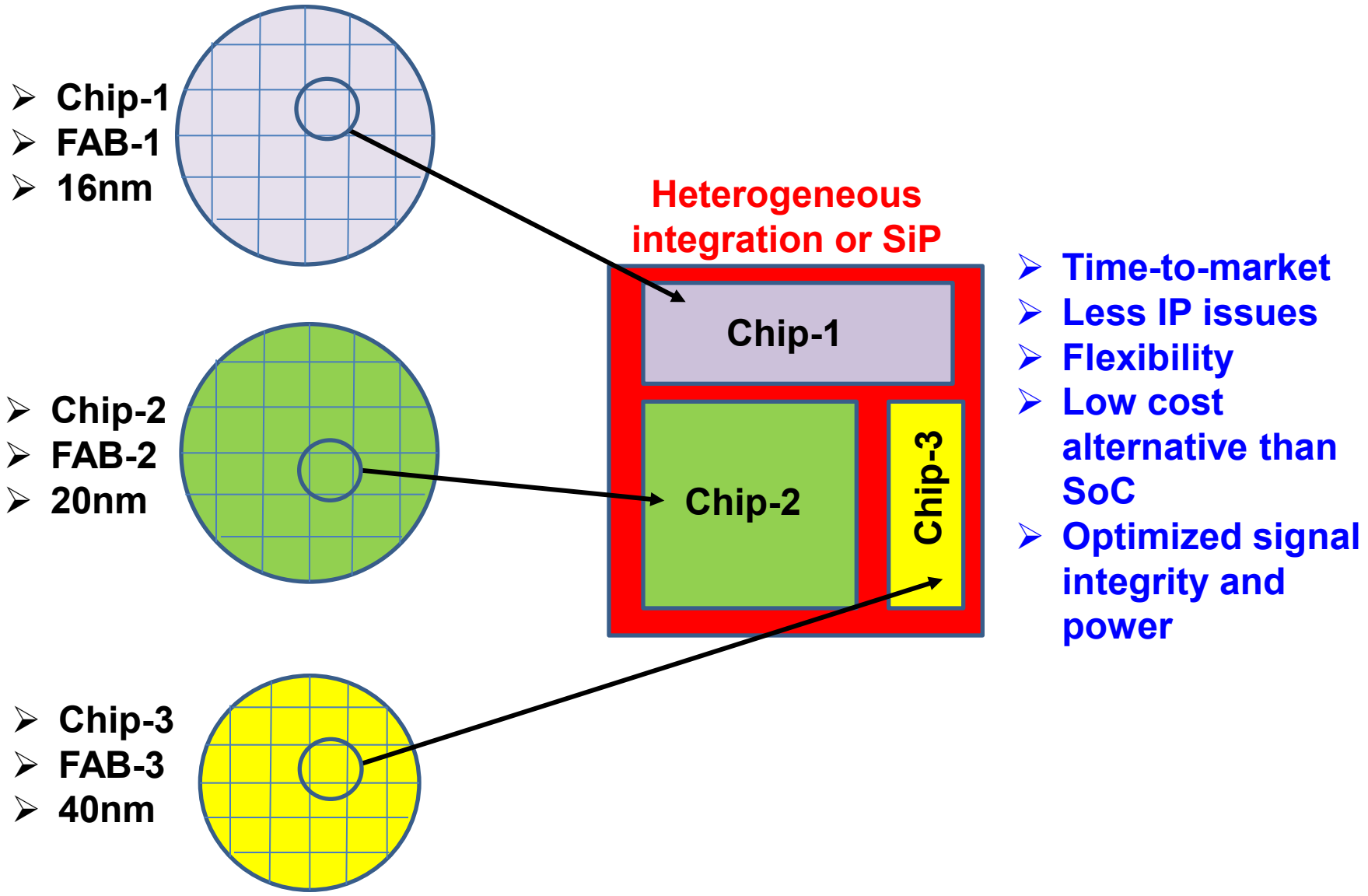
SiP integrates different chips + discrete as well as 3D chip stacking of neither packaged chips or bare chips (e.g., wide-bandwidth memory cubes and memory on logic with TSVs) side-by-side on a common (either silicon, ceramic, or organic) substrate to form a system or subsystem for smartphones, tablets, high-end networking, servers and computers applications.

SiP technology performs horizontal as well as vertical integrations. Some people also called SiP vertical MCM or 3D MCM. Unfortunately, because of the high cost of wide I/O memory with TSV technology for smartphones and tablets, it never materialized.

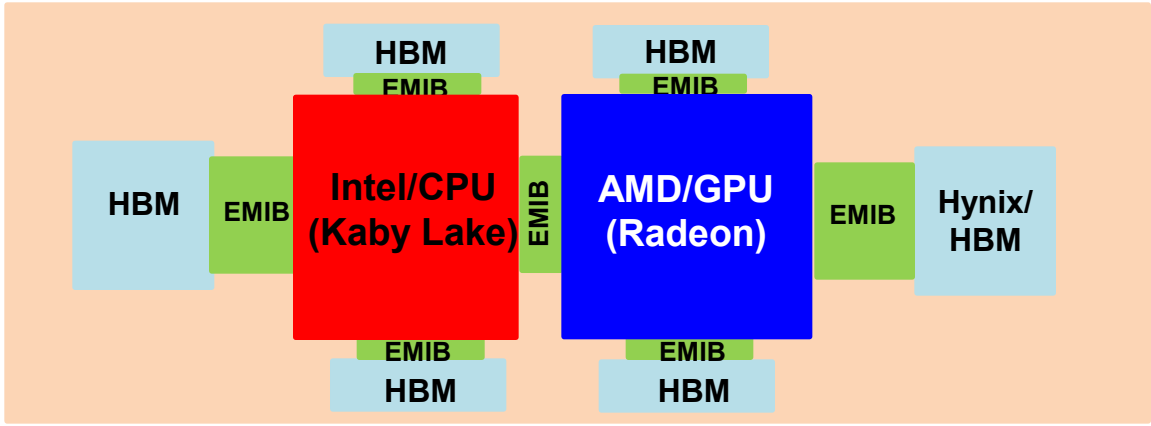
Most of the SiPs manufactured in the past 10 years are actually MCM-L for low-end applications such as smartphones, tablets, smart watches, medical, wearable electronics, gaming systems, consumer products and IoT-related products such as smart homes, smart energy, and smart industrial automation. Usually, the SiPs integrated two or more dissimilar chips and some discrete on a common laminated substrate.

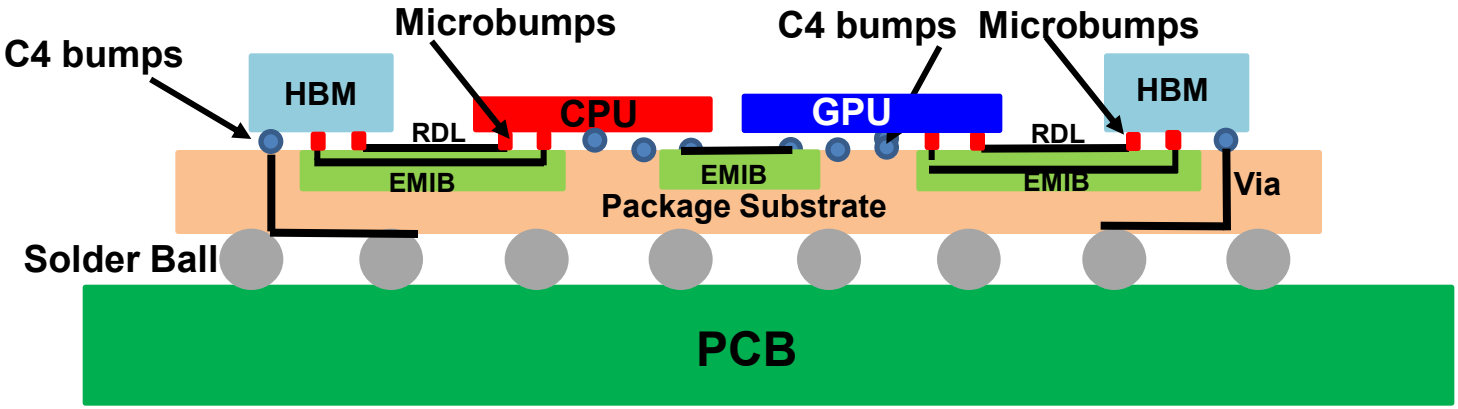
SiP is similar to heterogeneous integration but with less density and gross pitch.

Heterogeneous Integration



Intel/AMD/Hynix Heterogeneous Integration using Intel's EMIB





http://www.digitimes.com.tw/tw/dt/n/shwnws.asp?CnlID=1&Cat=10&id=493987&query=%A6%B3%A4F%AD%5E%AFS%BA%B8%A5%5B%AB%F9%A1A%B6W%B7L%B1N%B1o%A8%EC%A7%F3%A4j%AA%BA%A7U%A4O%B9%EF%A7%DCNVIDIA (2/20/2017)

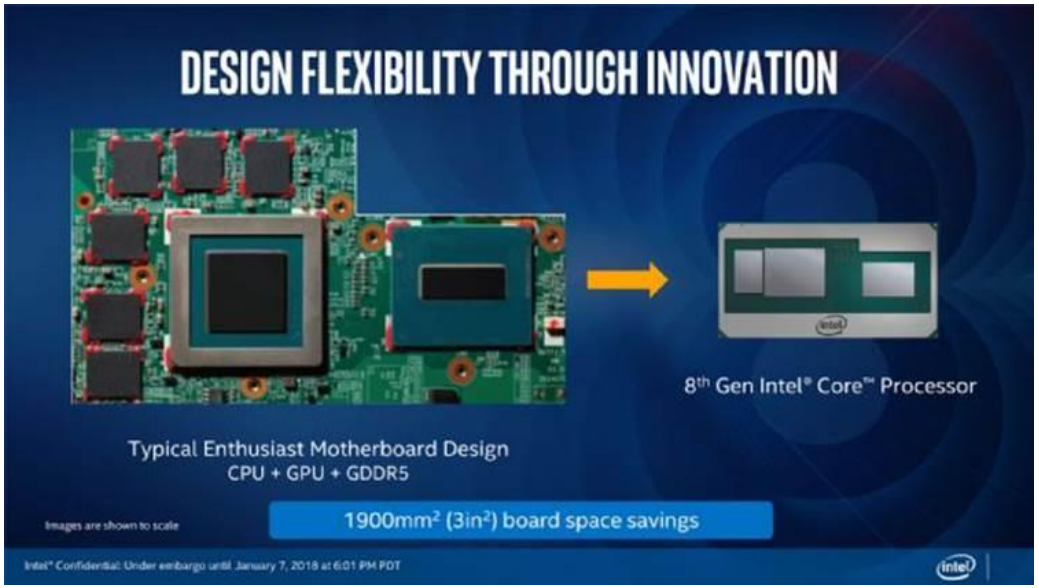
A Little History

On February 20, 2017, DIGITIMES disclosed the collaboration between Intel and AMD.

On May 17, 2017, Fortune had an article: “Why AMD's Shares Tumbled 9%?”. That’s because when Intel was asked about the deal with AMD, Intel didn’t say Yes or No.

On November 6, 2017, Intel has formally revealed it has been working on a new series of processors that combine its high-performance x86 cores CPUs with AMD GPUs (Radeon Graphics) into the same processor package (heterogeneous integration) using Intel’s own EMIB multi-die technology. If that wasn’t enough, Intel also announced that it is bundling the design with the latest high-bandwidth memory, HBM.

Intel's Heterogeneous Integration: Intel's CPU (Kaby Lake) and AMD's GPU (Radeon)



For NB to be shipped in 2018!

DIGITIMES/EE Times, November 6, 2017

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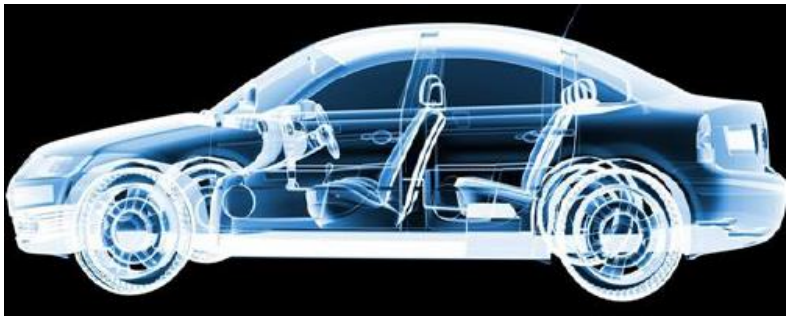
Amkor Automotive SiP

- Large singulated body SiP
- Infotainment & ADAS
- Autonomous driving
- Computers in a car
- Increasing trend in designs

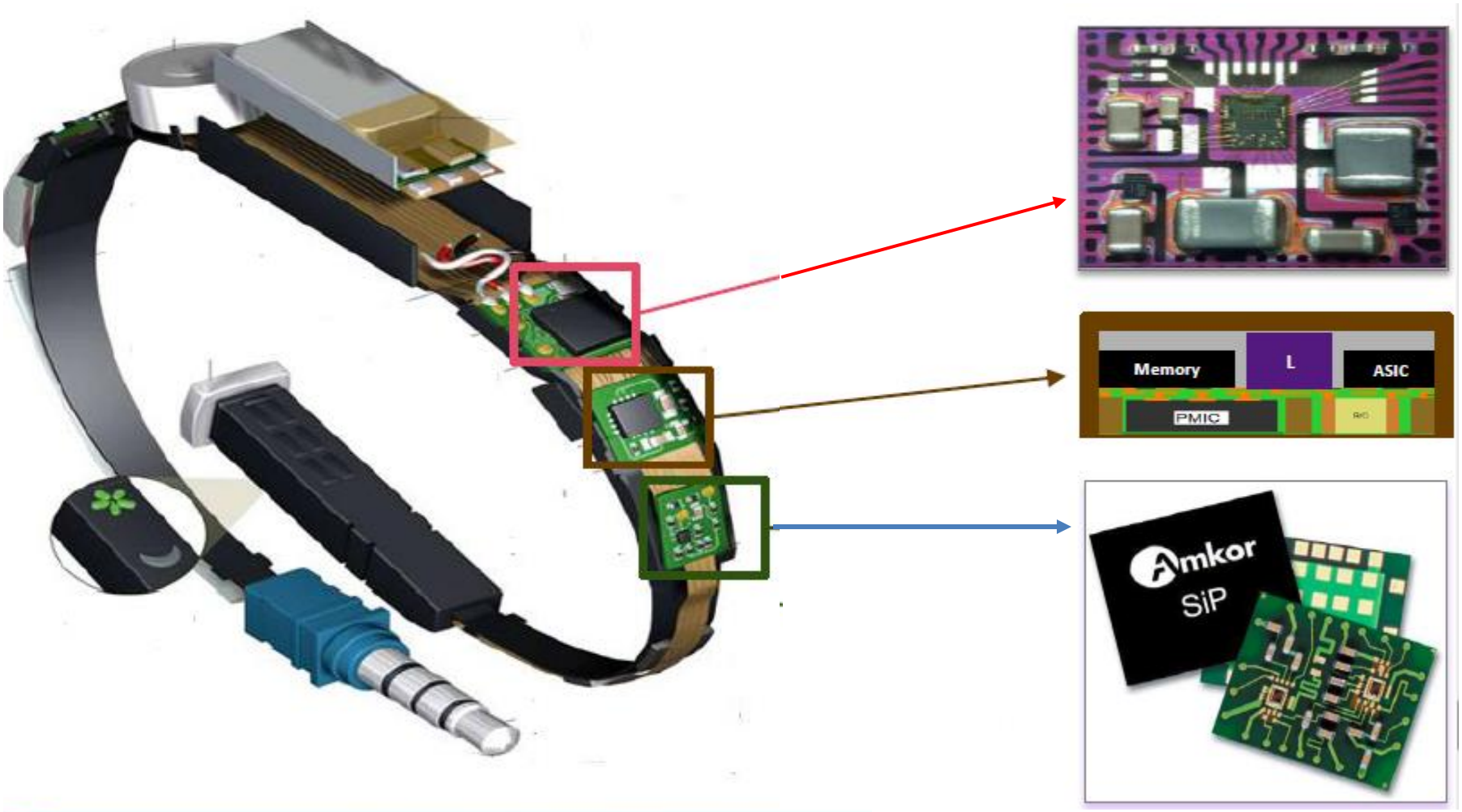


42.5 x 42.5 mm, Infotainment, Processor + DDR

55 x 72 mm, Network Switch, ASIC + Memory

Heterogeneous Integration with organic substrate

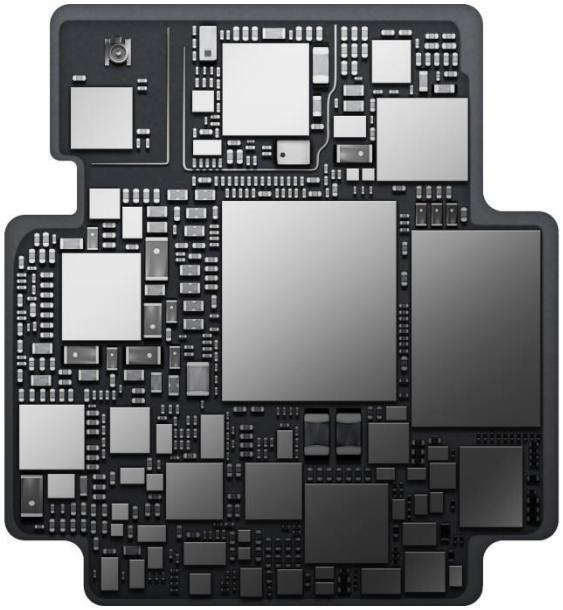
Amkor IoTs and Wearables SiP

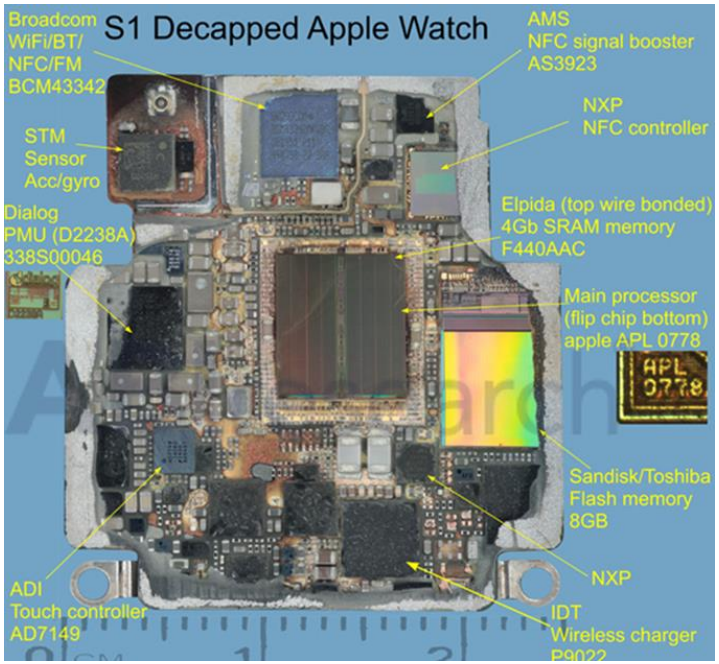


Amkor Technology®

Heterogeneous Integration with organic substrate

Apple Watch (S1)



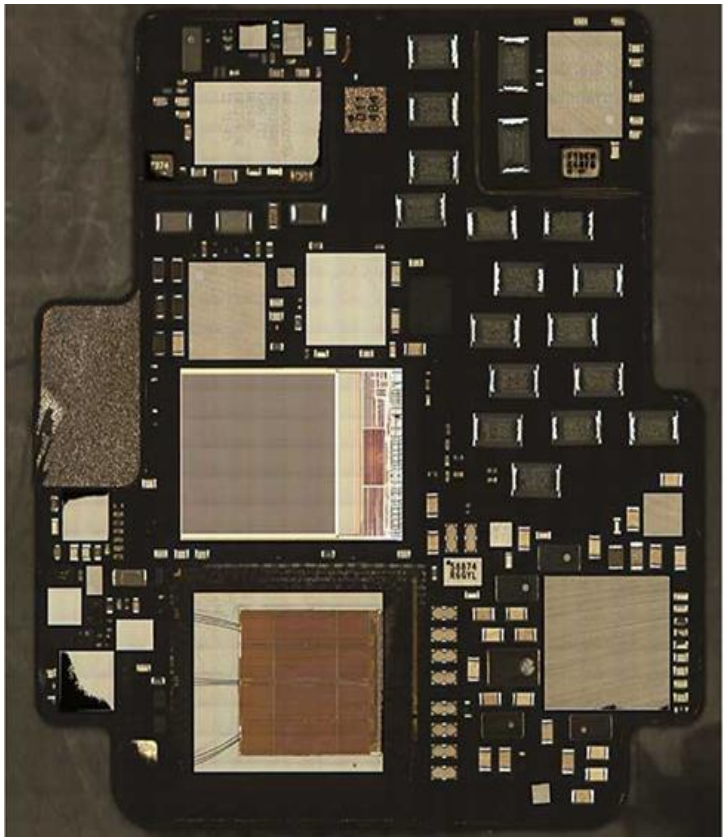


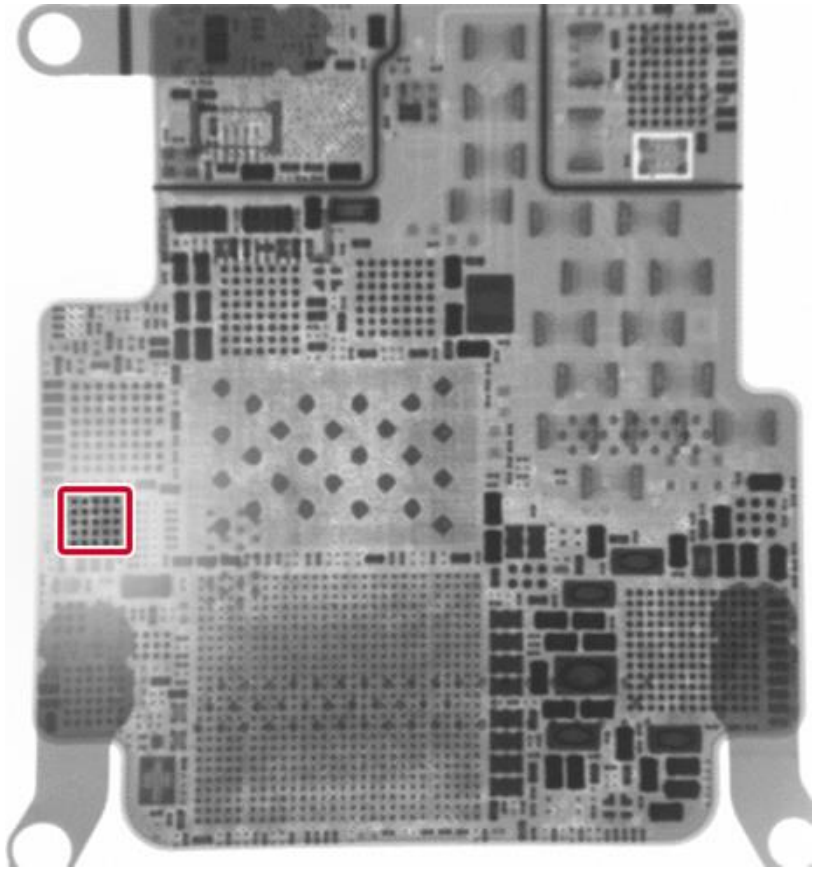
ABI Research

- The processor is integrated with the DRAM into a SoC.
- Apple then integrated the SoC, NAND flash, wireless connectivity chip, PMIC, sensors, and some special-purpose chips into a SiP called S1 for their Apple Watch.

Heterogeneous Integration with organic substrate

The Apple Watch (S2) Contains More Than 42 Chips!
The SiP (S2) was Assembled by ASE

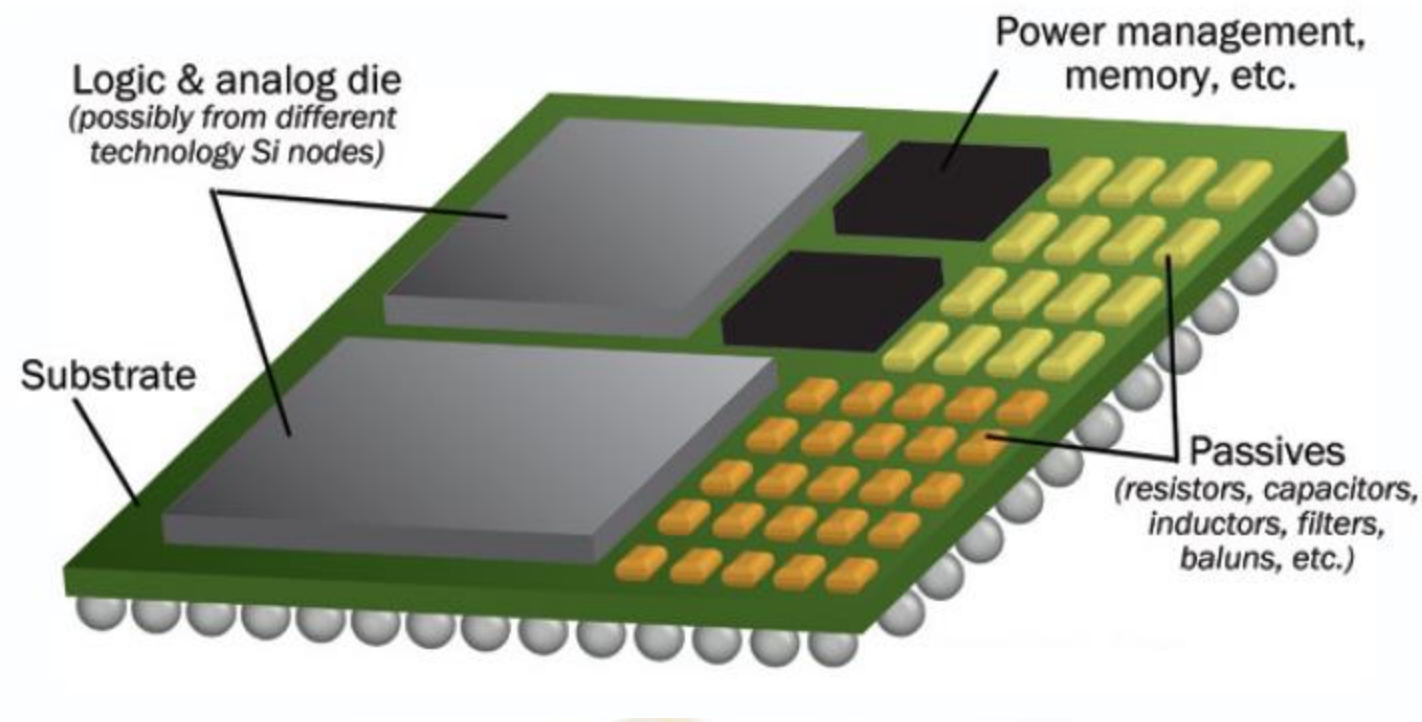


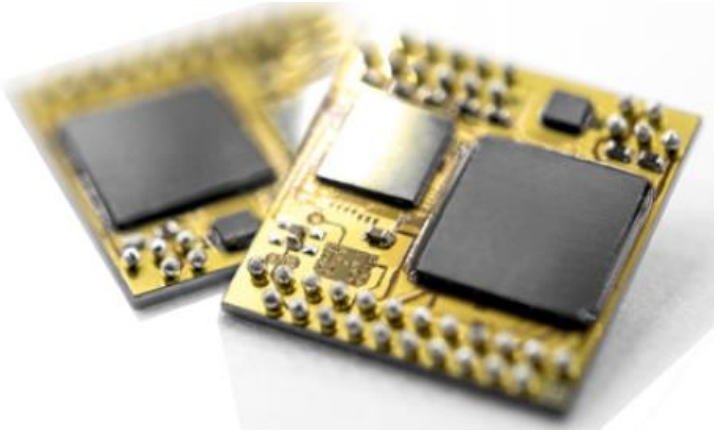


SiP (S2)

Heterogeneous Integration with organic substrate

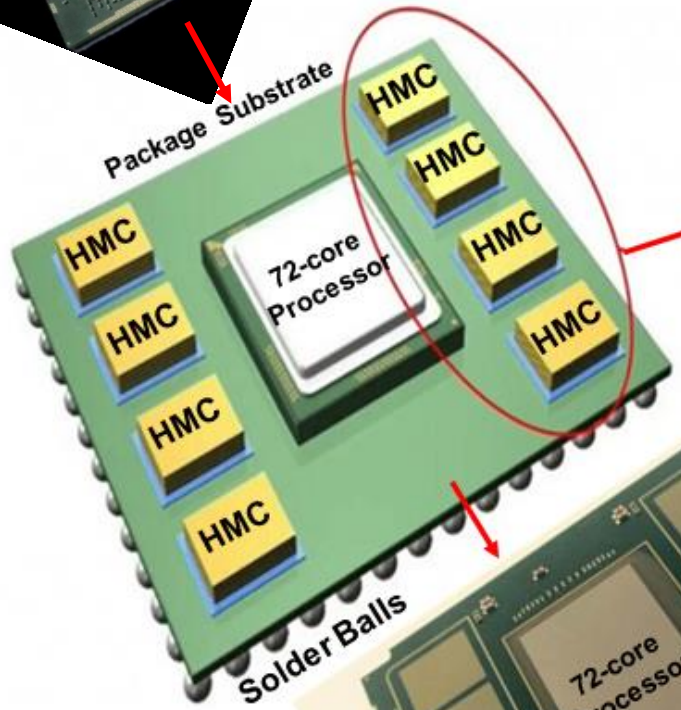
STATSChipPac System-in-Packaging (SiP)

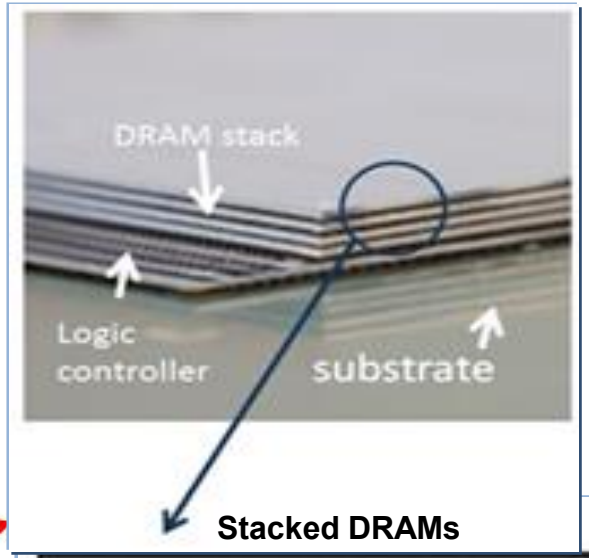


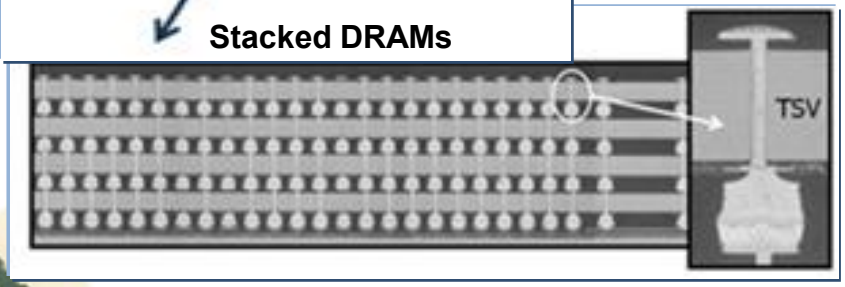


Heterogeneous Integration with organic substrate

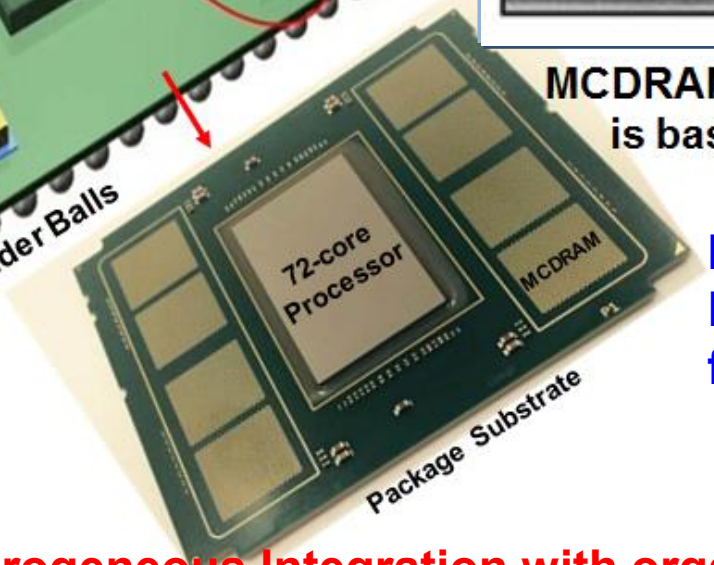
Intel's "Knights' Landing" with 8 HMC Fabricated by Micron







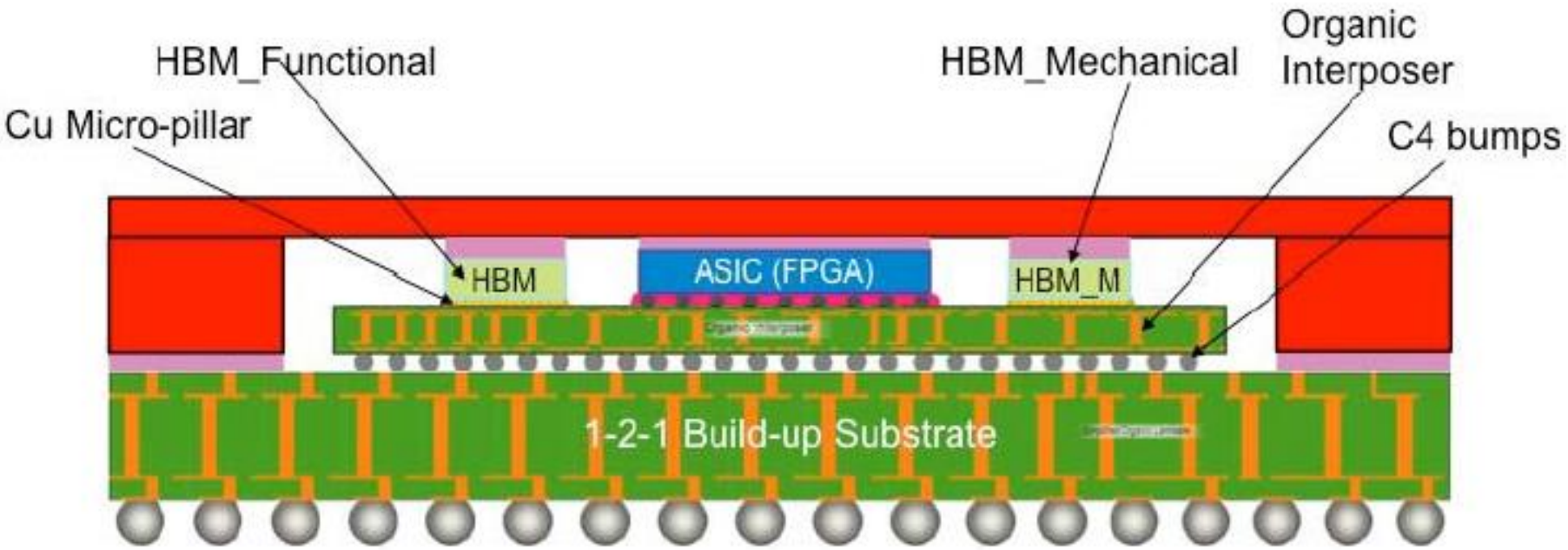
MCDRAM (Multi-Channel DRAM) is based on Micron's HMC

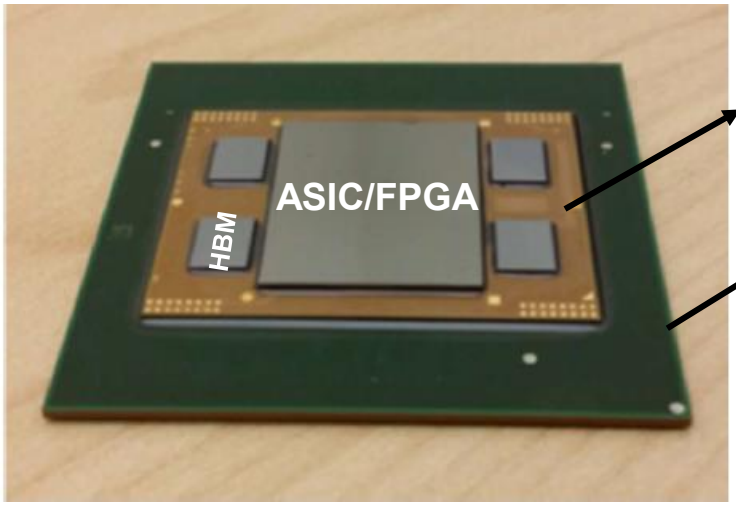


Intel has been shipping the Knights Landing to their favorite customers.

Heterogeneous Integration with organic substrate

Cisco's Organic Interposer for ASIC and Memory Heterogeneous Integration





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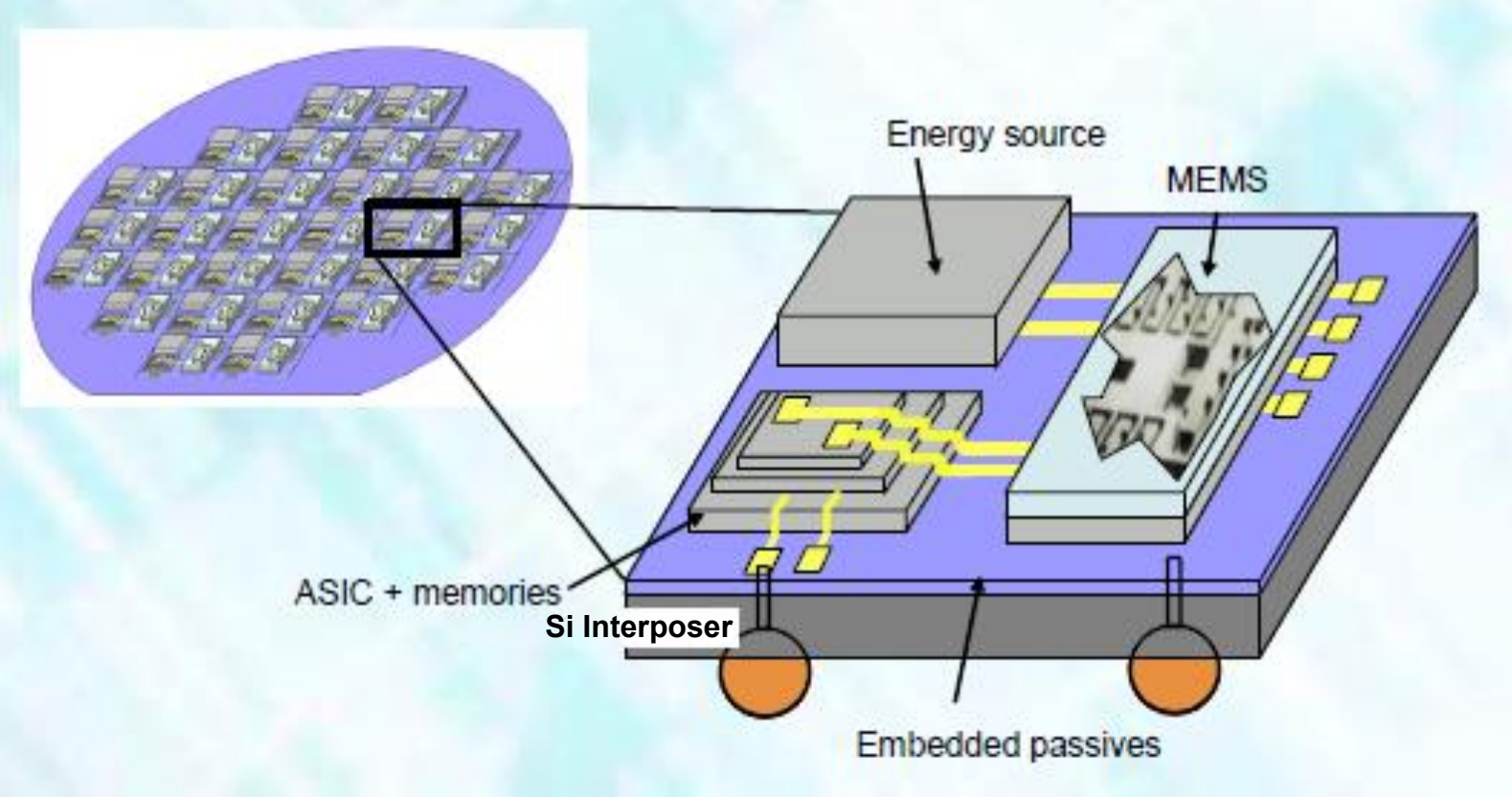
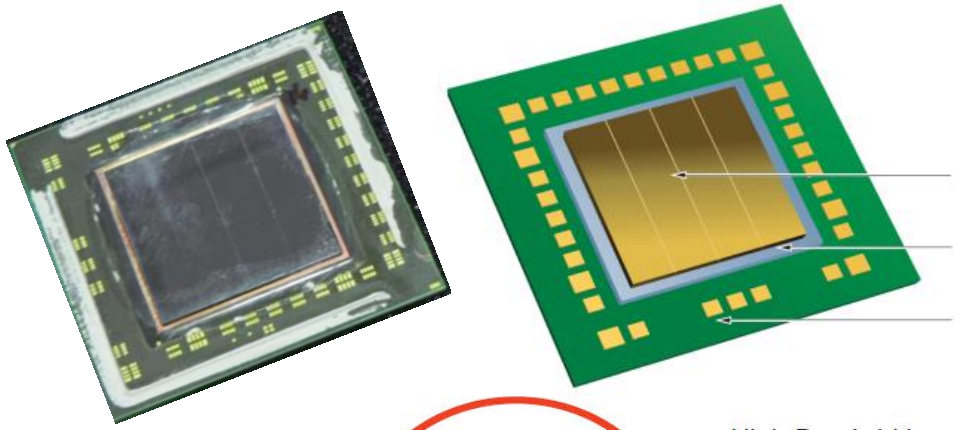
Leti's Heterogeneous Integration: System-on-Wafer (SoW)

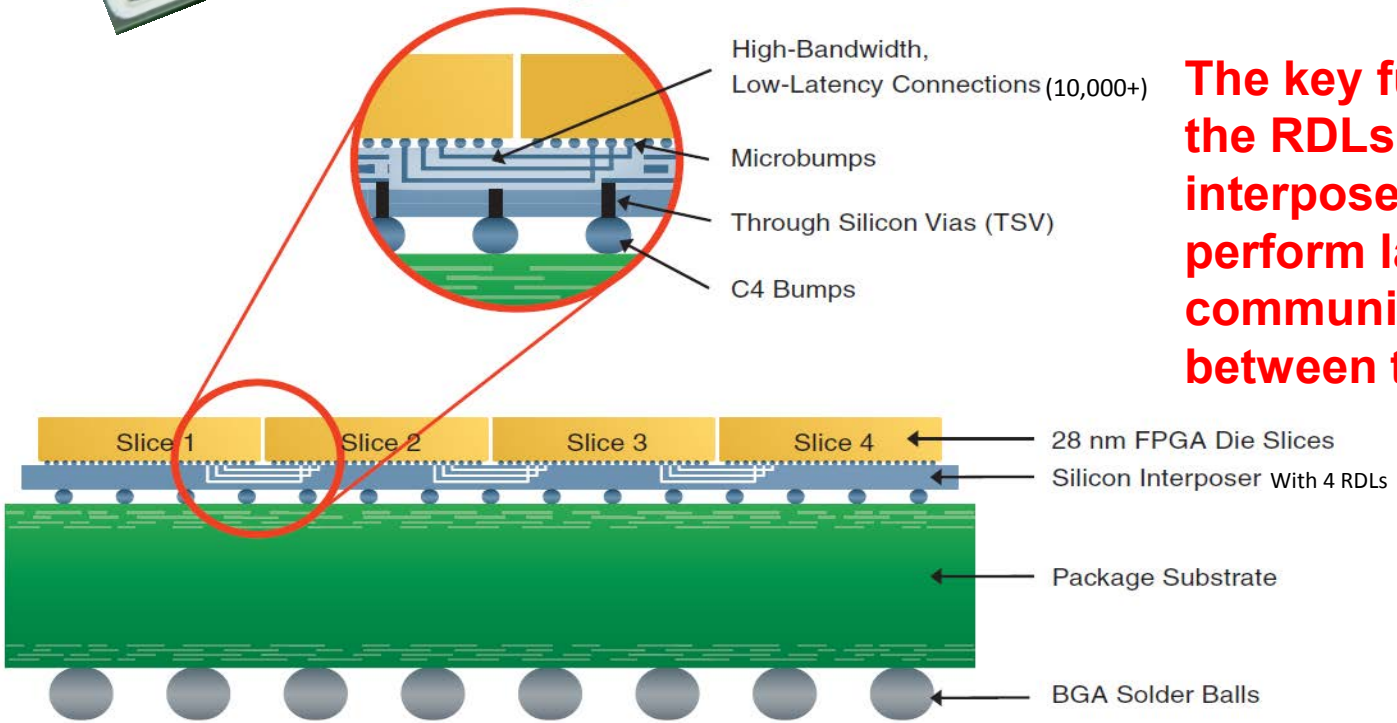


Heterogeneous Integration with silicon substrate

TSMC/Xilinx's Interposers with TSV and RDL for FPGA Products



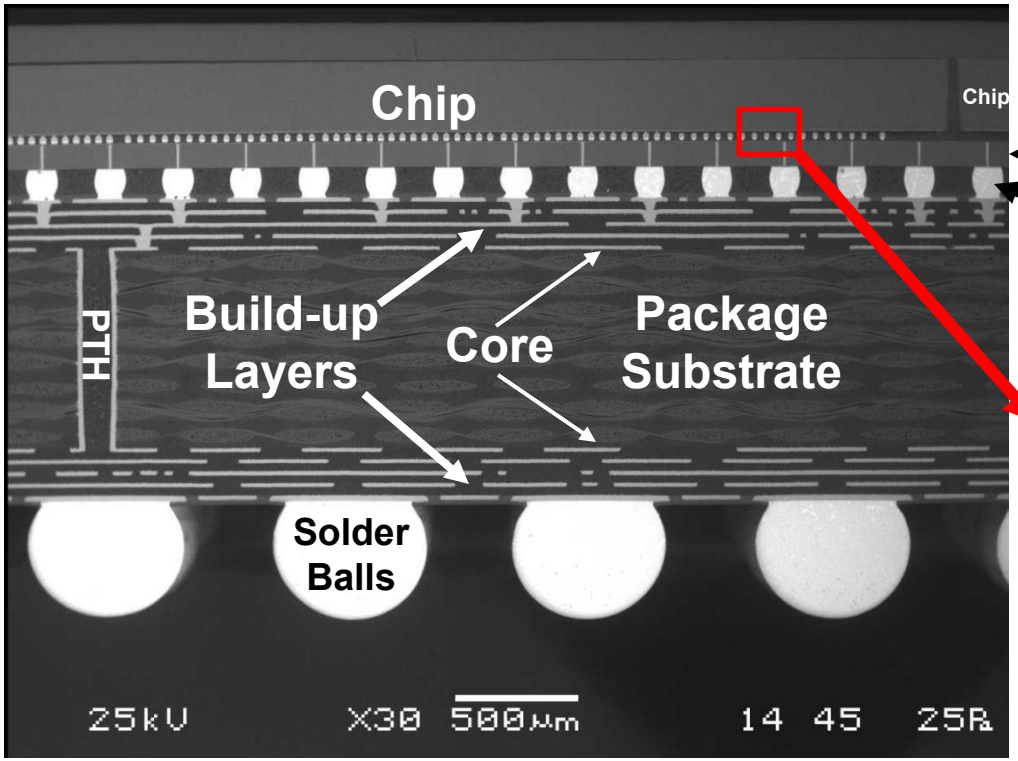
For better manufacturing yield (to save cost), a very large SoC has been sliced into 4 smaller chips (2011).

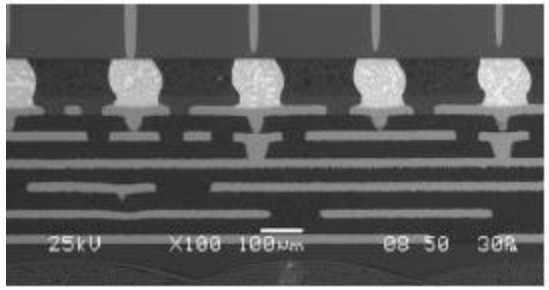


The key function of the RDLs on the interposer is to perform lateral communications between the chips.

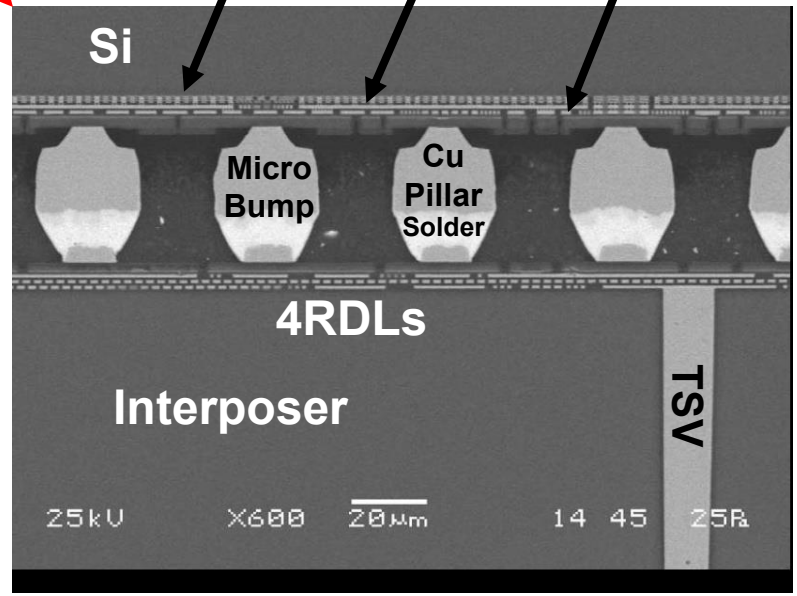
CoWoS (Chip on Wafer on Substrate)

Xilinx/TSMC's 2.5D IC Integration with FPGA





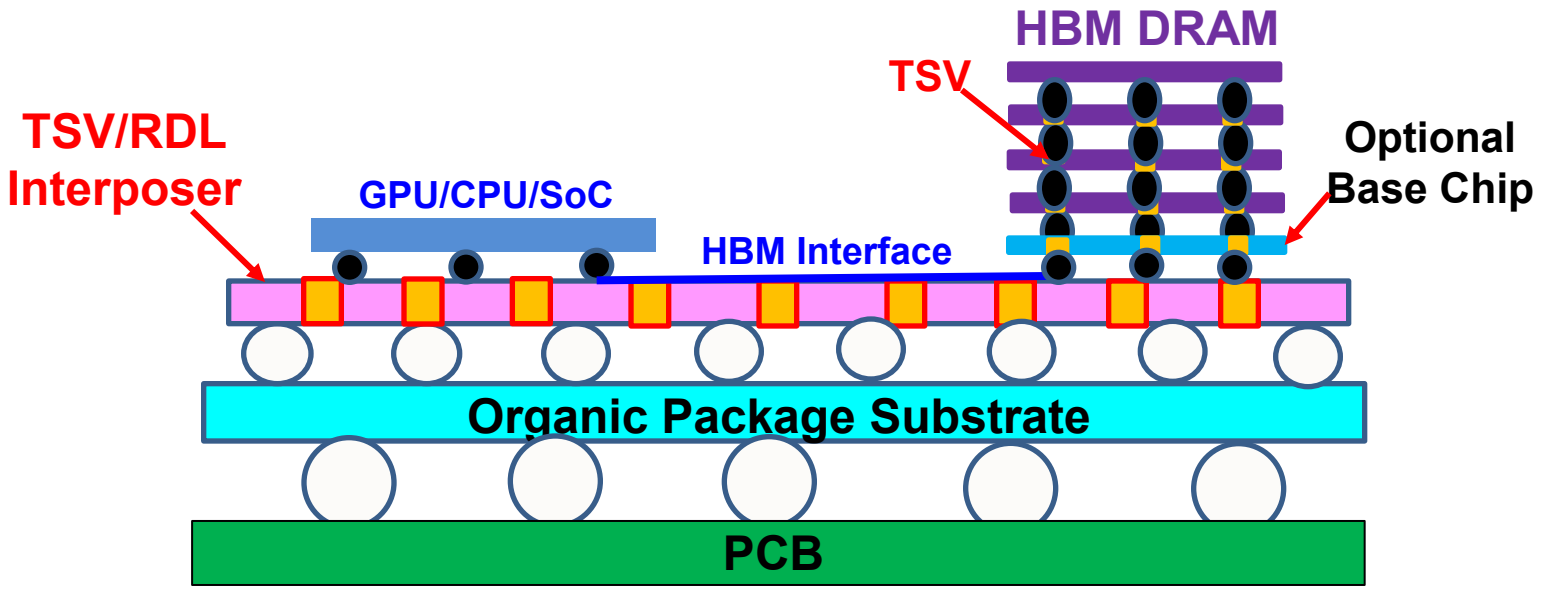
The package substrate is at least (5-2-5)



- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

High Bandwidth Memory (HBM) DRAM (Mainly for Graphic applications) JEDEC Standard (JESD235), October 2013

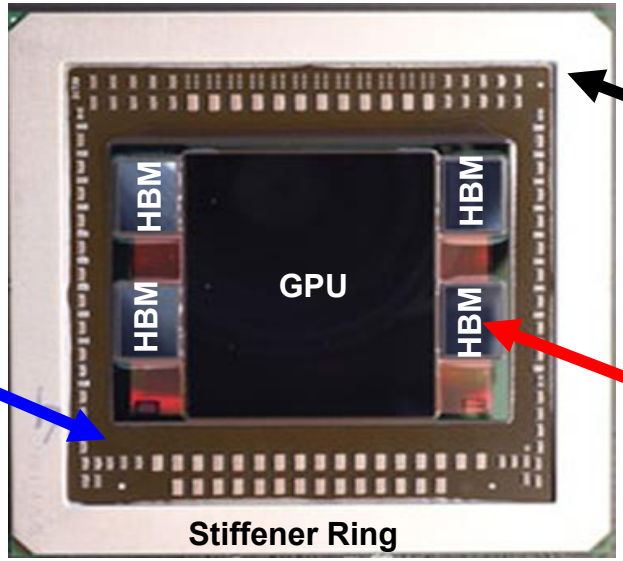
HBM is designed to support bandwidth from 128GB/s to 256GB/s



Underhill is needed between the interposer and the organic substrate. Also, underfill is needed between the interposer and the GPU/CPU and the memory cube

AMD's GPU (Fiji), Hynix's HBM, and UMC's Interposer

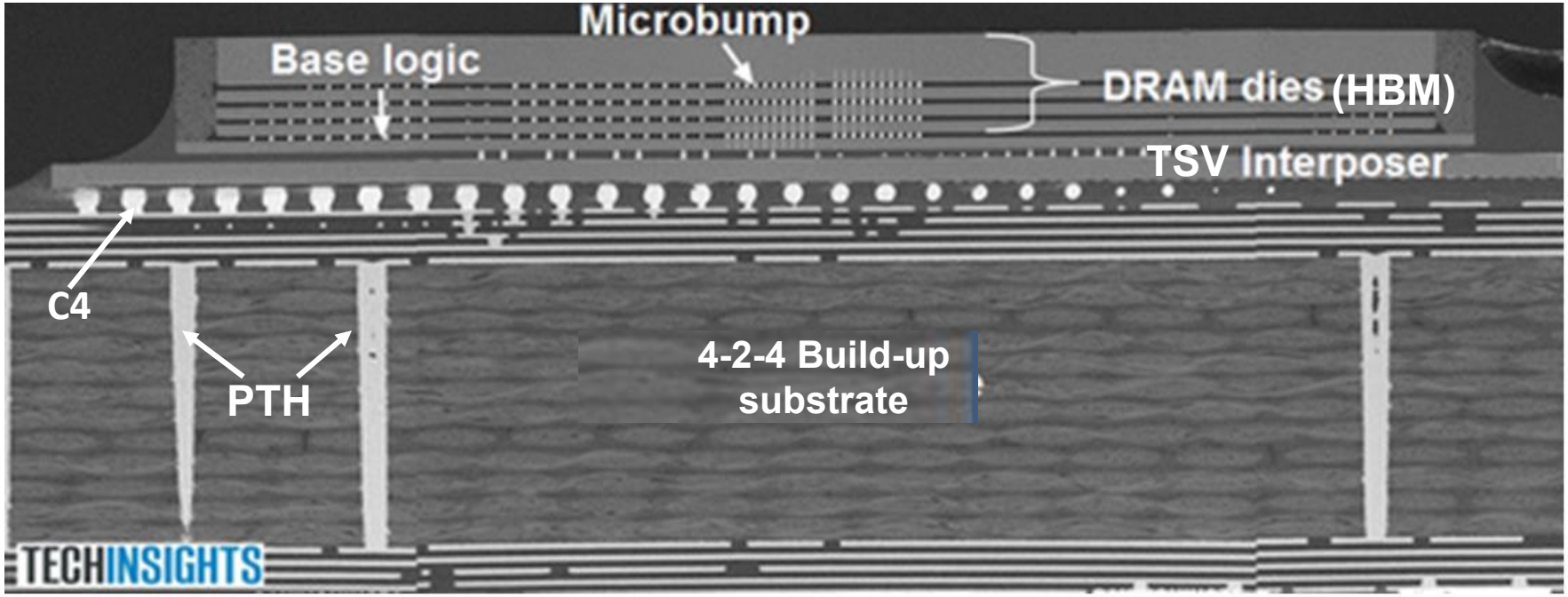
The GPU (23mmx27mm) is fabricated by TSMC's 28nm Process technology



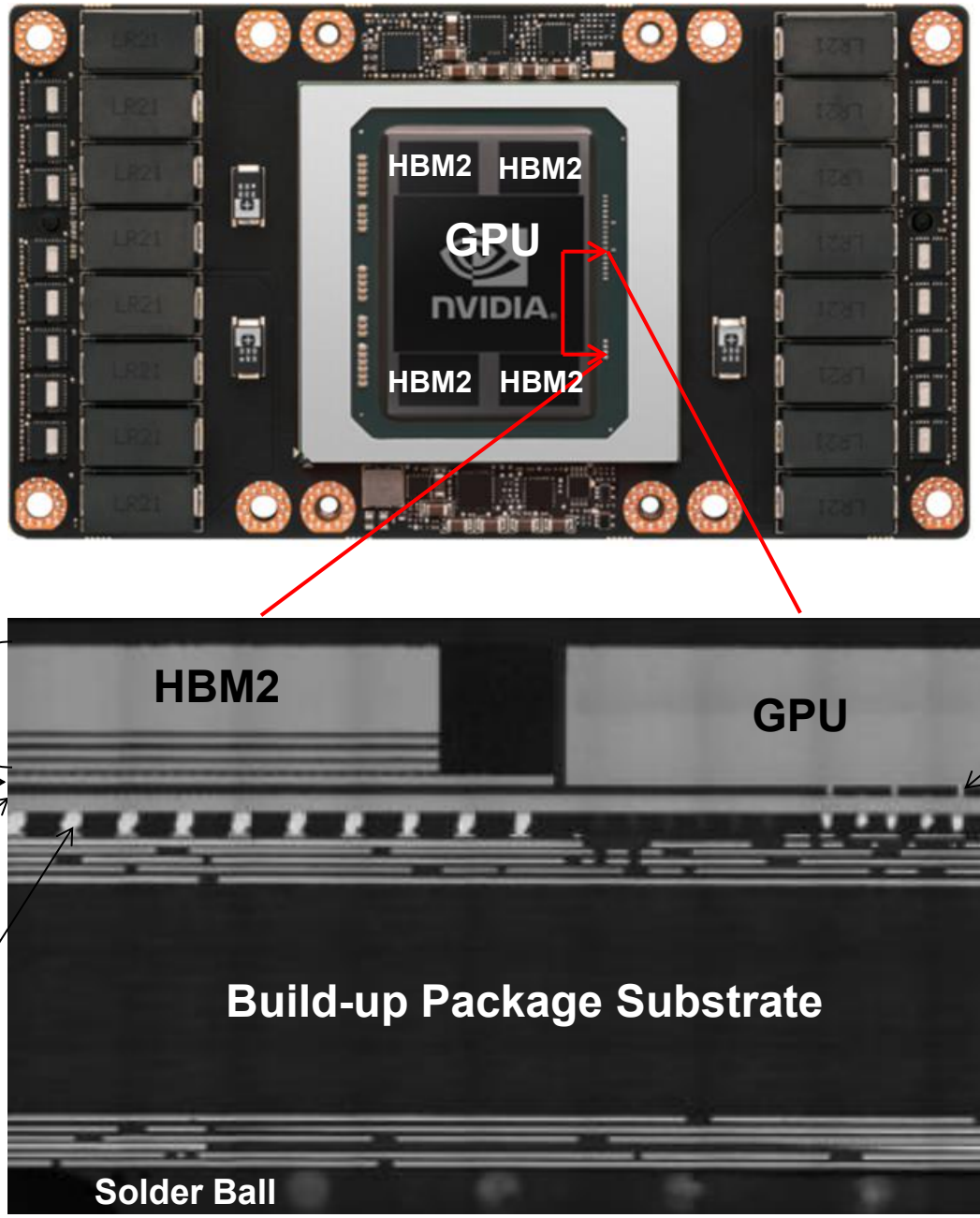
The Organic Substrate (54mm x 55mm) is with 2111 balls at 1.2mm pitch

The Si-interposer (28mmx35mm) is fabricated by UMC's 65nm process technology

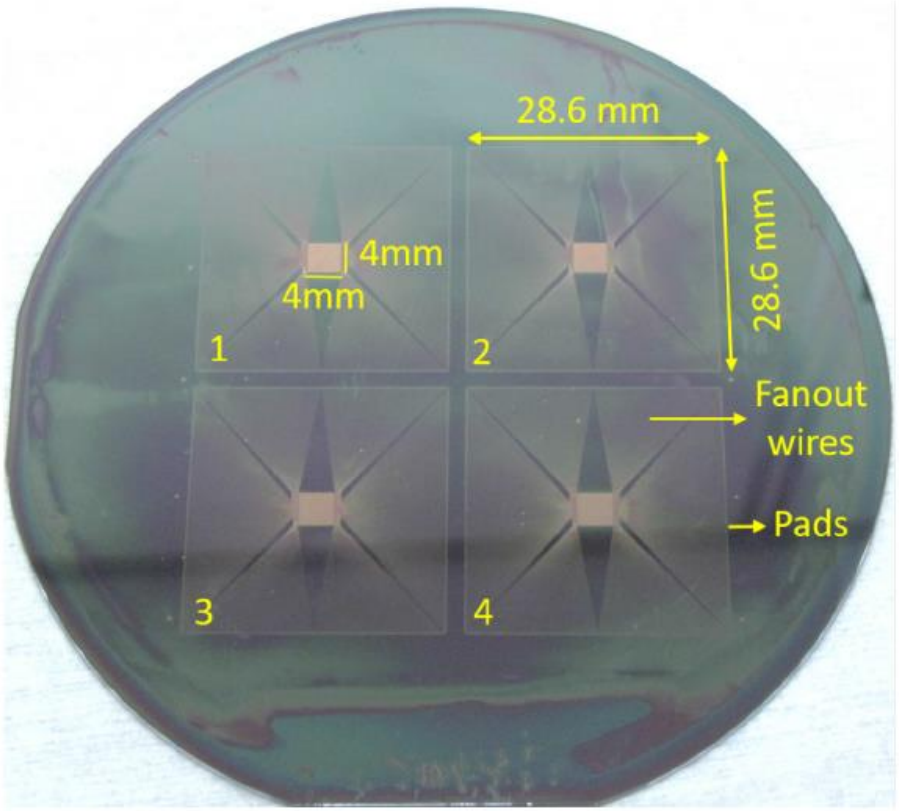
The HBM is fabricated by Hynix



Nvidia's P100 with TSMC's CoWoS and Samsung's HBM2



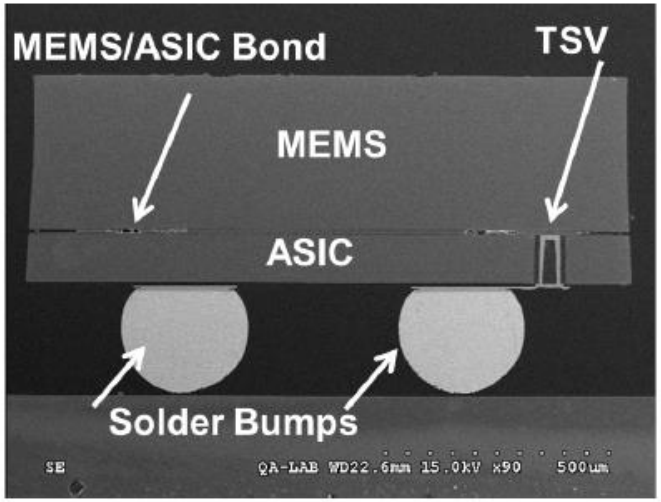
Planer view of fabricated Si-IF with Cu-pillars to accommodate 4 dielets

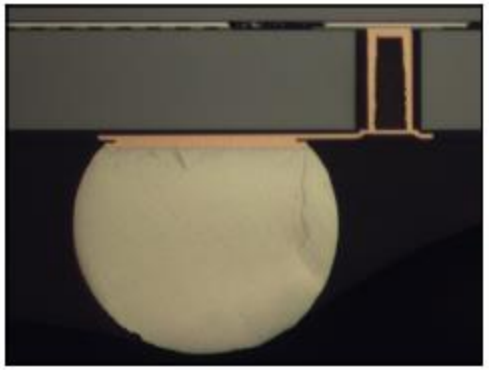


Silicon Interconnect Fabric (Si-IF) which allows us to interconnect dies at fine pitch. The Si-IF is fabricated using conventional Si-based BEOL processing with up to four levels of conventional Cu damascene interconnects with wire pitches in the range of 1 – 10µm and is terminated with Cu pillars of 2 – 5µm height & diameter also using a damascene process.

Heterogeneous Integration – MEMs + ASIC

MEMs + ASIC Wafer-Level Integration





ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

MEMs (Chip) to ASIC (Wafer) Bonding!

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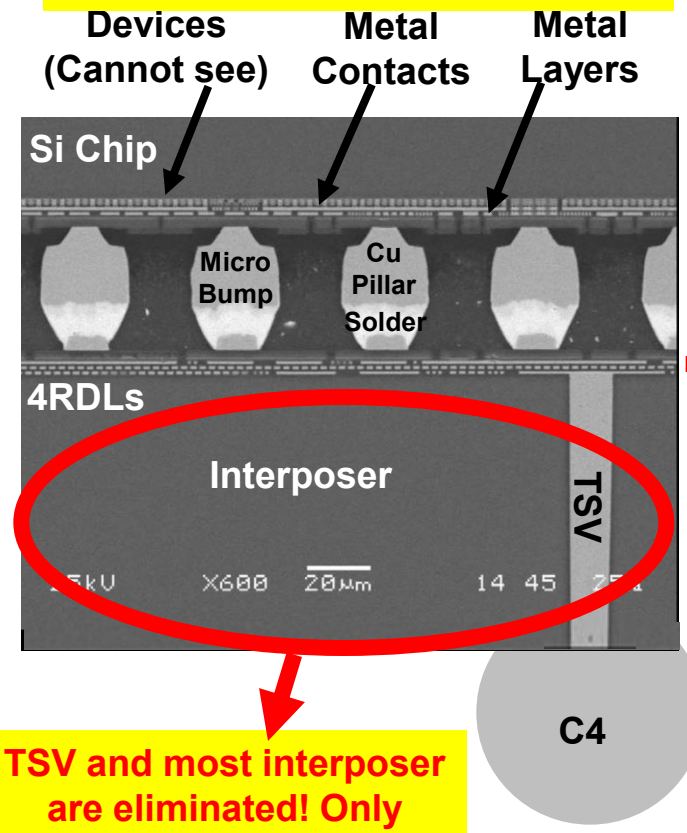
- **Heterogeneous Integration**
- **Heterogeneous Integration on Organic Substrates**
- **Heterogeneous Integration on Silicon Substrates**
- **Heterogeneous Integration on RDLs**
- **FOWLP for 3D IC Heterogeneous Integration**

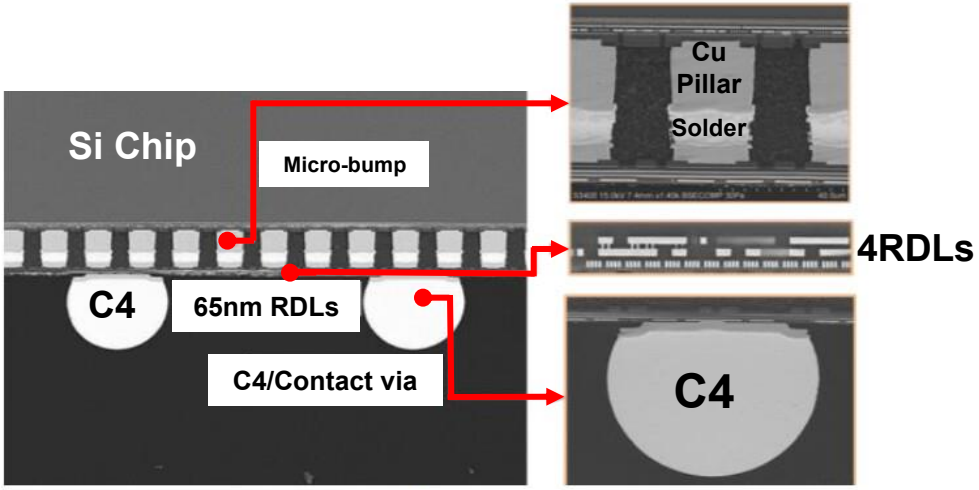
Xilinx/TSMC's CoWoS

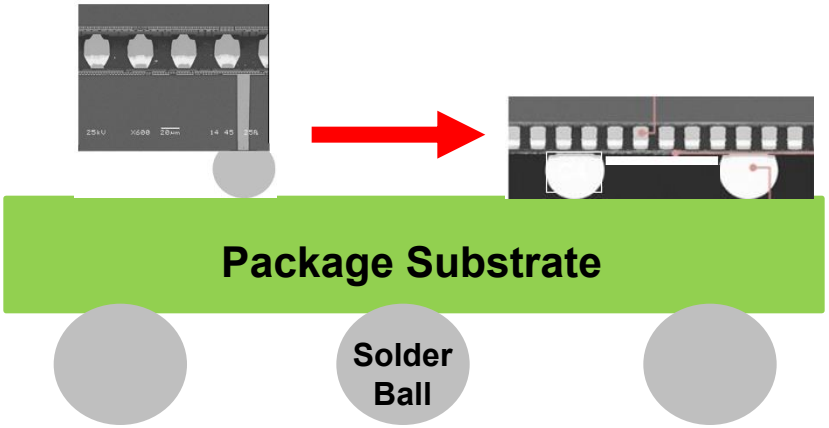


TSV and most interposer are eliminated! Only RDLs remained.

- Lower cost
- Better performance
- Lower profile

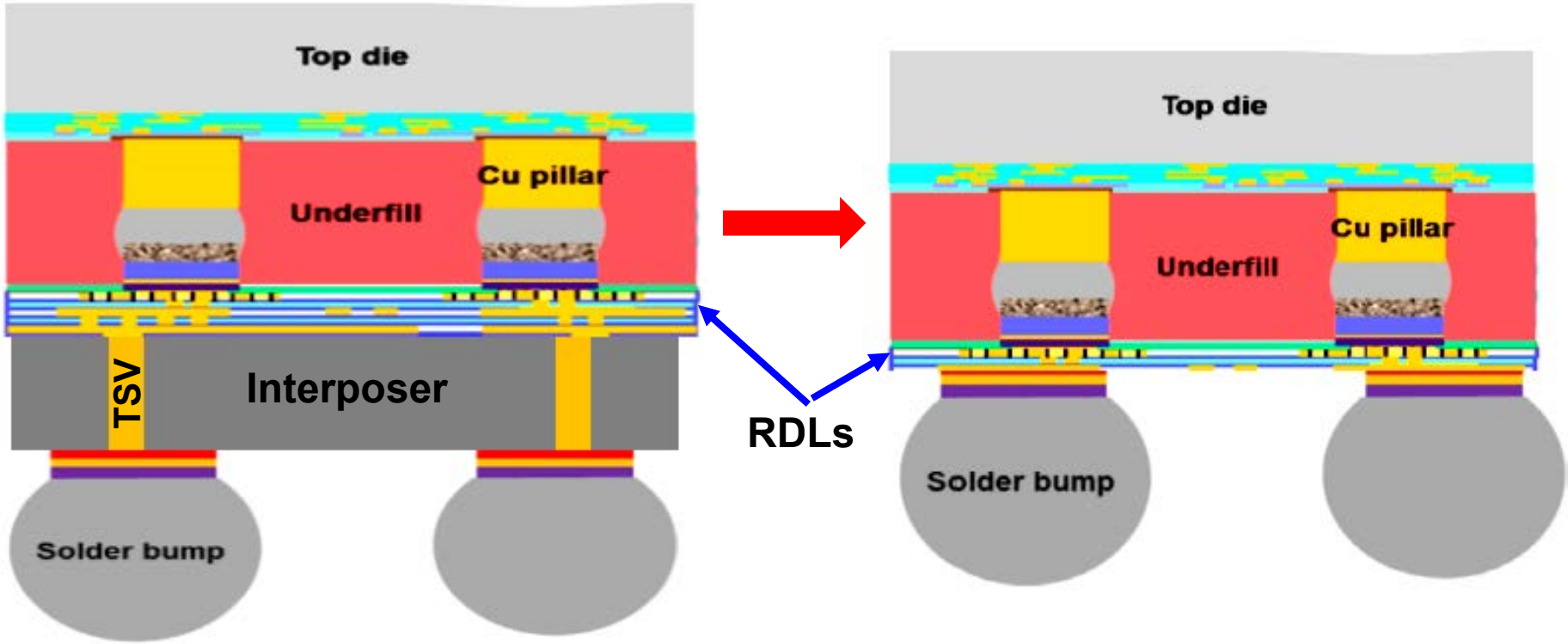
Xilinx/SPIL's SLIT





- No entire TSV fabrication module
- No thin wafer handling technology
- No novel backside TSV revealing process
- No multiple inspection & metrology steps for TSV fabrication & backside TSV revealing steps.

Amkor's SLIM (Silicon-Less Integrated Module)



- Foundry BEOL layers retained
- Same CuP bond pads
- Same UBM and solder bump
- No TSV
- Much thinner

US 20140070380A1

(19) **United States**

(12) **Patent Application Publication**

Chiu et al.

(10) **Pub. No.: US 2014/0070380 A1**

(43) **Pub. Date: Mar. 13, 2014**

(54) **BRIDGE INTERCONNECT WITH AIR GAP IN PACKAGE ASSEMBLY**

(76) Inventors: **Chia-Pin Chiu**, Tempe, AZ (US); **Zhiguo Qian**, Chandler, AZ (US); **Mathew J. Manusharow**, Phoenix, AZ (US)

(21) Appl. No.: **13/610,780**

(22) Filed: **Sep. 11, 2012**

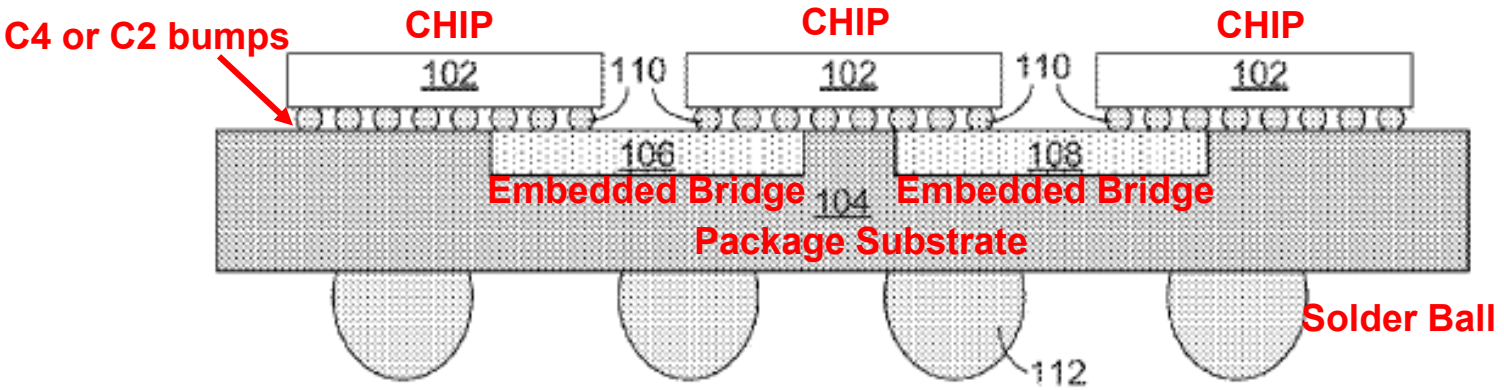
Publication Classification

(51) **Int. Cl.**
H01L 23/495 (2006.01)
H01L 21/60 (2006.01)

(52) **U.S. Cl.**
USPC **257/666**; 438/107; 257/E21.506; 257/E23.052

(57) **ABSTRACT**

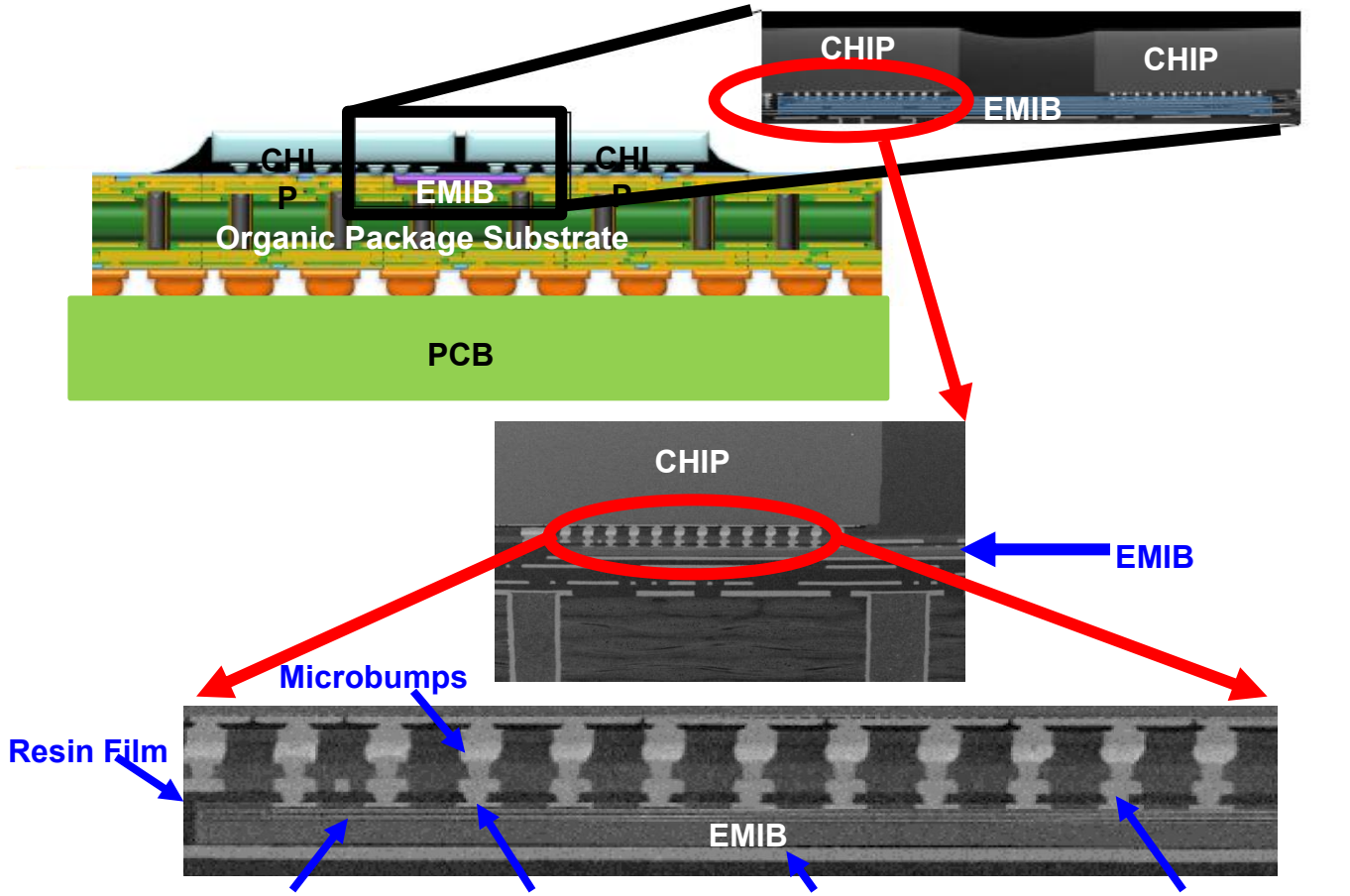
Embodiments of the present disclosure are directed towards techniques and configurations for a bridge interconnect assembly that can be embedded in a package assembly. In one embodiment, a package assembly includes a package substrate configured to route electrical signals between a first die and a second die and a bridge embedded in the package substrate and configured to route the electrical signals between the first die and the second die, the bridge including a bridge substrate, one or more through-hole vias (THVs) formed through the bridge substrate, and one or more traces disposed on a surface of the bridge substrate to route the electrical signals between the first die and the second die. Routing features including traces and a ground plane of the bridge interconnect assembly may be separated by an air gap. Other embodiments may be described and/or claimed.



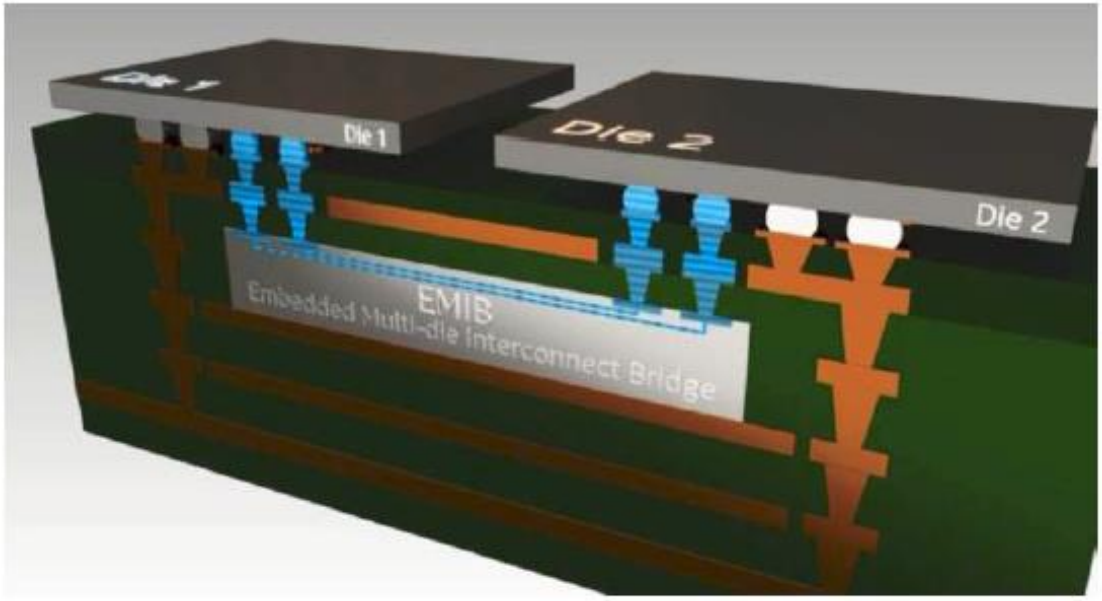
Embedded Multi-die Interconnect Bridge (EMIB)

Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect

Ravi Mahajan, Robert Sankman, Neha Patel, Dae-Woo Kim, Kemal Aygun, Zhiguo Qian, Yidnekachew Mekonnen, Islam Salama, Sujit Sharan, Deepti Iyengar, and Debendra Mallik
Assembly Test Technology Development
Intel Corporation
Chandler, Arizona, USA
ravi.v.mahajan@intel.com

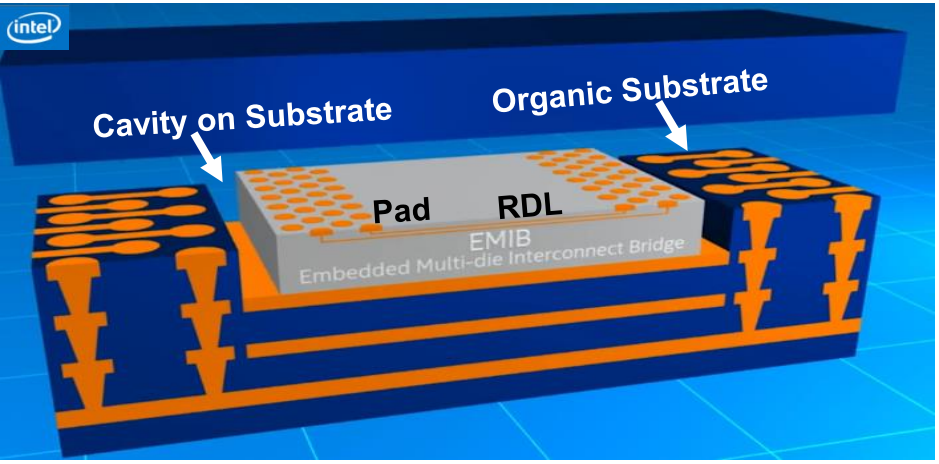


Schematic showing the EMIB concept

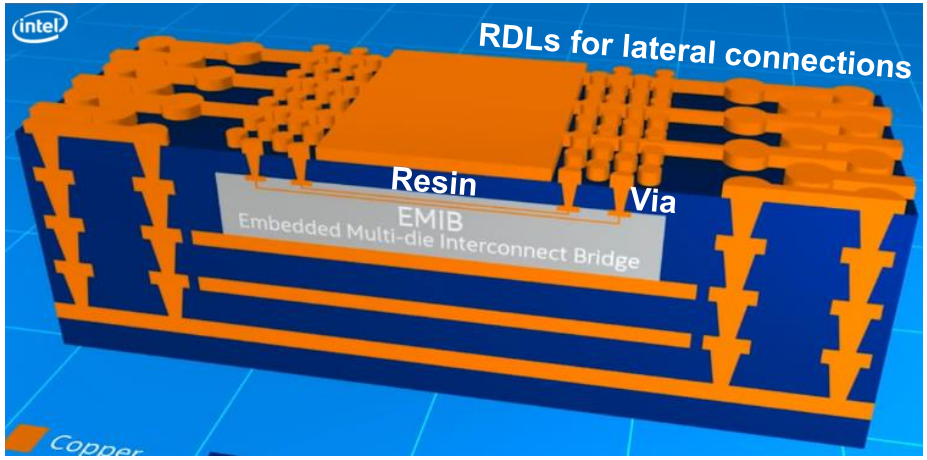


Attributes	EMIB Values
Bridge Size Range	2mm x 2mm - 8mm x 8mm (Current Range) – Higher sizes possible
Number of Bridges Per Package	> 5 possible
Metal Layers	Up to 4 routing metal layers + pad layer M1/M2/M3/M4: 2µm Lines & 2µm Spaces (lower dimensions possible) Via 1/Via2/Via3: 2µm (dual damascene; lower dimensions possible) 50 ~ 70% metal density on V_{ss} layer.

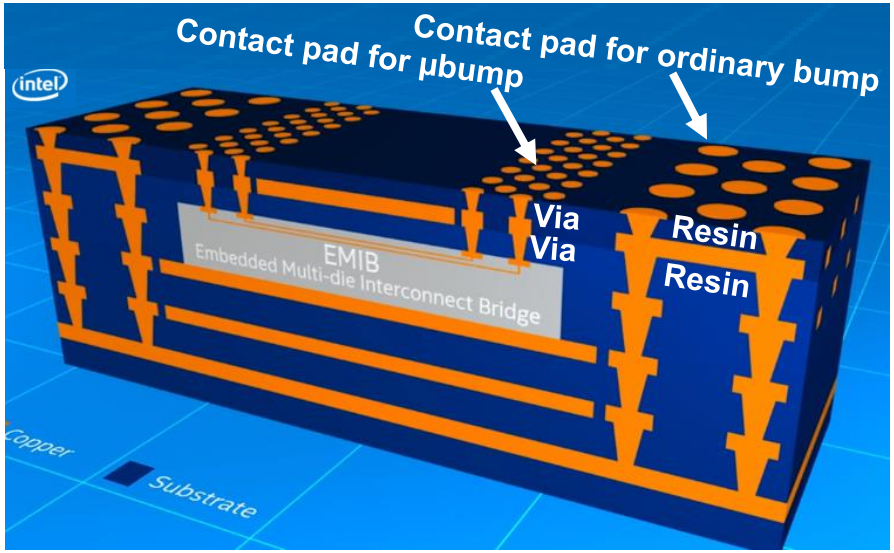
High level EMIB assembly process



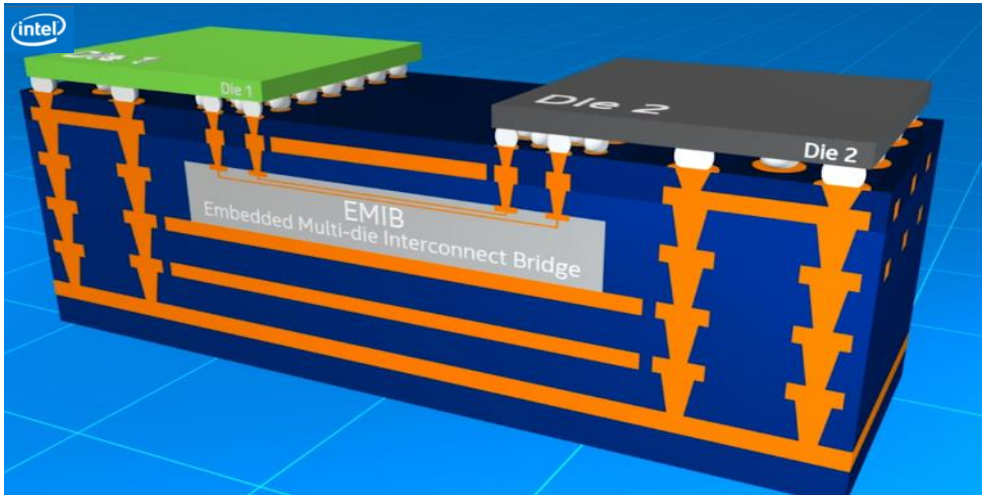
(a)



(b)

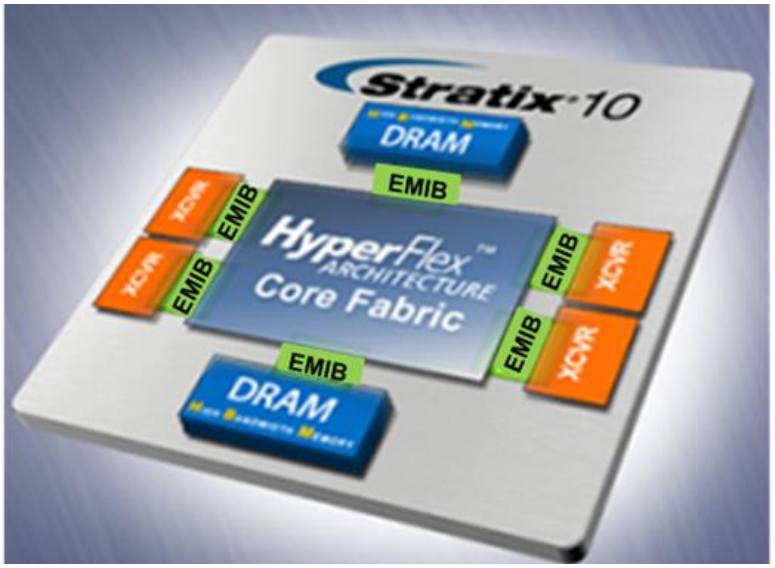


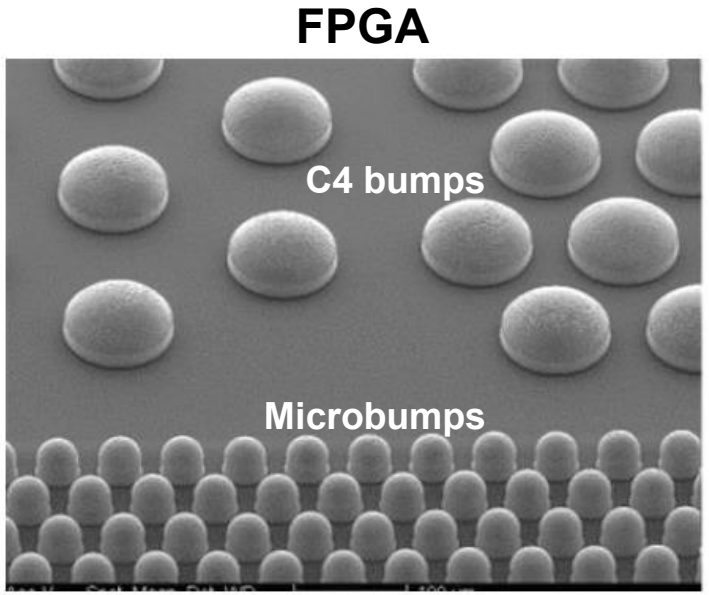
(c)

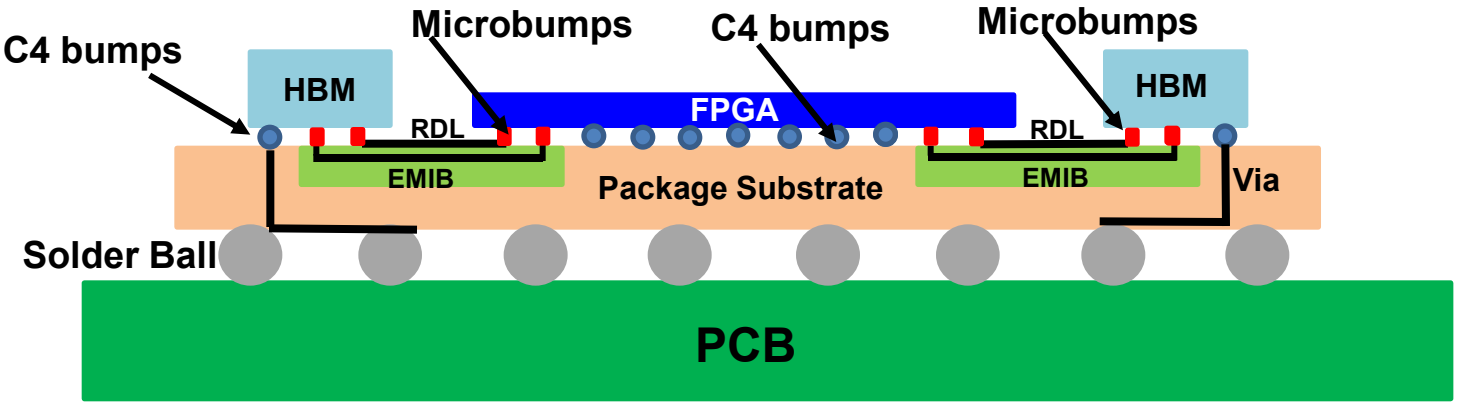


(d)

Heterogeneous Integration using Intel's EMIB and Altera's FPGA Technology

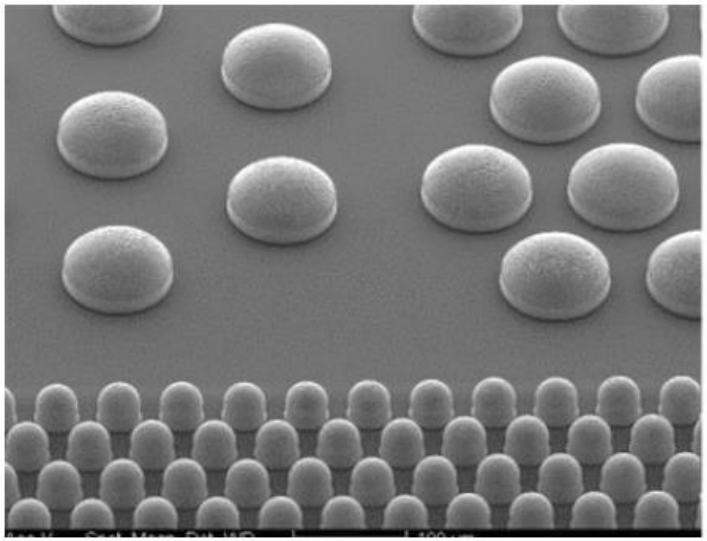




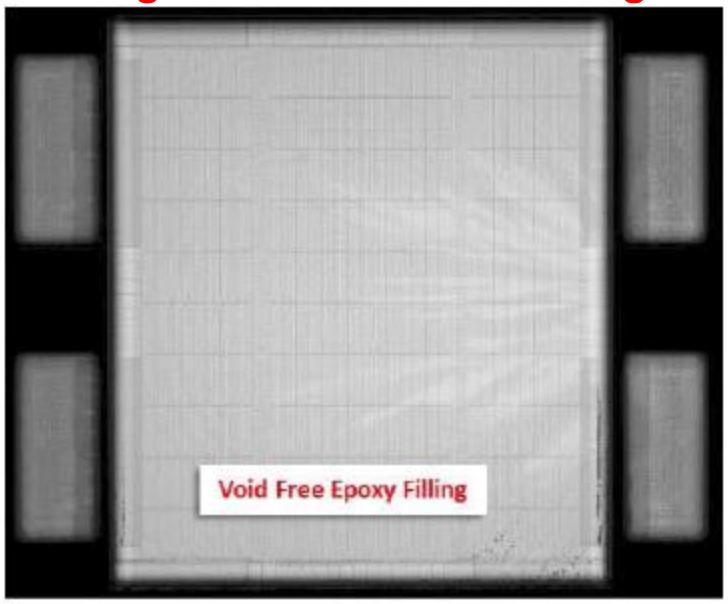


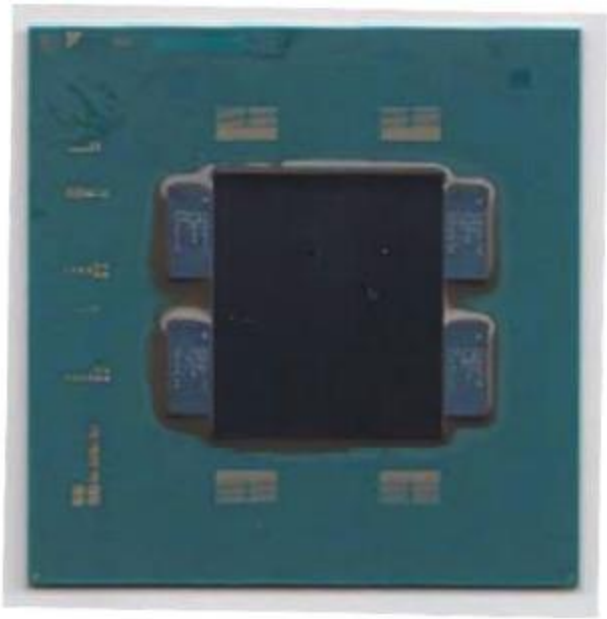
Intel/Altera, November 2015

Mixed CD/Mixed Pitch Bumps

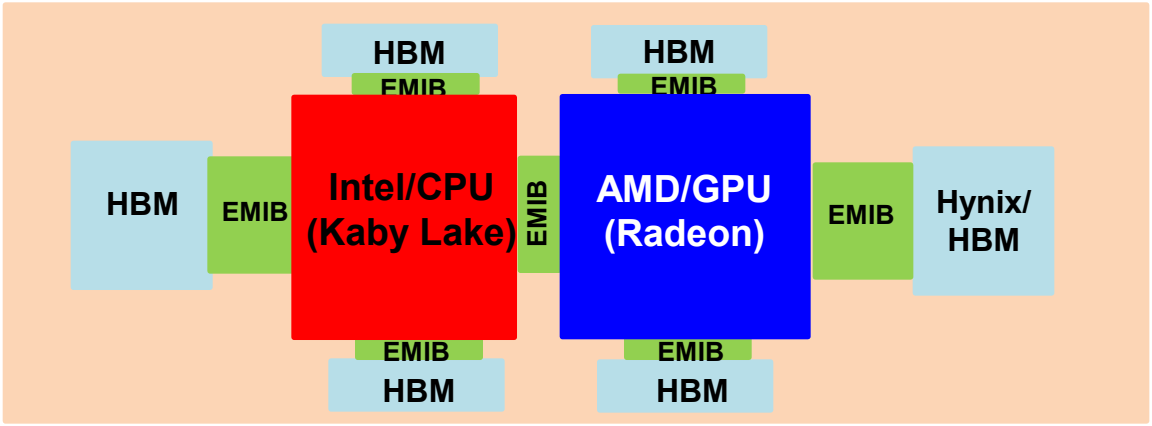


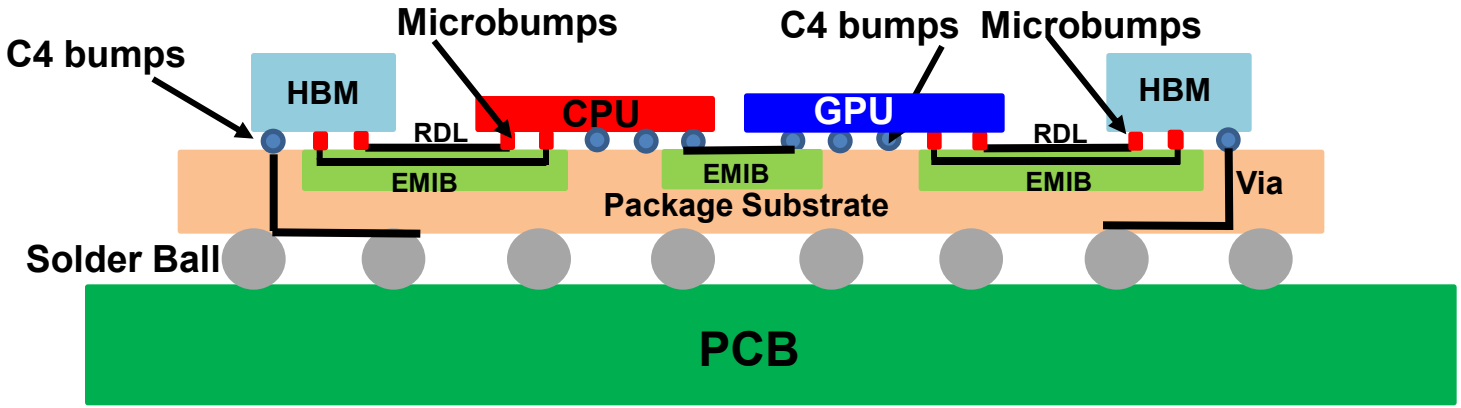
Fine pitch void-free filling has been accomplished through process and material enhancements. Image shows void-free filling for a 5-die MCP test vehicle with 4 bridges





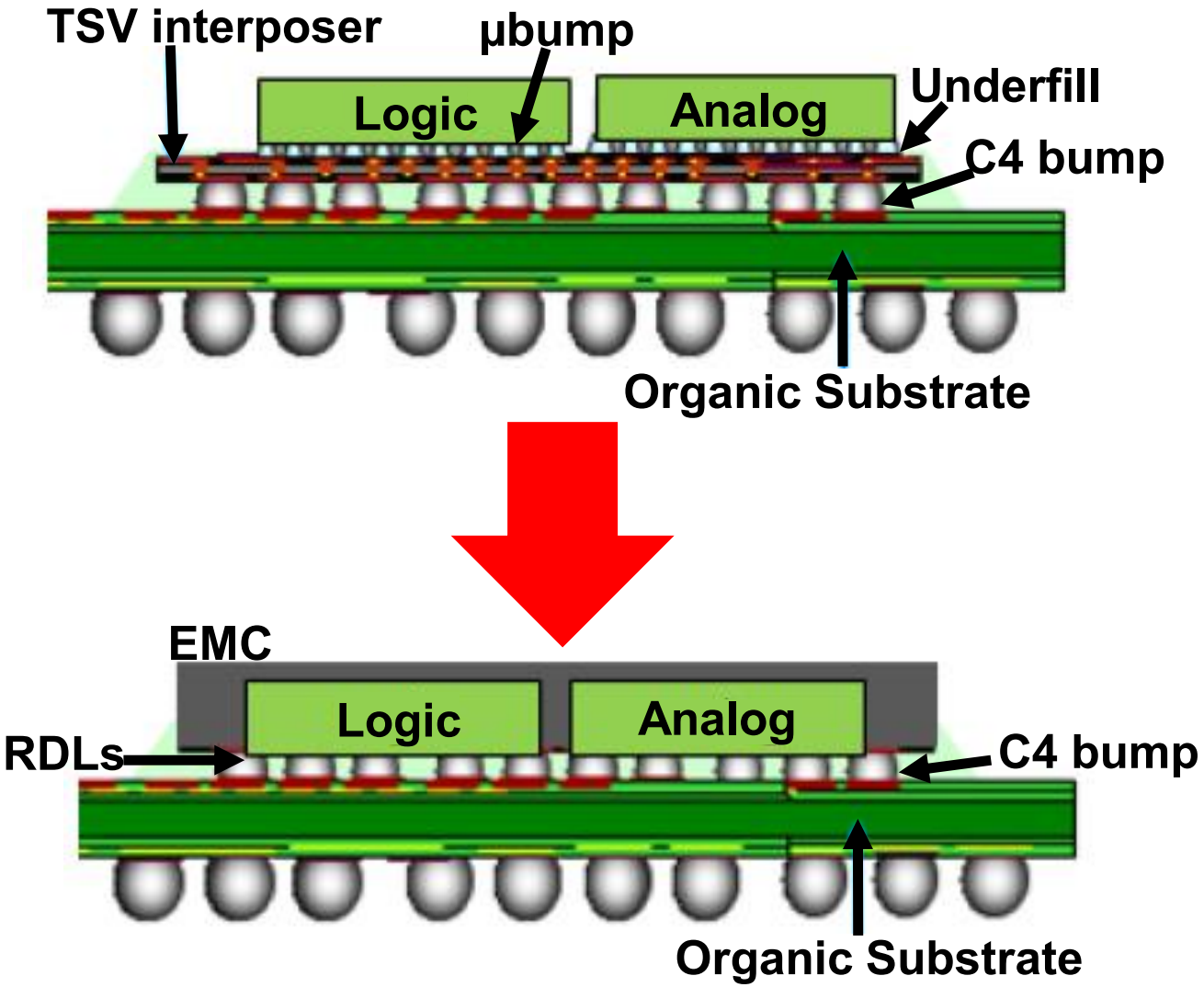
Intel/AMD/Hynix Heterogeneous Integration using Intel's EMIB





http://www.digitimes.com.tw/tw/dt/n/shwnws.asp?CnlID=1&Cat=10&id=493987&query=%A6%B3%A4F%AD%5E%AFS%BA%B8%A5%5B%AB%F9%A1A%B6W%B7L%B1N%B1o%A8%EC%A7%F3%A4j%AA%BA%A7U%A4O%B9%EF%A7%DCNVIDIA (2/20/2017)

Stats ChipPAC's TSV-less interposer – FOFC (Fan-out Flipchip)-eWLB



US 20130161833A1

(19) **United States**

(12) **Patent Application Publication**

Pendse

(10) **Pub. No.: US 2013/0161833 A1**

(43) **Pub. Date: Jun. 27, 2013**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF FORMING EXTENDED SEMICONDUCTOR DEVICE WITH FAN-OUT INTERCONNECT STRUCTURE TO REDUCE COMPLEXITY OF SUBSTRATE**

(75) Inventor: **Rajendra D. Pendse**, Fremont, CA (US)

(73) Assignee: **STATS CHipPAC, Ltd.**, Singapore (SG)

(21) Appl. No.: **13/336,860**

(22) Filed: **Dec. 23, 2011**

Publication Classification

(51) **Int. Cl.**

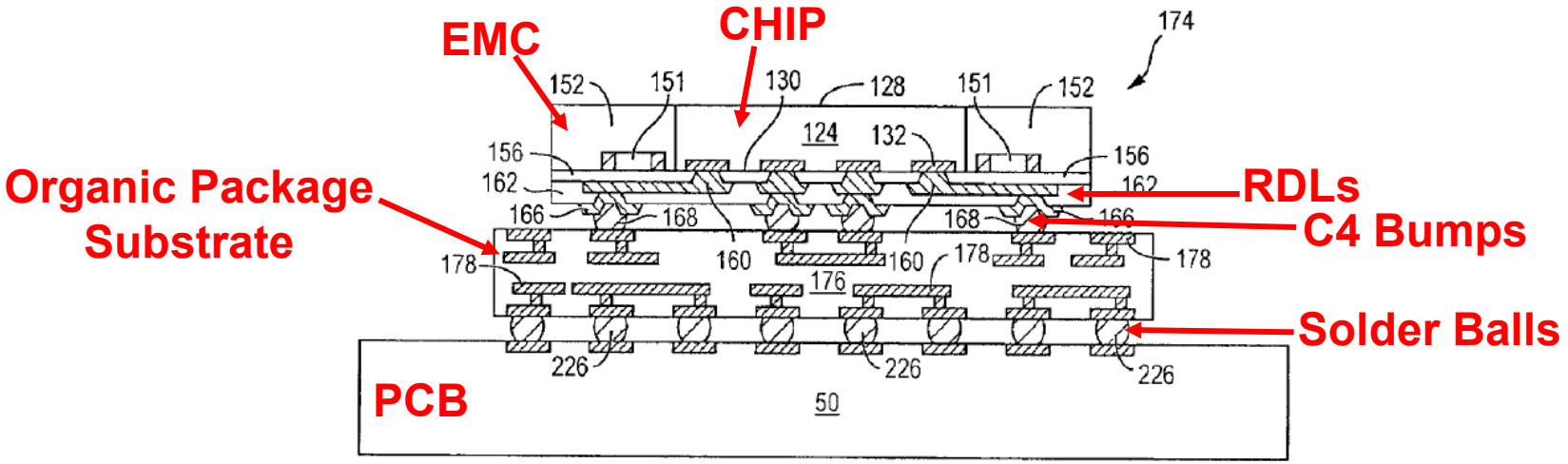
H01L 23/522	(2006.01)
H01L 21/56	(2006.01)
H01L 21/78	(2006.01)

(52) **U.S. Cl.**

USPC **257/777**; 438/113; 438/122; 438/124; 257/E23.142; 257/E21.502; 257/E21.599

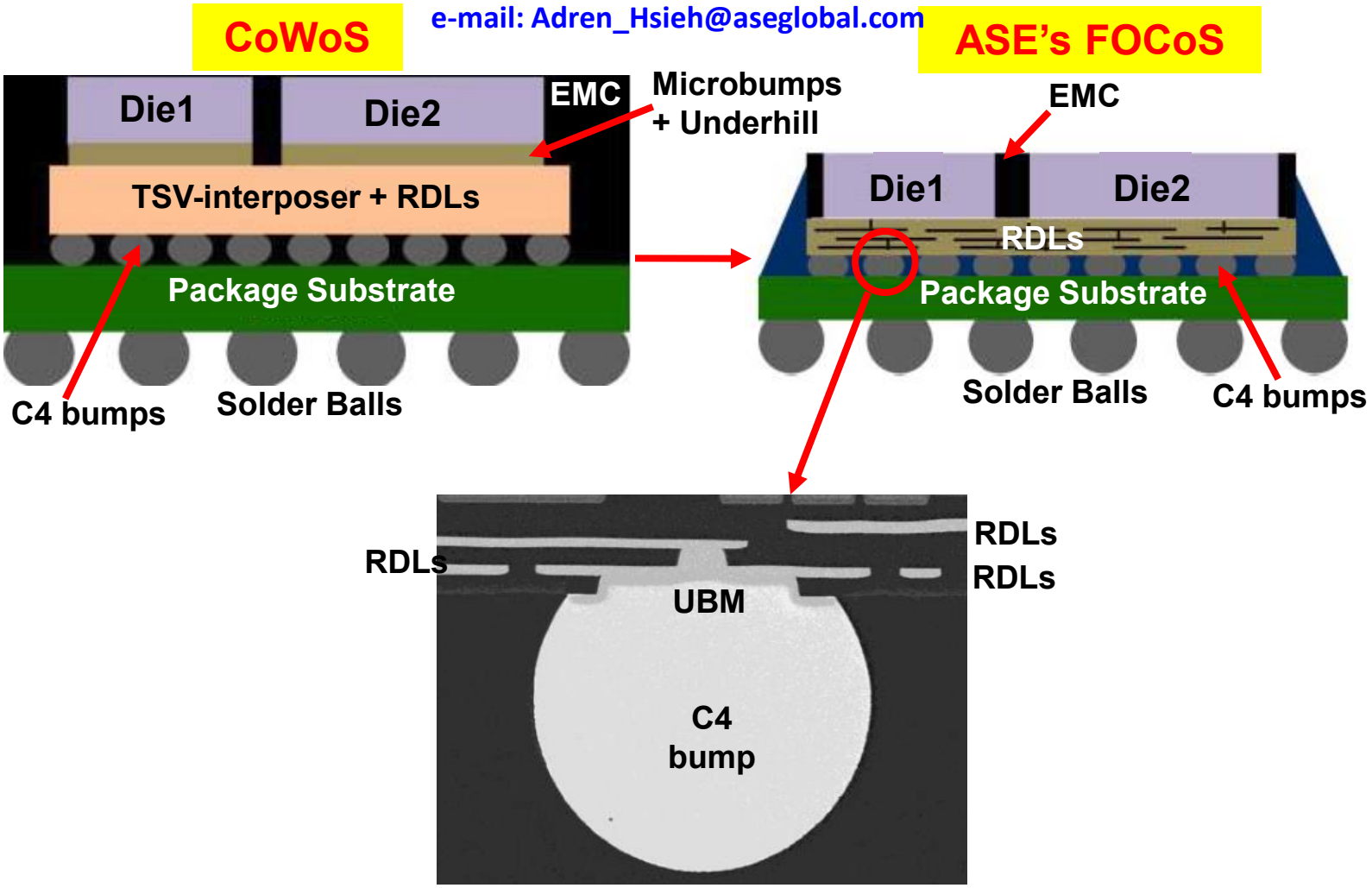
(57) **ABSTRACT**

A semiconductor device has a semiconductor wafer with a plurality of semiconductor die. Contact pads are formed on a surface of the semiconductor die. The semiconductor die are separated to form a peripheral region around the semiconductor die. An encapsulant or insulating material is deposited in the peripheral region around the semiconductor die. An interconnect structure is formed over the semiconductor die and insulating material. The interconnect structure has an I/O density less than an I/O density of the contact pads on the semiconductor die. A substrate has an I/O density consistent with the I/O density of the interconnect structure. The semiconductor die is mounted to the substrate with the interconnect structure electrically connecting the contact pads of the semiconductor die to the first conductive layer of the substrate. A plurality of semiconductor die each with the interconnect structure can be mounted over the substrate.



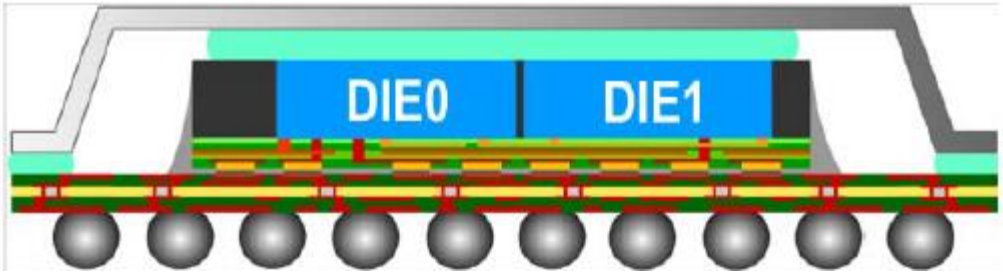
Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

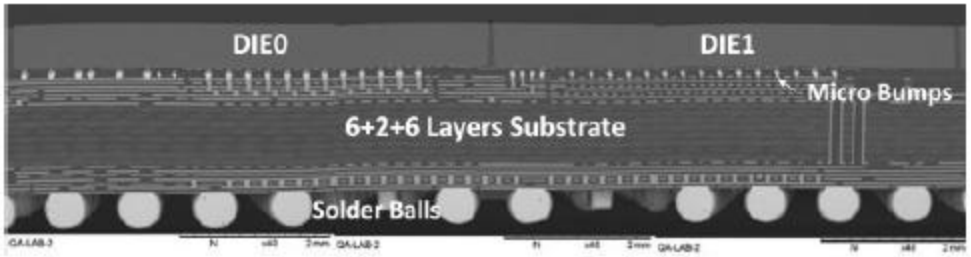
Yuan-Ting Lin, Wei-Hong Lai, Chin-Li Kao, Jian-Wen Lou,Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hseih*
Advanced Semiconductor Engineering (ASE), Inc.
Kaohsiung, Taiwan (ROC)
e-mail: Adren_Hsieh@aseglobal.com

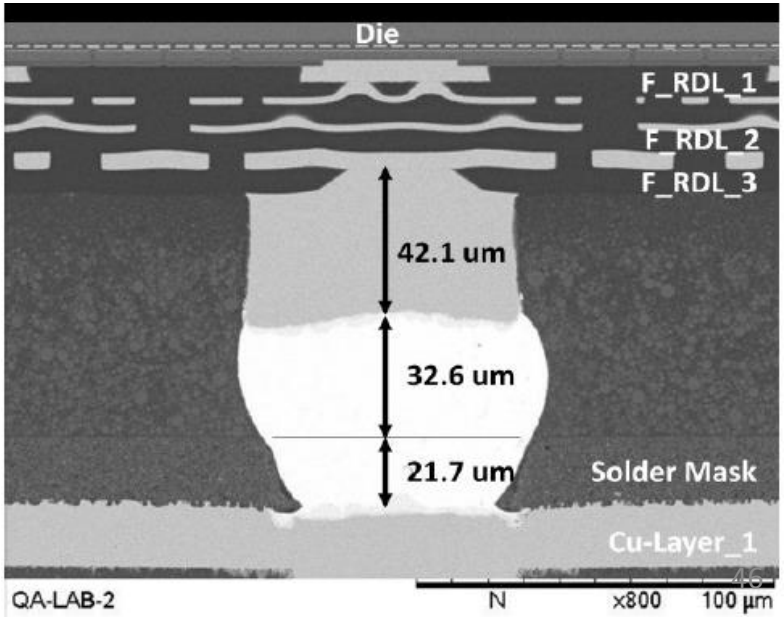


A Novel System in Package with Fan-out WLP for high speed SERDES application

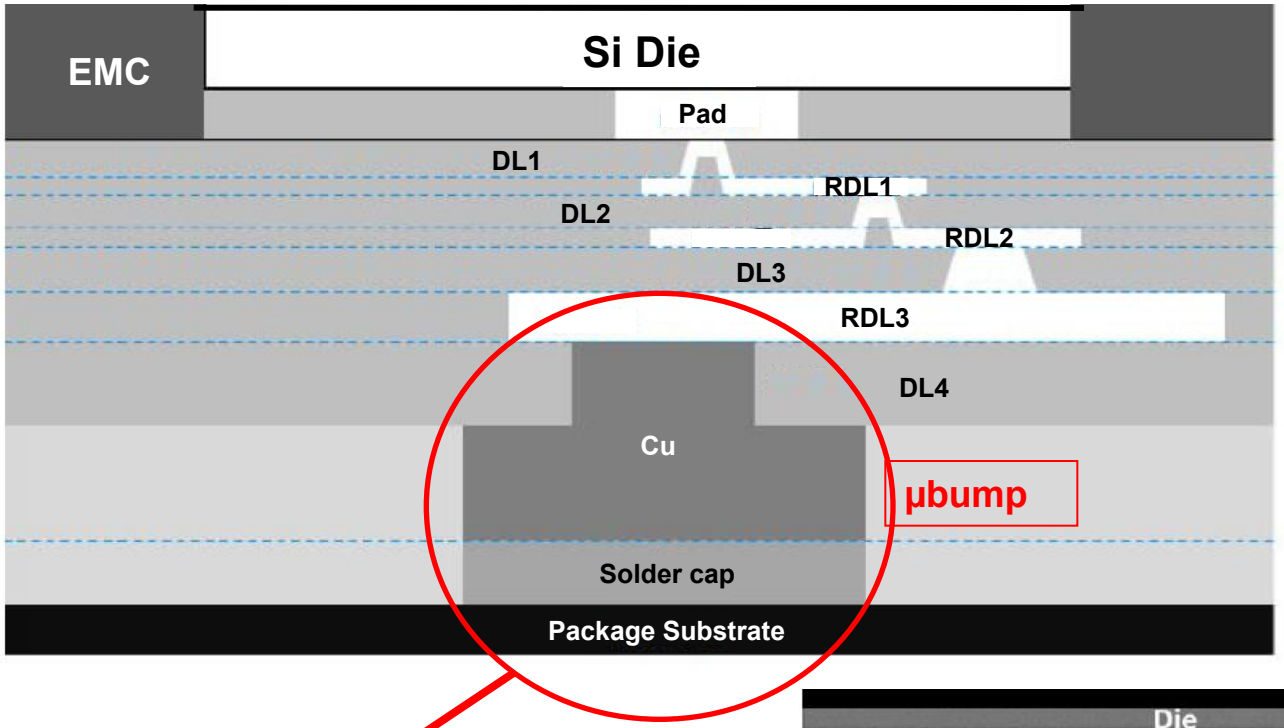
Nan-Cheng Chen, Tung-Hsien Hsieh, Jimmy Jinn, Po-Hao Chang, Fandy Huang,
JW Xiao, Alan Chou, Benson Lin
Mediatek Inc
Hsin-Chu City, Taiwan

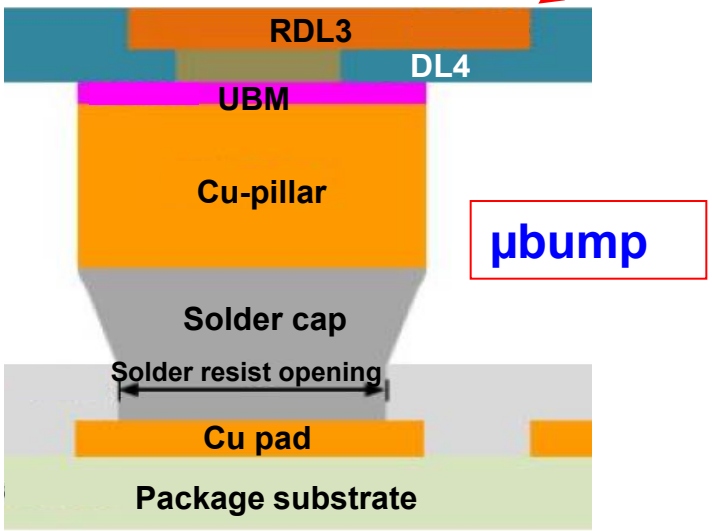


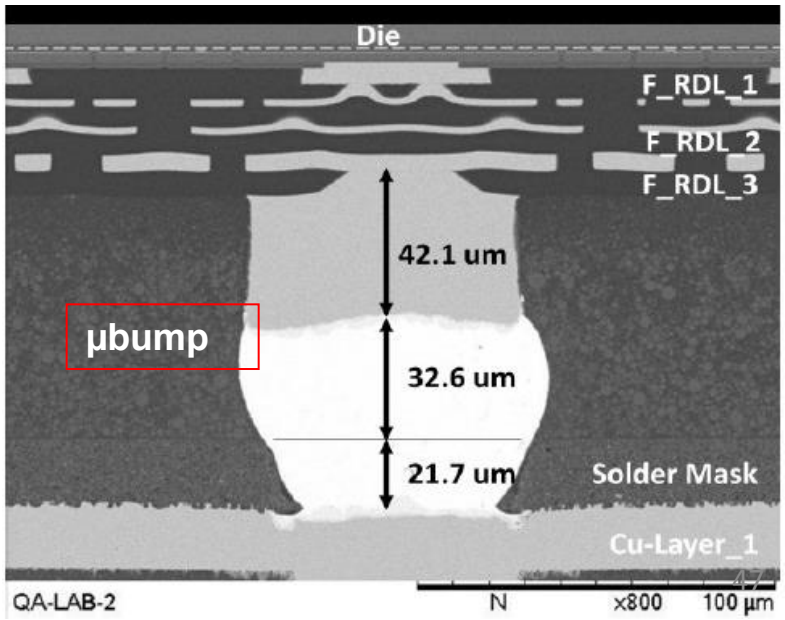




FOWLP carrier structure

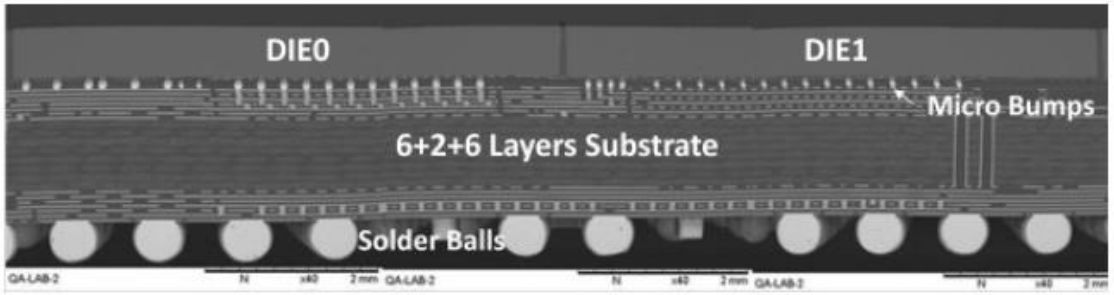




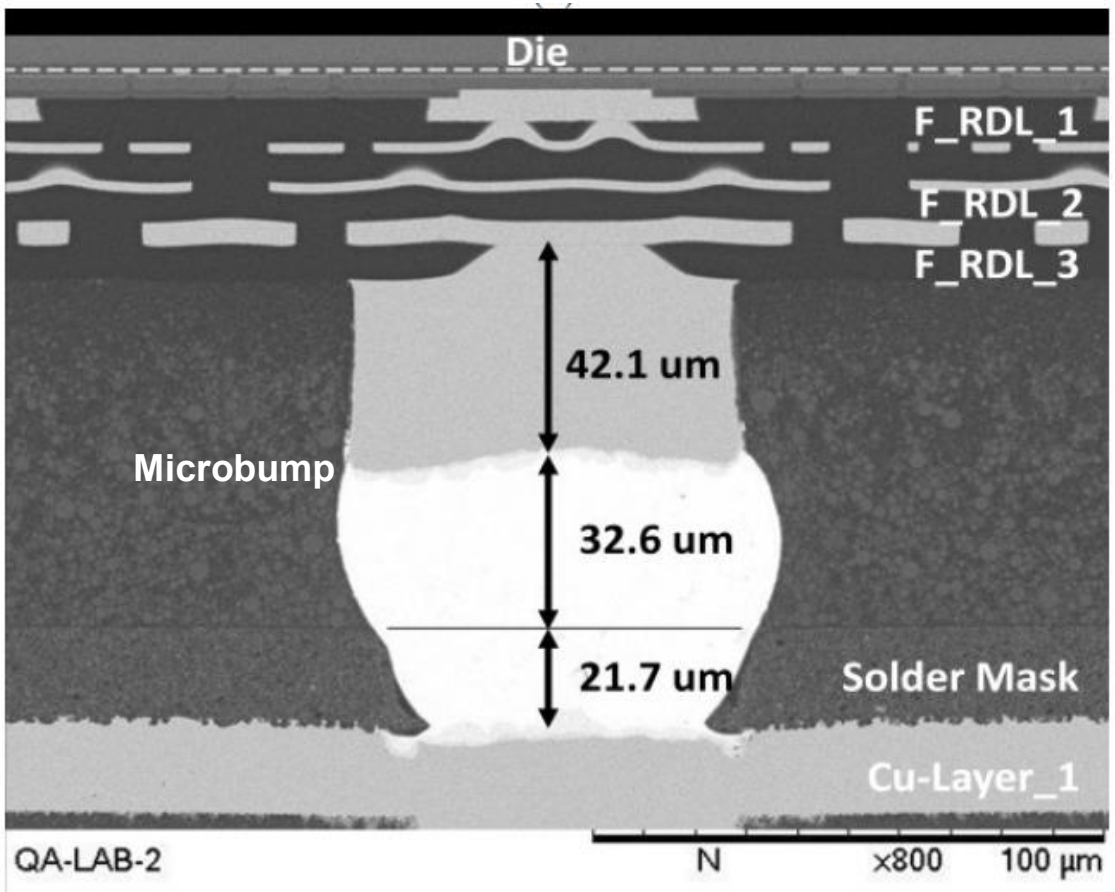


(a) Cross-section view of FOWLP, and (b) structure of micro bump connecting fan-out carrier and the BGA substrate.

(a)



(b)



PURPOSES

To present the recent advances and trends in the following semiconductor packaging technologies:

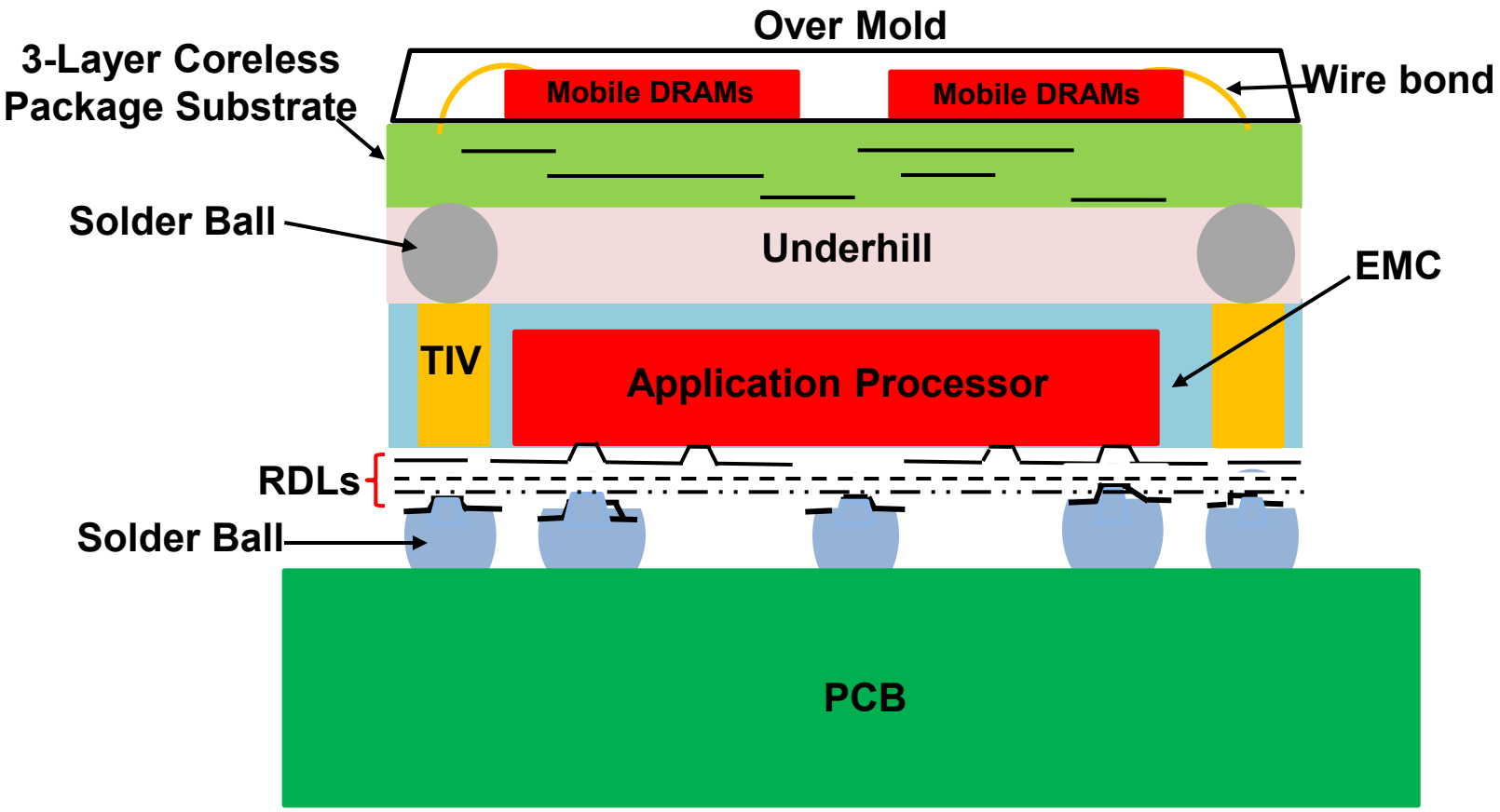
- **System-on-Chip (SoC)**
- **System-in-Package (SiP)**
- **Heterogeneous Integration**
- **Heterogeneous Integration on Organic Substrates**
- **Heterogeneous Integration on Silicon Substrates**
- **Heterogeneous Integration on RDLs**
- **FOWLP for 3D IC Heterogeneous Integration**

3D IC Heterogeneous Integration with FOWLP

- 3D IC Heterogeneous Integration for Application Processor Chipset
- 2D IC Heterogeneous Integration for Application/Graphic Processor Chipset

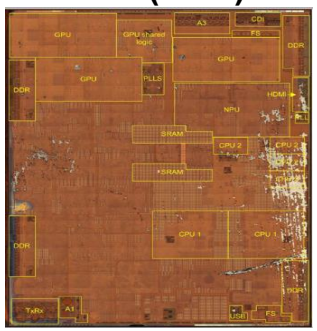
3D IC Heterogeneous Integration for Application Processor Chipset

Pop for packaging the application processor and mobile memory



Pop for the Mobile DRAMs and Application Processor of iPhone X/8/8+

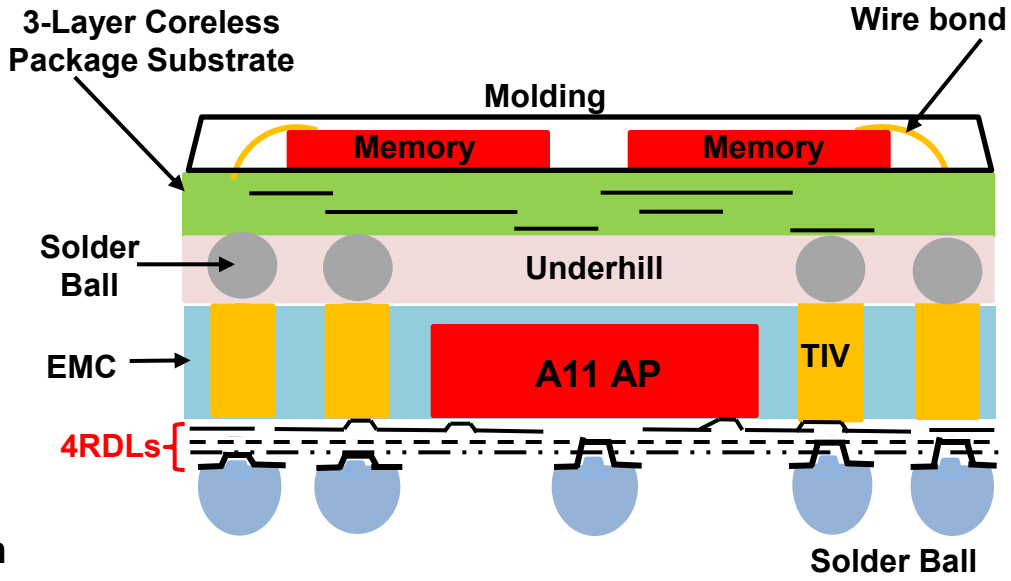
A11 (SoC)

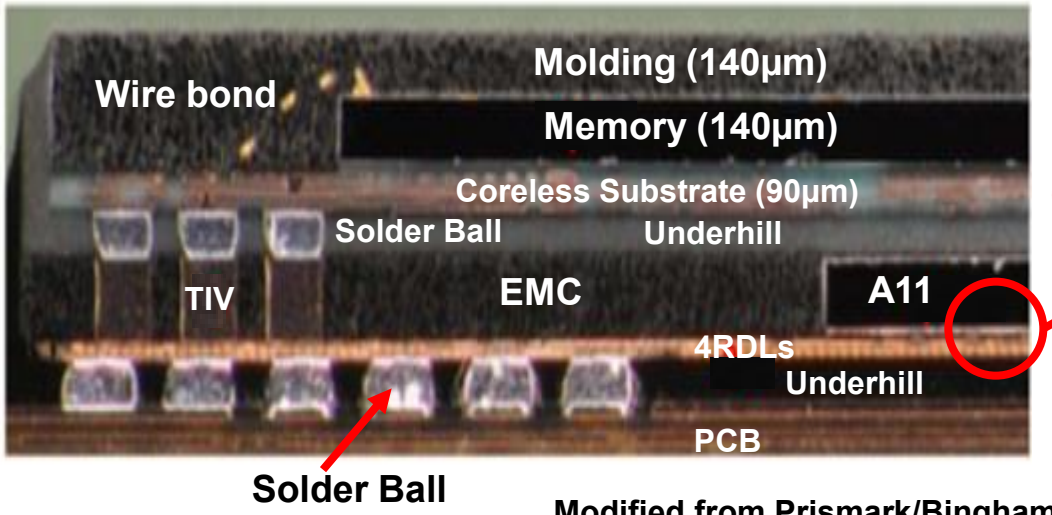


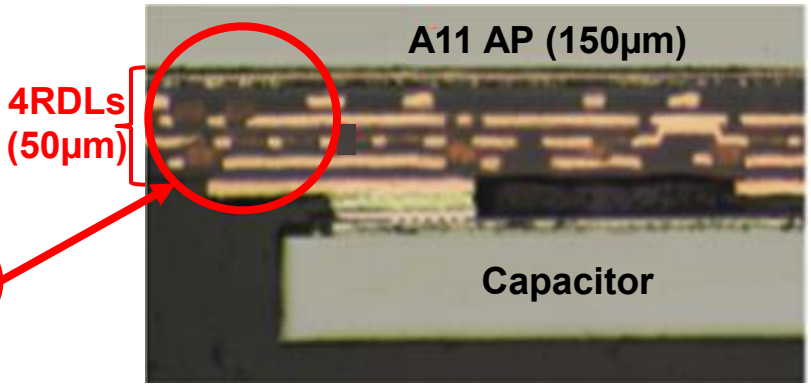
10mmx8.7mmx165μm

Pop

13.9mmx14.8mmx790mm

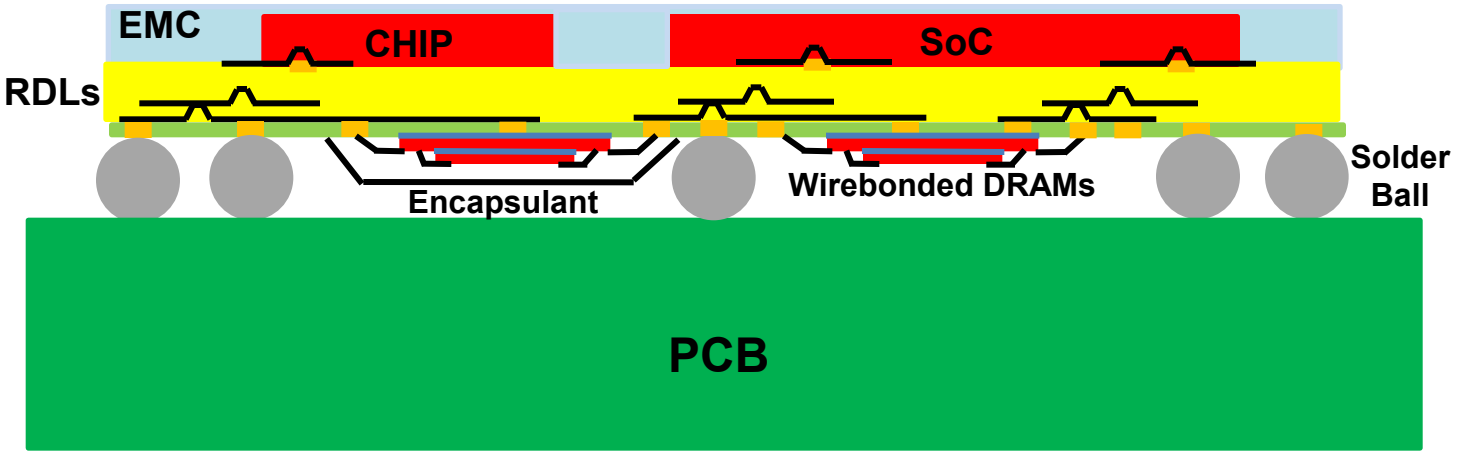




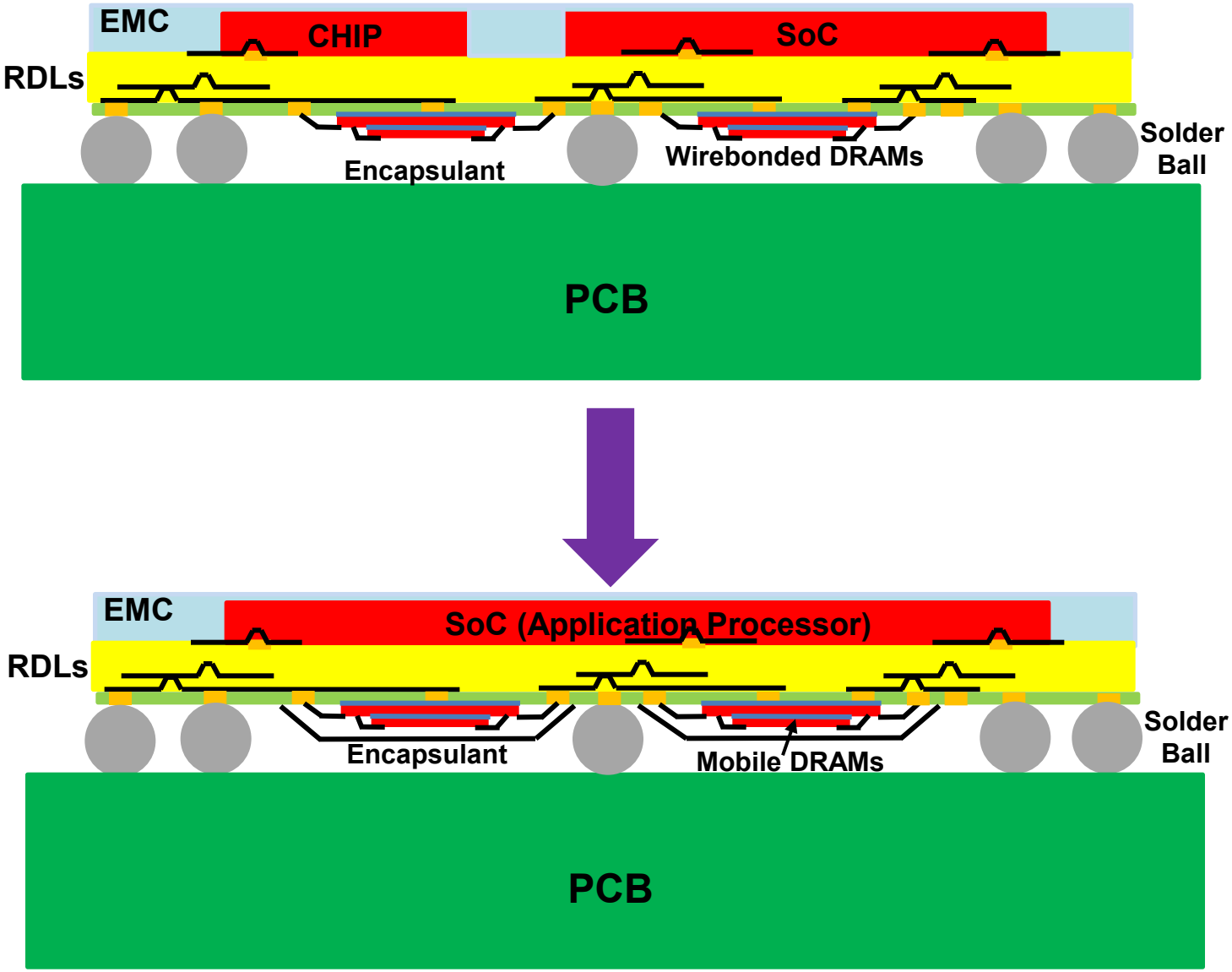


Modified from Prismark/Binghamton University

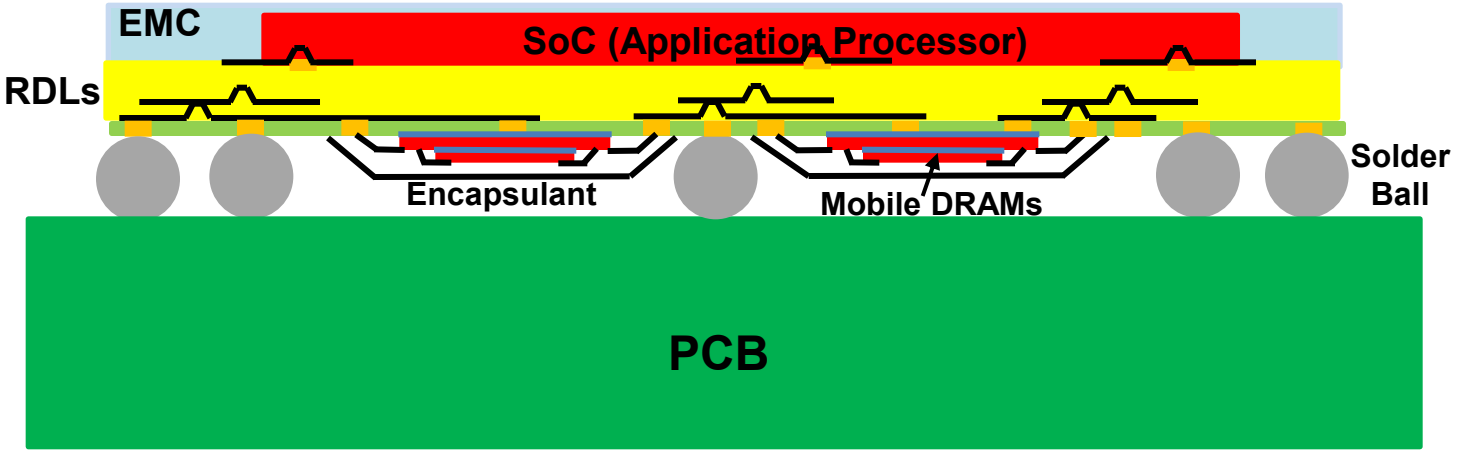
3D IC heterogeneous integration by FOWLP

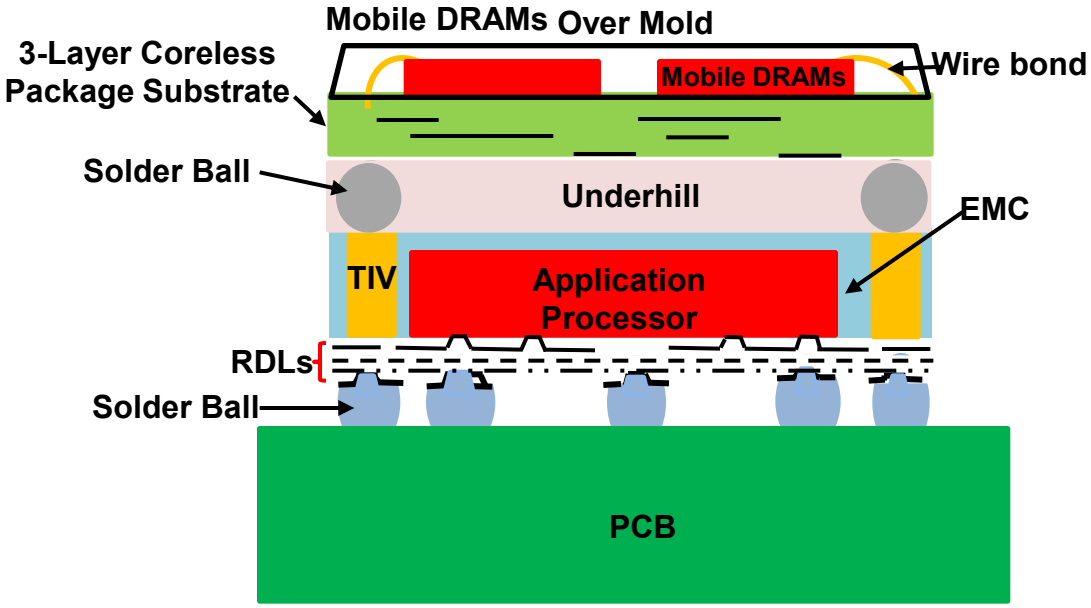


3D IC heterogeneous integration to package the application processor chipset



Application Processor Chipset: Pop vs. 3D IC Heterogeneous Integration



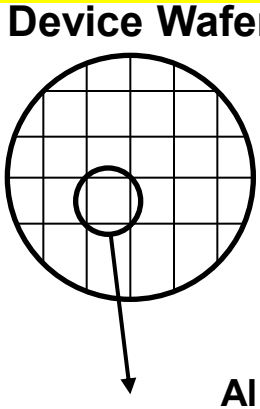


Advantages:

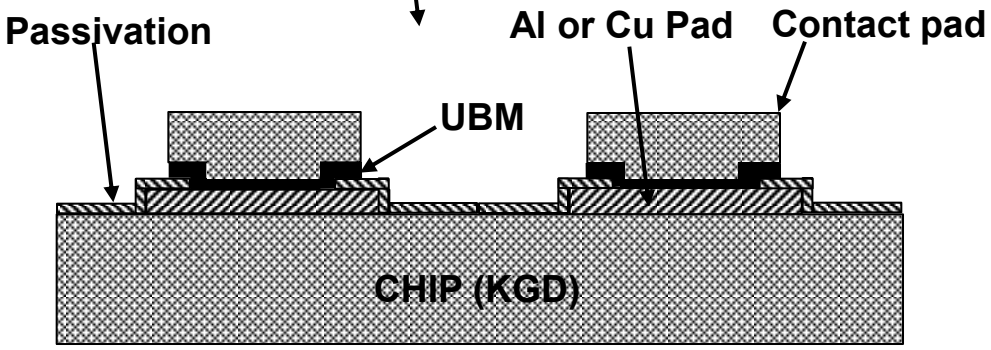
- Lower package profile
- Less interconnects
- More reliable because of less interconnects
- Better electrical performance
- Lower cost.

FOWLP: Chip-First (Face-up)

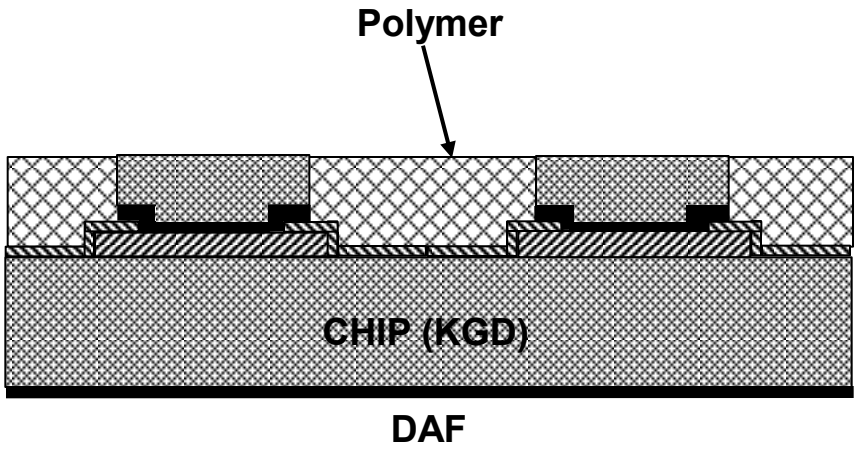
Test for KGD



Sputter UBM and electroplate Cu contact pad



Polymer on top, die-attach film (DAF) on bottom of device wafer, and dice the wafer



FOWLP: Chip-First (Face-up)

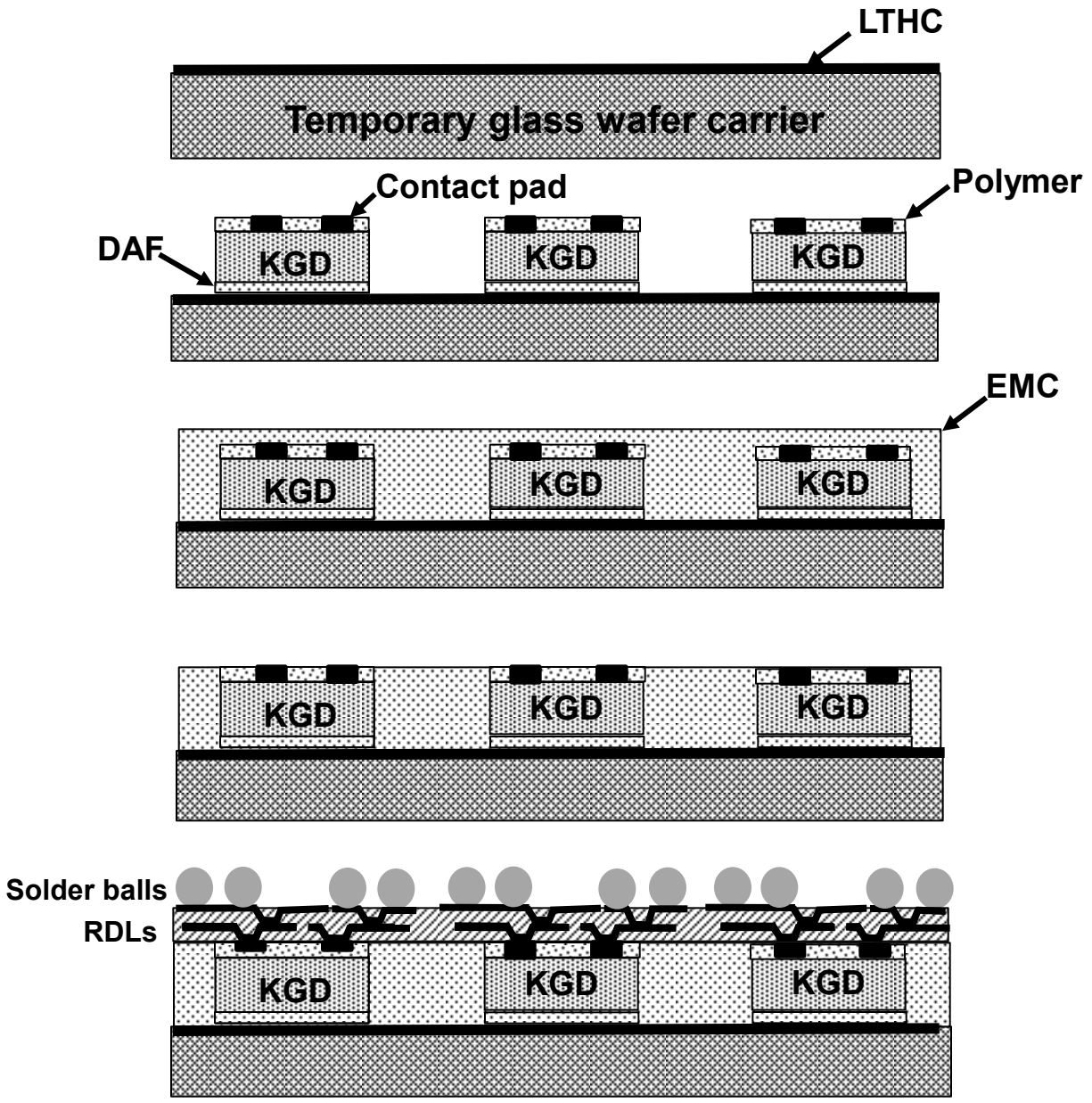
Coated with a light-to-heat conversion (LTHC) release layer

Place KGD (chip) face-up

Compression mold the EMC on the reconfigured carrier

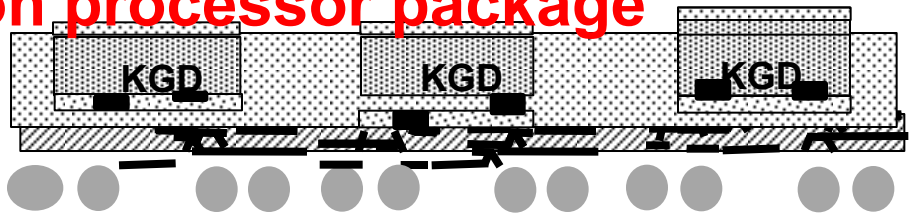
Backgrind the EMC and polymer to expose the contact pad

Build RDLs on contact pads and then mount solder balls

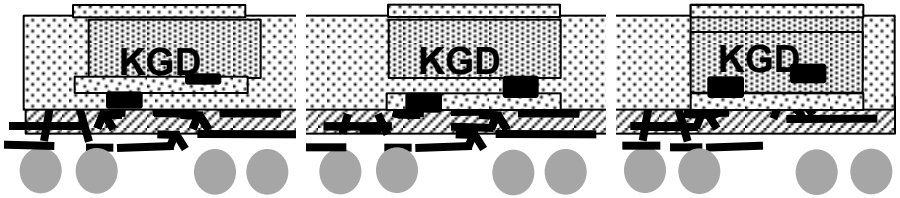


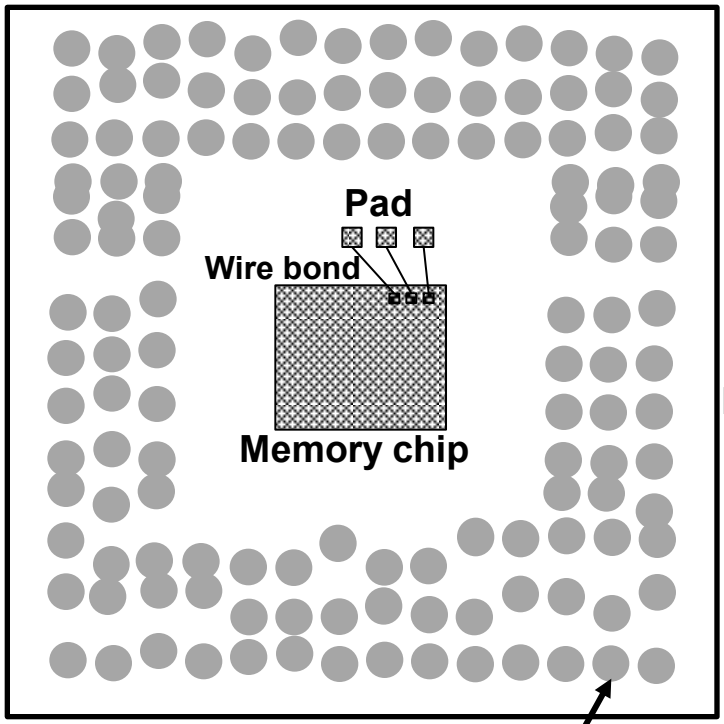
Wire bonding memory chip at the bottom of individual application processor package

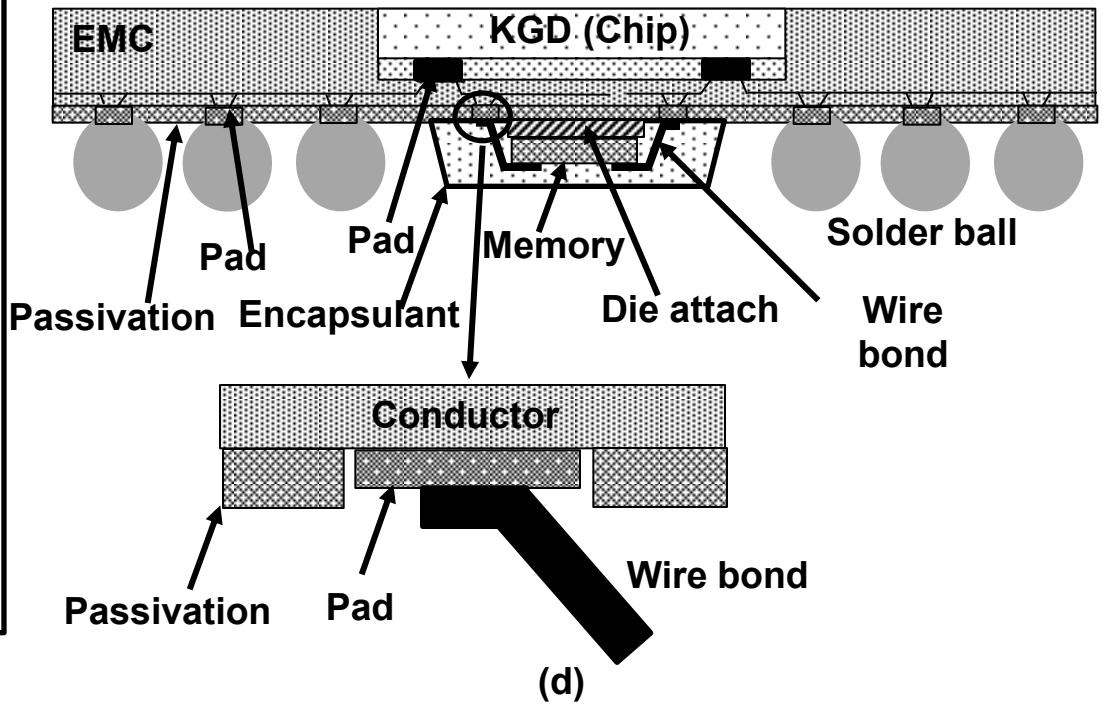
(a) Remove the glass carrier by a laser



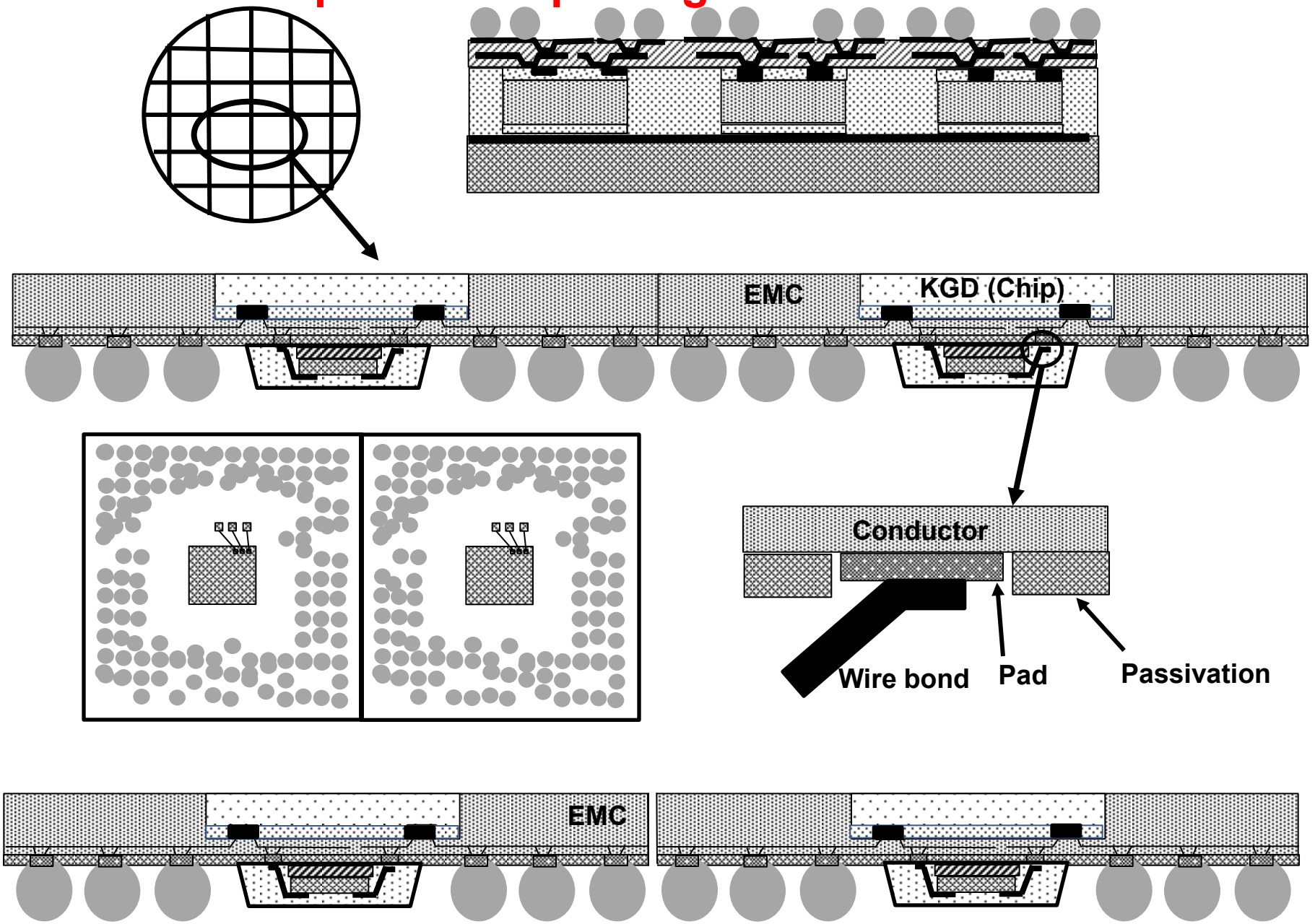
(b) Dice the molded wafer into individual package



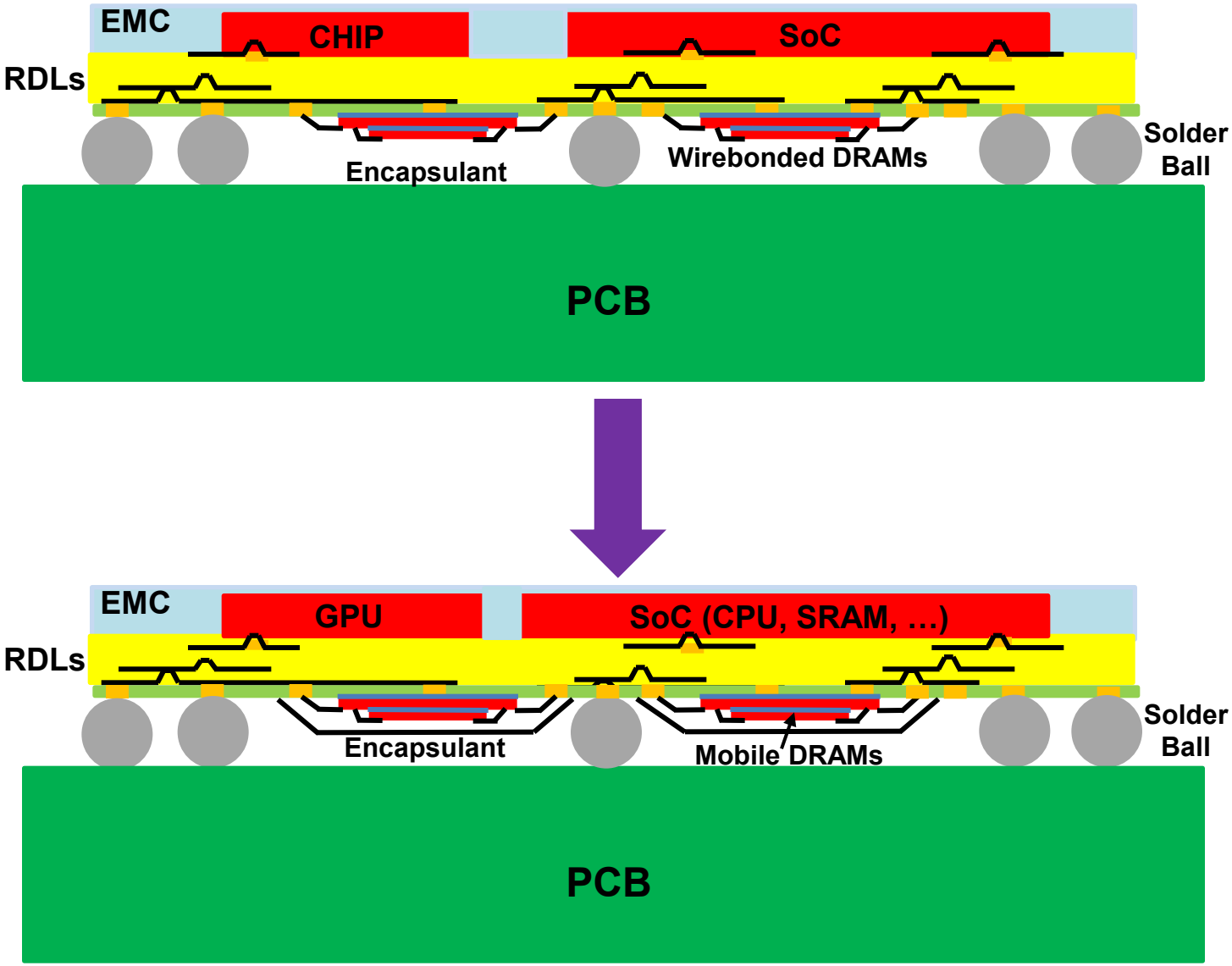




Wire bonding memory chip at the bottom of application processor package on a wafer

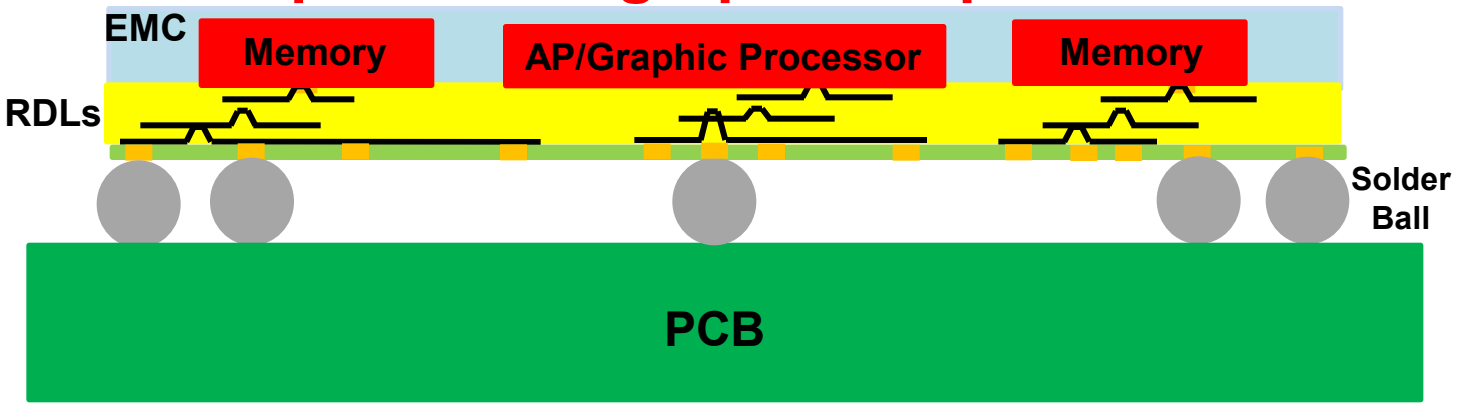


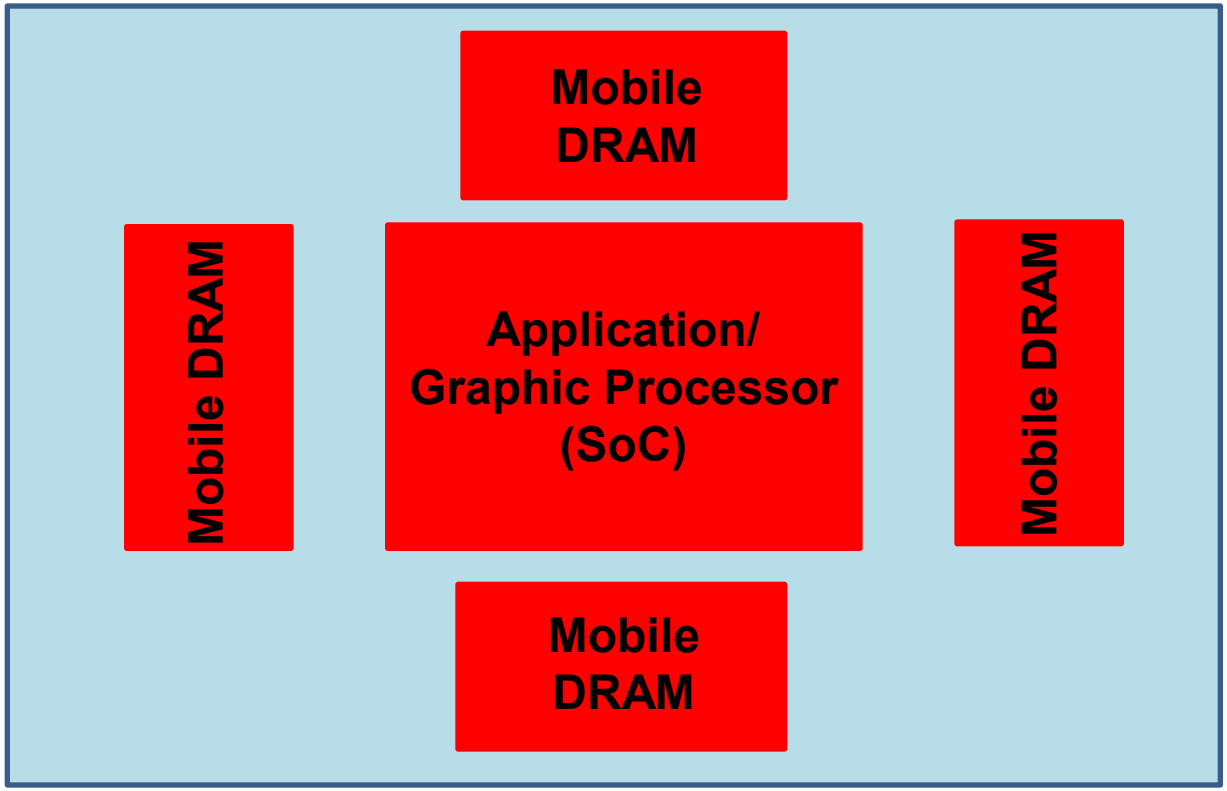
3D IC heterogeneous integration to package the application processor chipset



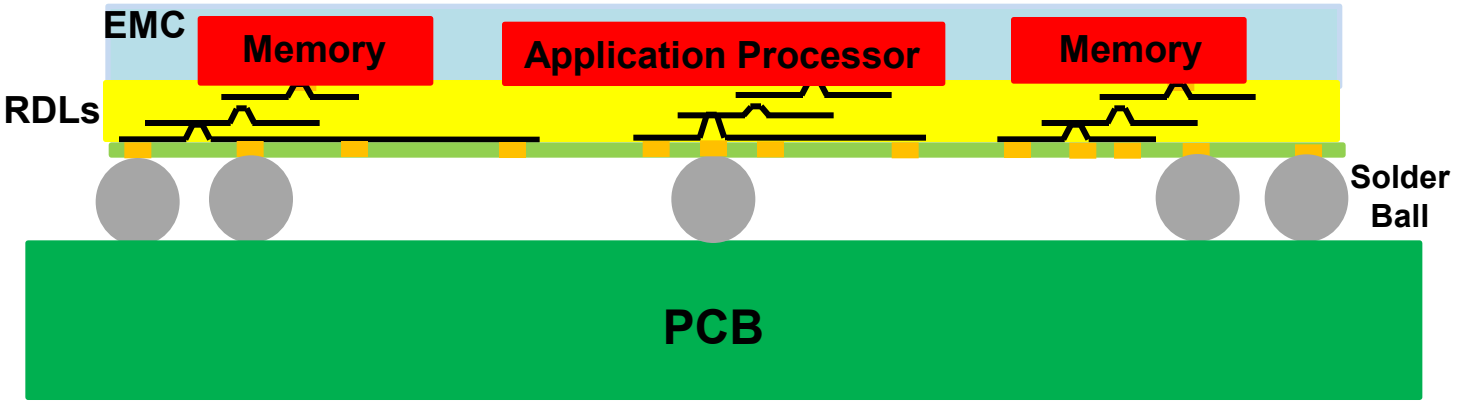
2D IC Heterogeneous Integration for Application/Graphic Processor Chipset

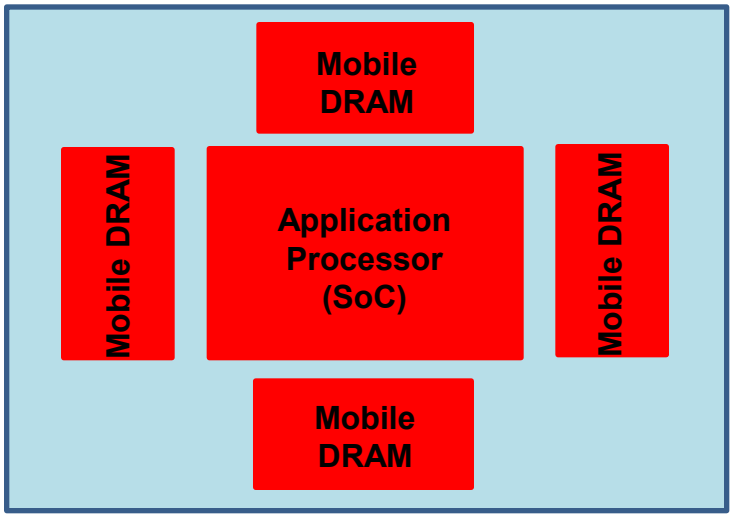
2D IC heterogeneous integration to package the application processor/graphic chipset

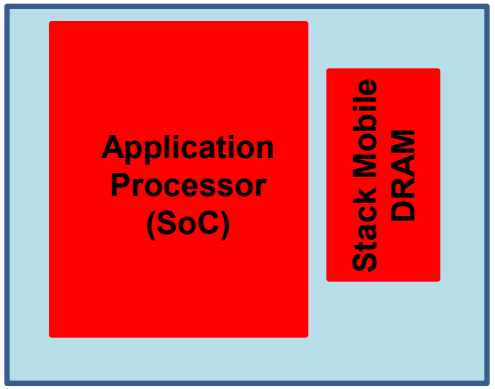




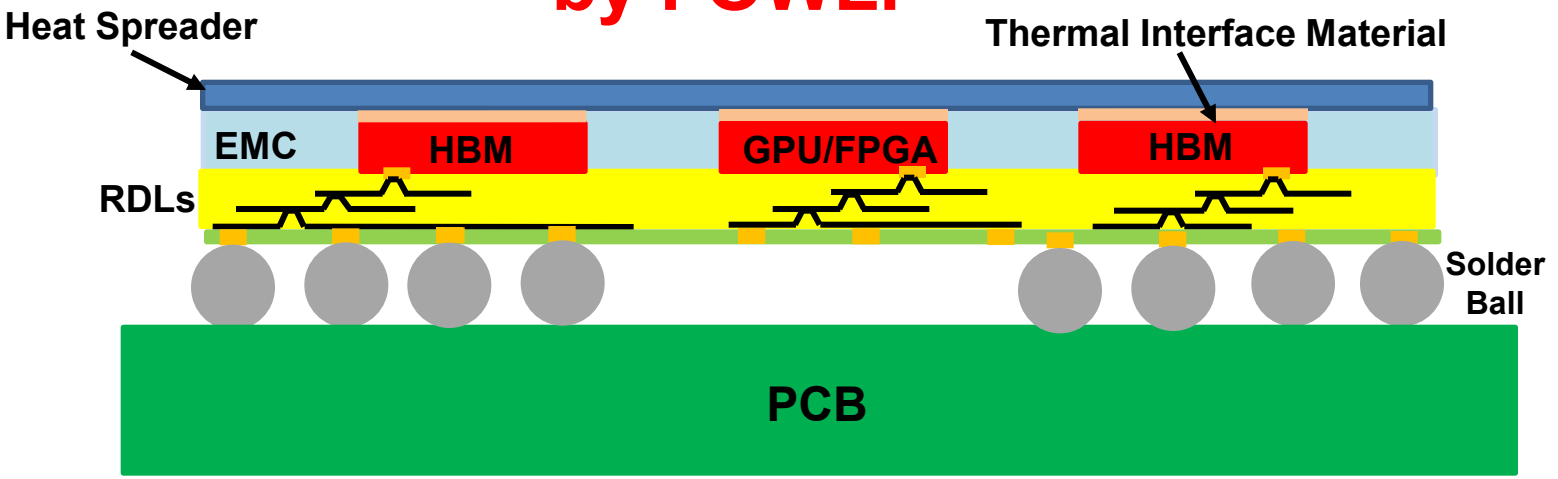
FOWLP for Application Processor Chipset and High Bandwidth Server/Network

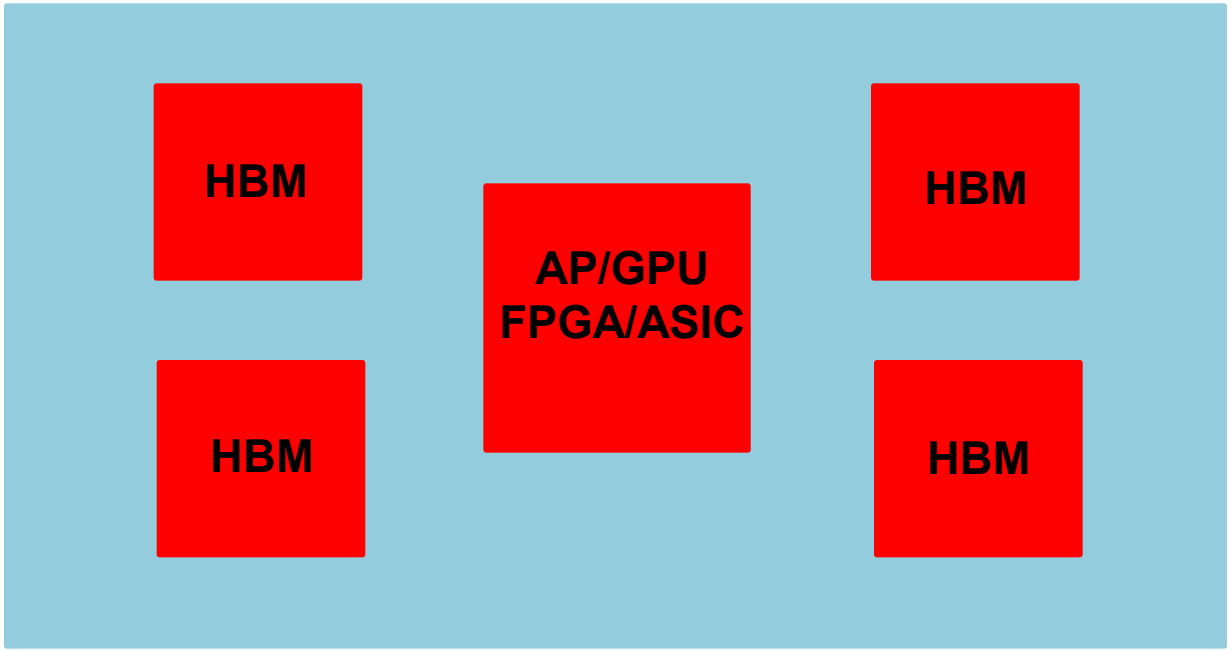






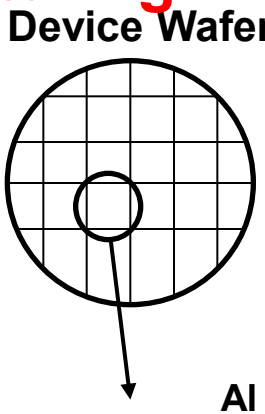
3D IC high-performance heterogeneous integration by FOWLP



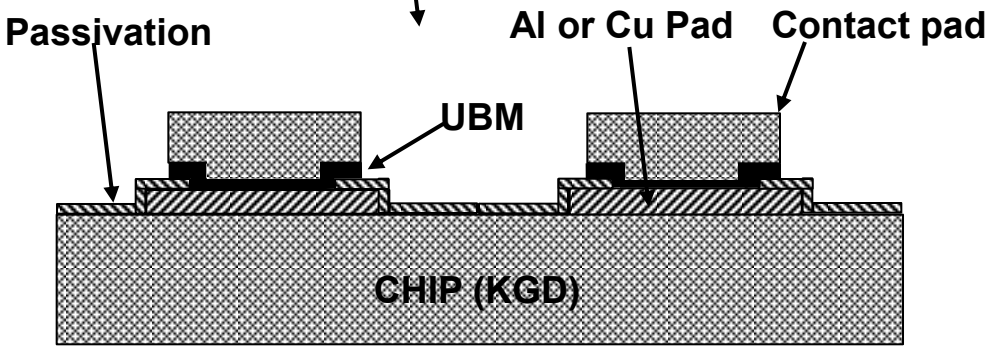


3D IC High-Performance Heterogeneous Integration by FOWLP Manufacturing Process

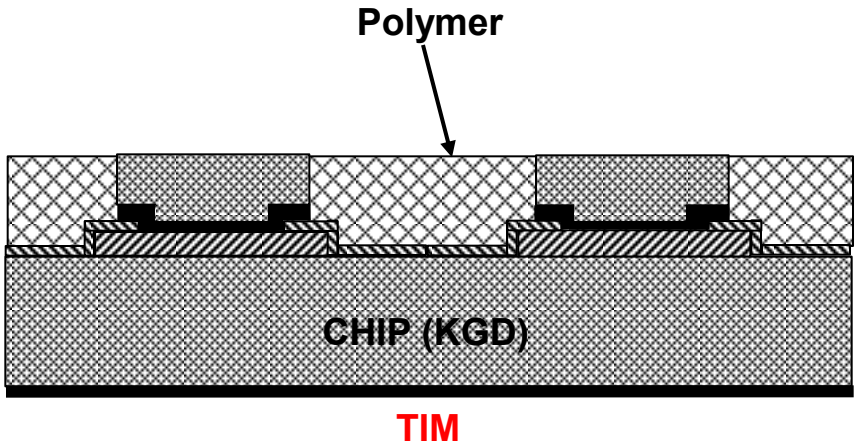
Test for KGD



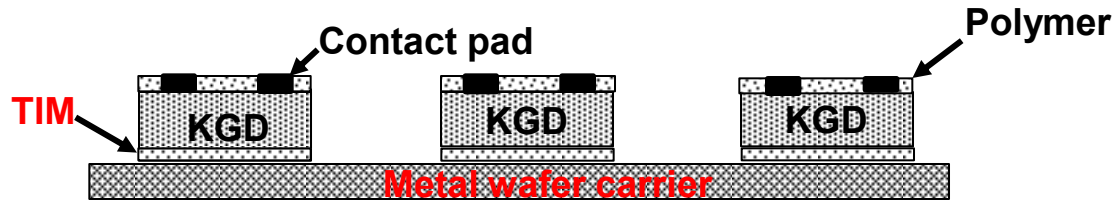
Sputter UBM and electroplate Cu contact pad



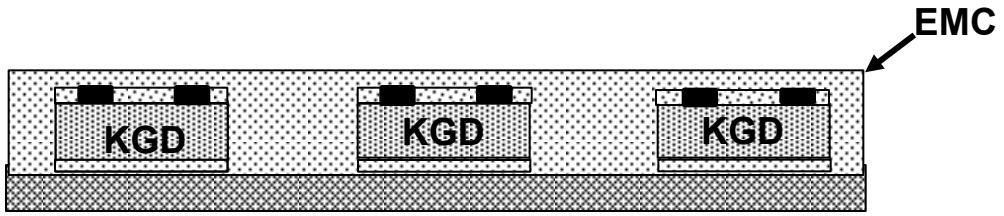
Polymer on top and thermal interface material (TIM) on bottom of the device wafer, and dice the wafer



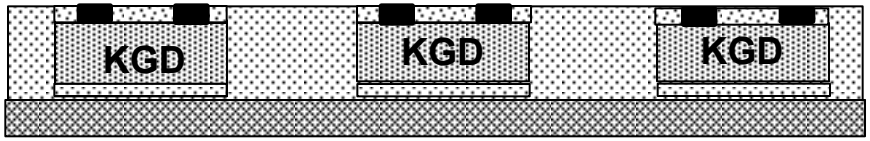
Place KGD (chip) face-upon on a metal wafer carrier



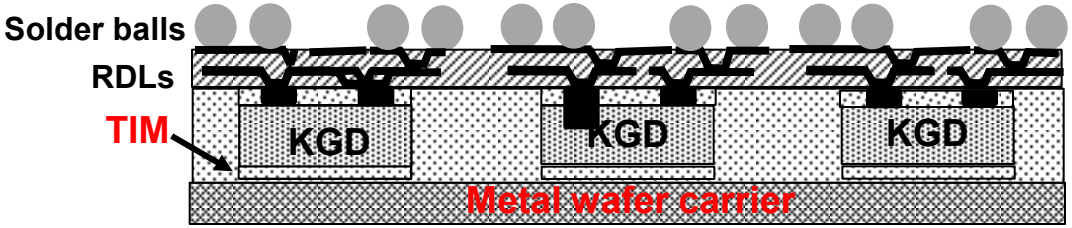
Compression mold the EMC on the reconfigured carrier



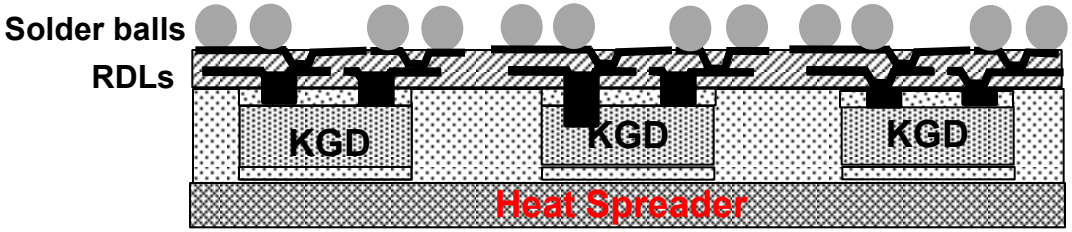
Backgrind the EMC and polymer to expose the contact pad



Build RDLs on contact pads and then mount solder balls



Dice the reconstituted wafer with the metal carrier into individual package. The metal carrier becomes the heat spreader



Advantages of the New Proposal

Traditional Method

- Laminate a LTHC layer on a glass carrier.
- Laminate a DAF on the device wafer and singulate the wafer.
- P&P the chip face-up on the glass carrier.
- Molding and PMC.
- Backgrind the EMC to expose the contact-pads of the chips.
- Build RDLs.
- Ball mounting.
- Remove the carrier (debonding).
- Dicing into individual package.
- Thermal interface material (TIM).
- Heat Spreader attach

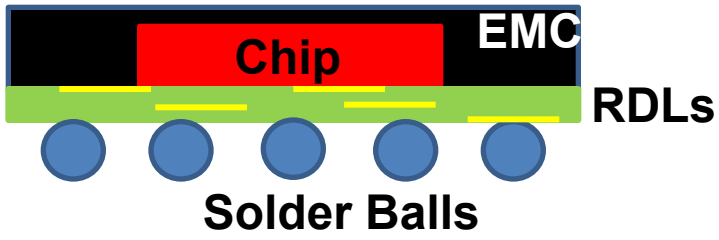
New Method

- Laminate a thermal interface material (TIM) on the device wafer and singulate the wafer.
- P&P the chip face-up on the metal carrier.
- Molding and PMC.
- Backgrind the EMC to expose the contact-pads of the chips.
- Build RDLs.
- Ball mounting.
- Dicing into individual package.

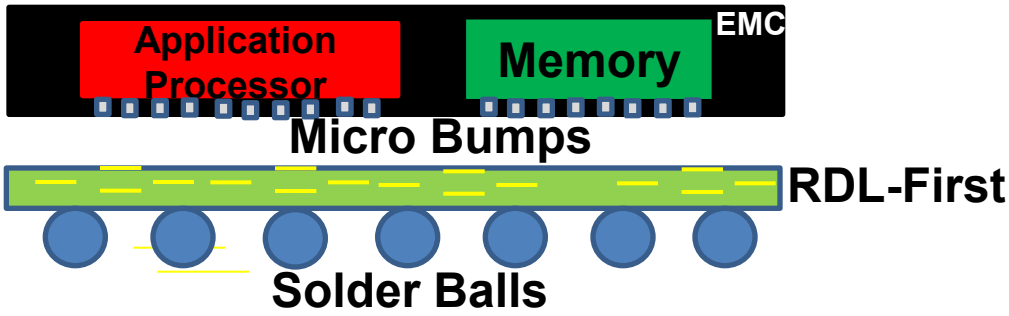
- Lower cost
- Less process steps
- Higher yield process

Samsung's Roadmap

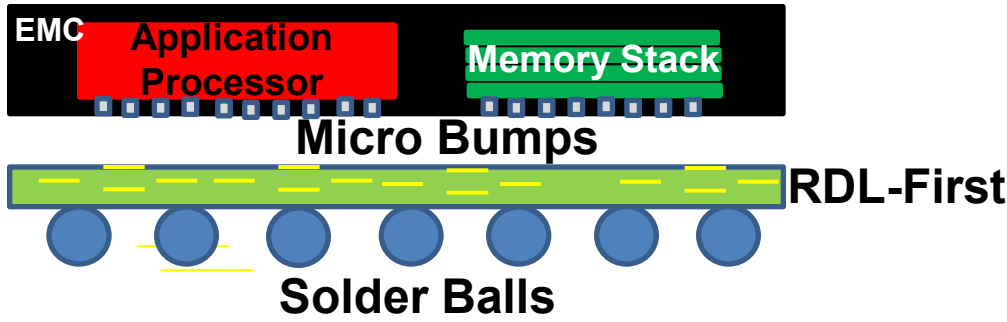
ePLP (Chip-First) — Production (Soon)

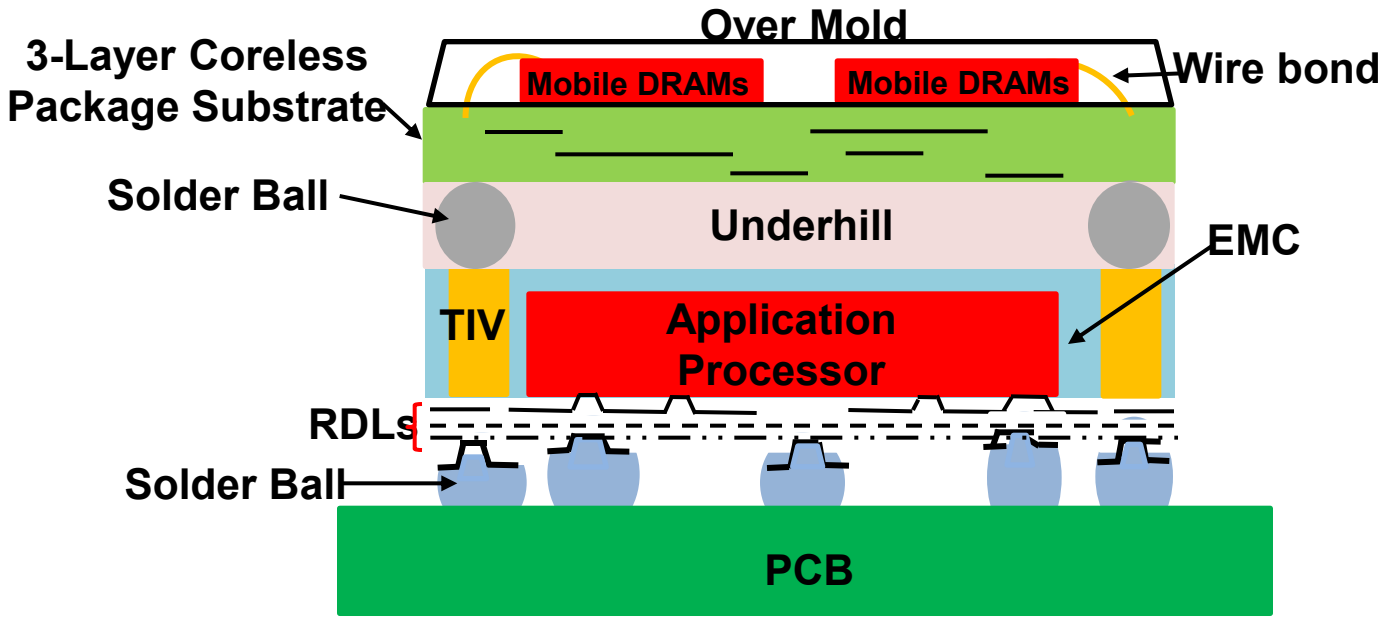


PLP-m (Chip-Last) — Production (2018 Q4)



PLP-m (Chip-Last) — Production (2020)

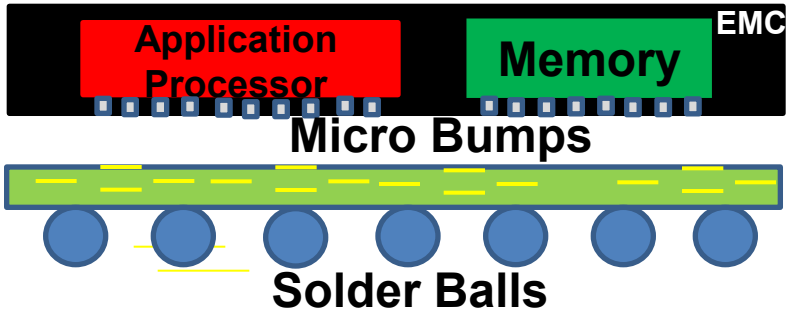




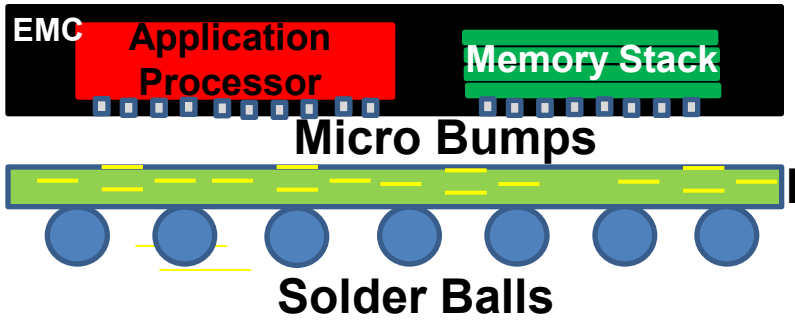
Application Processor Chipset: Pop is going to be Disappeared

PLP-m (Chip-Last)

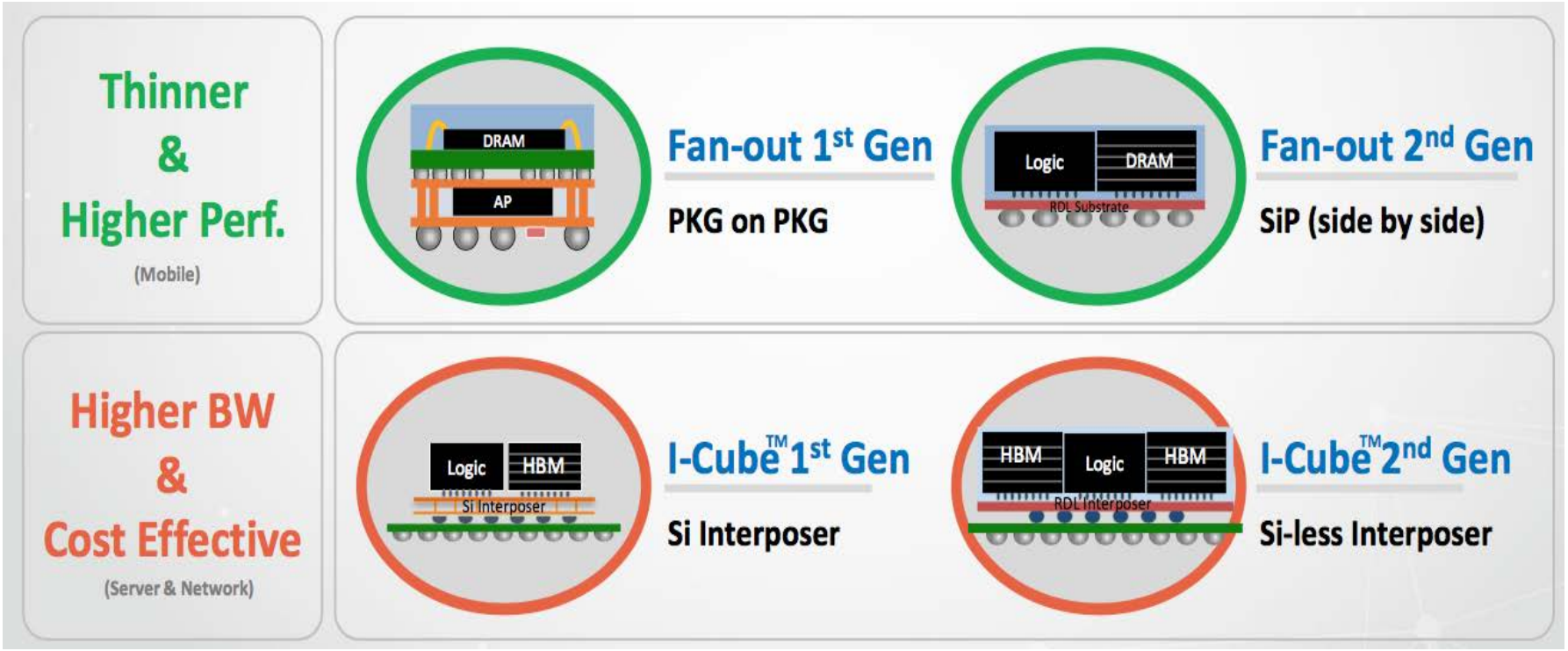
Production (2018 Q4)



Production (2020)



Samsung FOWLP for Application Processor Chipset and High Bandwidth Server/Network



Source: Samsung

SUMMARY

For the next few years, we will see more of a higher level of heterogeneous integration, whether it is for:

- **time-to-market**
- **performance**
- **form factor**
- **power consumption**
- **cost**
- **etc.**

on high-end applications such as:

- **high-end smartphones, tablets, wearables**
- **networkings**
- **telecommunications**
- **supper computings**
- **big data/cloud computing**
- **etc.**

The trends will be toward to finer pitch (≤ 50μm) and higher density.

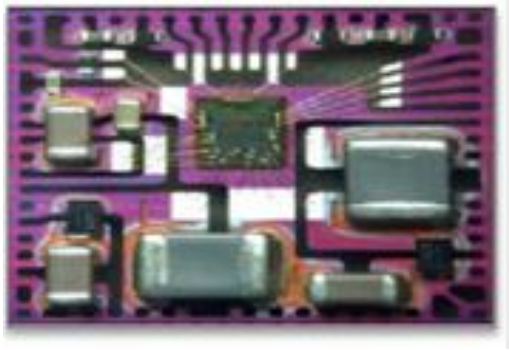
PURPOSES

To present the recent advances and trends in the following semiconductor packaging technologies:

- **System-on-Chip (SoC)**
- **System-in-Package (SiP)**
- **Heterogeneous Integration**
- **Heterogeneous Integration on Organic Substrates**
- **Heterogeneous Integration on Silicon Substrates**
- **Heterogeneous Integration on RDLs**
- **FOWLP for 3D IC Heterogeneous Integration**
- **Trends in Heterogeneous Integration**

Heterogeneous Integration on organic substrate

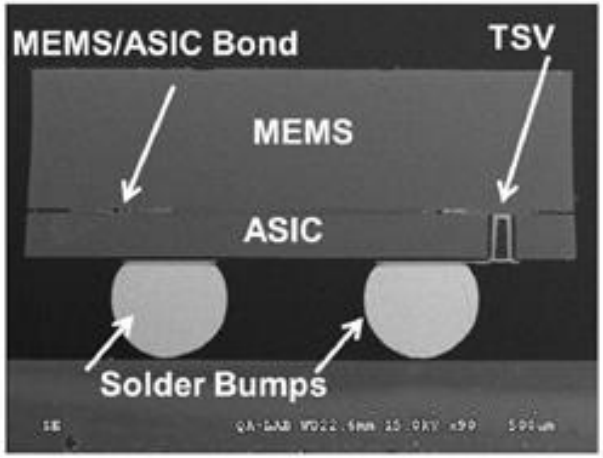
SiP Assembly

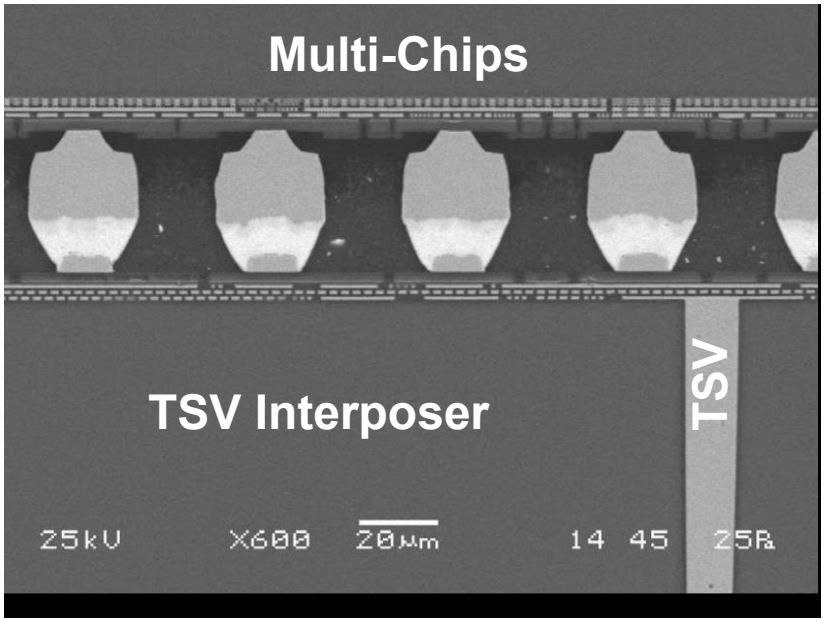


- SMT & Chip Shooter
- Stencil and Solder Paste Printing
- Mass Reflow
- Wire Bonding Chips on Board
- Flip Chip Mass Reflow

Heterogeneous Integration on Si Substrates

Chip-on-Wafer





- If the pitch is ≤ 50µm, then use Thermocompression Bonding.
- If the pitch is > 50µm, then use Mass Reflow.

Heterogeneous Integration on RDLs

RDL Fabrications

Organic RDLs:

By using a polymer to make the dielectric layer and Cu-plating + etching to make the conductor layer for all the RDLs.

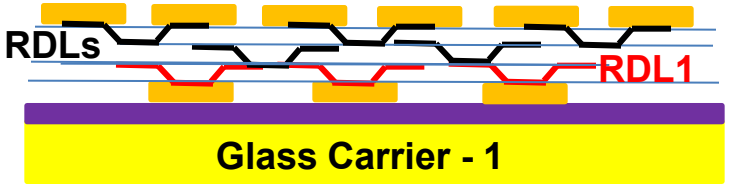
Inorganic RDLs:

By using PECVD to make the SiO_2 (or SiN) dielectric layer and Cu-damascene + CMP to make the conductor layer of all the RDLs.

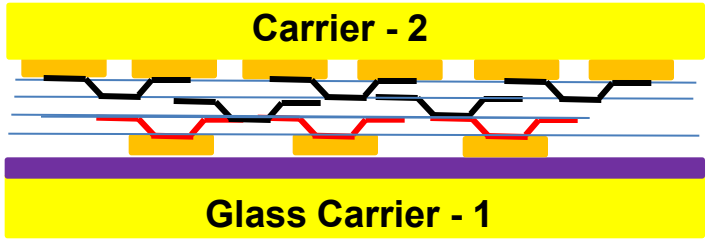
Hybrid RDLs:

By using PECVD and Cu-damascene + CMP to make the first fine line width and spacing RDL and then using a polymer to make the dielectric layer and Cu-plating + etching to make the conductor layers for the rest of not so fine line width and spacing RDLs.

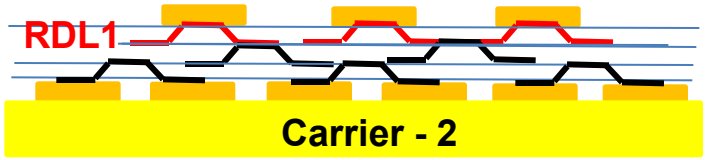
(a) Coated a sacrificial layer on a glass carrier



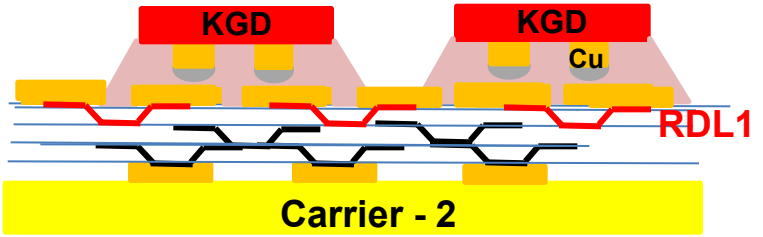
(b) Build contact pads, first RDL (RDL1) with PECVD/ Cu-damascene/CMP, and the rest RDLs with polymer/Cu-plating



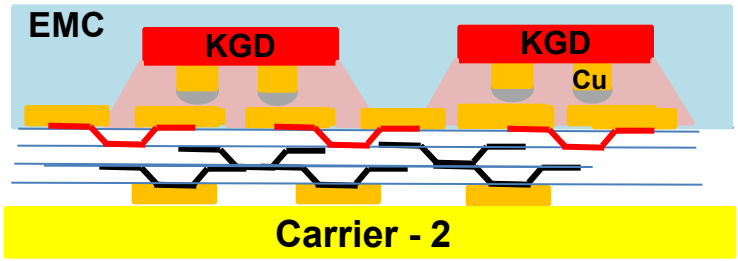
(c) Attach carrier-2



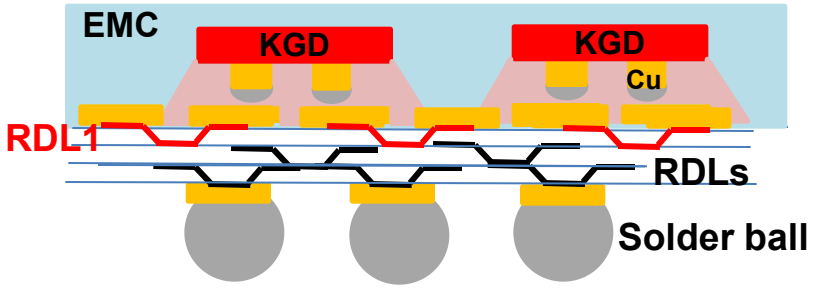
(d) Laser debond of carrier - 1



(e) Chip-to-wafer bonding, underfilling



(f) EMC compression molding



(g) De-bonding of carrier – 2 and solder ball mounting

The development and the integration of the 5μm to 1μm half pitches wafer level Cu redistribution layers

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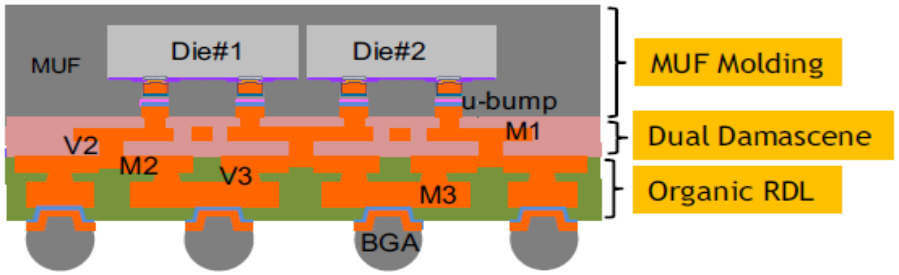
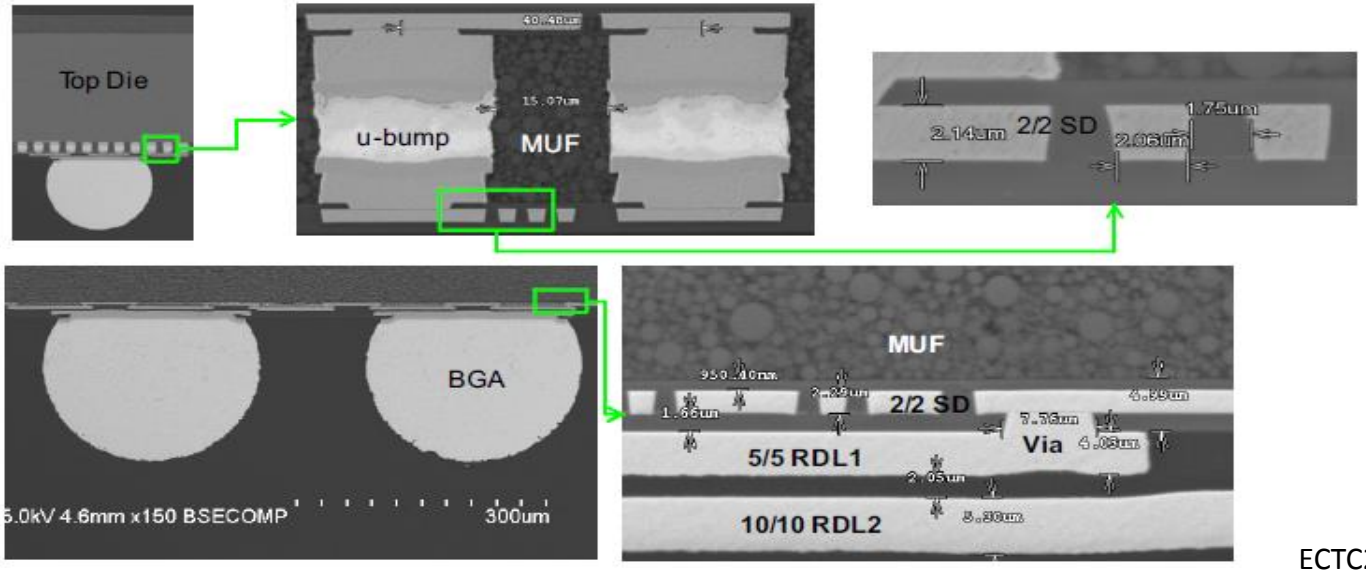
Email: mikema@spil.com.tw



Layer	Scheme (thk)	Dielectric
M1: L/S 2/2 um	FS- RDL1	SiO2/SiNx
M2: L/S 5/5 um	BS- RDL2	PBO
M3: L/S 10/10um Contact to BGA Ball	BS- RDL3	PBO



Thank You Very Much for Your Attention!