# 2D TO 3D ARCHITECTURES: BACK TO THE FUTURE

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INTEL CORPORATION

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# ACKNOWLEDGEMENTS

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# OUTLINE

- On-Package Heterogeneous Integration Drivers: Data, Data, Data!!
- 2D and 3D MCP Architectures: Back to the Future
  - Nomenclature, Definitions, Metrics..
  - Comparing Architectures using Metrics
- Future Opportunities for Heterogeneous On-Package Integration

# THE AGE OF DATA

## BY 2020

AVG. INTERNET USER **1.5 GB** OF TRAFFIC / DAY

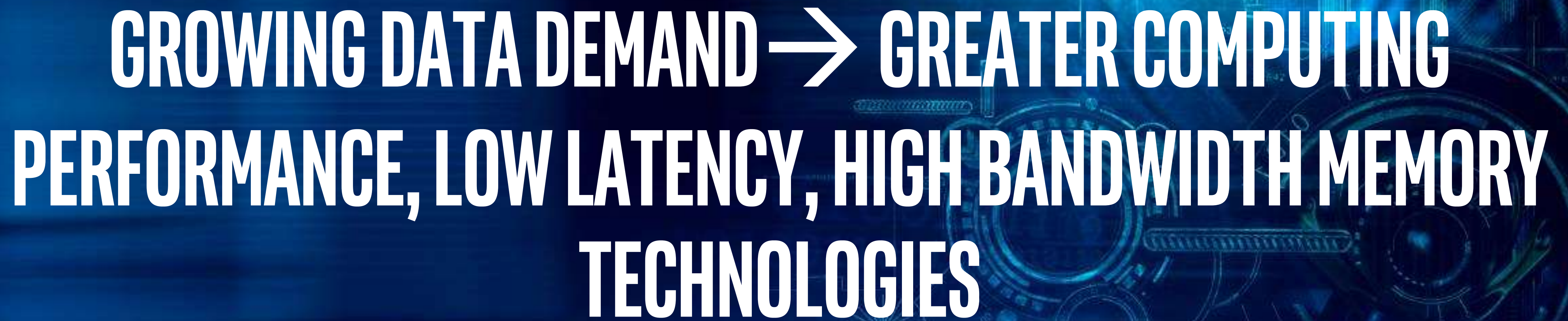
AUTONOMOUS VEHICLES **4 TB** OF DATA / DAY

CONNECTED AIRPLANE **5 TB** OF DATA / DAY

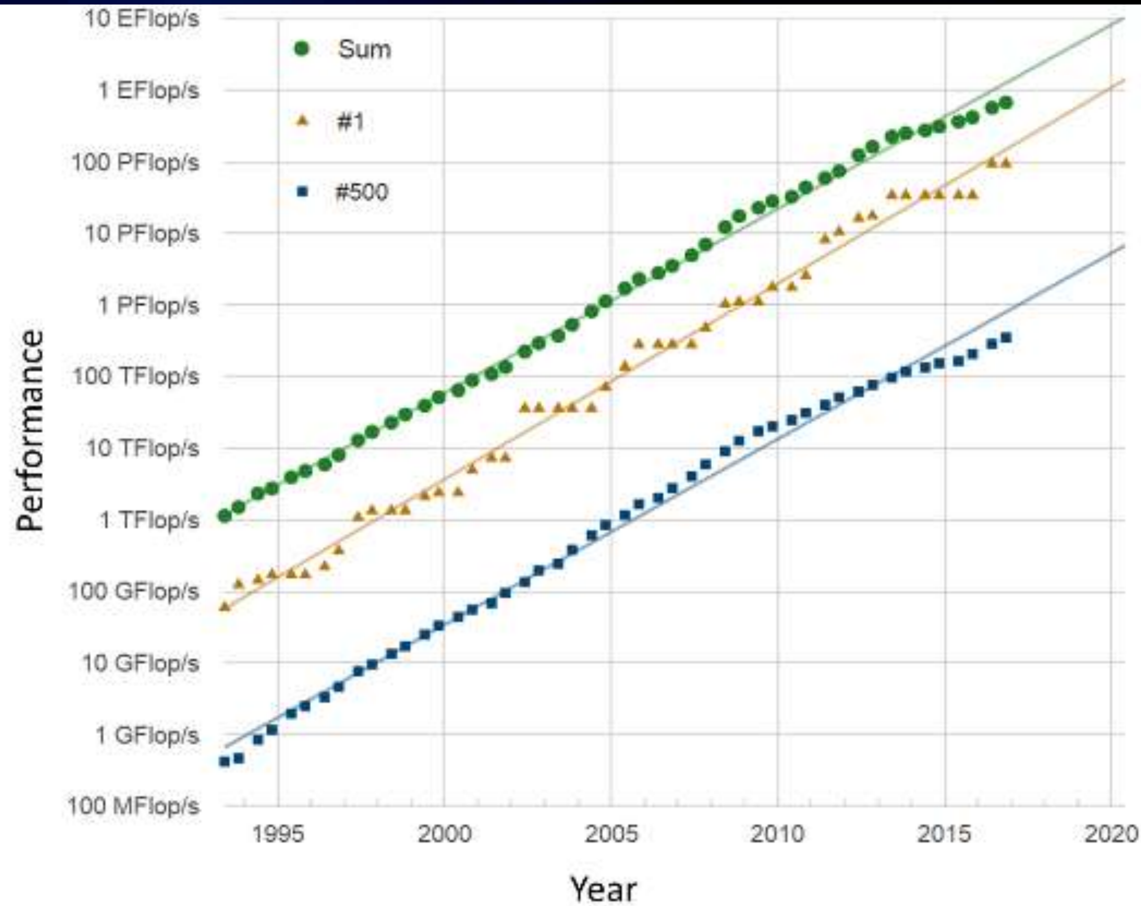
SMART FACTORY **1 PB** OF DATA / DAY

CLOUD VIDEO PROVIDERS **750 PB** OF VIDEO / DAY

Images from the web, Data from Intel presentations

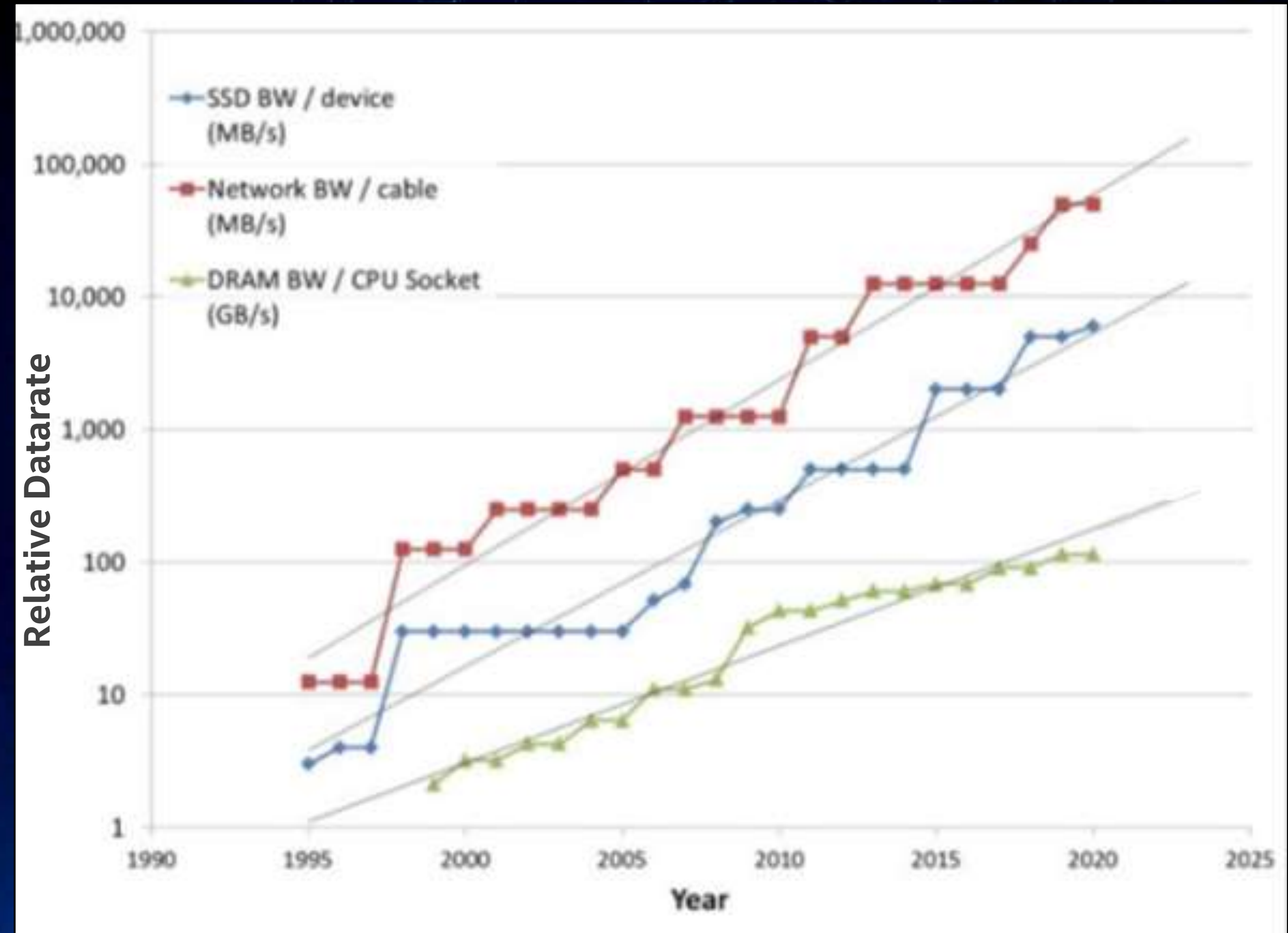

GROWING DATA DEMAND → GREATER COMPUTING PERFORMANCE, LOW LATENCY, HIGH BANDWIDTH MEMORY TECHNOLOGIES

## Projected Supercomputer Performance




Source: Top500.org

## Projected Growth in Comms Datarate




Source: https://itblog.sandisk.com/cpu-bandwidth-the-worrisome-2020-trend/

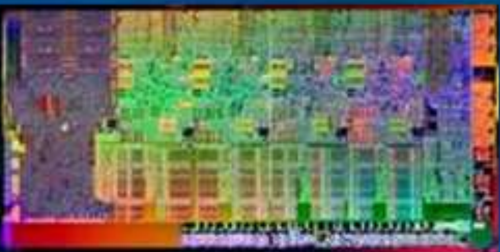
# *System Designers Continue to "Raise the Bar" for Overall Performance*

Ack: Babak Sabi, 2017 ECTC keynote

# IMPROVED MEMORY TECHNOLOGIES ARE CRITICAL ....

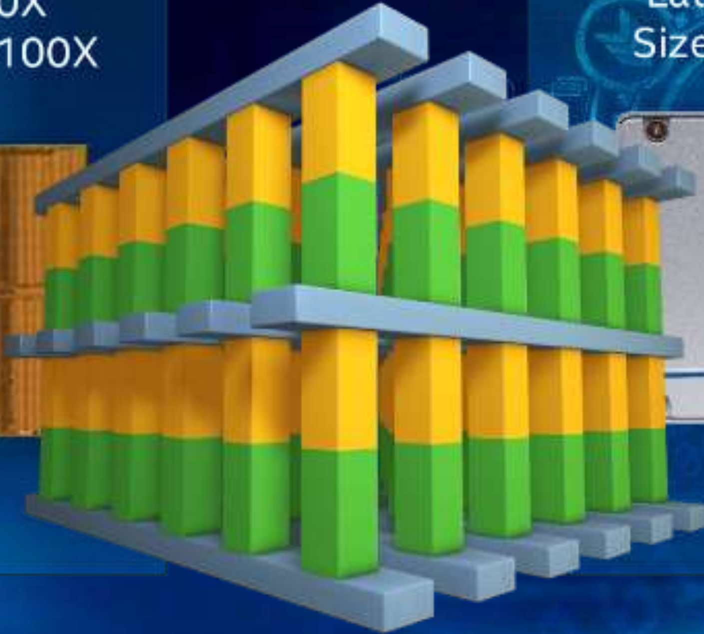
## MEMORY + STORAGE

**SRAM**
Latency: 1X
Size of Data: 1X

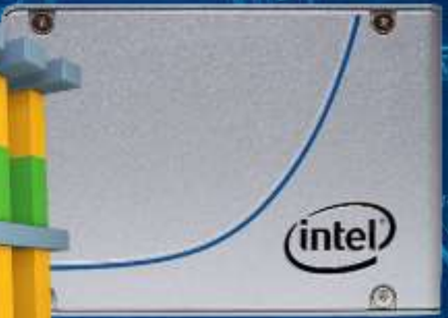


**DRAM**
Latency: ~10X
Size of Data: ~100X

**3D XPoint™**
Latency: ~100X
Size of Data: ~1,000X



**NAND SSD**
Latency: ~100,000X
Size of Data: ~1,000X

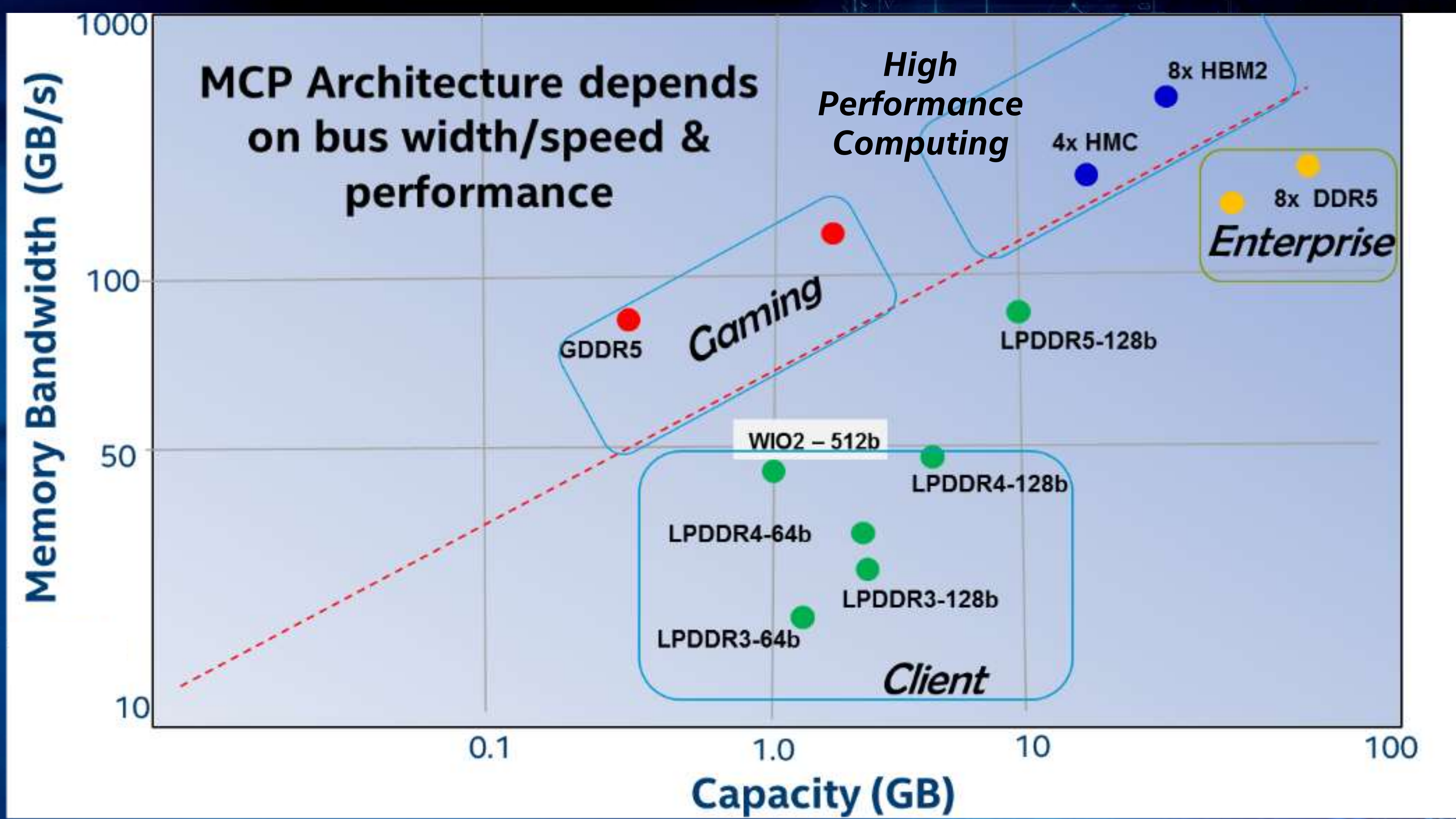



**HDD**
Latency: ~10 Million X
Size of Data: ~10,000X

chnology claims are based on comparisons of latency, density and write cycling metrics amongst memory technologies recorded on published specifications of in-market memory products against internal Intel specifications.

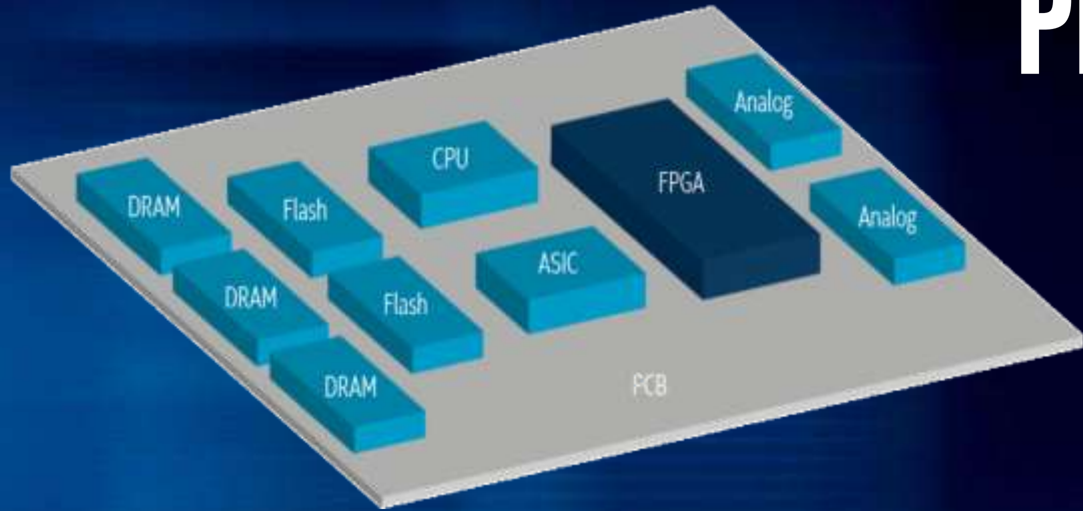
Ack: Babak Sabi, 2017 ECTC keynote

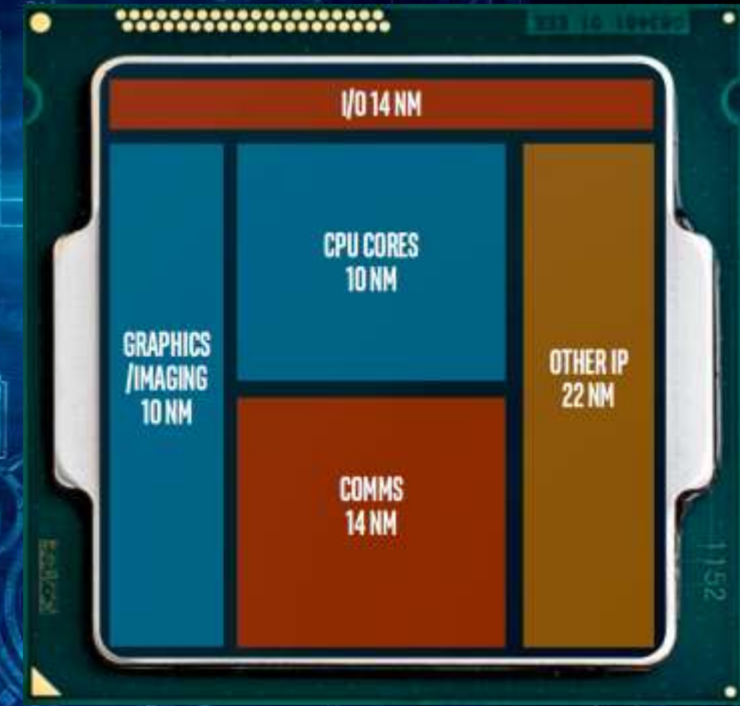
# CPU-MEMORY BANDWIDTH TRENDS



HIGH PERF MEMORY TECHNOLOGIES→ HIGH BANDWIDTH,
LOW LATENCY, LOW POWER…

# PACKAGE IS THE IDEAL HETEROGENEOUS INTEGRATION PLATFORM






**PCB Integration**

- Limited Interconnect Density → Limited BW
- Long Interconnects → Increased Power
- Large Form Factor

**On-Package Integration**

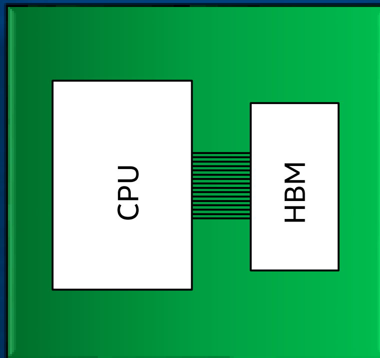
✓ Higher Interconnect Density→ Higher BW

✓ Shorter Interconnects→ Lower Power

✓ Heterogeneous Integration of Multiple Nodes, Multiple IP, & Multiple Functions without form factor penalty

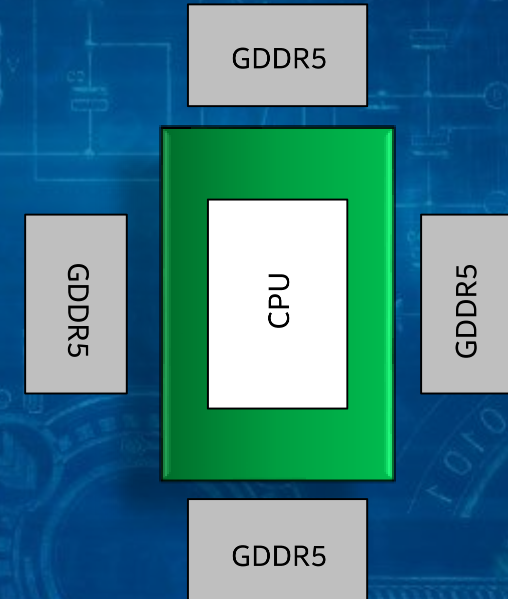
Ack: Babak Sabi, 2017 ECTC keynote

# ON -PACKAGE VS. OFF-PACKAGE INTEGRATION




**HBM**

- Wide and Slow
- Total Capacity 4GB (4x 1GB)
- Data rate – 1 - 2Gb/s
- Total BW – 256 GB/s
- IO Power Efficiency (Energy/bit) – 1X




**GDDR5x**

- Narrow and Fast
- Total Capacity 4GB (1GB each)
- Data rate – 12Gb/s
- Total BW – 192 GB/s
- IO Power Efficiency (Energy/bit) – (1.75 – 3)X

1. http://www.memcon.com/pdfs/proceedings2015/MKT105_SKhynix.pdf
2. https://www.micron.com/~/media/documents/products/technical-note/dram/tned02_gddr5x.pdf

***On Package Integration is More Compact, Lower Power & Higher BW***

Ack: Babak Sabi, 2017 ECTC keynote

# ON PACKAGE MCP ARCHITECTURES: 2D AND 3D

## 2D MCP Architecture

Side by side active Silicon interconnected on the package

Package

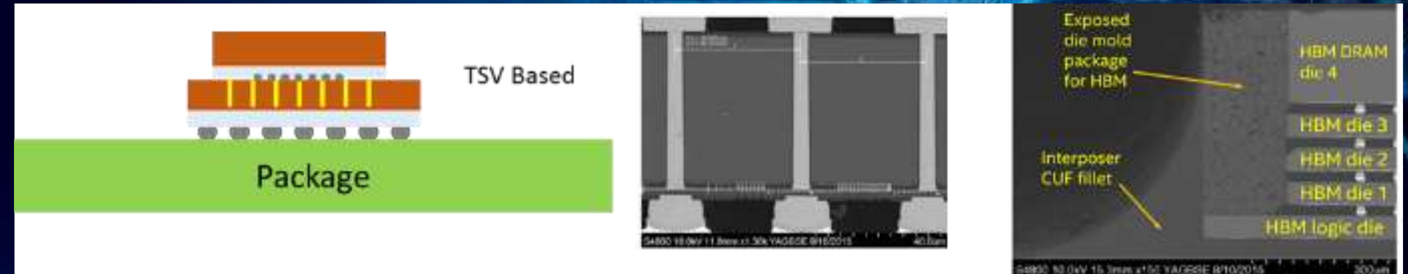
DRAM Package

SOC Die

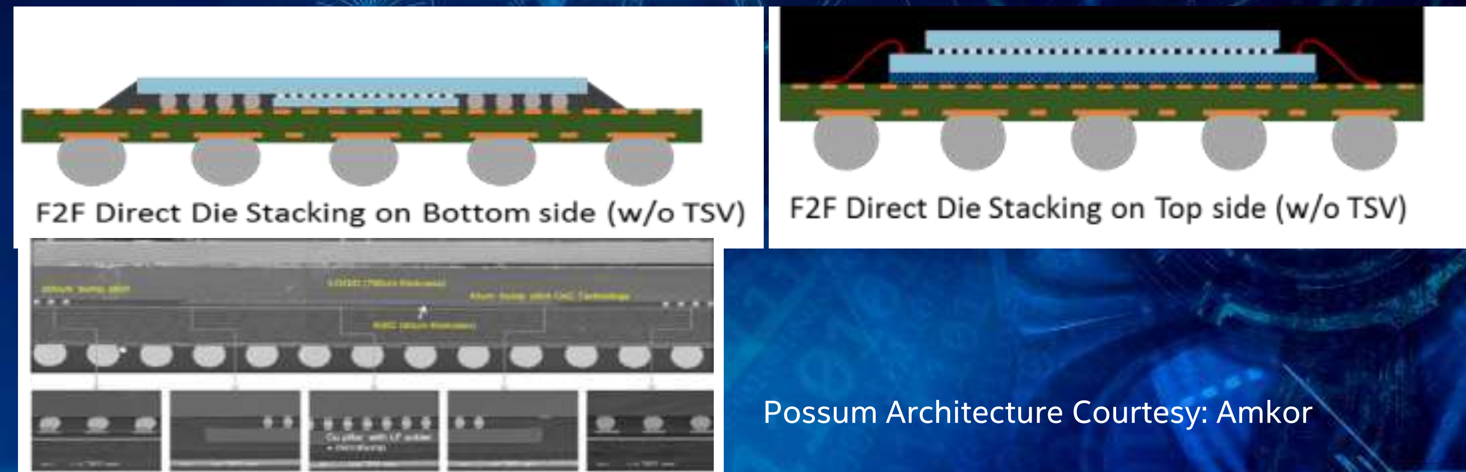
## 3D MCP Architecture

Active Silicon stacked and interconnected on Active Silicon without agency of the package

1. With TSV




2. Without TSV

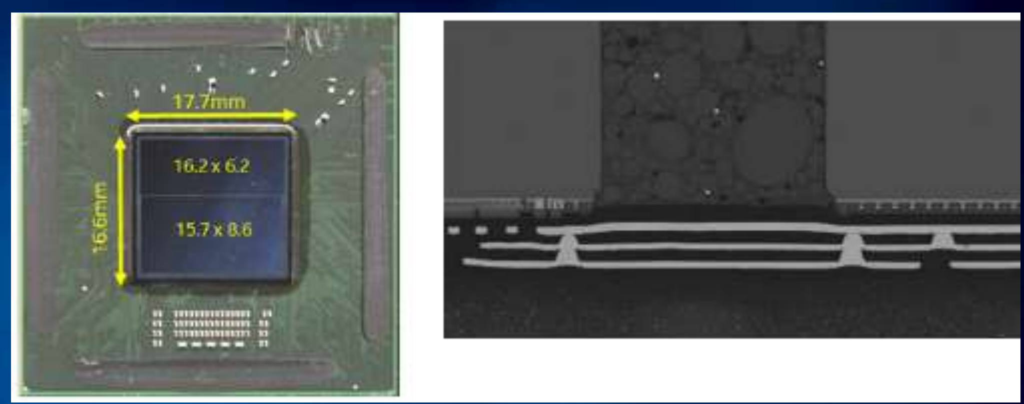



Possum Architecture Courtesy: Amkor

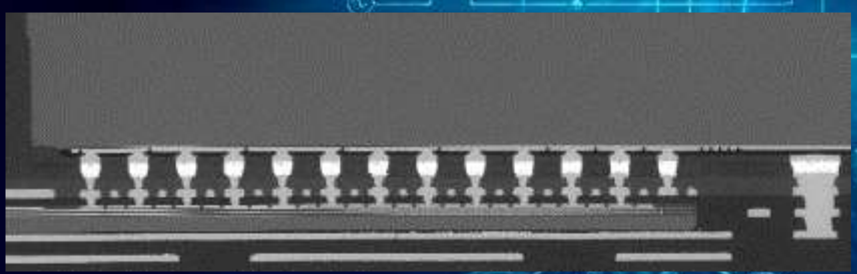
Pictures from teardowns, X-sections available on the web

# THE RISING STARS: 2.X D ARCHITECTURES

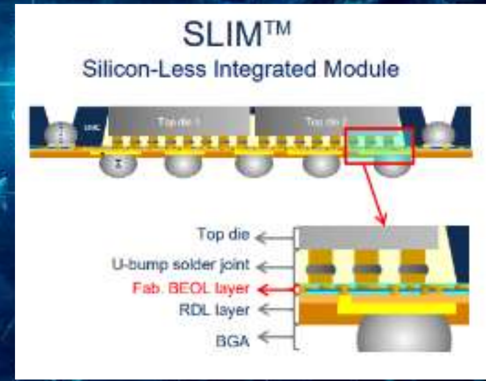
FoCoS: 2.1/2.3D?



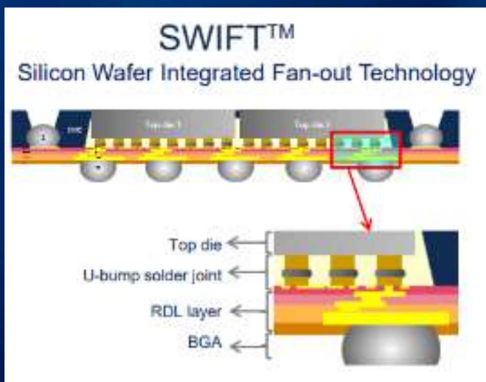

EMIB: 2.5D?



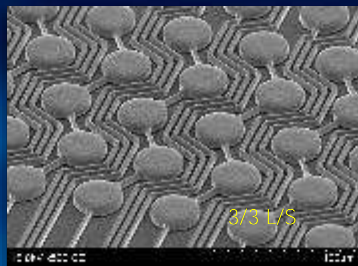
SLIM: 2.5D?

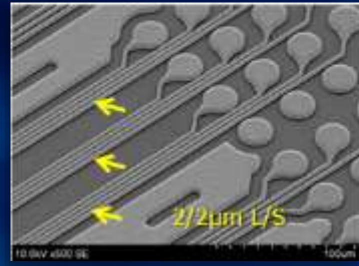



SWIFT: 2.1/2.3D?




HD organic package: 2.1/2.3D?




INFO: 2.xD?

CoWoS: 2.5D?

SWIFT, SLIM trademarks of Amkor; FoCoS trademark of ASE; CoWoS, INFO trademarks of TSMC

→NEW NOMENCLATURE: 2D ENHANCED ARCHITECTURES

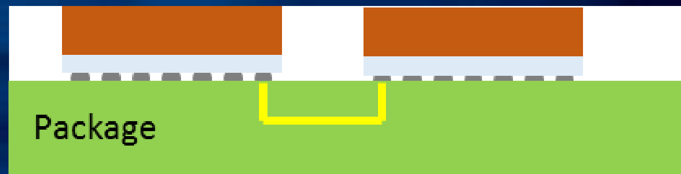
# 2D ENHANCED ARCHITECTURES

Side by side active Silicon interconnected at higher densities using...

## Organic Based

## 2DO

a. Chip Last

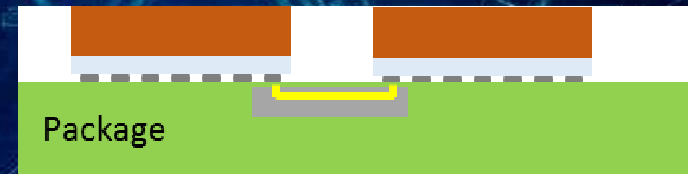



b. Chip First

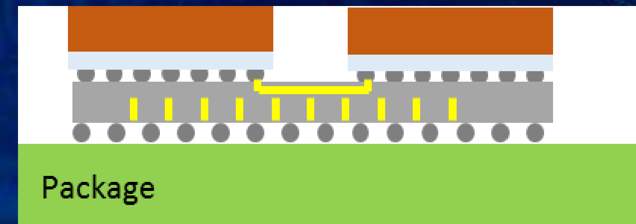
## Passive Si based

## 2DS

a. Without TSV

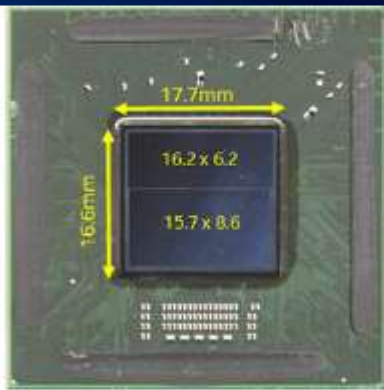


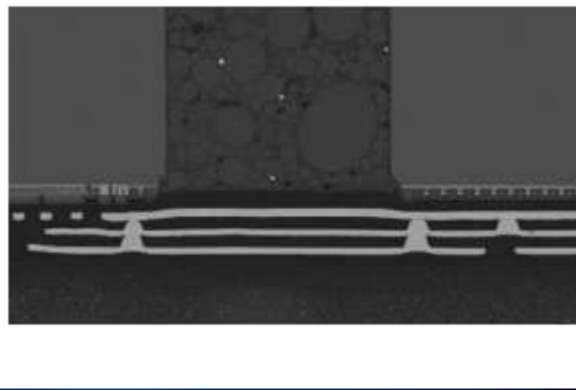

b. With TSV



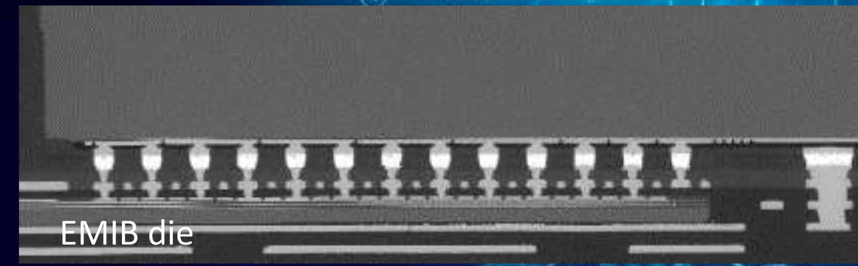
# 2D ENHANCED ARCHITECTURES

FoCoS: 2DO Chip Last/First

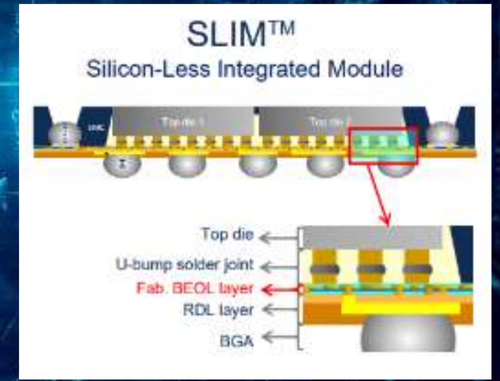


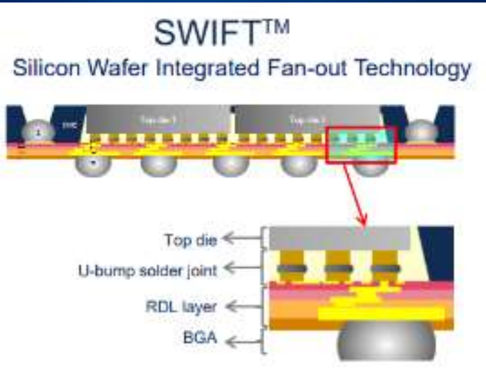
EMIB: 2DS without TSV



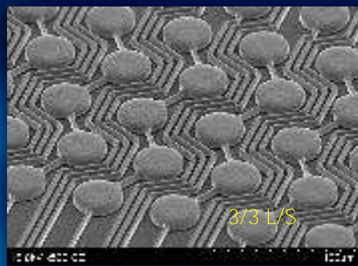

SLIM:

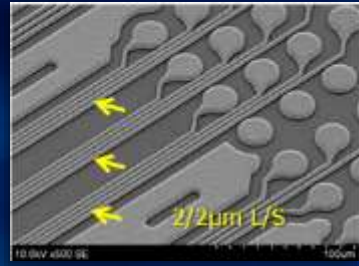



SWIFT:
2DO Chip Last

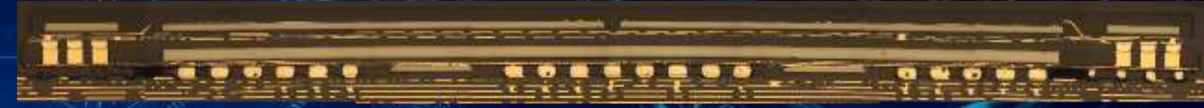



HD organic package:
2DO Chip Last




INFO: 2DO Chip First

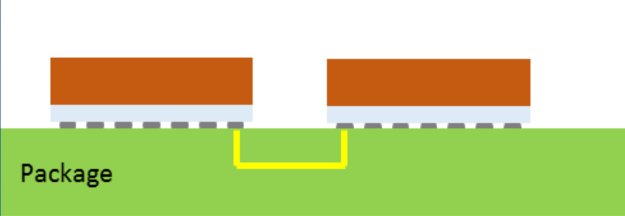


CoWoS: 2DS with TSV

SWIFT, SLIM trademarks of Amkor
FoCoS trademark of ASE
CoWoS, INFO trademarks of TSMC

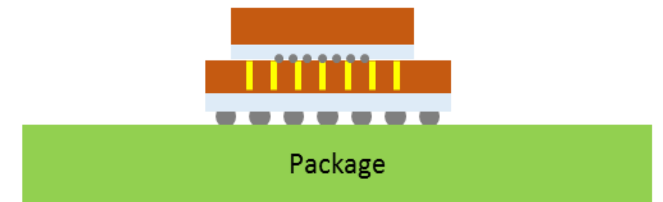
# ON-PACKAGE MCP ARCH. "ORG CHART"

## 2D Architecture



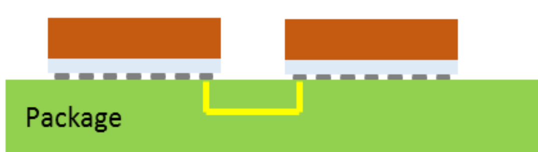

## 2D Enhanced Architecture

## 3D Architecture

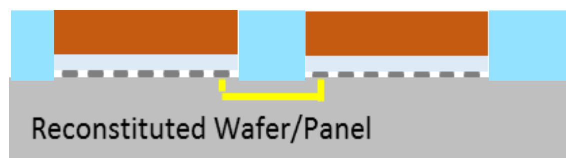



### 2DO Organic Based

#### Chip Last



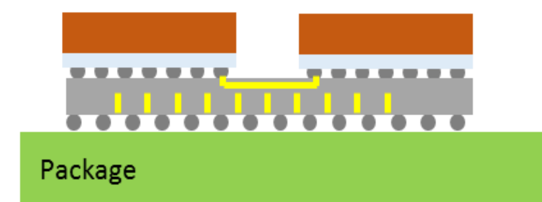

#### Chip First




### 2DS Passive Si* based

#### Without TSV

#### With TSV




*Can be glass based as well

# COMPARING ARCHITECTURES: KEY METRICS

Min Active (or Bump) Si
Interconnect Layer Via Pad

**Interconnect Energy Density (pJ/bit)**

Min-Max Die Thickness

**Linear Interconnect Density** (Wires/mm/layer)

**Data Rate Capability (Gtps)**

Min-Max Die Size

**Dielectric Materials**

Interfacial Layer
Min L/S

Min Active Si/Bump
Interconnect Pitch

Dielectric loss tangent (tan δ)

**Process Differentials (Chip First vs. Chip Last)**

Dielectric Thickness

Conductor (Cu) Thickness

**Areal Interconnect Density** (Bumps/$mm^2$)

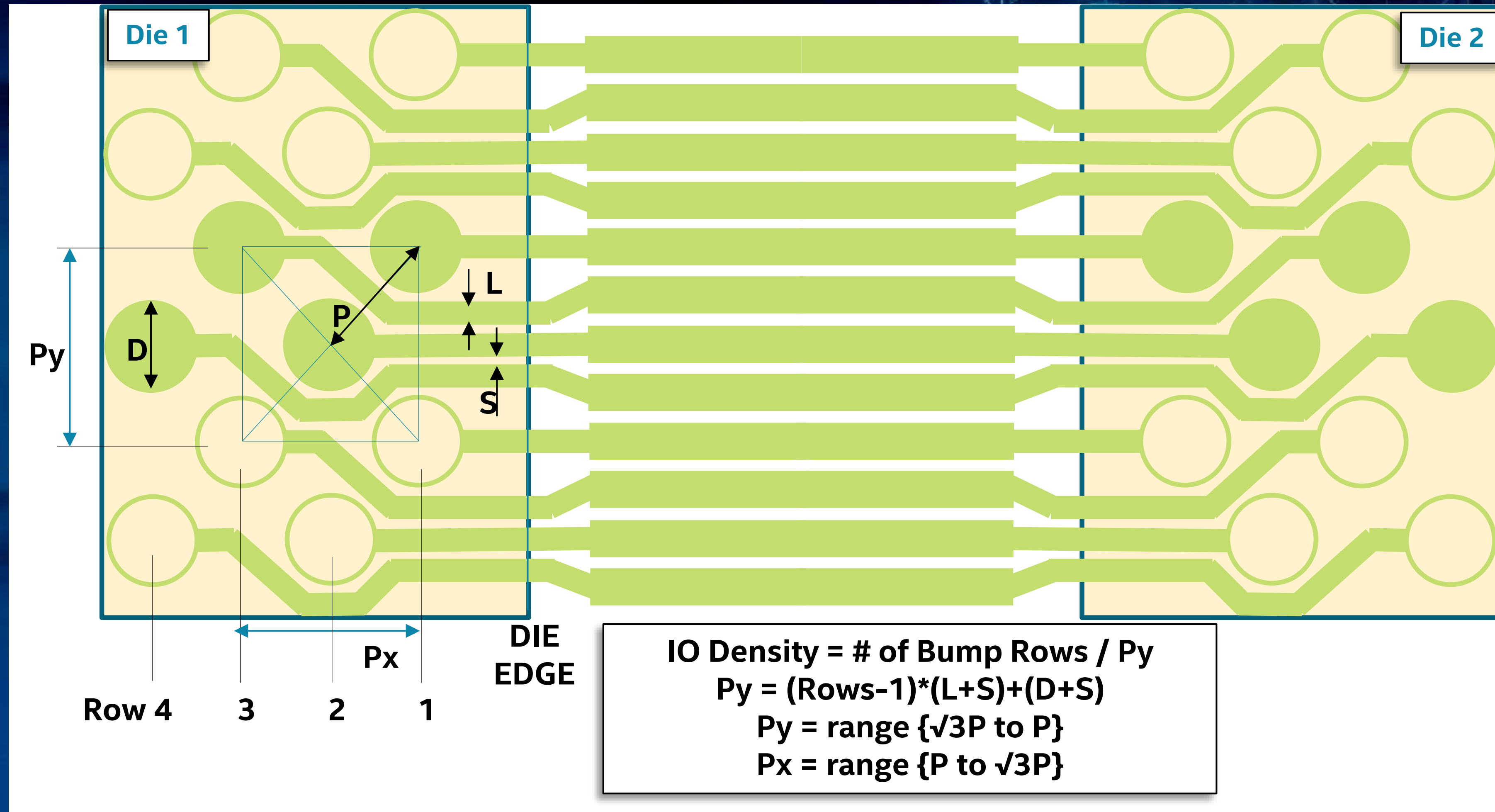
Interconnect Materials

**Power Delivery Resistance**

Min-Max Package/Interposer size

**Thermal Resistance**

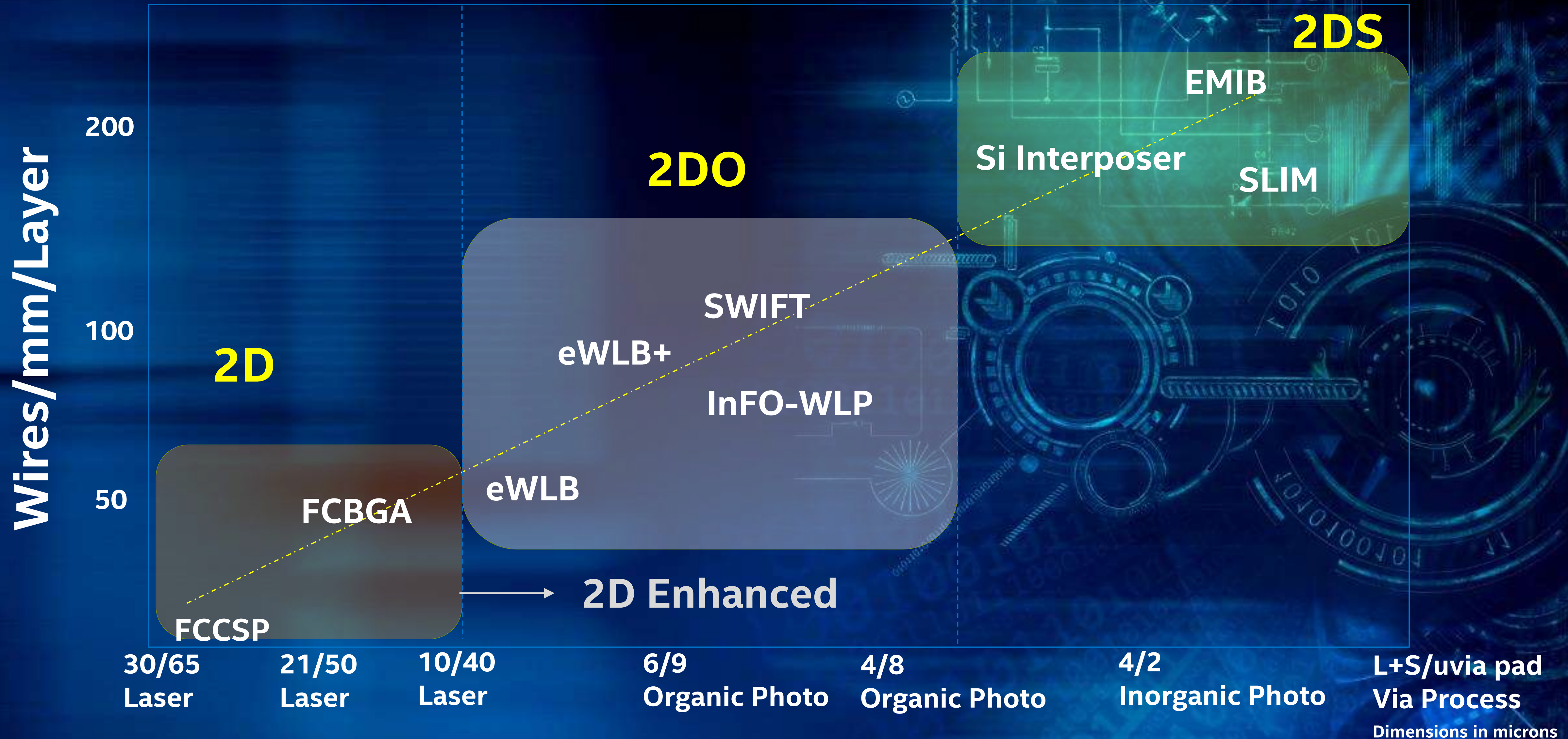
# LINEAR INTERCONNECT DENSITY: WIRES/MM/LAYER



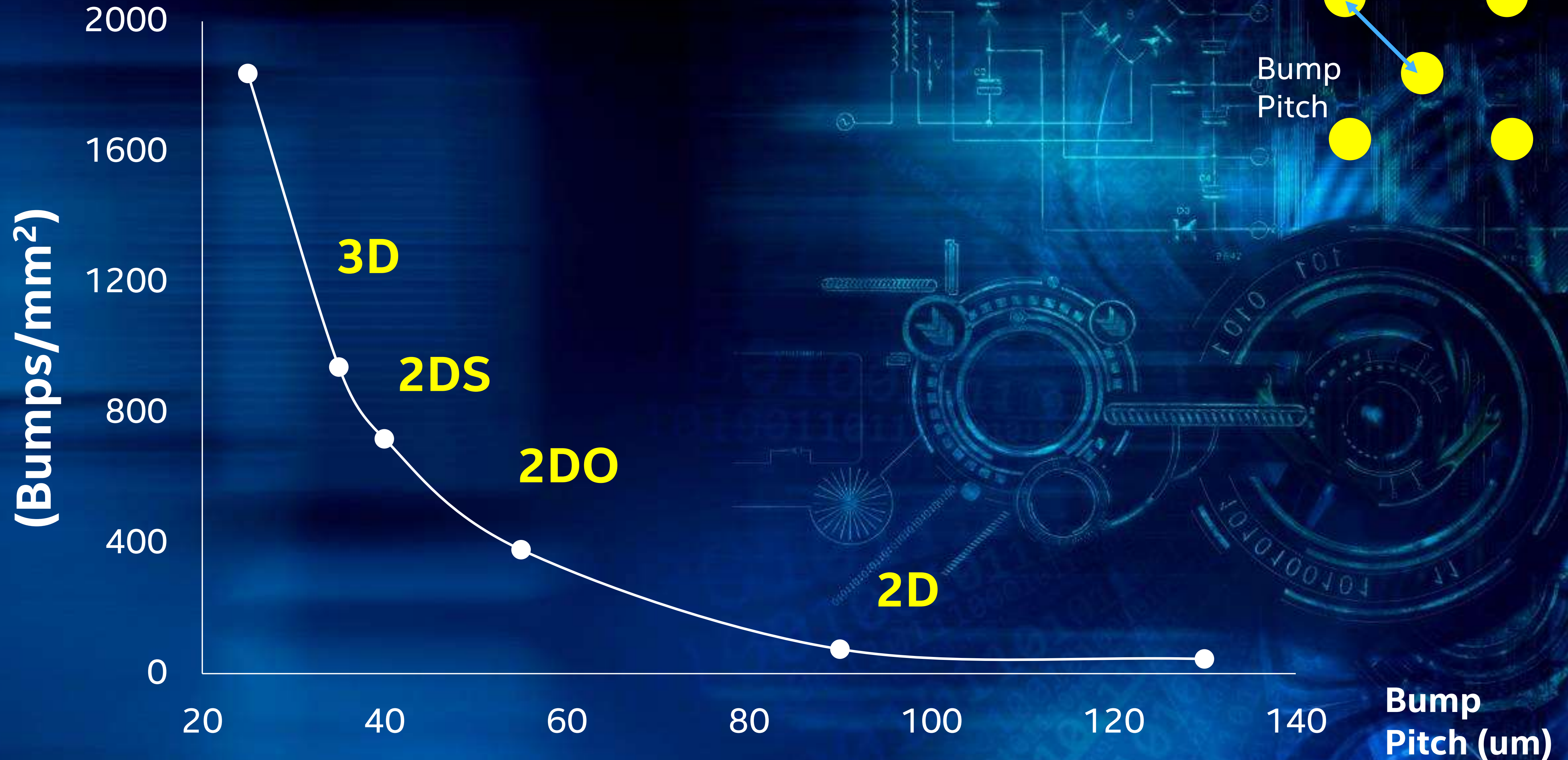

Number of wires escaping per millimeter of die edge is **the key metric** used to compare 2D architectures

# COMPARING ARCHITECTURES: LINEAR DENSITY

Linear density not applicable metric for 3D architectures



# COMPARING ARCHITECTURES: AREAL DENSITY

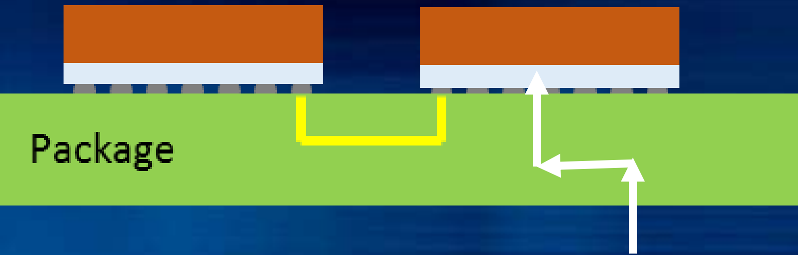


# COMPARING ARCHITECTURES: SIGNALING PERF

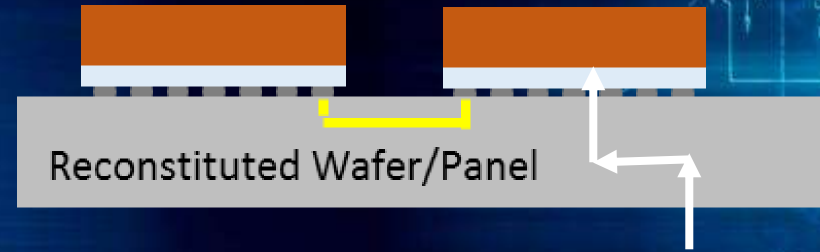
| Key Metric | 2D Architecture | 2D Enhanced Architecture | | 3D Architecture |
|---|---|---|---|---|
| | | 2DO | 2DS | |
| Interconnect Energy Density(pJ/bit) | 5-10 | 2-5 | <1 | <1 |
| Data Rate Capability (Gtps) | 6-10 | 6-8 | 2-5 | 1-5 |
| Dielectric Materials | Std. Organic DE | Enhanced (Photo/Laser) Org | Inorganic: $SiO_2$ | -- |
| Dielectric loss tangent ($\tan \delta$) | 0.005-0.01 | 0.002-0.005 | ≤0.001 | -- |
| Dielectric Thickness | 15-20u | 3-10u | 0.5u | -- |
| Conductor Material | Cu | Cu | Cu | Cu |
| Conductor Thickness | 15-20u | 3-12u | 1-2u | 1-2u |

# COMPARING ARCHITECTURES: POWER DELIVERY RESISTANCE

2D

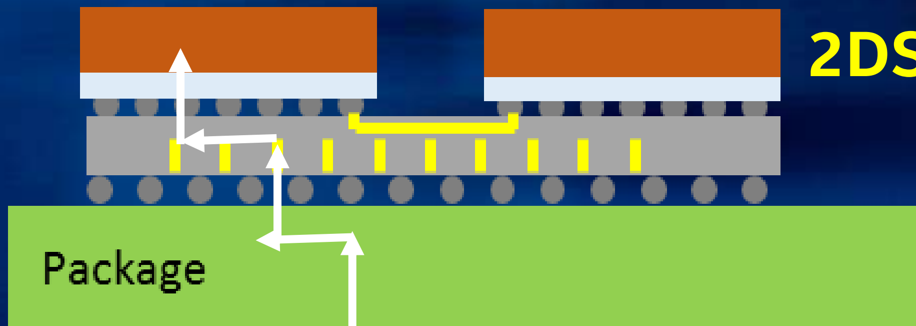



2DO



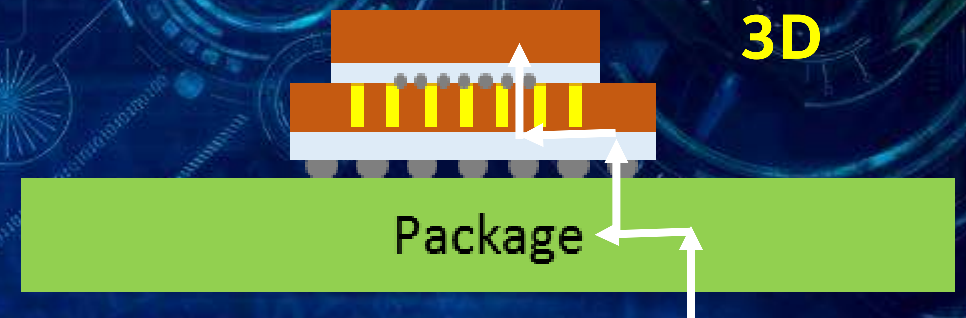

2DS (without TSV)

Direct power delivery path through thick Cu planes/traces in substrate/ RDL layers + dedicated power/ground planes→ Less resistive



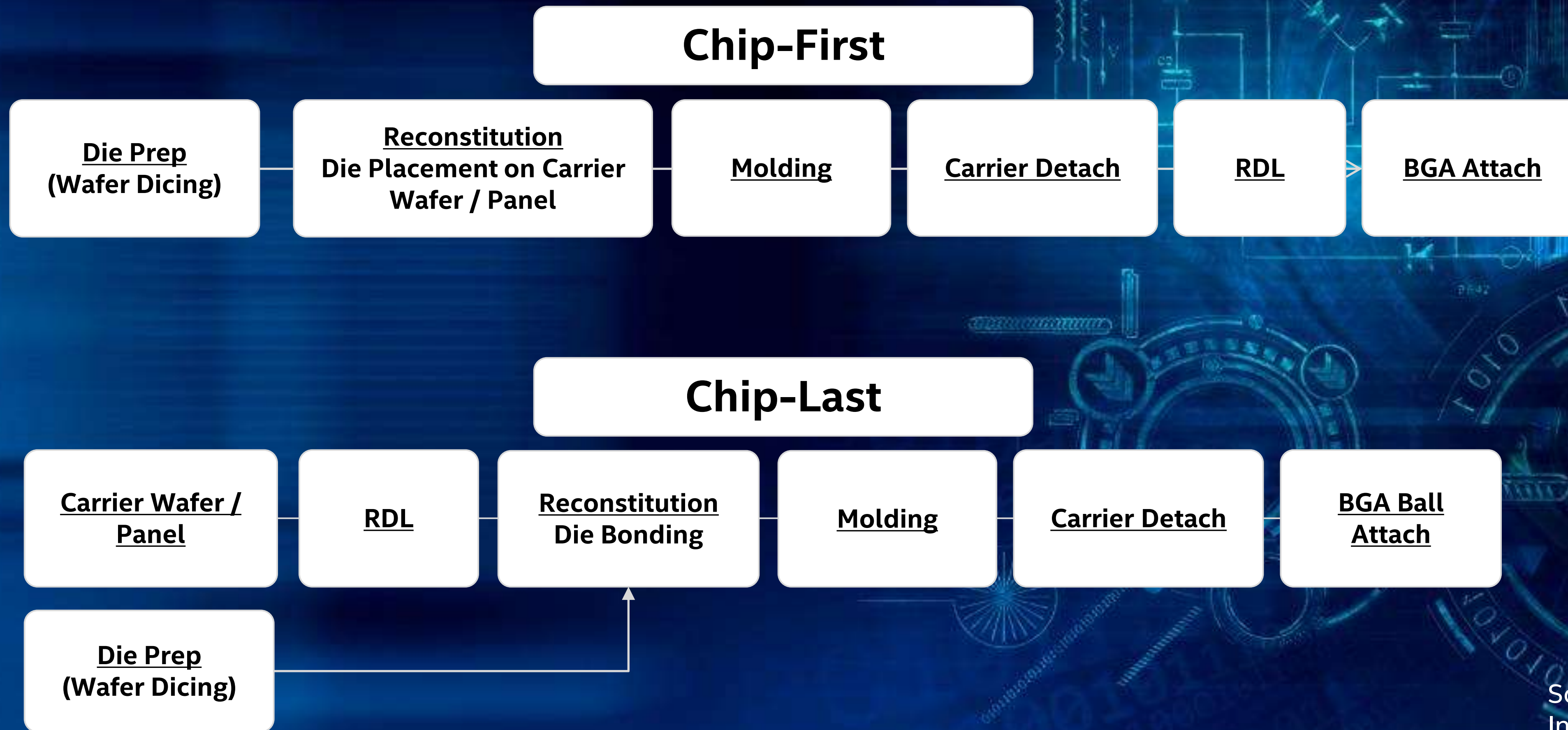

2DS (with TSV)

3D




Power delivery path weaves through thin Cu traces in Silicon + minimal power/ground planes→ Highly resistive

# COMPARING ARCHITECTURES: PROCESS FLOWS

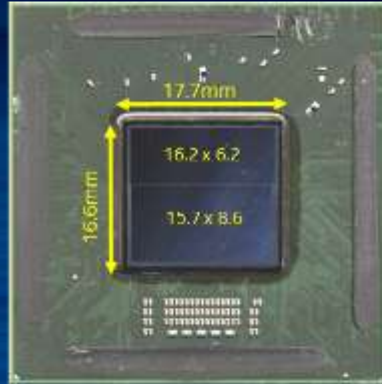



Source: TechSearch International Inc.

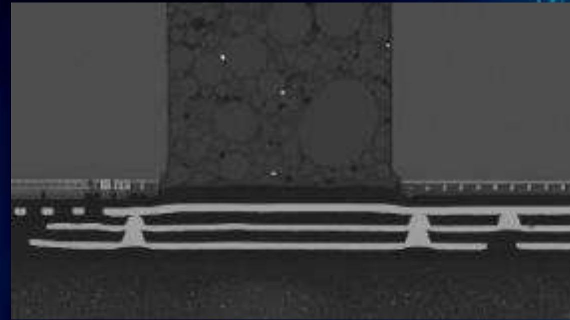
- Chip First RDL: No KGP (known good packages) related tradeoffs
- Panel level processes also have similar considerations

# TODAY'S MULTI-CHIP PACKAGING SPECTRUM

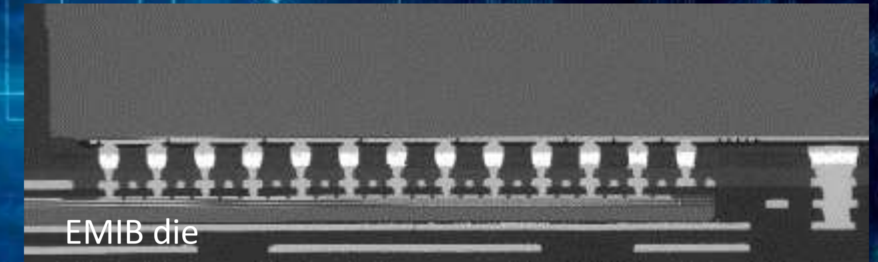
2D SbS




2DO

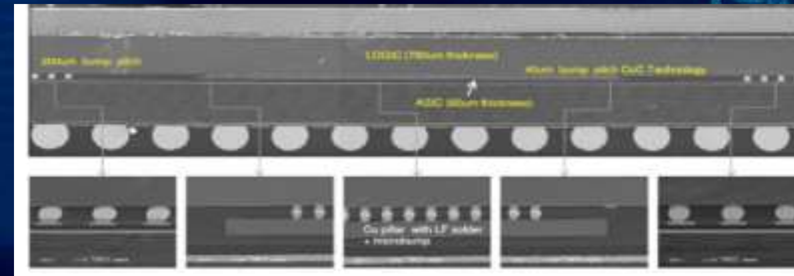


2DS (without TSV)

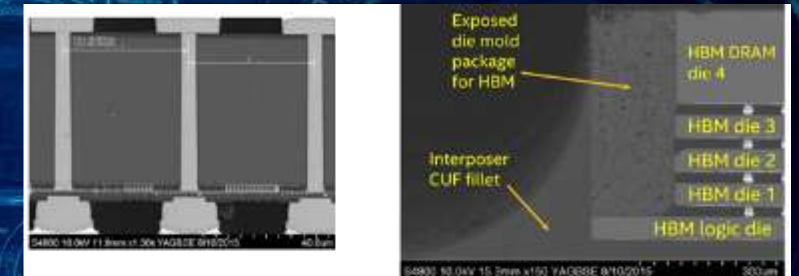



2D PoP

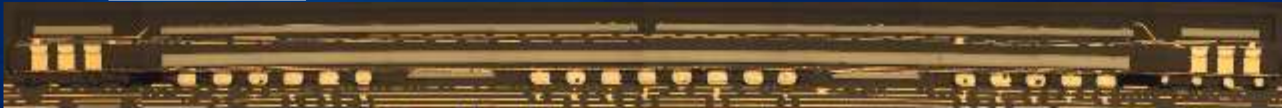
3D F2F



3D TSV




2DO PoP

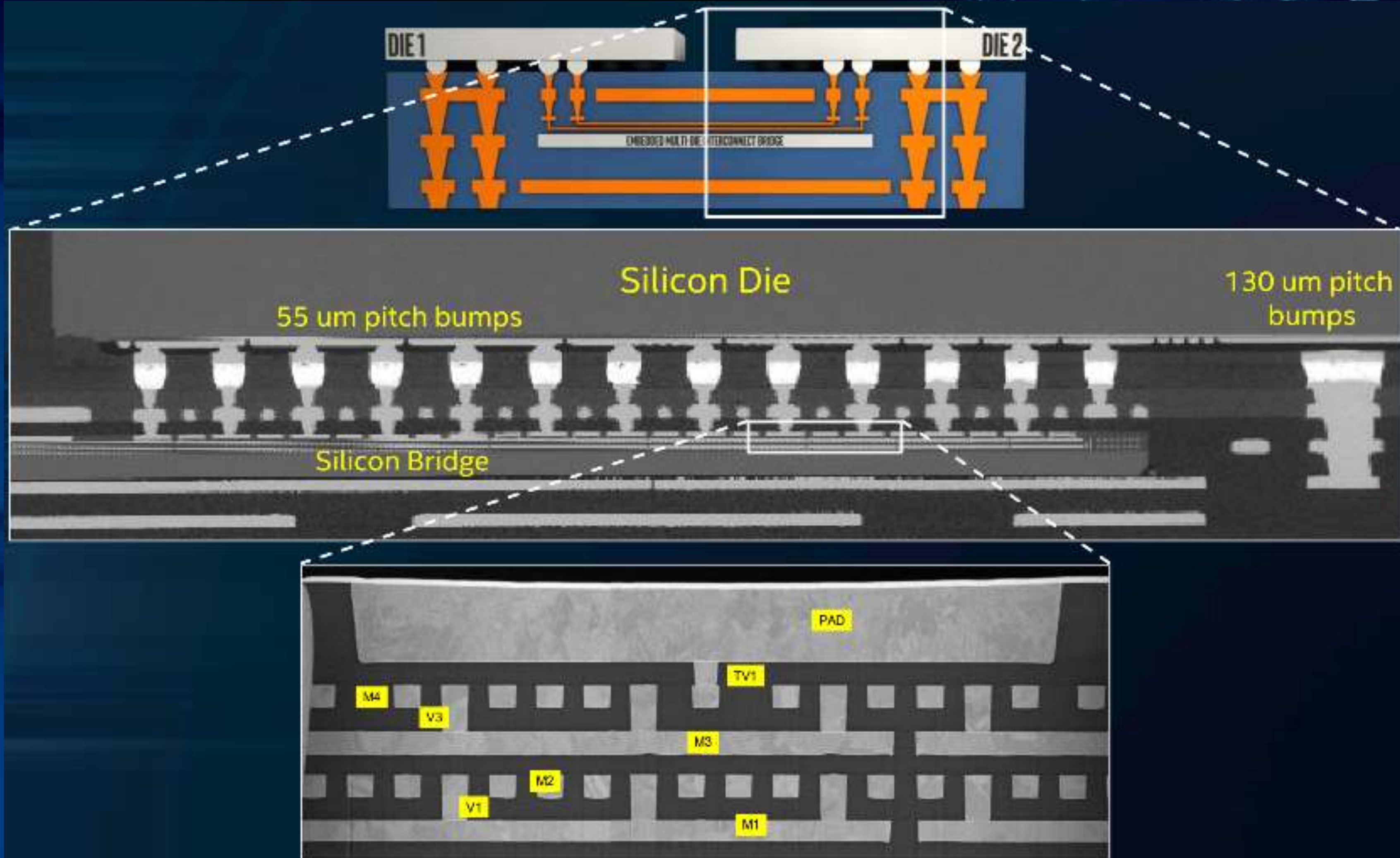


2DS with TSV

***Many Package Options Exist!!***

***Designers Pick the Optimal Solution for a Specific System***

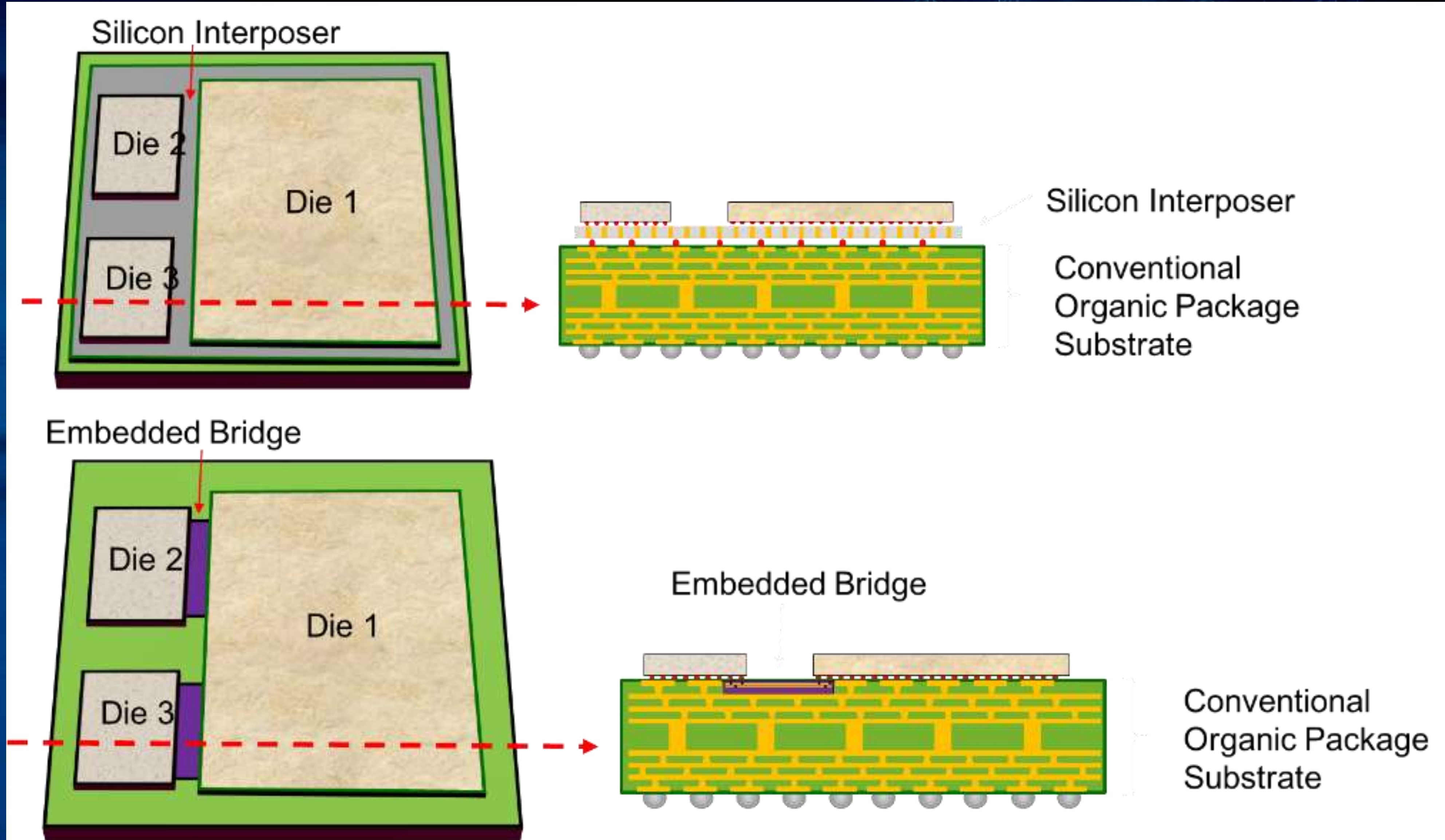
# EMIB: INTEL'S 2DS ARCHITECTURE




EMIB allows for Localized high density, ultra-high Bandwidth/Low Power Interconnect Solution (2DS without TSV architecture)

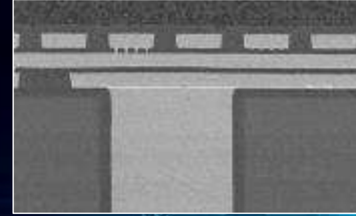
Ack: Mark Bohr, Intel Technology and Manufacturing Day, 2017

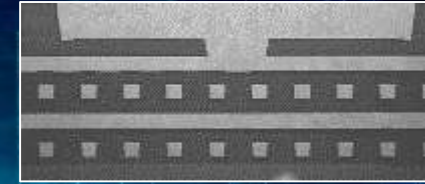
# 2DS ARCHITECTURES: EMIB VS. SI INTERPOSER




Ack: Ravi Mahajan, 2016 IMAPS PDC keynote

# 2DS ARCH COMPARISON: EMIB VS. SI INTERPOSER





| | Si Interposer | EMIB |
|---|---|---|
| Linear Interconnect Density | | |
| Chip-to-Chip Signal Integrity | | |
| Through Package Signal Integrity | | No TSV for other signals |
| Through Package Power Delivery | | Thick Cu traces, P/G planes |
| Silicon Processing | | No TSV processes |
| Substrate Processing | Baseline sub | |
| Assembly Processing | | Eliminates one TCB step |
| Total Chip/Si Area on Package | | |
| Overall Cost | | |

Ack: Ravi Mahajan, 2017 IMAPS PDC keynote

# DESIGNING WITH EMIB

Intel Stratix 10

Intel HyperFlex FPGA Architecture

TILE EMIB

144 Transceivers Operating at up to 30 Gbps

PCIe Gen3 Transceiver

Initial Tile Variant

Ethernet Transceiver

PCIe Gen4 Transceiver

Other Transceiver

56G Transceiver

PAM-4 Transceiver

Optical

Example Future Tile Variants

XCVR

FPGA

FPGA Die 2.8M Logic Elements

Transceiver Die (1-6 per package)

HBM

Gfx

intel

CPU

Kaby Lake-G

"MIX AND MATCH" HETEROGENEOUS DESIGN

I/O 14 NM

CPU CORES 10 NM

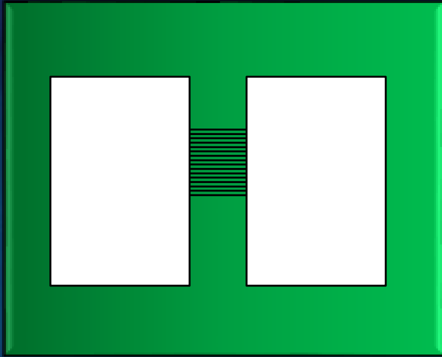
GRAPHICS /IMAGING 10 NM

OTHER IP 22 NM

COMMS 14 NM

Source: Intel Technology Manufacturing Day, 2017

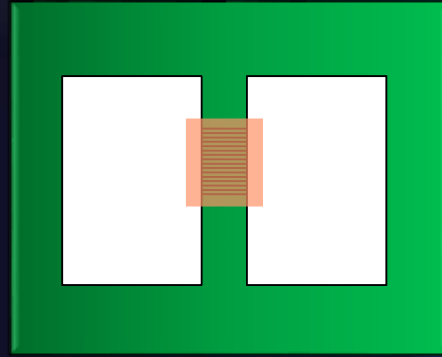
# DIRECTIONS FOR HETEROGENEOUS PACKAGING IN THE FUTURE



Traditional MCP
10's of IO/mm
~100 Gb/s BW

Die-Package Interconnect Pitch ~100μm

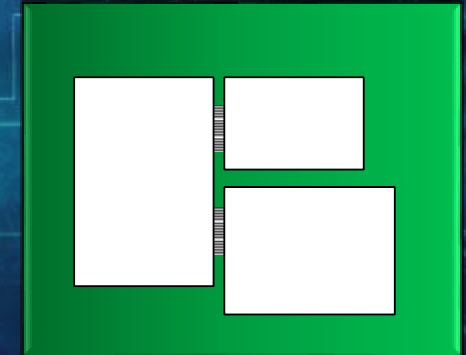
Substrate Technology – Advanced Laminate
Assembly Technology – Reflow CAM
Test Technology – Array Sort Probing



State of the Art MCP
100's of IO/mm
~500 Gb/s BW

Die-Package Interconnect Pitch ~50μm

Substrate Technology – EMIB, (Si Int + Laminate)
Assembly Technology – TCB
Test Technology – Array Sort + Self Test



The Future of MCP's
1000's of IO/mm
1+ Tb/s BW

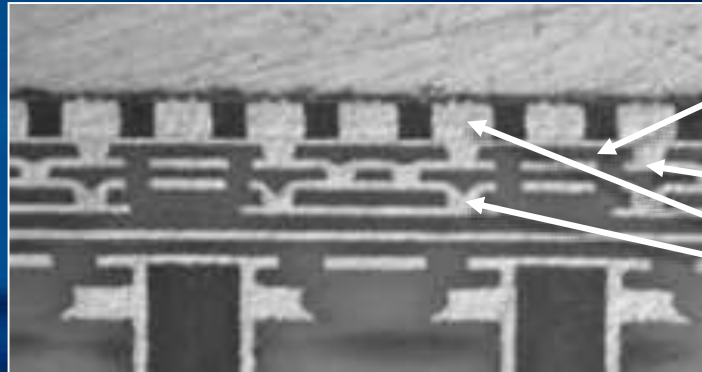
Die-Package Interconnect Pitch ~10μm

Substrate Technology – TBD
Assembly Technology – TBD
Test Technology – TBD

***Industry is Challenged to Invent New Solutions for Ultra-high Density Multi-Chip Packaging***

Ack: Babak Sabi, 2017 ECTC keynote

# PACKAGE TECHNOLOGIES WILL BECOME MORE WAFER FAB-LIKE

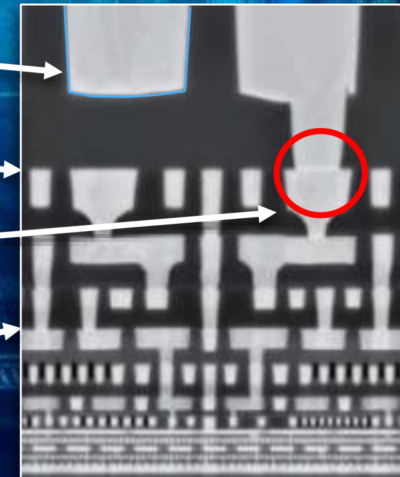


Inorganic Thin Films

Planarization

Pad-less Vias

Cu-Cu Bumps & Vias



***Achieving Interconnect Densities to Support 1+ TB/s on-Package Interconnects Will Require Novel Substrate and Assembly Capabilities***

Ack: Babak Sabi, 2017 ECTC keynote

# IN SUMMARY…

- On-Package level heterogeneous integration expected to increasingly complement Moore's Law scaling
- Industry transitioning to new standardized, physics based nomenclatures for 2D to 3D architectures
- Key metrics driving evolution of architectures described; expected to drive focus in industry/academia on critical technology trends for next generation packages
- Packaging industry will push the boundaries for Heterogeneous On-Package Integration with new enabling technologies

THANK YOU!!