



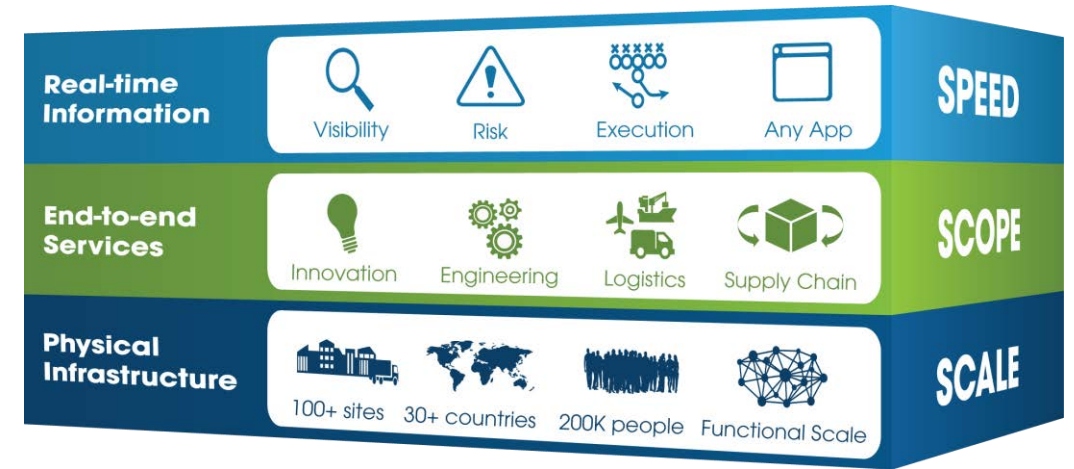
SiP for Miniaturized Electronics Modules: An Update

Dr. Dongkai Shangguan

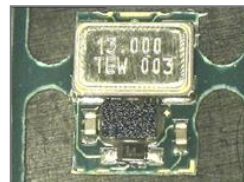
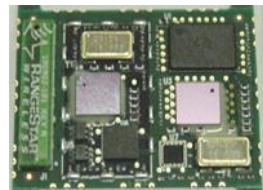
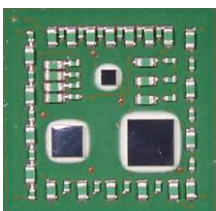
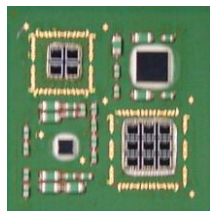
October 2019

Outline

- SiP Overview
- Industry Landscape
- Competency Development
- Eco-System
- Summary



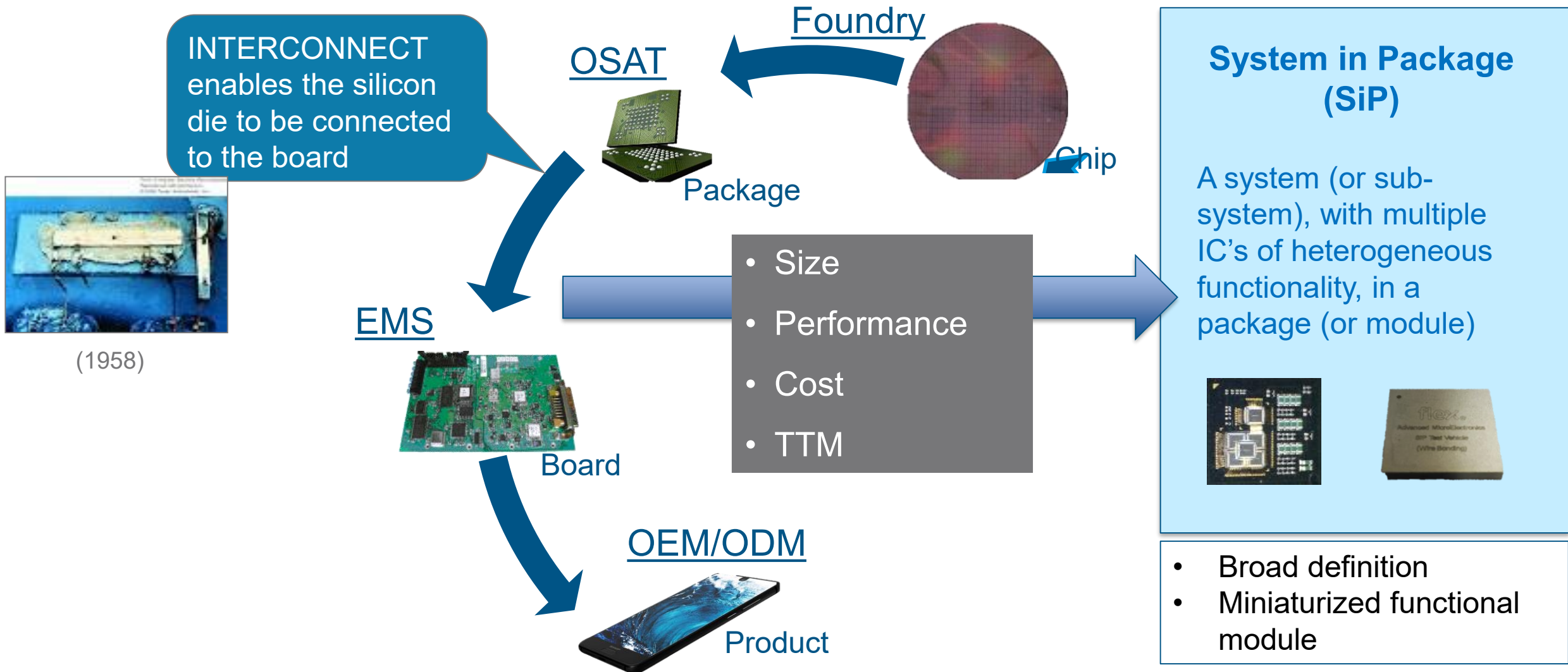
... towards cost effective solutions for SiP and miniaturized functional modules from technology to commercial products





SiP Overview

Microelectronics Packaging



Benefits of SiP

Miniaturization

small form factor / higher functional density

Modular Solution

for specialization, re-usability, and upgradability

- Pre-certification
- Yield management (known good sub-system)

Very Diverse

in complexity & configuration

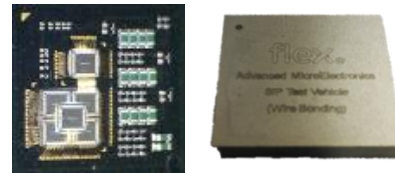
Numerous Applications

in different market segments

Faster

time to market as compared with SOC

- Design flexibility



Lower

total system cost

Higher Performance

through shorter interconnect paths

- Latency / bandwidth / power

Opportunity

for differentiation, optimization & value-add

More than Moore

Heterogeneous Integration

different functionalities and fab nodes

- Each die optimized based on its merits - for cost effectiveness
- Simplified IP ownership, testing, ...
- "Disintegration at the die level and integration in the SiP"
- Flexibility - "Mix & match"

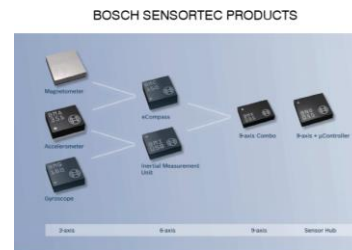
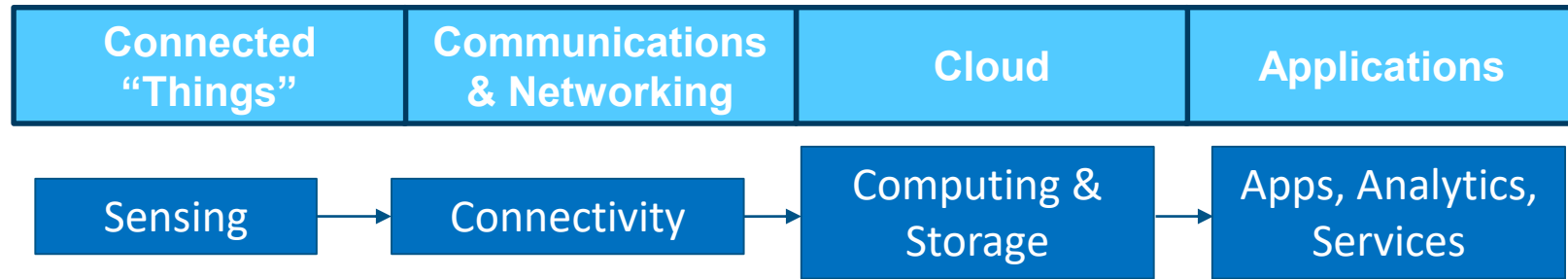
Market Demand for Miniaturization & Modularization (Example)

IoT Module

- Sensor(s)
- MCU / AP
- Connectivity
- Memory
- Power

Market Drivers

- Low Cost
- Low Power
- Miniaturization
- Modularization
- Ease of design & integration



Reason for SiP Adoption

Item	Percentage specifying item
Form factor/miniaturization	100%
Low Power	36%
High Performance	64%
EMI noise reduction	36%
Total cost reduction	57%

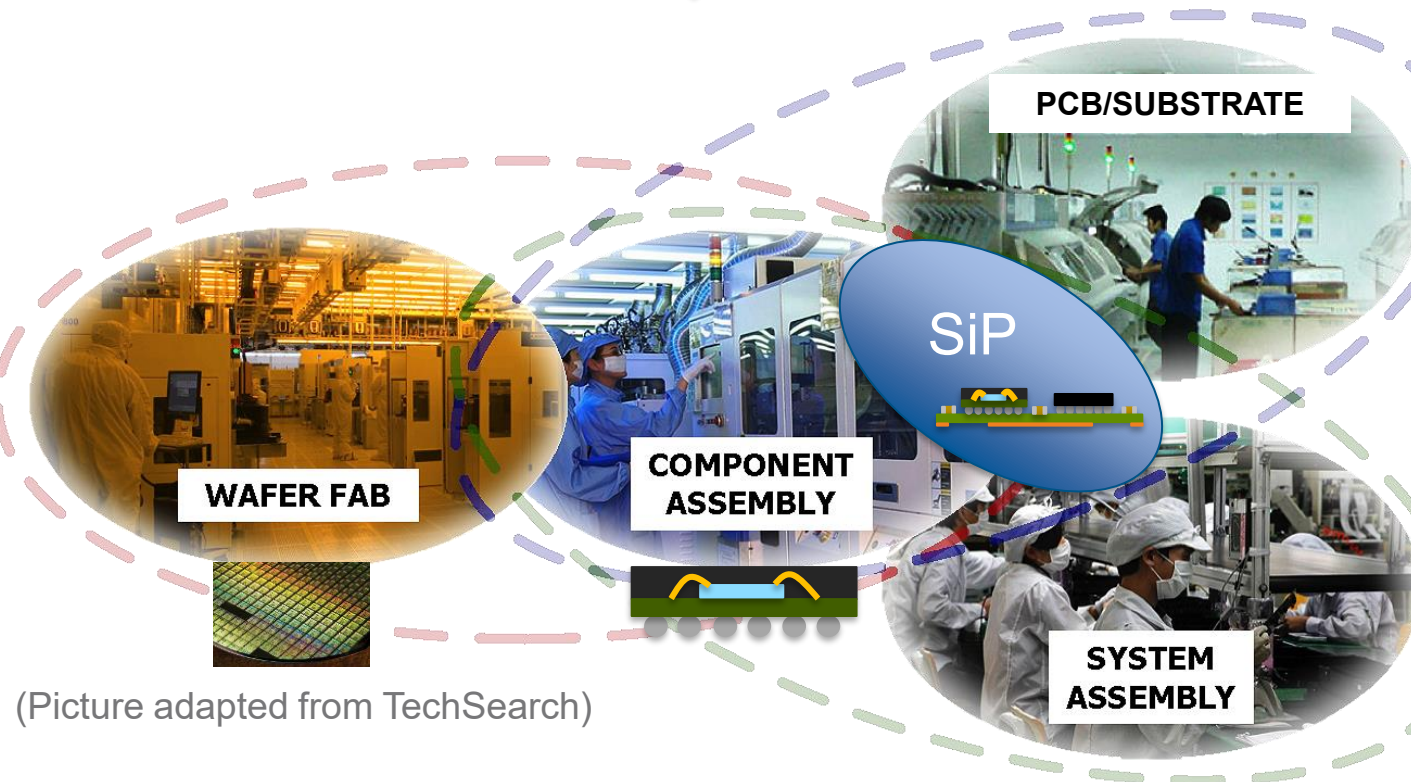
Source: TechSearch International, Inc.

(Pictures from various sources)

The background of the slide is a dark blue color with a complex, light blue technical drawing or circuit board pattern. The pattern consists of various geometric shapes, including rectangles, circles, and lines, some of which are interconnected to form a network-like structure. The lines are thin and light blue, creating a subtle, futuristic aesthetic.

Industry Landscape

Industry Landscape



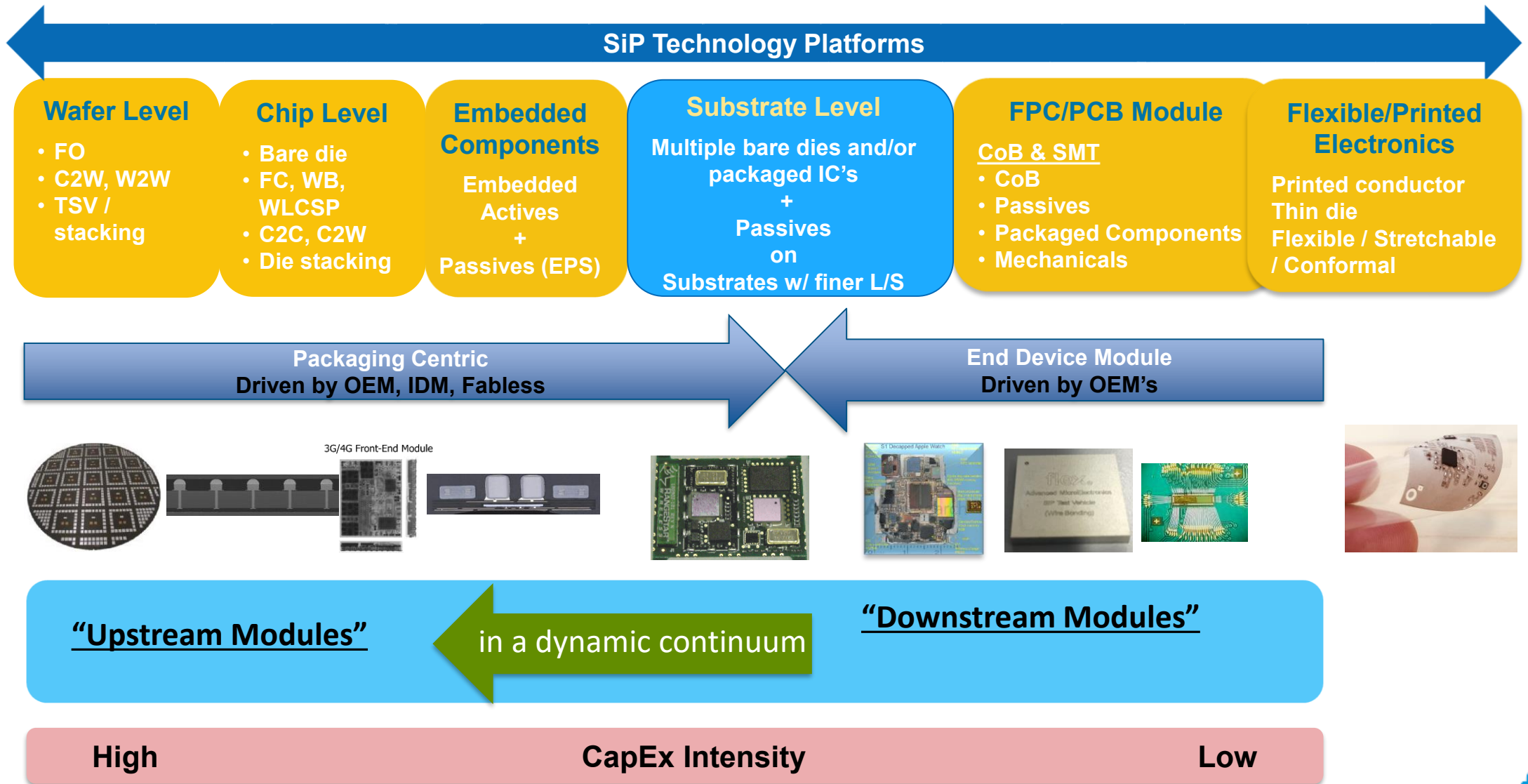
(Picture adapted from TechSearch)

Flex Strength in SiP

- Multi-disciplinary, multi-industry knowledge
- System level expertise
- OEM relationships
- Eco-system & supply chain
- Existing SMT asset and expertise
- Global footprint & scale
- Operational excellence
- Certifications (auto, medical, ...)
- One stop turnkey solution
(SiP + PCBA + System Integration)

SiP optimization creates opportunities in system cost and performance

Technology Landscape



SiP and Module

- **SiP is the technology; Module is the device**
- **They can have many different configurations and processes**
 - Depending on the application requirements
 - Performance, size, cost, ...
 - Opportunity to optimize
- **Need to pass MSL**

- Organic substrate
- Ceramic substrate
- Si substrate
 - With TSV
 - Without TSV
- Leadframe
- Fan-out
- Printed flexible
- ...

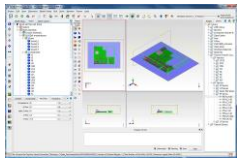


Competency Development

Competency Development

Design

- Product platforms
- Package architecture & configuration
- System design / electrical
- Substrate layout
- Mechanical / thermal / Reliability
- JEDEC/MIL standards



Process Development

- Technology Roadmap
- Design rules
- Qualified materials
- Equipment selection
- Process Characterization
- Reliability & FA



- High density SMT
 - Fine pitch FC/CSP
- Wafer handling
- D/A, W/B
- Molding / Shielding
- Ball attach
- Singulation, T/R

Test Development

- Structural
- Functional
- RF / Digital
- Diagnostic / FA
- Component level / System level

Test programs
Tester / Handle
Fixture



Proto & NPI

- Process Qualification
- Process Control Plan

Volume Manufacturing

- Quality management
- Line configuration
- LEAN
- Automation



SiP Design & Development Cycle

Architecture /Schematic

Package design

Engineering build

Test development

Qualification / NPI

Mass Production

Schematic design/simulation
BOM optimization

Package architecture
Netlist input
Floor plan
Layout
Simulation
Design optimization

Assembly instruction
BOM readiness

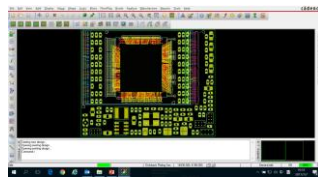
Test strategy
Test program
Hardware design /
Fabrication

Qualification build
REL testing
Line audit

Yield improvement
Cost reduction

Layout Tools

Cadence SIP Layout XL
Cadence SIP RF option



Simulation

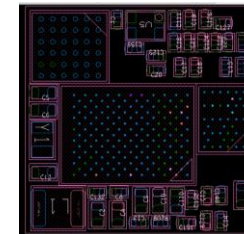
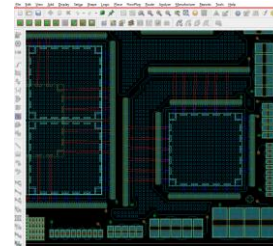
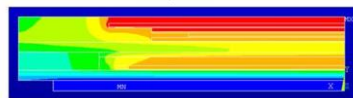
SI/PI

Sigrity XtractIM
Power SI
Power DC



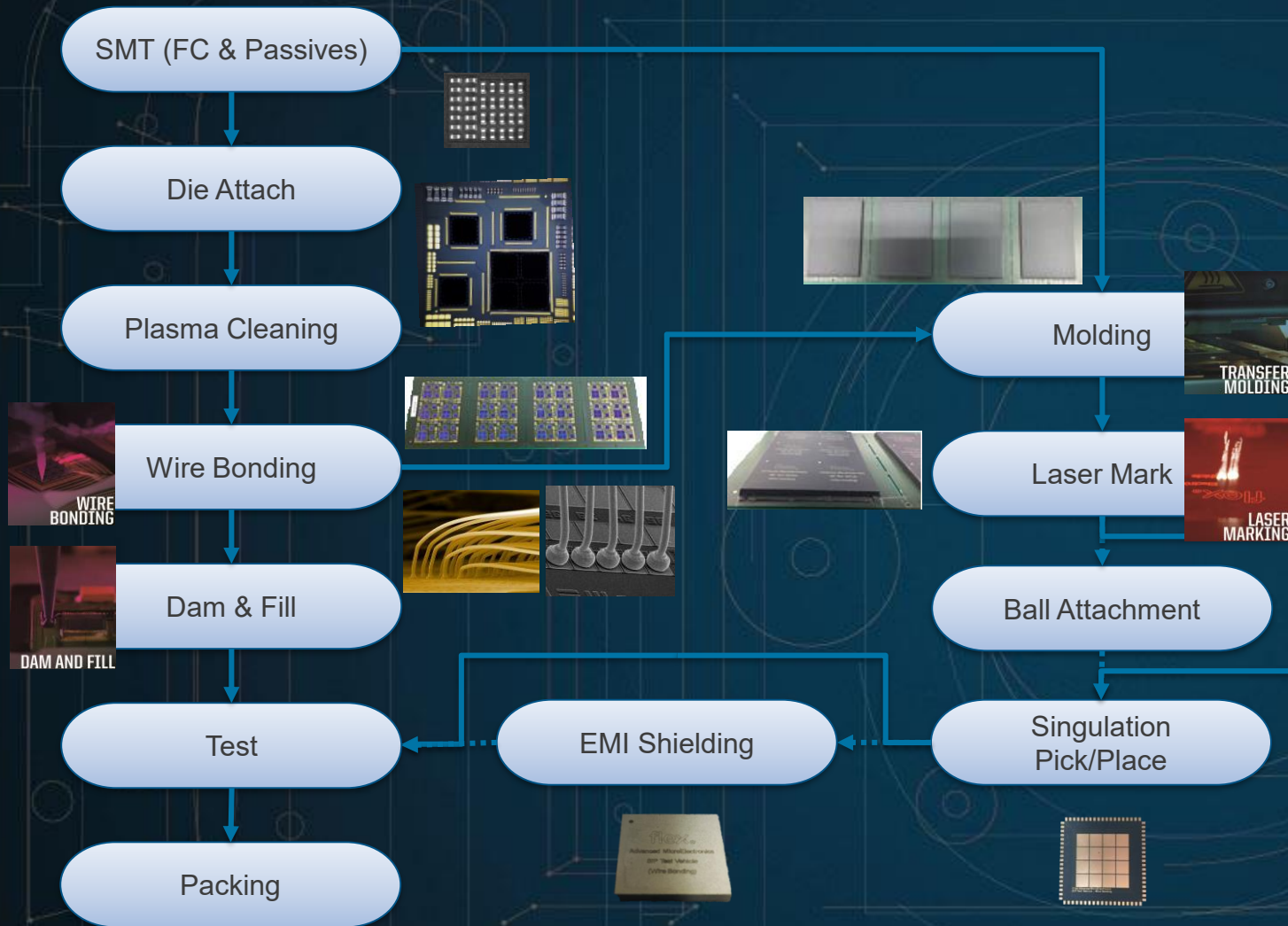
Thermal

Flotherm



(Example)

SiP Processes



- High thermal conductivity (>100W/mK) D/A
- High precision D/A
- Fine pitch wire bond for Au & Al
- Die stacking
- Fine passive component placement
- Fine pitch FC / CSP
- Fine filler (<20um) mold compound (MUF)
- Conformal EMI

(Example – for illustration only)

Miniaturization & Functional Densification

Design

Advanced design rules
Fine L/S
Fine pitch FC

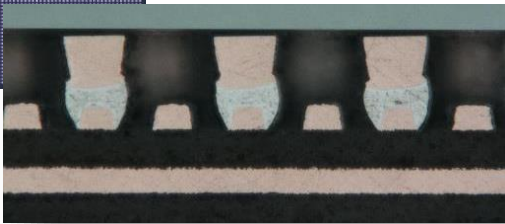
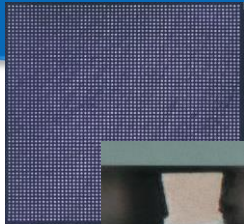
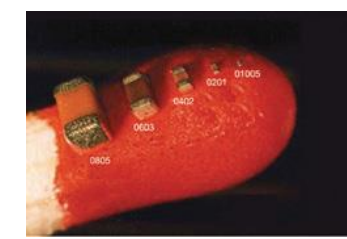
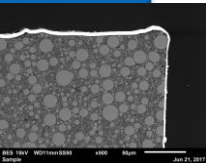
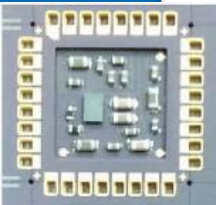
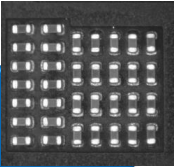
Miniaturization

Processes

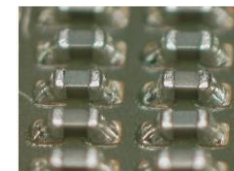
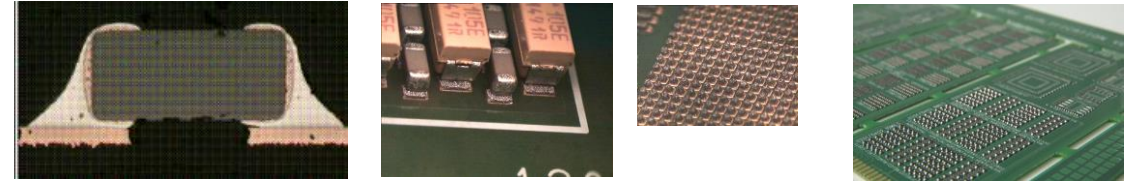
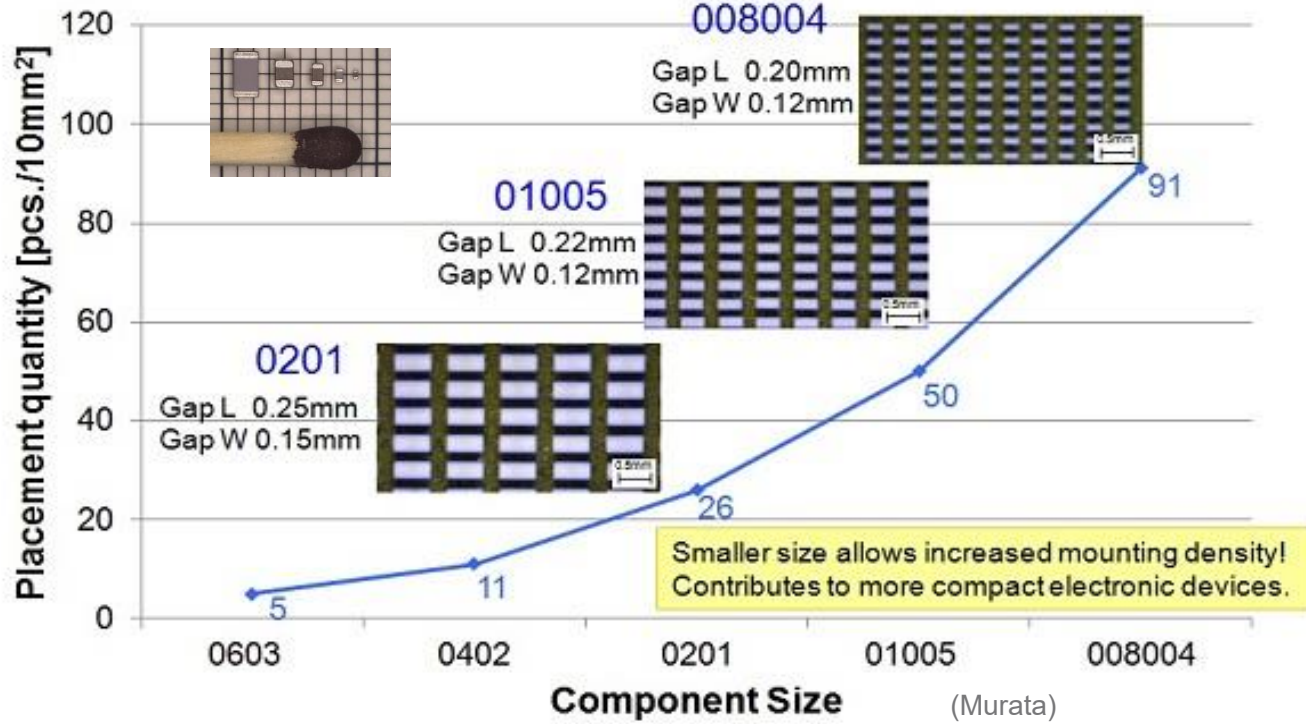
Advanced SMT
Bare die (FC, WB)
Cavity
Underfill (CUF/MUF)
Thin Molding
EMI

Materials

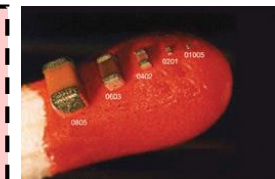
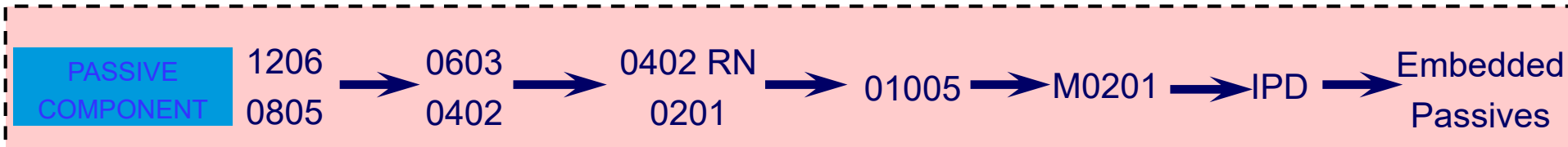
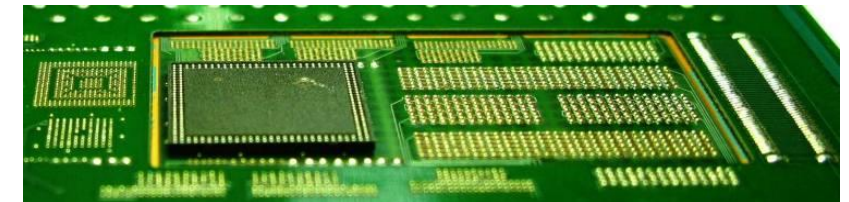
Thin Die
Passives (0402 → 008004)
Substrate (thin & fine L/S)
MUF (Fine fillers)
Paste (fine particles)



Small Passive Components



Cavity Assembly



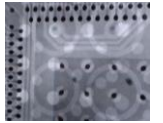
16 Example



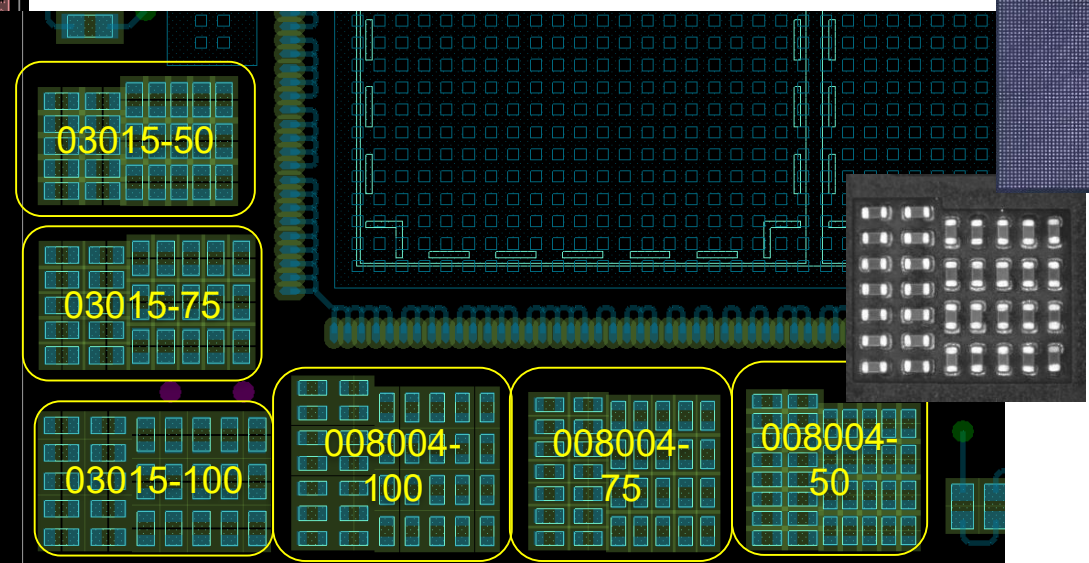
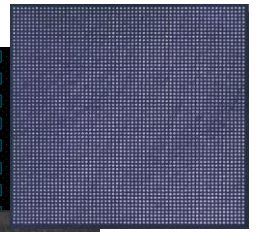
Key features

- Wire bonding & Flip chip (150/100um pitch)
- Die stacking
- SMT: 03015 and 008004 passives @ 100/75/50um spacing
 - Mixed with large components
- CUF & MUF
- EMI conformal shielding

100um pitch FC after reflow
6x6mm Cu Pillar

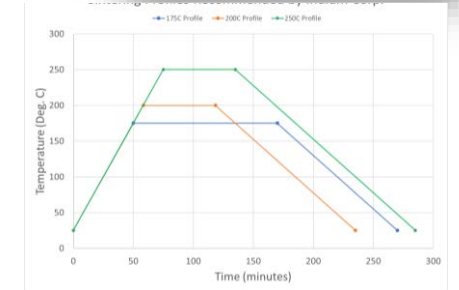
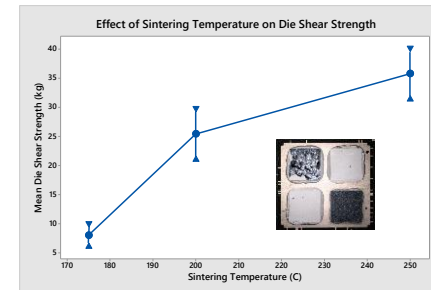
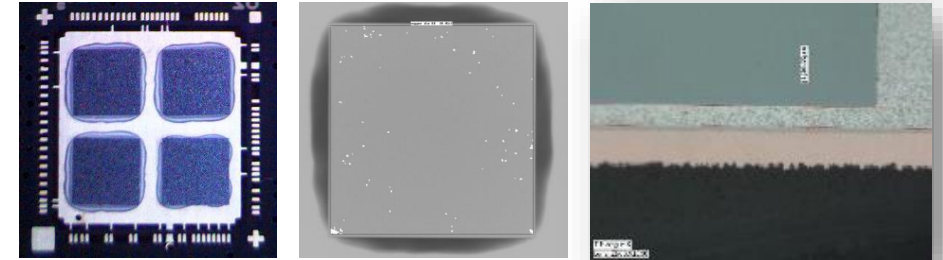
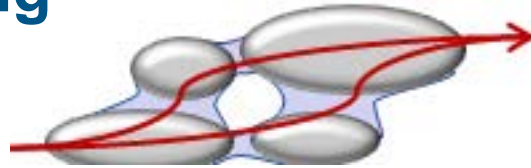


150um pitch FC
10x10mm full array >3700 I/O



High Thermal Conductivity Die Attach (example)

- Nano-Ag
- Thermal Conductivity: >100 W/(mK)
- Paste dispensing process for D/A
 - Consistent bond line thickness (0.8-1 mil)
- Pressure-less sintering
 - Voiding $<5\%$
- Die Shear
 - Consistent after MSL / 260C reflow
- Can withstand 260C reflow
- Can withstand 1000 T/C
 - Consistent die shear strength
 - No delamination



Thermal Cycling

• IPC 9701-A Standard TC3 / NTC-C Profile.

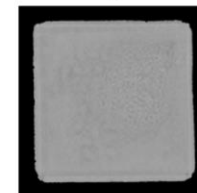
• - 40C to +125 C

• 15 mins dwell time

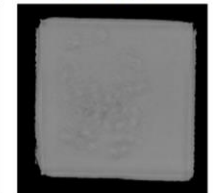
• 1000 Cycles

C SAM Analysis does not reveal any delamination defect even after 1000 Thermal Cycles

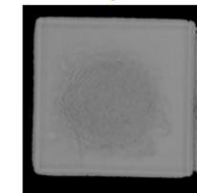
250 cycles



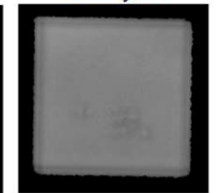
500 cycles



750 cycles

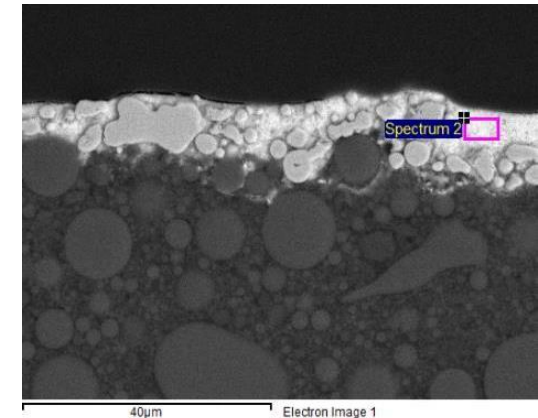
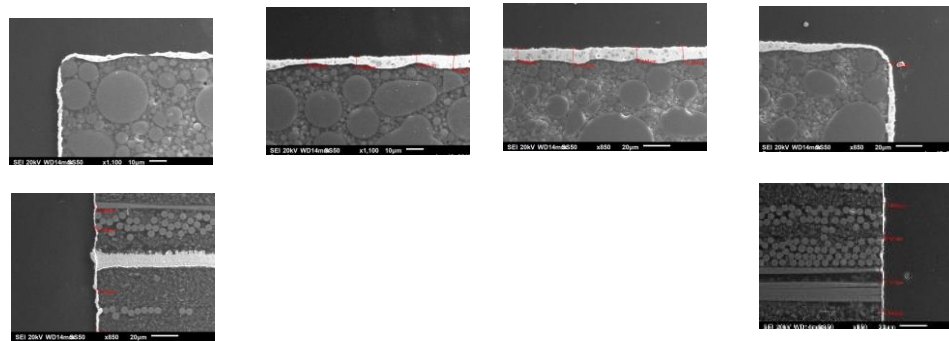


1000 cycles



EMI Shielding

- Metal can
- Sputtering
- Spray



Characterization

- Thickness uniformity
- Adhesion
- Electrical Resistance
- Shielding Effectiveness

Reliability Testing

- MSL
- HTS
- T/RH
- T/C

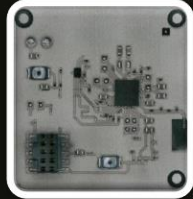
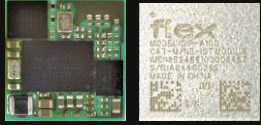
Performance

- Shielding effectiveness
- Durability
- TCO
 - Materials
 - Capex
 - Throughput, Yield

SiP Competency

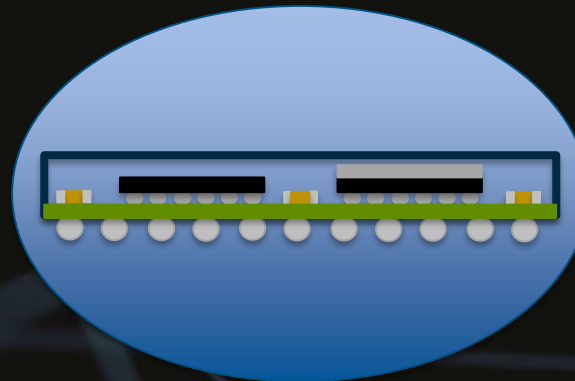
MODULE DESIGN

- Substrate Design
- Package Design
- Electrical / Thermal / Mechanical Simulation
- Thermal Management



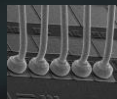
VOLUME MANUFACTURING

- Certification (automotive, medical, ...)
- Low/medium/high volume
- Lean manufacturing
- Cleanroom management
- Global footprint



ASSEMBLY PROCESSES

- High Density SMT
- Wire Bonding
- Flip Chip
- Die Stacking
- Underfill (CUF/MUF)
- Transfer Molding
- Ball attach
- EMI shielding
- Marking / Singulation



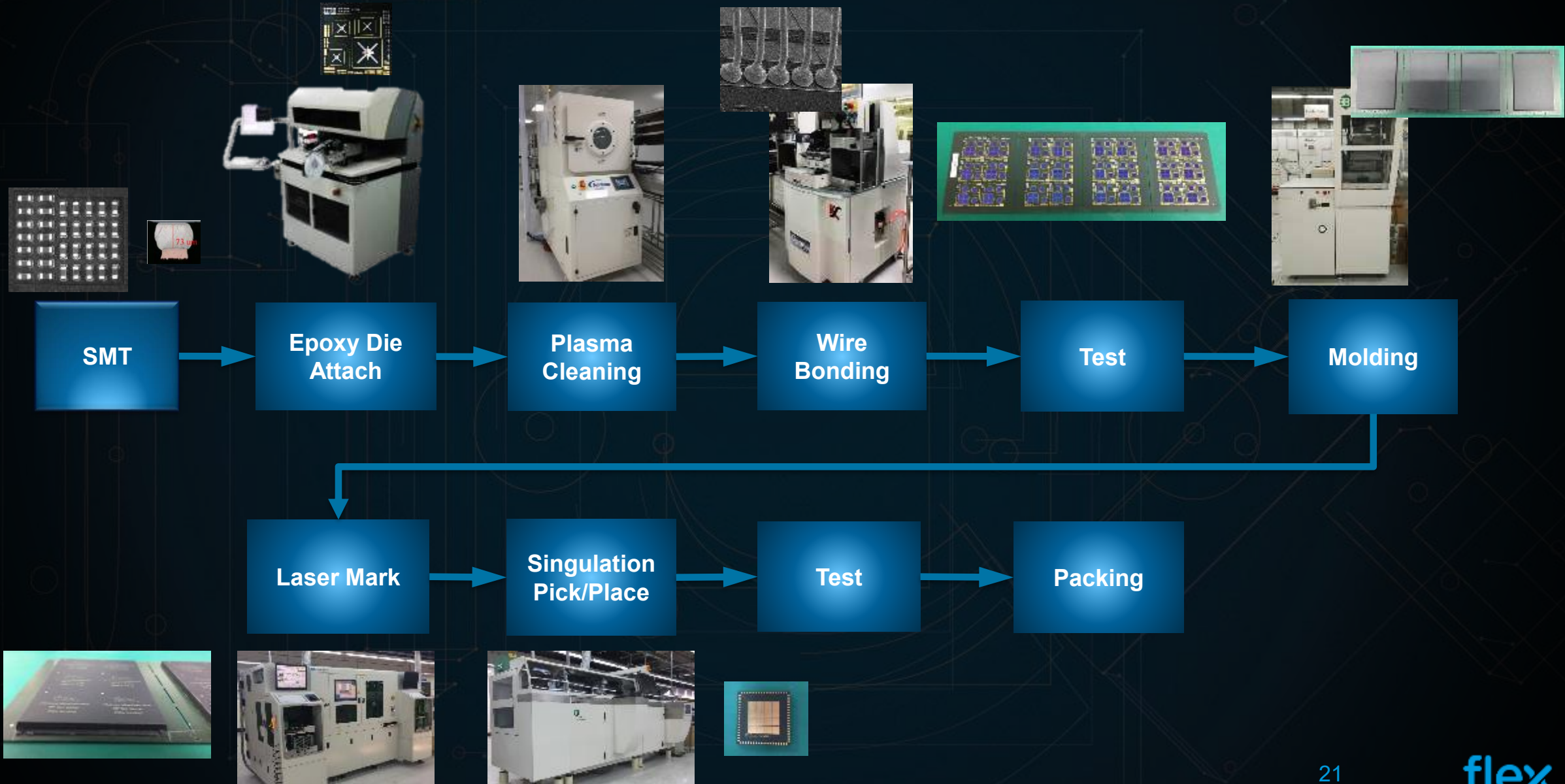
RELIABILITY & FAILURE ANALYSES

- JEDEC, MIL REL tests
- Comprehensive failure analyses

TEST

- Structural / Functional
- RF / Digital
- Diagnostics / FA
- System level test (SLT)
- Tester / Handler / Fixture

SiP Processes



Bump on Trace (2003 paper)

Assembly Processes for Flip Chips on Substrates

THIS PAPER PROVIDES NEW DATA ON ASSEMBLY OF SOLDER FLIP CHIP DEVICES.

BY DAVID A. GEIGER, JONAS SIOBERG, PATRICK WONG AND DONGKAI SHANGGUAN

Flip chip assembly is a key capability to enable product miniaturization. Our previous studies have investigated several flip chip interconnection types, including anisotropic conductive film or paste, and Au-Au thermosonic bonding. This project focuses on the assembly of 0.200- and 0.250-mm-pitch solder flip chip devices. Two methods of applying flux for the flip chip are investigated: the dip fluxing method, and jet fluxing of the substrate. The placement accuracy of a traditional SMT pick-and-place system (upgraded for flip chip) is investigated and the results are discussed. The impact of the reflow process in air vs. nitrogen is also examined. Two underfill materials are evaluated for compatibility with the flux. Results of reliability testing (including thermal cycling, mechanical shock and vibration) are presented.

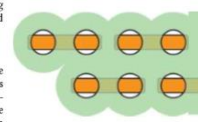


Figure 1. Area array land pattern

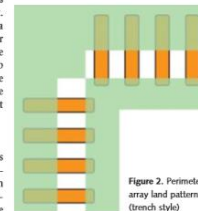


Figure 2. Perimeter array land pattern (trench style)

Component Selection

The components selected for this study are shown in Table 1. Flip chip components are all daisy-chained die to allow continuous checks throughout the process. The die substrate is nitride on all the flip chip pads. For the PB-8 flip chip, the UBM is 82 µm in diameter, and the bump is 120 µm in diameter and 95 µm in height. The FA-10 and the PST01 flip chips have a UBM diameter of 102 µm, bump diameter of 135 µm, with a height of 120 µm. All the solder bumps in this study are Sn/Pb eutectic alloy. The other components are surface mount type parts that may be found on a similar device that this test vehicle emulates.

Test Vehicle Design

The test vehicle is a module format that is 28.575 × 22.225 mm in size. It is then partitioned in a 127 × 177.8 mm panel with 20 modules per panel. The board is 6 layers with a total thickness of 0.5 mm. The

board material is FR-4 ($T_g = 140^\circ\text{C}$, $\text{CTE}_x, y = 12\text{-}16 \text{ ppm}/^\circ\text{C}$). The surface finish is an electrolytic nickel and immersion gold (ENIG), with 3.81-5.08 µm for the Ni thickness and 0.0762-0.203 µm for the Au thickness over the nickel. The components are on a single side, allowing one SMT process step; however, the module was designed so that it can accommodate solder spheres on the secondary side.

The land patterns for all the surface mount components are standard land patterns, including the 0201 component.

For the flip chip, two types of land patterns were used. For the perimeter array type and the other for the full area array. For the area array packages (0.250-mm pitch), the land pattern was designed as shown in Figure 1. This land pattern will only work for this daisy chain sample; if a real part is to be used, then the copper would need to be changed to an individual pad and would need to contain a micro-via in order to route. For the perimeter array package, a trench-type design was used (Figure 2). This land pattern was used for the PB-8 (0.200-mm pitch) and the PST-01 (0.250-mm pitch) devices.

Experimental Work

Incoming Inspection. The die and the boards were inspected prior to running any boards for the study. For the die, some defects were found, including missing solder spheres, damaged solder spheres and contamination (Figure 3). The defective samples were removed from the build.

Solder Paste & Fluxing Materials. The solder paste used for surface mount parts is a typical eutectic Sn/Pb solder paste. For the flip chip parts, two types of fluxes and

Method of Providing a RF Shield of an Electronic Device (Filed 2008; Granted 2011)



US007971350B2

(12) **United States Patent**
Joshi

(10) **Patent No.:** US 7,971,350 B2
(45) **Date of Patent:** Jul. 5, 2011

(54) **METHOD OF PROVIDING A RF SHIELD OF AN ELECTRONIC DEVICE**

(56) **References Cited**

(75) Inventor: **Rajeev Joshi**, Cupertino, CA (US)
(73) Assignee: **Flextronics AP, LLC**, Broomfield, CO (US)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 169 days.

Primary Examiner — C. J Arbes
(74) Attorney, Agent, or Firm — Haverstock & Owens LLP

(21) Appl. No.: 12/221,256
(22) Filed: Jul. 31, 2008

(57) **ABSTRACT**
A shielding assembly is configured to provide electromagnetic shielding and environmental protection to one or more electronic components coupled to a substrate. The shielding assembly includes a non-conductive mold compound layer, such as a dielectric epoxy. The mold compound layer is applied to a top surface of the substrate, thereby covering the electronic components and providing protection against environmentally induced conditions such as corrosion, humidity, and mechanical stress. The shielding assembly also includes a conductive layer applied to a top surface of the mold compound layer. The conductive layer is coupled to a ground plane in the substrate, thereby enabling the electromagnetic shielding function. The conductive layer is coupled to the ground plane via one or more metallized contacts that are coupled to the substrate and extend through the mold compound layer.

(65) **Prior Publication Data**
US 2009/0032300 A1 Feb. 5, 2009

(58) **Field of Classification Search** 29/825, 29/830, 832, 840, 852, 841; 257/734
See application file for complete search history.

(100) **Related U.S. Application Data**
Provisional application No. 60/963,115, filed on Aug. 1, 2007.

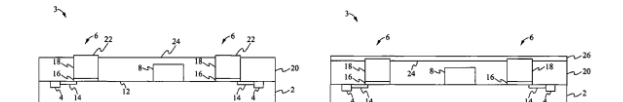
(51) **Int. Cl.**
H05K 3/00 (2006.01)

(52) **U.S. Cl.** 29/841; 29/832; 29/840; 257/734

(58) **Field of Classification Search** 29/825, 29/830, 832, 840, 852, 841; 257/734
See application file for complete search history.

(100) **Related U.S. Application Data**
Provisional application No. 60/963,115, filed on Aug. 1, 2007.

(51) **Int. Cl.**
H05K 3/00 (2006.01)



29 Claims, 4 Drawing Sheets

Inline PoP

San Jose Lab (2002)

Production (2003)

IEEE IEMT Paper (2003)

Package Stacking in SMT for 3D PCB Assembly

David Geiger, Dongkai Shangguan, Samuel Tam, and Dan Rooney
Flextronics
San Jose, CA, USA

Abstract
The need for continued miniaturization, functional densification and integration in handheld electronics products provides the strong incentive for printed circuit board (PCB) assembly in three-dimensions (3D). One way to accomplish 3D assembly is through the use of die stacking in chip scale packages (CSP), where the dice are stacked internally in the package. The other way to accomplish 3D assembly is through the use of package stacking. This is the process where two packages are placed on top of each other during the traditional surface mount placement process and then soldered together during the SMT (surface mount technology) reflow. In this paper, package stacking as part of the SMT process is described. The process, materials, and solder joint formation are characterized, and key issues highlighted.

Key words: CSP Stacking, Ball Stacking, Package Stacking

Introduction
Die stacking inside a package is one way to increase the functionality per unit area on a PCB assembly. However, there can be some drawbacks to creating a stacked package solution. First, this method is a customized solution. If any of the dice to be used changes, the die stack needs to be evaluated to see if any changes are needed in the package. For example, a die shrink may occur which could change the whole package structure. Second, each package is tested as a whole unit. If one or more of the dice fail, the whole unit will have to be scrapped, which would lead to increased cost. This is the well known "compounded yield" issue. Lastly, trying to coordinate the many semiconductor suppliers to provide dice to a packaging house to do the die stacking can be a challenging task.

With the advent of package stacking, some of these issues are addressed. Each package is a single unit that can be fully tested as a normal IC package is done today, so the yield would be comparable to the normal yield commonly seen today. Another advantage would be the ability to have second source options that could be easily inserted into the process. The stacked package can be processed in a traditional SMT environment with a few upgrades that are readily available.

Therefore, package stacking enables configurable assemblies and provides greater flexibility in supply

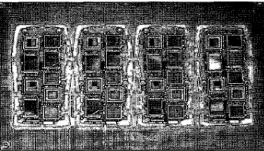


Figure 1. Test Vehicle

Several package types have been evaluated with the test vehicle, including over-mold and under-mold types of packages (Figures 2 and 3). The packages evaluated range in size from 10x12mm up to 12x16mm. The pitches range from 0.5 to 0.8mm, and the I/O goes from 34 all the way up to 300+. The bottom package is designed so that the top package will match up with it. The bottom package has a pad on the top for the top package to be surface mounted. Both solder mask defined (SMD) and non-solder mask defined (NSMD) pads have been evaluated for the top and bottom packages.

Each package may contain multiple dice. The parts were daisy chained and a matching daisy chain pattern was designed into the board.

Both Sn/Pb and lead-free versions of the packages were assembled. The Sn/Pb package used eutectic

2003 IEEE CPMT/SEM Int'l Electronics Manufacturing Technology Symposium

2000

2010

2016

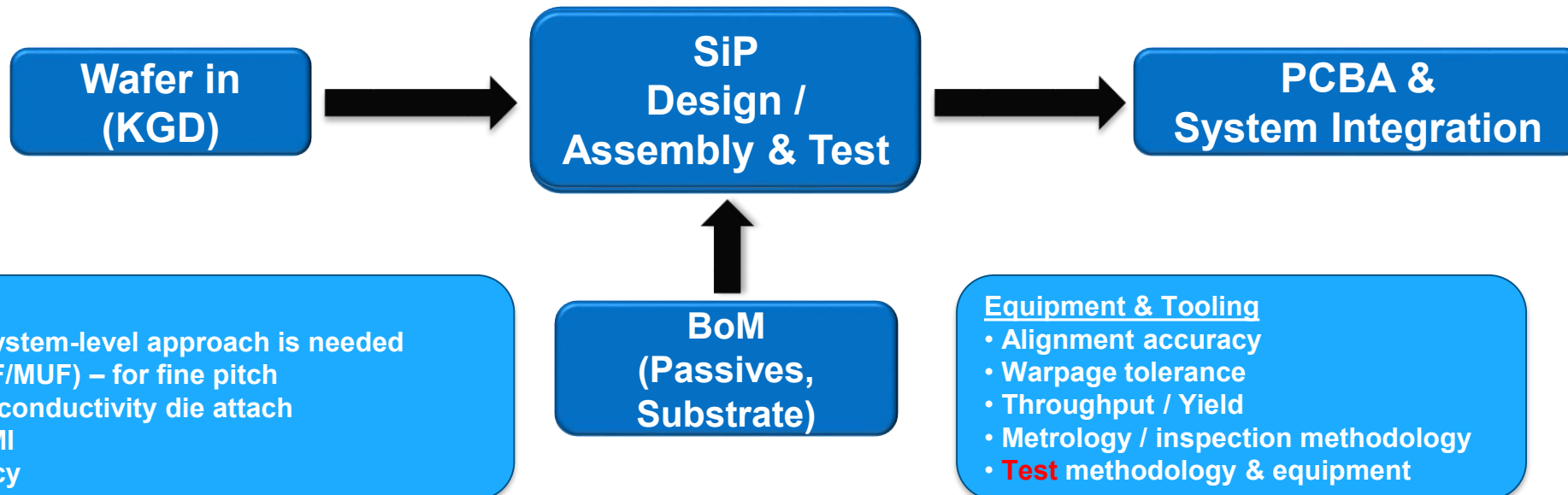
Supply Chain Focus Areas (examples)

Design

- EDA tools & design guidelines
 - Cross domain, multi-physics
- Architecture & partition
- Silicon-Package-PCB co-design
- Electrical: SI/PI/EMI
- Thermal: high density, heat flow path, space constrain, transient
- Mechanical: stress during assembly process and usage, warpage
- Reliability
- **System level total optimization**

Value Chain

- Cost (system cost, TCOO)
- KGD...Tolerance stack-up
- Multiple IC vendors
- Process flow & partition
- Inter-operability
- Infrastructure
- Standards & specifications
- Convergence, Integration, and Business Model



Materials

- Warpage: a system-level approach is needed
- Underfill (CUF/MUF) – for fine pitch
- High thermal conductivity die attach
- Conformal EMI
- High frequency

Equipment & Tooling

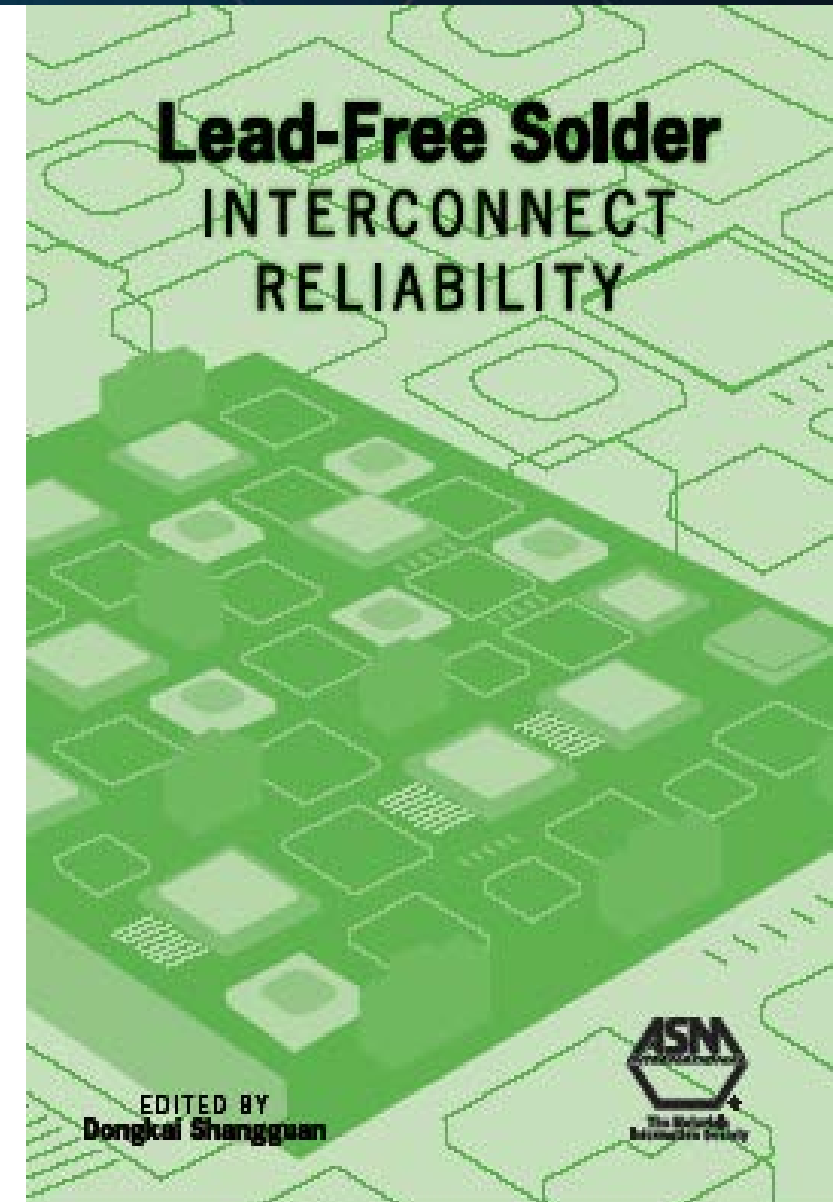
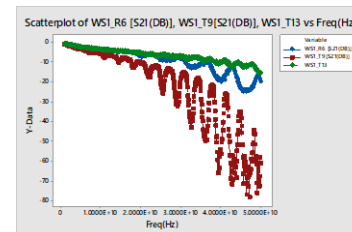
- Alignment accuracy
- Warpage tolerance
- Throughput / Yield
- Metrology / inspection methodology
- **Test** methodology & equipment



Reliability & High Frequency Performance

Reliability ~ Miniaturization

- Smaller solder interconnects – more susceptible to thermomechanical failures
- Higher current density – electromigration
- Tighter spacing – solder extrusion, whiskering, ...
- Importance of the interface as the solder volume decreases
- Interfacial IMC's
- Heterogeneous integration and diversity of packaging methods (devices, materials, interfaces) in the same module – more complex (often interactive) reliability failure modes and mechanisms
- Process yield
- Electrical – cross talk, EMI.....in the 5G era
- Thermal

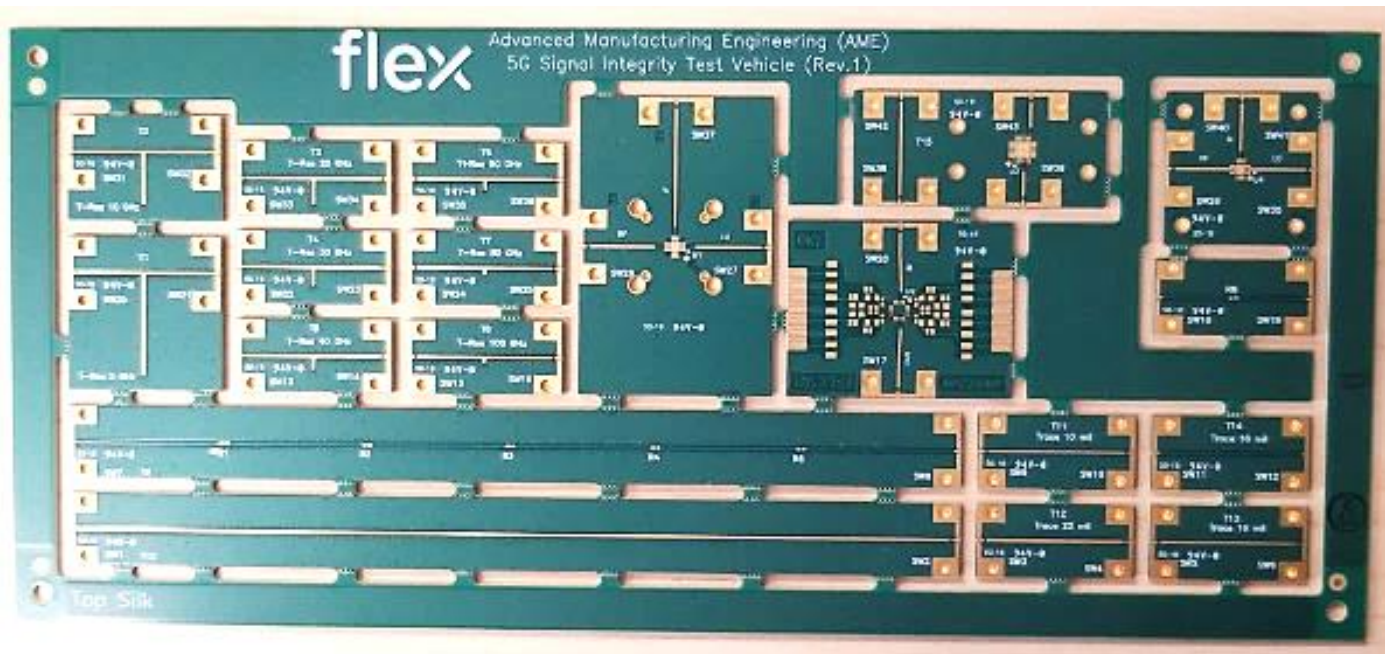


High Frequency Applications

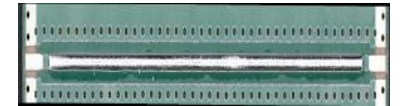
Signal Integrity vs. No-Clean Residue

- No-clean flux residue becomes a concern when products operate at high frequency, as it can provide an alternate path to signals

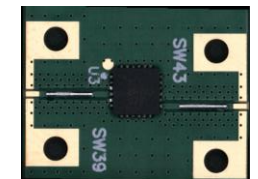
- Initial study (2003): up to 15GHz
- New study (2019): up to 50GHz



- Trace Designs
 - Different Length
 - Different Width
 - Solder Mask vs. Solder
 - Traces with 0Ω Resistors



- Components
 - T-Resonator
 - Band Pass Filter
 - Wideband Mixer
 - Low Noise Amplifier



- Process Variables
 - Water Soluble
 - No Clean
 - Cleaning No Clean Residue
 - Humidity Testing

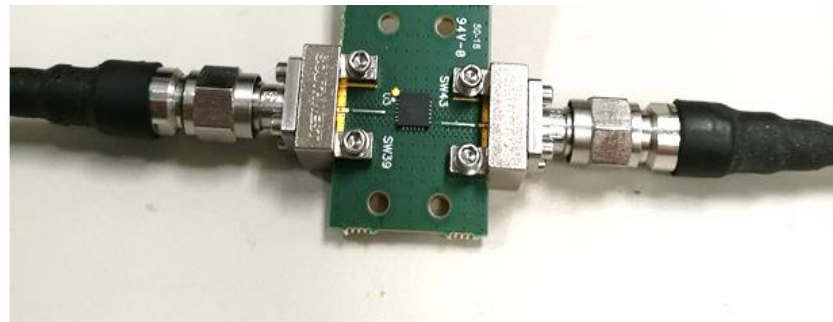
Signal Integrity vs. No-Clean Residue

- **Response Functions: Insertion Loss**

- An insertion loss is considered significant in this study if
 - > 10% change in the signal integrity performance, or
 - or 2dB



Vector Network Analyzer (VNA)



Example of a Device Under Test (DUT)

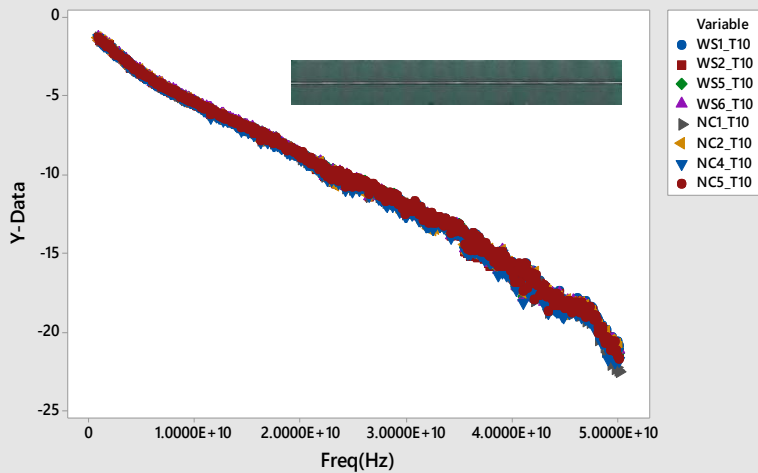
- DoE
- GR&R
- Data analysis

Signal Integrity vs. No-Clean Residue

Preliminary Results (examples)

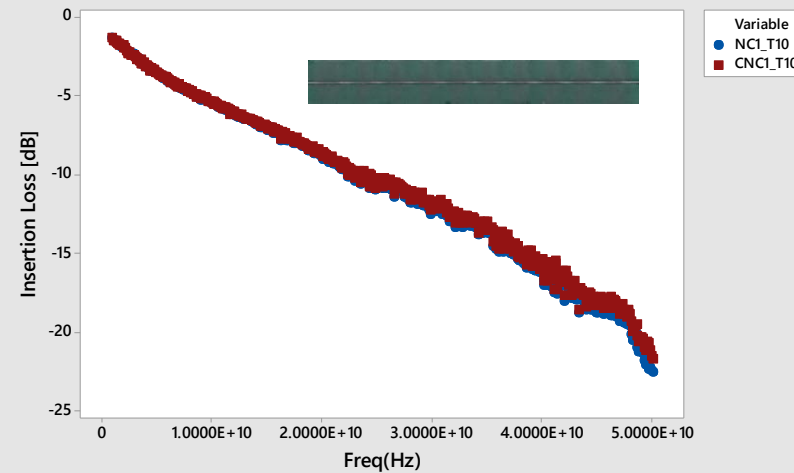
WS vs. NC

Scatterplot of WS1_T10, WS2_T10, WS5_T10, WS6_T10, ... vs Freq(Hz)



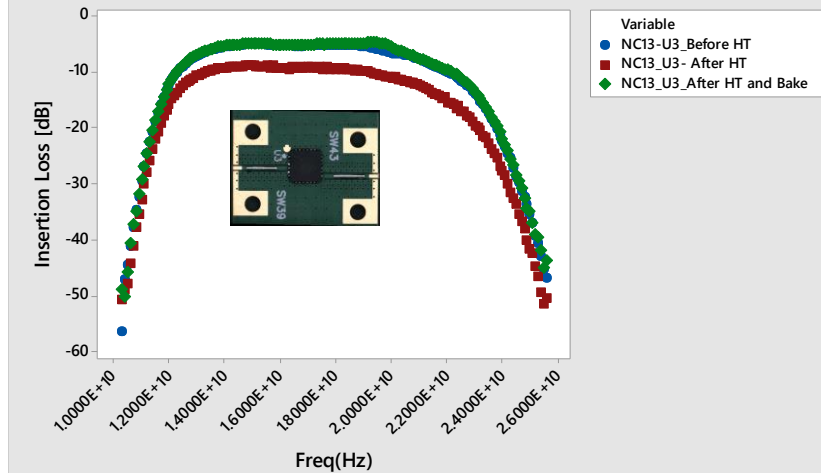
Before and After NC Residue Cleaning

Scatterplot of NC1_T10, CNC1_T10 vs Freq(Hz)



85°C/85%R. H for 168 hours

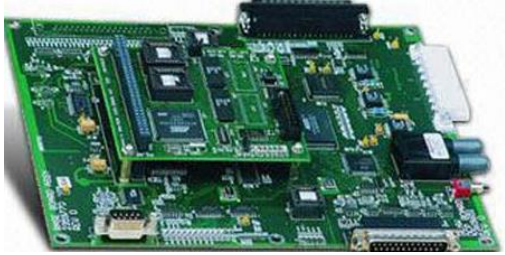
Effect of Moisture on Signal Integrity



- The effect of no-clean residue on signal performance was relatively small and insignificant as compared to other variables such as frequency, design and moisture.
- Higher frequency can result in higher loss, depending on the component design. Wider trace would help to lessen the signal loss when the product operates at high frequency.
- Moisture can be a critical factor resulting in high signal insertion loss and affecting the signal integrity performance.

Flexible Hybrid Electronics

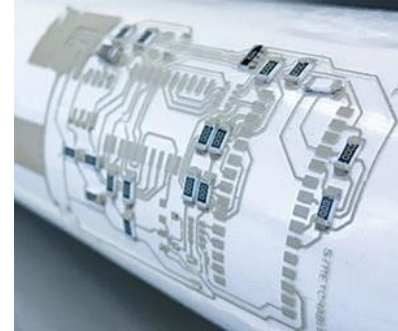
Rigid PCB/Assembly



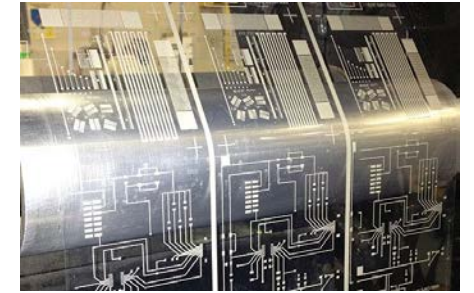
Flexible Printed Circuit



Flexible Hybrid Electronics (FHE)



All Printed Electronics

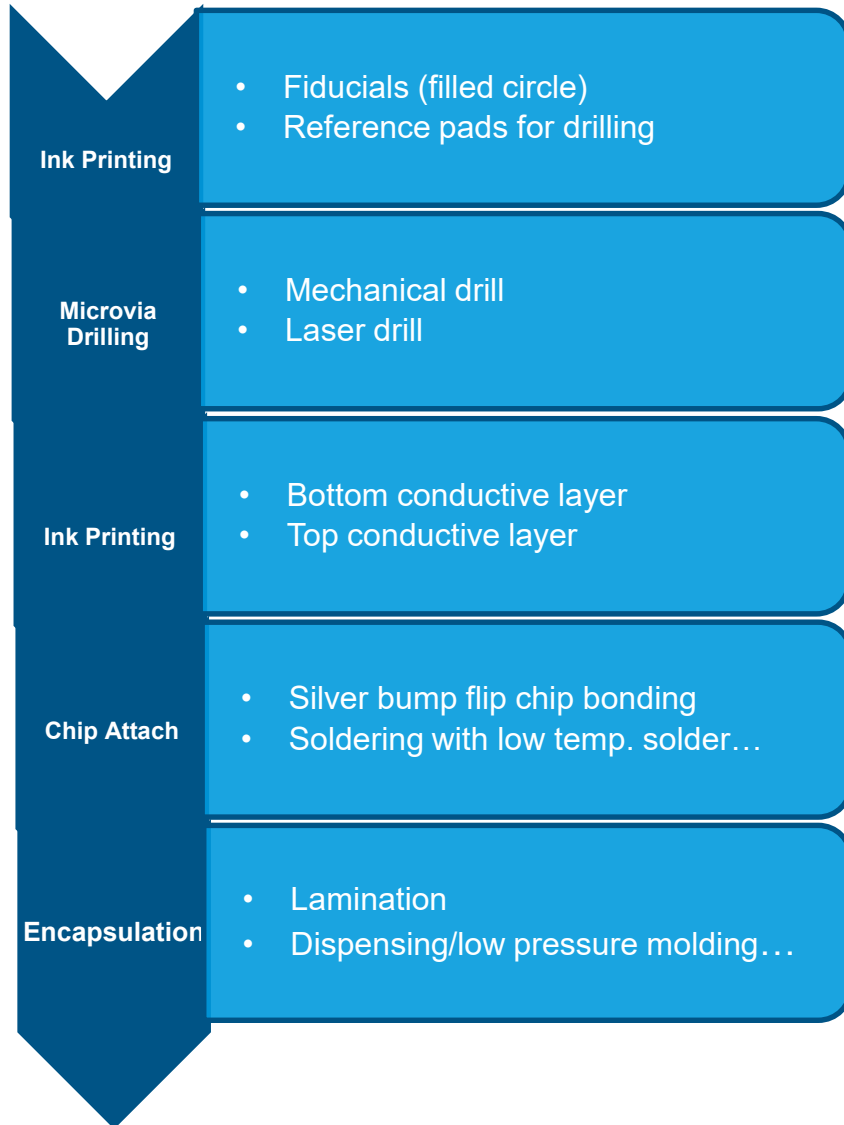
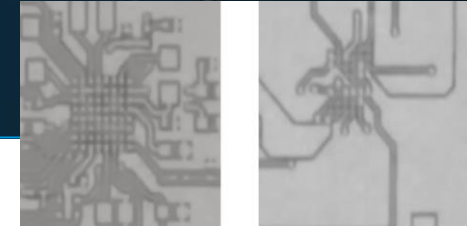


(From various sources)

Benefits of printed electronics

- Flexible/Stretchable/Conformable
 - Electronics on curved shapes/3D objects
- Additive
- Low cost high volume production
- Lightweight
- Bio-compatible

Process Flow



Substrates

- Compatibility with conductive ink
- Mechanical properties: Flexibility / Stretchability / Conformability
 - Low elastic modulus, high elongation
 - Ability to recover from bending, stretching, twisting, or other deformation
- Compatibility: Temperature; Chemical resistance; Electrical;...
- Cost: PI > PC > TPU > PET

Conductive ink

- Resistivity, esp. for power and high frequency applications
- Mechanical properties: Flexibility, stretchability, creasability/foldability
- Process capability: thixotropy, low cure temperature, working life, solderability

Dielectric ink

- Electrical properties: Insulation resistance, dielectric breakdown voltage
- Mechanical properties: Flexibility, stretchability, creasability/foldability
- Process capability: low cure temperature/UV, working life, printing quality
- Reliability: waterproof, high temp./high humidity, sweat resistant

Printing methods

- Screen printing, gravure, flexography, inkjet, aerosol...

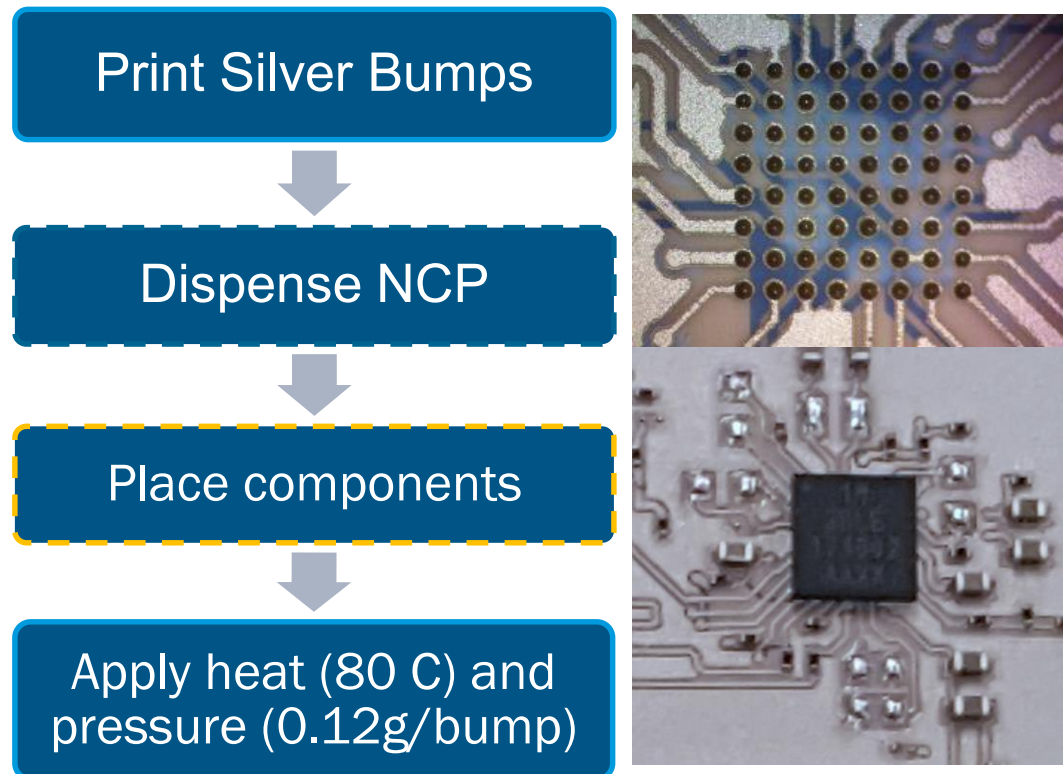
Multi-layer interconnect structure

- Conductive ink/dielectric ink build up
- Micro vias and hole filling



Component Attach

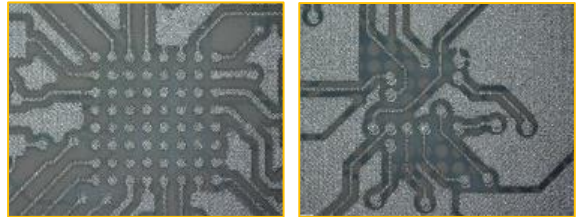
- **Thin chip (<50um thickness) pick & place**
- **Compatibility with conventional assembly process**
 - Solderable ink / Low temperature solder
 - Heat/pressure if ACF/ACP bonding



Printed Flexible Electronics SiP IoT Module Platform



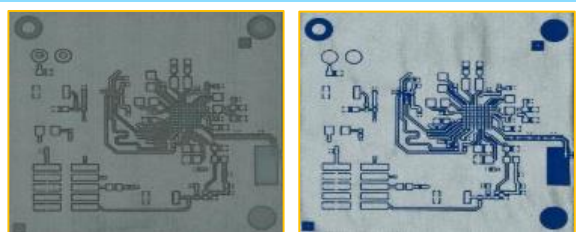
FINE LINE INK PRINTING



- 64 IO's
- 0.4mm Pitch
- 250um diameter
- 100um line width
- 100um spacing

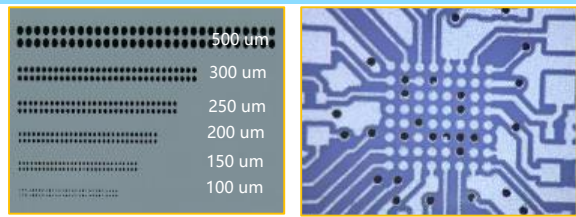
TOP SIDE BOTTOM

FLEXIBLE & STRETCHABLE SUBSTRATE



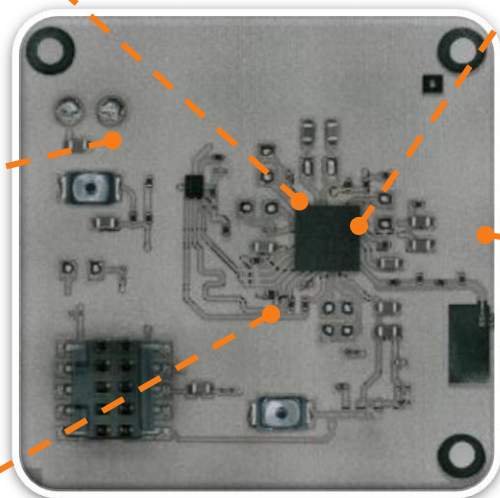
PET TPU

MECHANICAL DRILLING MICRO VIAS



Filled micro vias with conductive adhesive

- 150 um diameter
- 250 um diameter



SOLDERABLE INK w/ LOW TEMP SOLDER

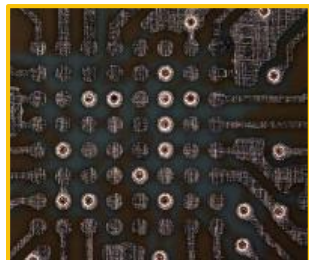


Require fixture with top cover before reflow



FLEXIBLE COPPER CLAD TECHNOLOGY

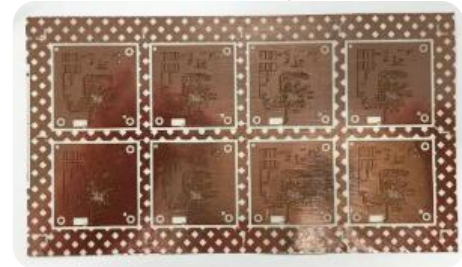
Micro vias with 50um diameter



Test vehicle for copper clad on high temperature flexible substrate

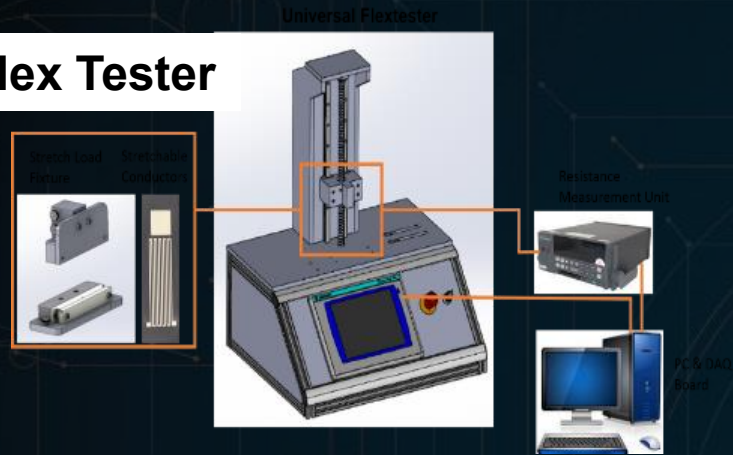
Flexible IOT Module Platform

- Ultra low power platform with Bluetooth LE capability
 - Low power MCU + Bluetooth LE (plus chip antenna)
 - Integrated with accelerometer
- Flexible hybrid technology with multilayer interconnect structure with printed ink
- Flexible copper clad technology



Reliability Testing - FHE

Universal Flex Tester

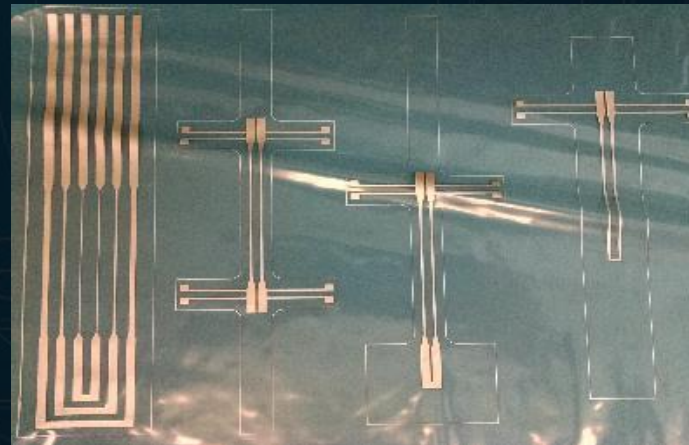


IPC 9204: Flexibility Testing of Printed Electronics

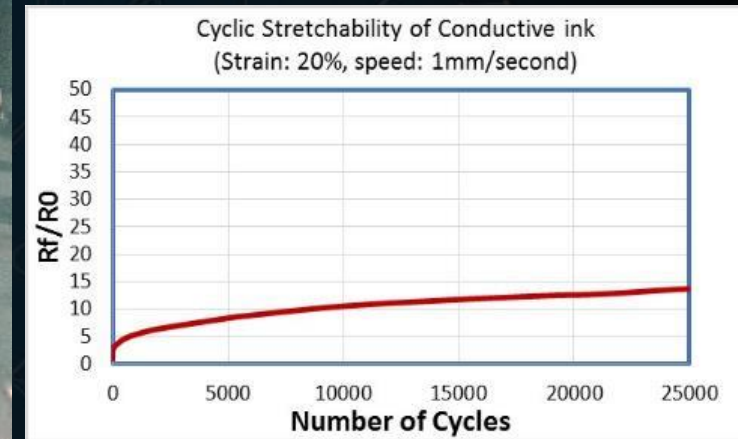
The universal tester can do 9 different tests:

1. Stretchability Testing
2. Variable Radius Bending Test
3. Sliding Plate Flexibility Test
4. Variable Angle Bend Test
5. Variable Diameter Rolling Test
6. Multi Modal Torsion Test
7. Free Arc Bend Test
8. Multi Mode Bend Test
9. Compression Crush Test

Test Coupon



Printed Ink Stretchability



First cycle stretchability

Laundryability of E-Textiles

- **Chemical**

- Water
- Impurities
- Detergent
- Bleach
- Softener

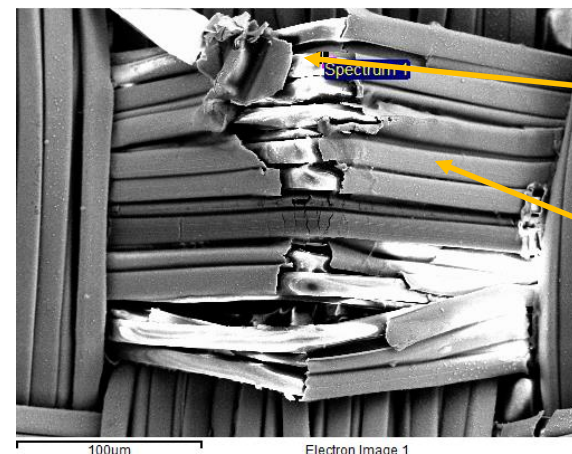
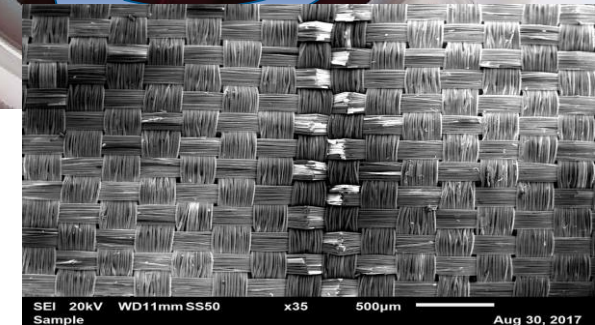
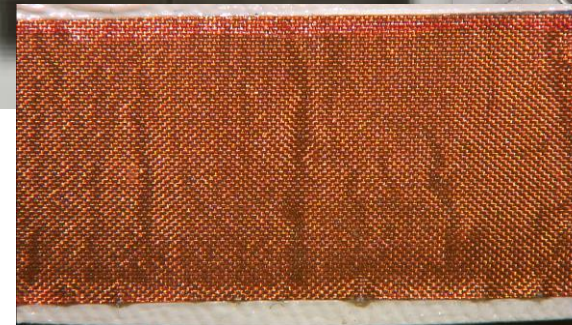
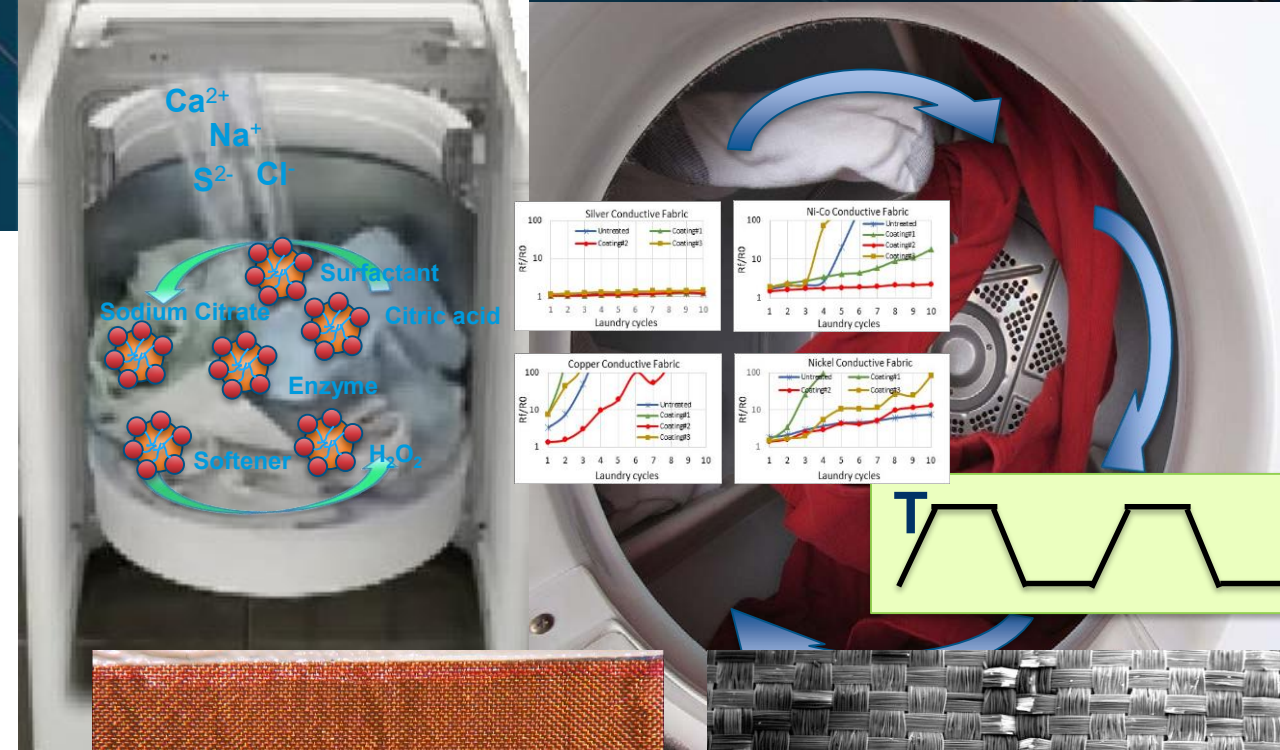
- **Mechanical**

- Water flow
- Abrasion
- Agitation
- Tumbling
- Crumpling
- Torsion
- Bending/folding

- **Thermal**

- Temperature
- Temp. swing

- 10 cycles of washing and drying performed
- Resistance of the conductive fabrics shows increase with laundry cycles. The level of increase depends on the type of fabric:
 - Performance ranking: Silver fabric > nickel fabric ~ cobalt fabric > copper fabric
- With water resistance coatings, resistance of the conductive fabrics continue to show increase with laundry cycles
 - Coating#2 shows certain improvement, especially with Ni-Co and copper fabrics



Element	Weight%	Atomic%
C K	67.46	73.84
O K	31.61	25.97
Cu K	0.93	0.19

Element	Weight%	Atomic%
C K	35.61	70.93
O K	4.25	6.35
Cl K	0.27	0.18
Cu K	59.87	22.54



(Liu, Li, Shangguan et al, 2018)

- What are the factors affecting the e textile laundryability performance?
- What are the mechanisms causing the degradation of e textile materials during laundry (e.g. metal leach into water)?
- What are the design rules to make e textiles robust and laundry proof?

Cost Effective Solutions

Design

- **Platforms** – each optimized for a sub-segment of the market
(**Modular – Leverageable**)
- Package architecture & configuration optimized for cost & yield
WB vs. FC vs. WLCSP
- Substrate – layer count, panelization, L/S, ...
- Cost optimized options – CUF vs. MUF
- **Design for Cost**

Process Development

- Process options
- Qualified materials
- Optimized supply chain

Test Development

- Test equipment
- Handler
- Parallelism / Throughput & cycle time

Proto & NPI

- Tooling cost
- KGD

Volume Manufacturing

- Line configuration & equipment utilization
- Cycle time
- Quality & first pass yield
- LEAN
- Automation

Total cost optimization - throughout product life cycle

Summary: SiP Value Proposition

Product

Performance,
cost, form
factor, reliability

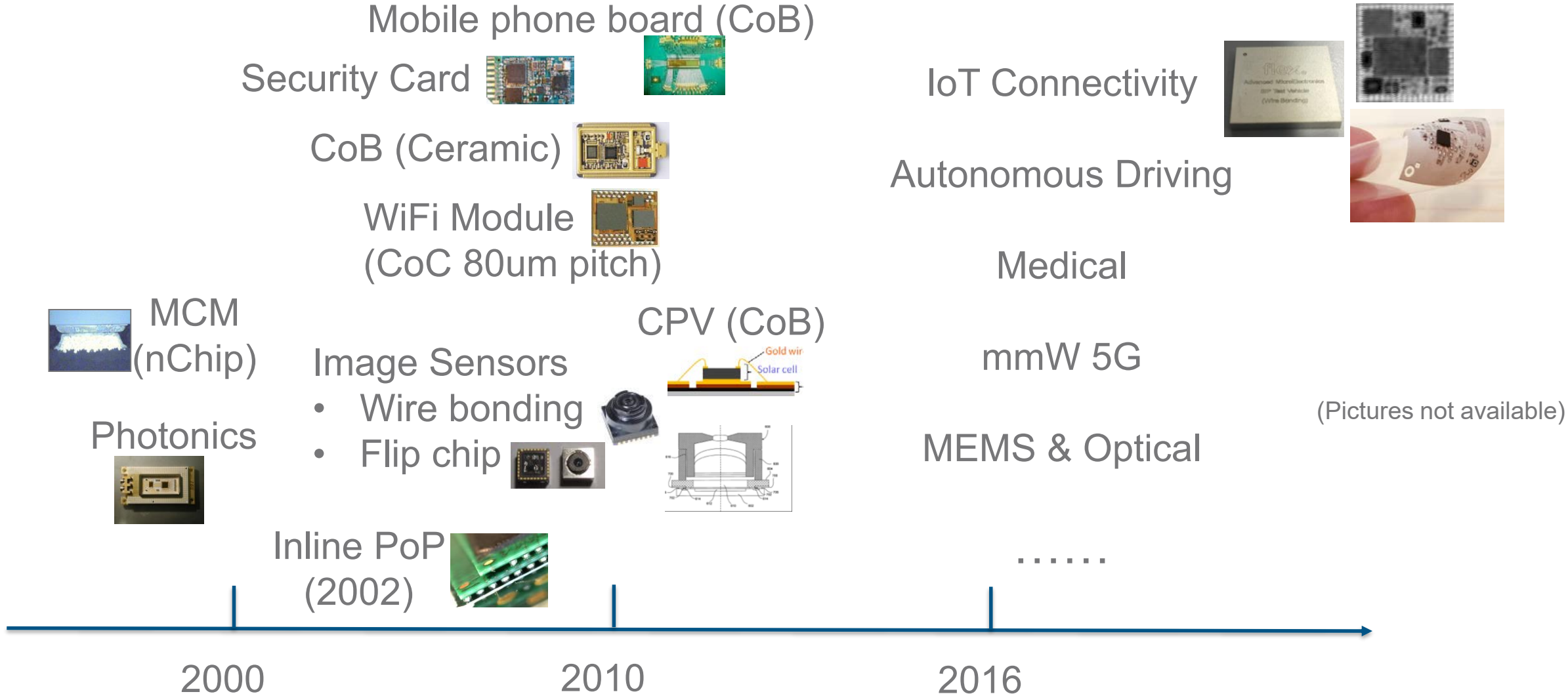
Technology

Heterogeneous
Integration,
Modularization,
Functional
Densification &
Miniaturization

- **Industry-leading technology portfolio for SiP**
 - Advanced SiP Design capabilities
 - System level expertise – across market segments
 - Advanced manufacturing capabilities for SiP: rigid, flex
 - Reliability; High frequency
- **One stop turnkey solution**
 - System miniaturization, package design, process & test, proto / NPI / HVM
 - Microelectronics packaging, PCBA, System
 - Sketch to Scale
- **Optimized technology platforms & packaging configurations across market segments**
- **Flexible business models**
- **Low / medium / high volume manufacturing, global footprint & operational excellence**
- **Advanced supply chain solutions & lower total manufacturing cost**

SiP Applications (examples)

Very diverse in technology and in applications



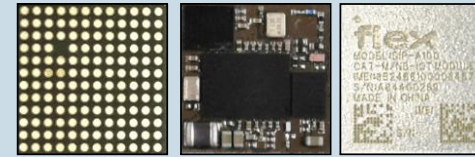
SiP Development Platforms for IoT

Program Description

Cellular

Smallest Cellular IoT Connectivity Module on the market

- Optimized LTE CAT-M1 & NB-IoT (NB1) modem
- Integrated GNSS engine
- Integrated MCU with memory
- Single-SKU with global RF coverage



10mm x 10mm

BLE

Smallest IoT Sensing Module

- Ultra low-power MCU
- Optimized Bluetooth 5.0 Low Energy (BLE) radio
- Built-in BLE antenna inside the SiP
- Integrated sensors: 3-axis accelerometer & IR-based temperature sensor

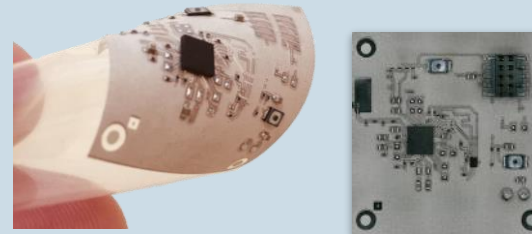


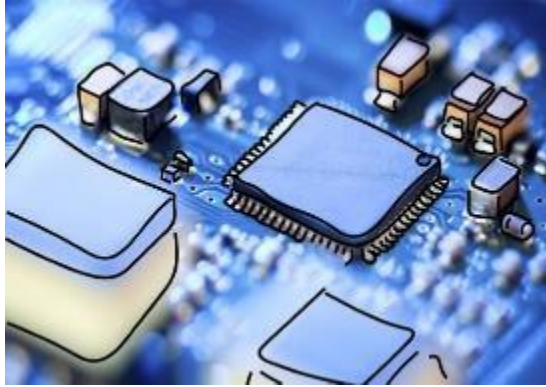
11mm x 12mm

FHE

Flexible IoT Development Platform

- MCU + BLE + Antenna + Sensor
- Solderable Ink with low temp solder
- Flexible copper clad technology





flexTM
Thank You