SiP for Miniaturized Electronics Modules: An Update

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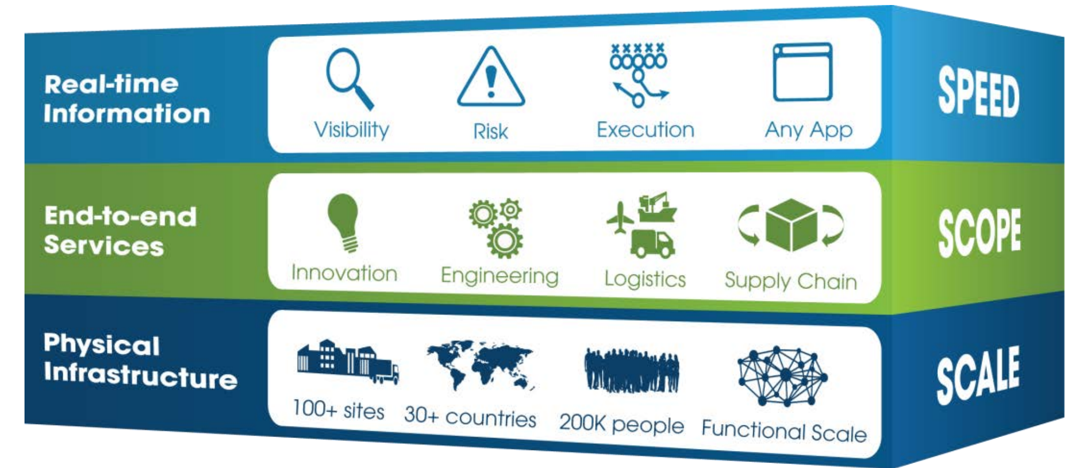
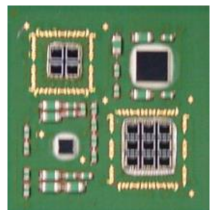
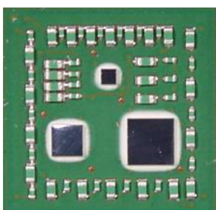
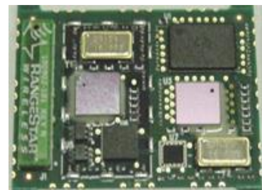
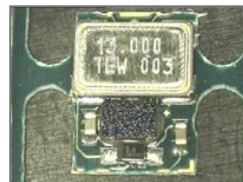
October 2019

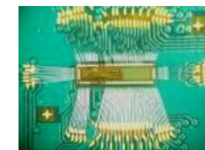
Outline

- SiP Overview
- Industry Landscape
- Competency Development
- Eco-System
- Summary



… towards cost effective solutions for SiP and miniaturized functional modules from technology to commercial products



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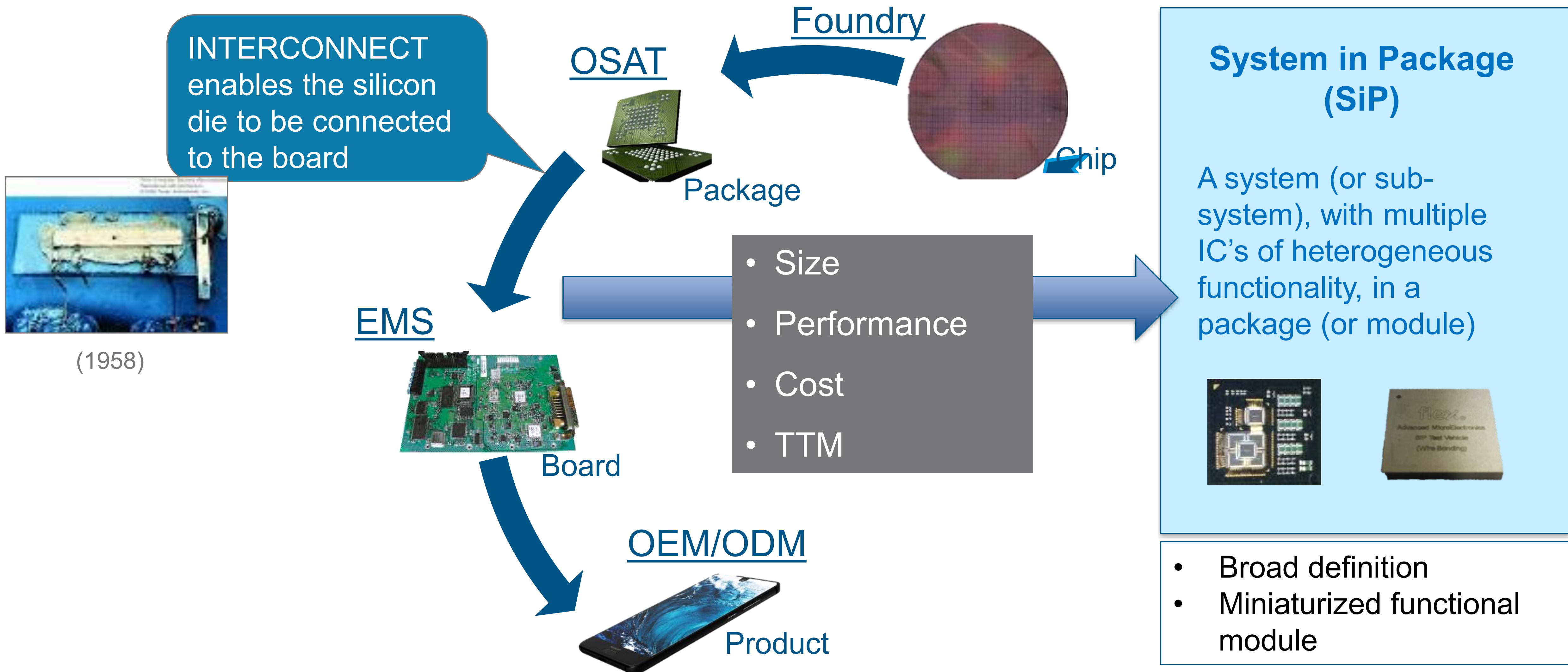
SiP Overview

Microelectronics Packaging



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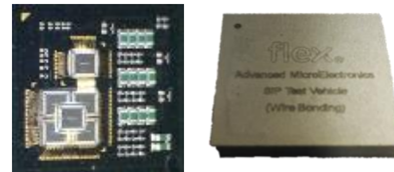
Benefits of SiP

Miniaturization
small form factor / higher functional density

Modular Solution
for specialization, re-usability, and upgradability
- Pre-certification
- Yield management (known good sub-system)

Very Diverse
in complexity & configuration

Faster
time to market
as compared with SOC
- Design flexibility



Numerous Applications
in different market segments

More than Moore

Heterogeneous Integration
different functionalities and fab nodes
- ➢ Each die optimized based on its merits - for cost effectiveness
- ➢ Simplified IP ownership, testing, …
- ➢ "Disintegration at the die level and integration in the SiP
- ➢ Flexibility - "Mix & match"

Higher Performance
through shorter interconnect paths
- Latency / bandwidth / power

Lower
total system cost

Opportunity
for differentiation, optimization & value-add

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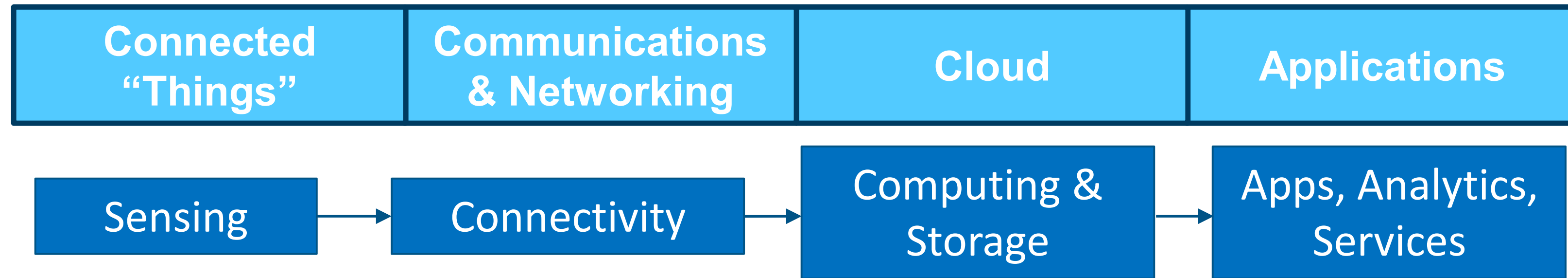
Market Demand for Miniaturization & Modularization (Example)

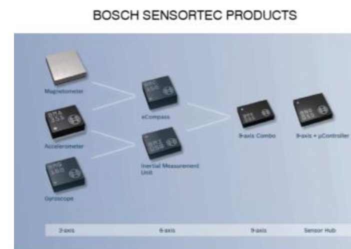


IoT Module

- Sensor(s)
- MCU / AP
- Connectivity
- Memory
- Power

Market Drivers

- Low Cost
- Low Power
- Miniaturization
- Modularization
- Ease of design & integration



(Pictures from various sources)

Reason for SiP Adoption

Item	Percentage specifying item
Form factor/miniaturization	100%
Low Power	36%
High Performance	64%
EMI noice reduction	36%
Total cost reduction	57%

Source: TechSearch International, Inc.

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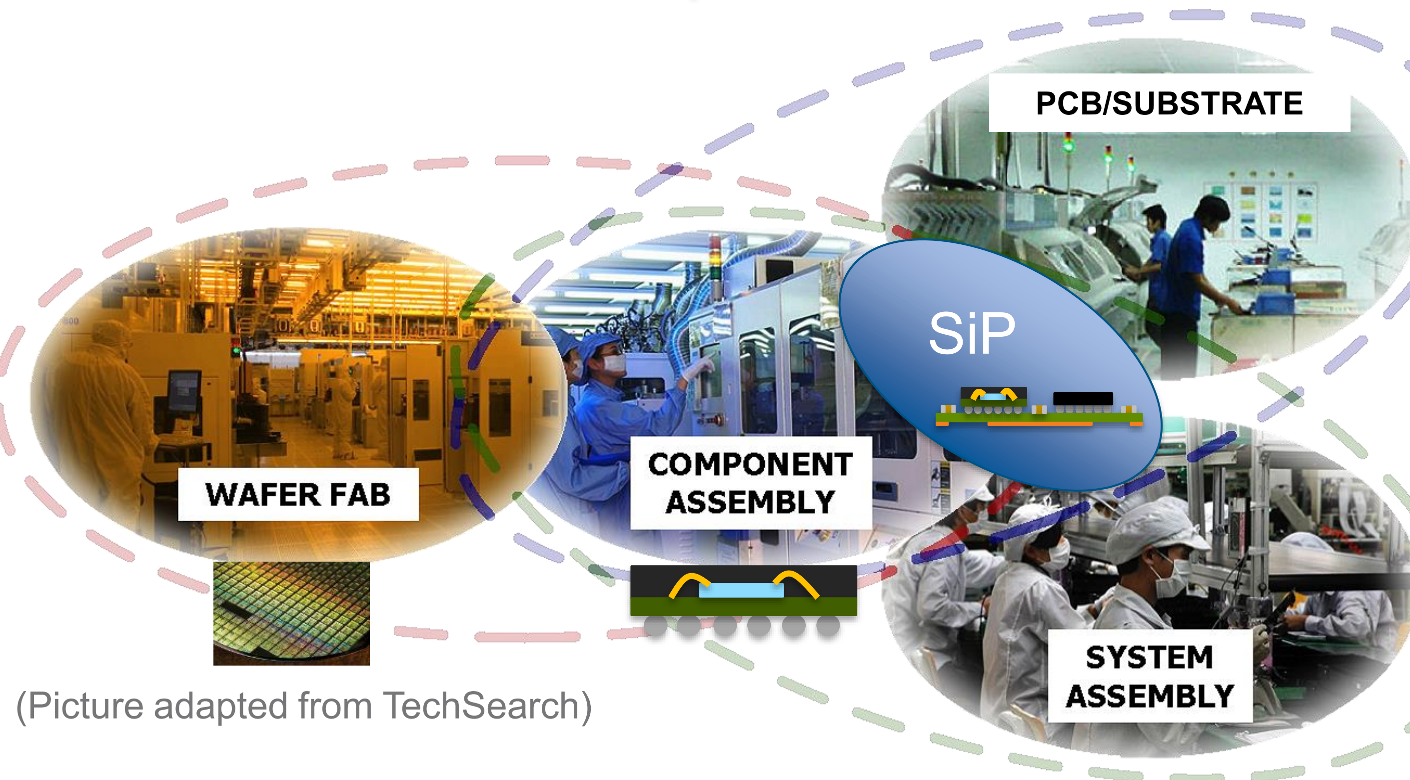
Industry Landscape



(Picture adapted from TechSearch)

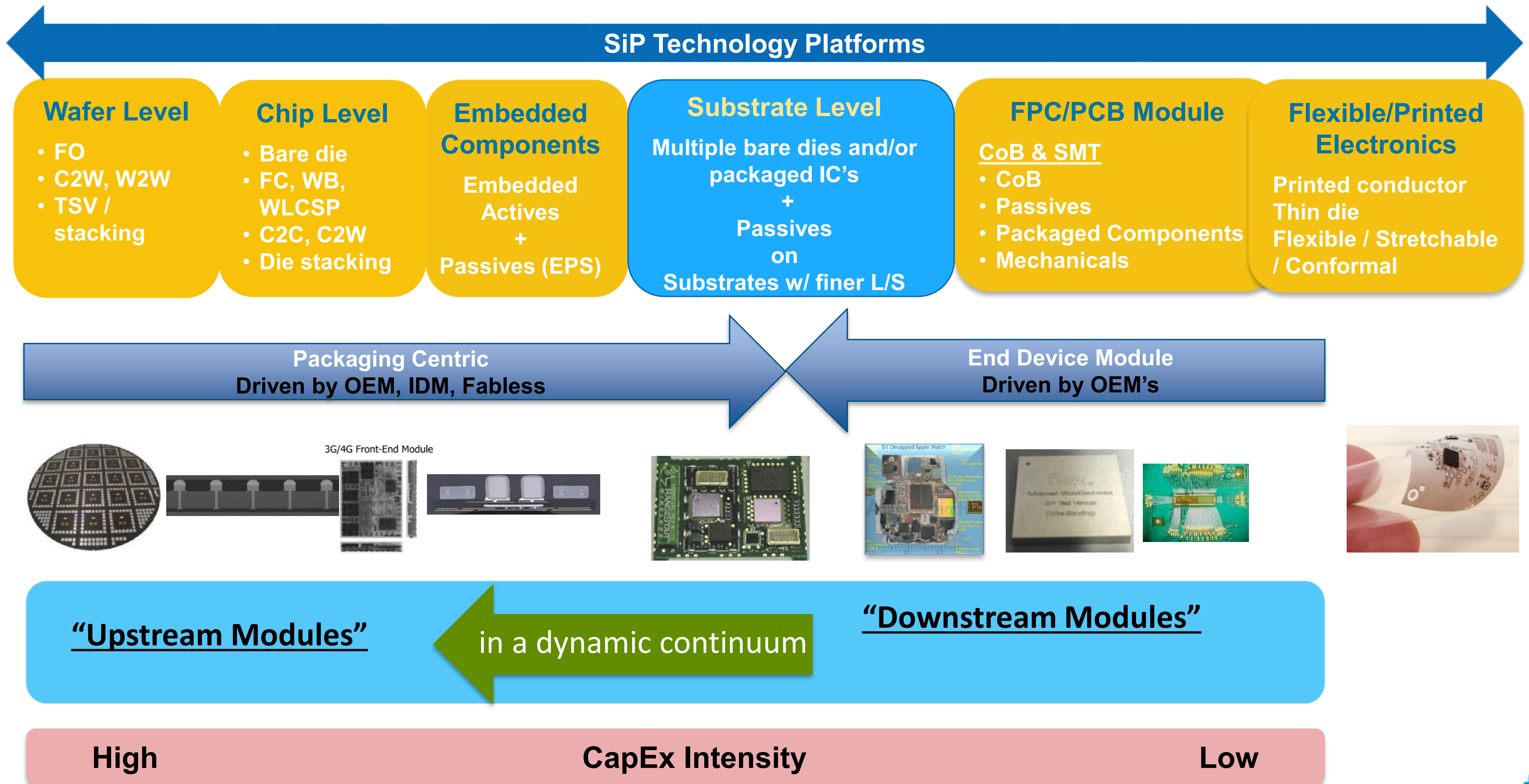
Flex Strength in SiP

- Multi-disciplinary, multi-industry knowledge
- System level expertise
- OEM relationships
- Eco-system & supply chain
- Existing SMT asset and expertise
- Global footprint & scale
- Operational excellence
- Certifications (auto, medical, …)
- One stop turnkey solution

  (SiP + PCBA + System Integration)

SiP optimization creates opportunities in system cost and performance

Technology Landscape



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SiP and Module

- **SiP is the technology; Module is the device**
- **They can have many different configurations and processes**
    - Depending on the application requirements
        - Performance, size, cost, …
    - Opportunity to optimize
- **Need to pass MSL**

- Organic substrate
- Ceramic substrate
- Si substrate
    - With TSV
    - Without TSV
- Leadframe
- Fan-out
- Printed flexible
- …

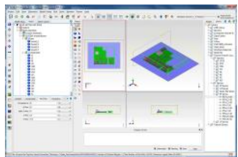
Competency Development

Competency Development

Design → **Process Development** → **Test Development** → **Proto & NPI** → **Volume Manufacturing**

Design

- Product platforms
- Package architecture & configuration
- System design / electrical
- Substrate layout
- Mechanical / thermal / Reliability
- JEDEC/MIL standards



Process Development

- Technology Roadmap
- Design rules
- Qualified materials
- Equipment selection
- Process Characterization
- Reliability & FA

- High density SMT
  - Fine pitch FC/CSP
- Wafer handling
- D/A, W/B
- Molding / Shielding
- Ball attach
- Singulation, T/R

Test Development

- Structural
- Functional
- RF / Digital
- Diagnostic / FA
- Component level / System level

Test programs
Tester / Handle
Fixture

Proto & NPI

- Process Qualification
- Process Control Plan

Volume Manufacturing

- Quality management
- Line configuration
- LEAN
- Automation

SiP Design & Development Cycle

Architecture /Schematic → **Package design** → **Engineering build** → **Test development** → **Qualification / NPI** → **Mass Production**

Architecture /Schematic
- Schematic design/simulation
- BOM optimization

Package design
- Package architecture
- Netlist input
- Floor plan
- Layout
- Simulation
- Design optimization

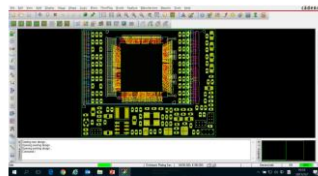
Engineering build
- Assembly instruction
- BOM readiness

Test development
- Test strategy
- Test program
- Hardware design / Fabrication

Qualification / NPI
- Qualification build
- REL testing
- Line audit

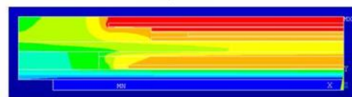
Mass Production
- Yield improvement
- Cost reduction

<u>Layout Tools</u>
Cadence SIP Layout XL
Cadence SIP RF option

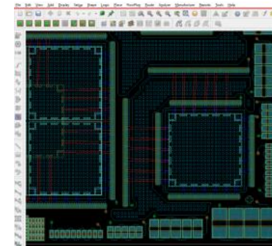


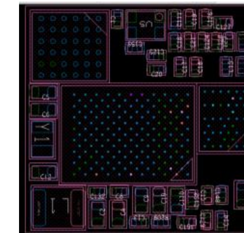
<u>Simulation</u>
SI/PI
- Sigrity XtractIM
- Power SI
- Power DC

Thermal
- Flotherm

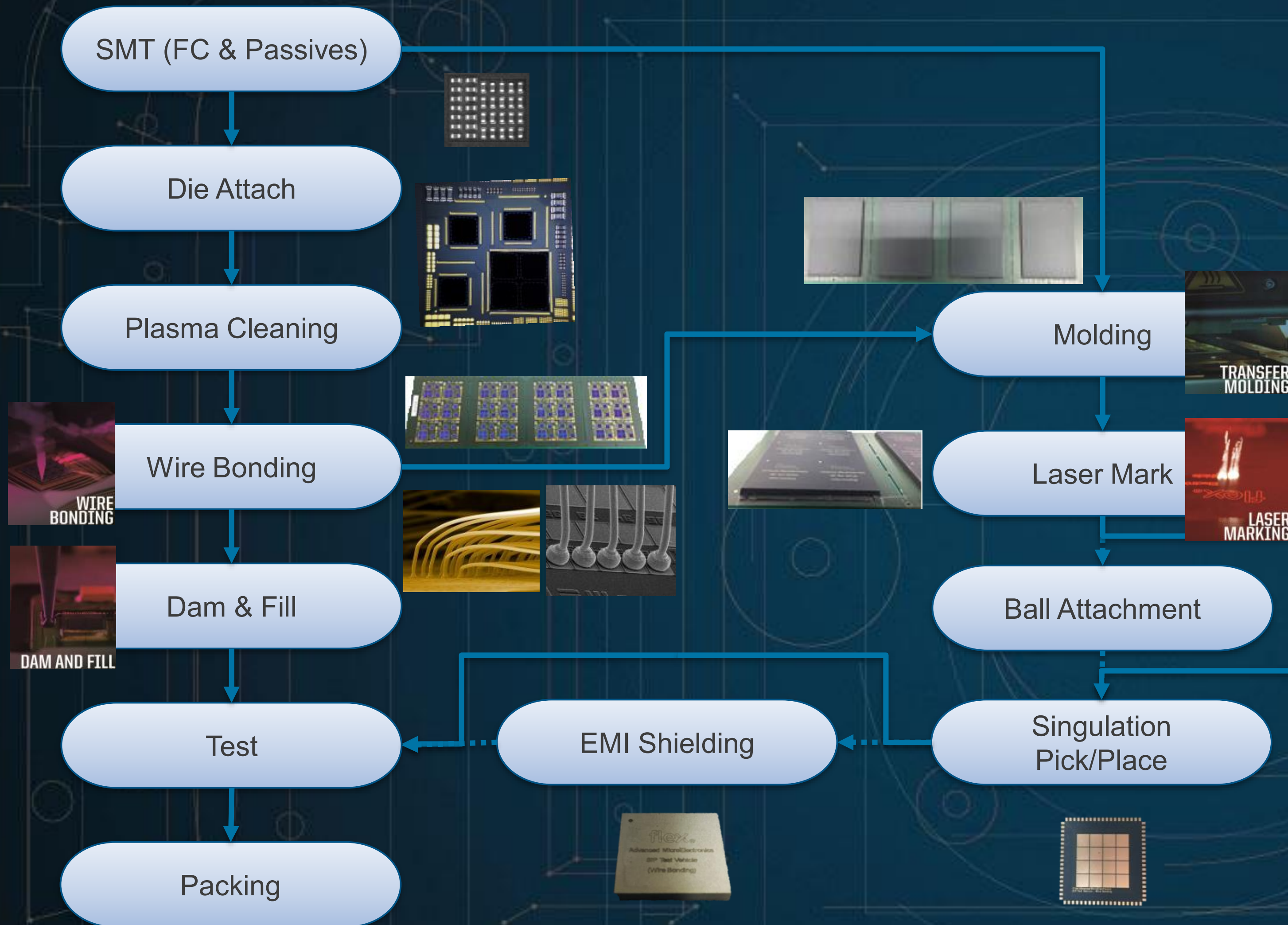


(Example)





SiP Processes



- High thermal conductivity (>100W/mK) D/A
- High precision D/A
- Fine pitch wire bond for Au & Al
- Die stacking
- Fine passive component placement
- Fine pitch FC / CSP
- Fine filler (<20um) mold compound (MUF)
- Conformal EMI

(Example – for illustration only)

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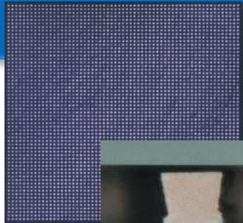
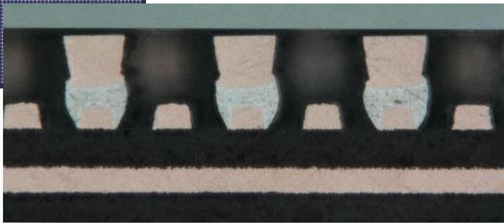
Miniaturization & Functional Densification

Design

Advanced design rules
Fine L/S
Fine pitch FC

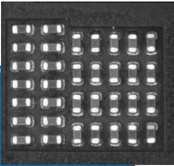


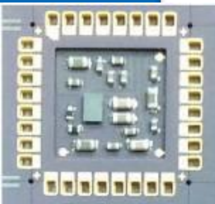


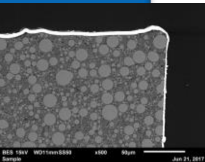
Miniaturization

Processes

Advanced SMT
Bare die (FC, WB)
Cavity
Underfill (CUF/MUF)
Thin Molding
EMI

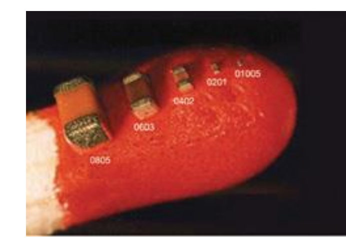




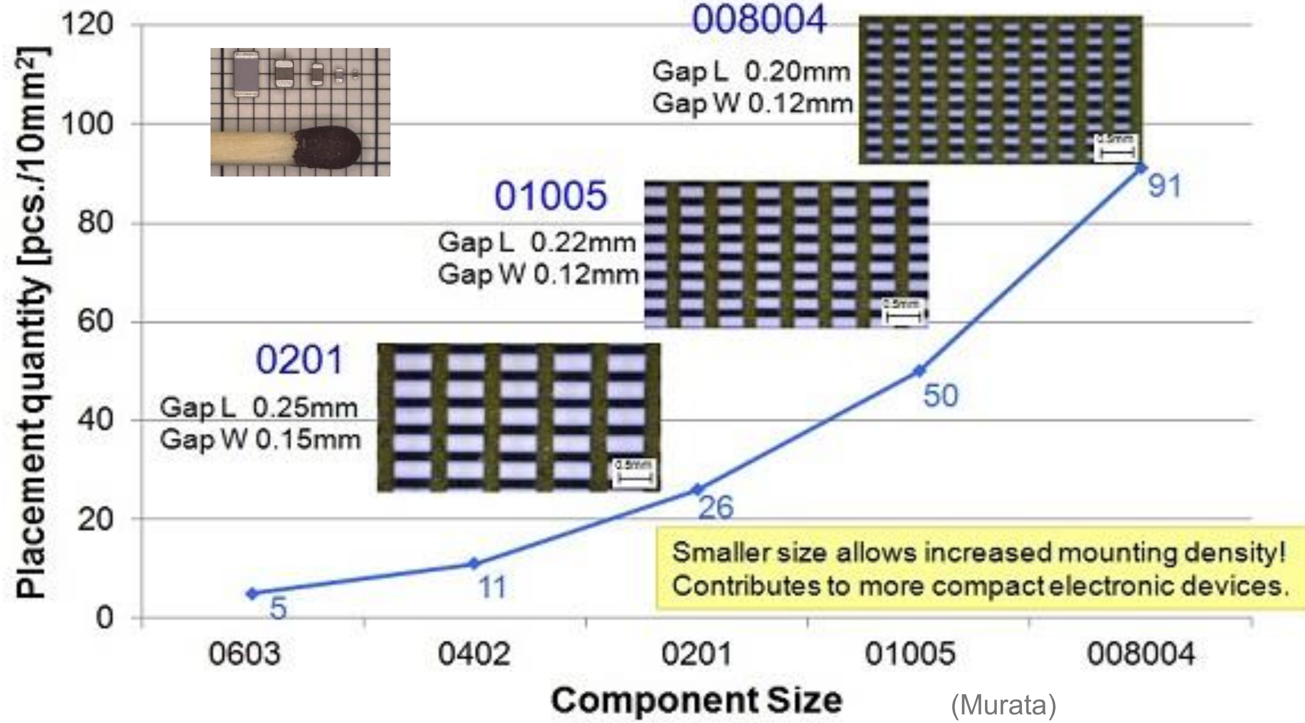


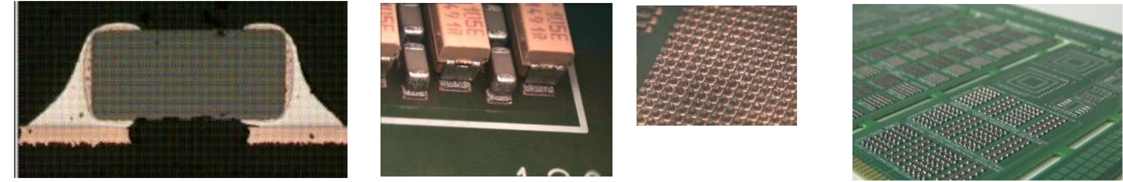
Materials

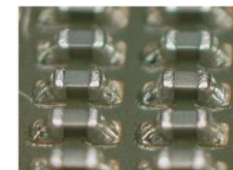
Thin Die
Passives (0402 → 008004)
Substrate (thin & fine L/S)
MUF (Fine fillers)
Paste (fine particles)



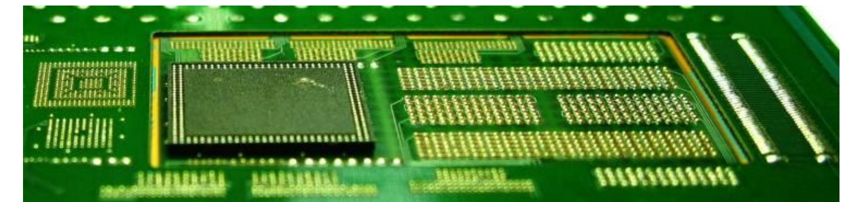
Small Passive Components

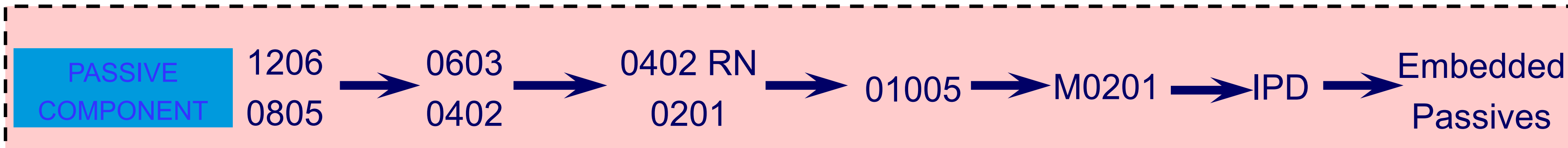


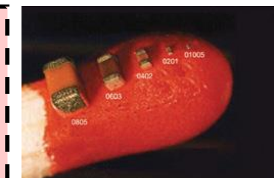




Cavity Assembly







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Example

50
75
100

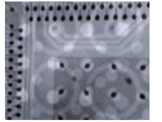
Passives spacing
100
75
50

008004
L0806
L0806
FC150
FC100
008004
MLF 0.4
Vertical
Horizontal
150/15
100/100
75/75
50/50
0

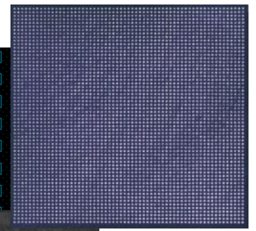
Key features

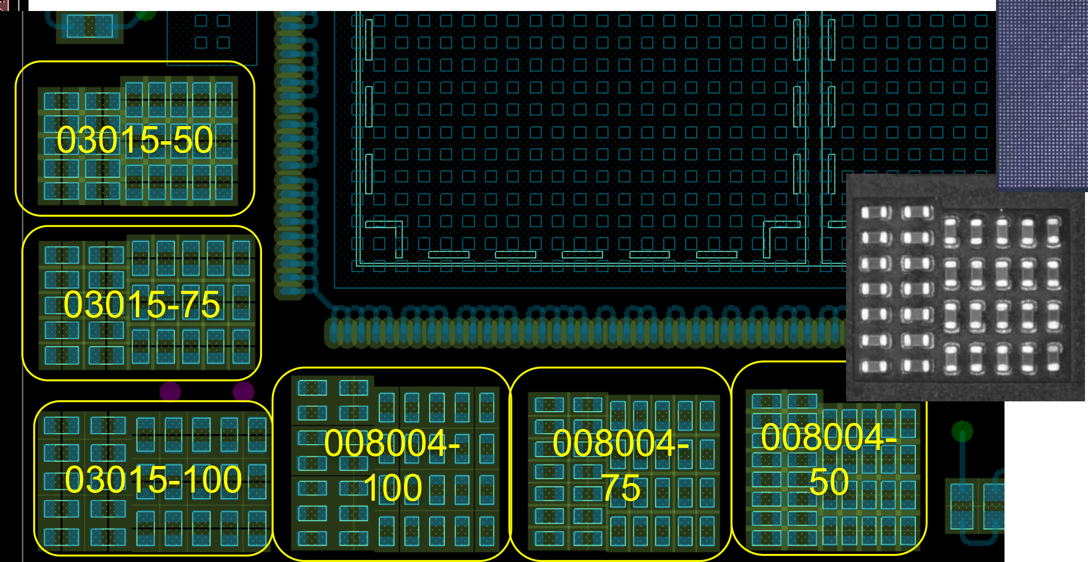
- Wire bonding & Flip chip (150/100um pitch)
- Die stacking
- SMT: 03015 and 008004 passives @ 100/75/50um spacing
    - Mixed with large components
- CUF & MUF
- EMI conformal shielding

100um pitch FC after reflow
6x6mm Cu Pillar



150um pitch FC
10x10mm full array >3700 I/O





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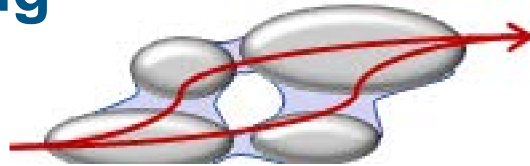
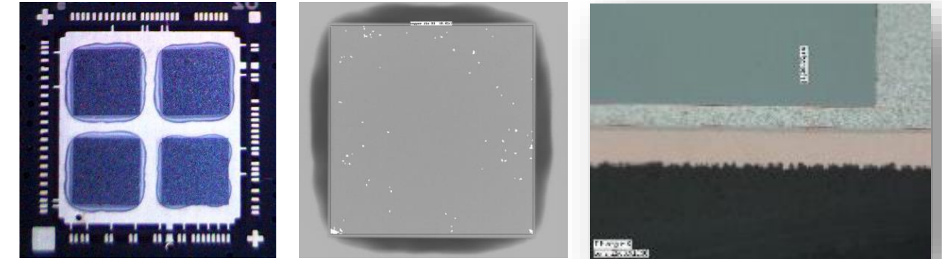
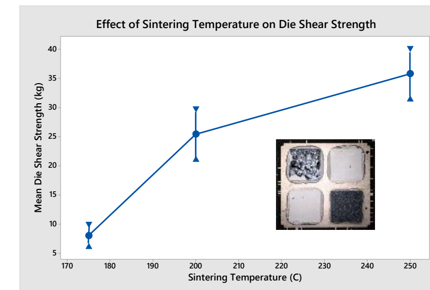
High Thermal Conductivity Die Attach (example)

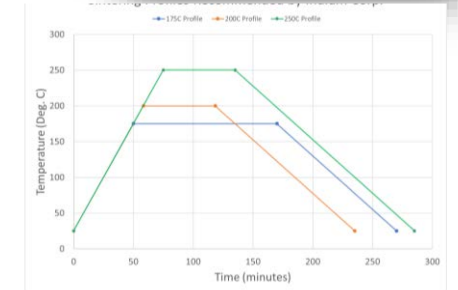
- **Nano-Ag**
- **Thermal Conductivity: >100 W/(mK)**
- **Paste dispensing process for D/A**
  - Consistent bond line thickness (0.8-1 mil)
- **Pressure-less sintering**
  - Voiding <5%



- **Die Shear**
  - Consistent after MSL / 260C reflow
- **Can withstand 260C reflow**
- **Can withstand 1000 T/C**
  - Consistent die shear strength
  - No delamination





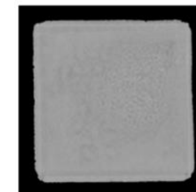


Thermal Cycling

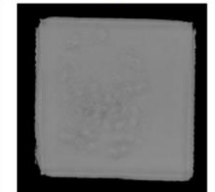
- IPC 9701-A Standard TC3 / NTC-C Profile.
- - 40C to +125 C
- 15 mins dwell time
- 1000 Cycles

C SAM Analysis does not reveal any delamination defect even after 1000 Thermal Cycles

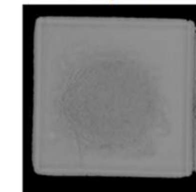
250 cycles



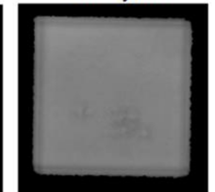
500 cycles



750 cycles



1000 cycles



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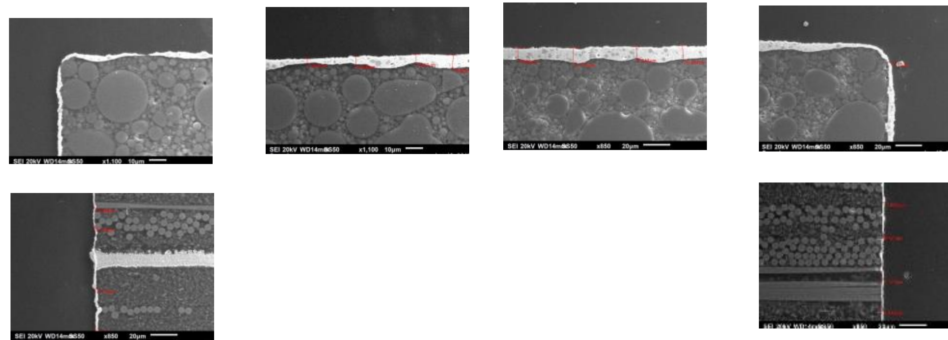
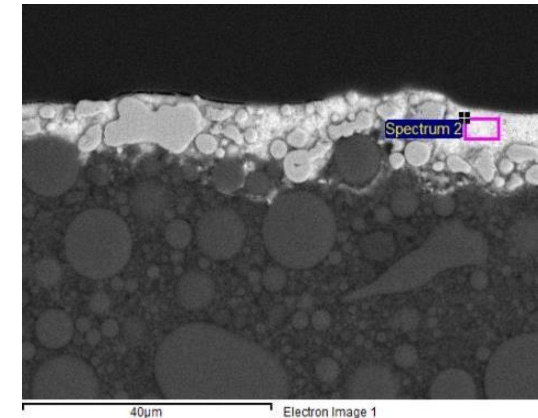
EMI Shielding

- **Metal can**
- **Sputtering**
- **Spray**





Characterization
- Thickness uniformity
- Adhesion
- Electrical Resistance
- Shielding Effectiveness

Reliability Testing
- MSL
- HTS
- T/RH
- T/C

- **Performance**
  - Shielding effectiveness
  - Durability
- **TCO**
  - Materials
  - Capex
  - Throughput, Yield

Eco-System

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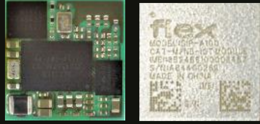
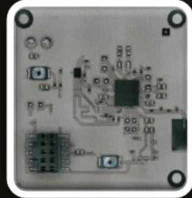
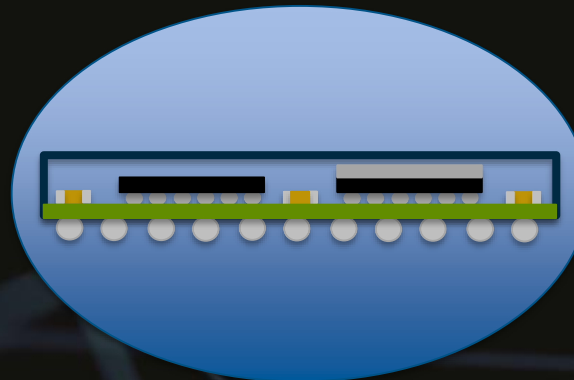
SiP Competency



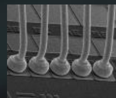
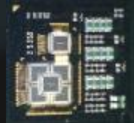


MODULE DESIGN
- *Substrate Design*
- *Package Design*
- *Electrical / Thermal / Mechanical Simulation*
- *Thermal Management*

VOLUME MANUFACTURING
- *Certification (automotive, medical, …)*
- *Low/medium/high volume*
- *Lean manufacturing*
- *Cleanroom management*
- *Global footprint*



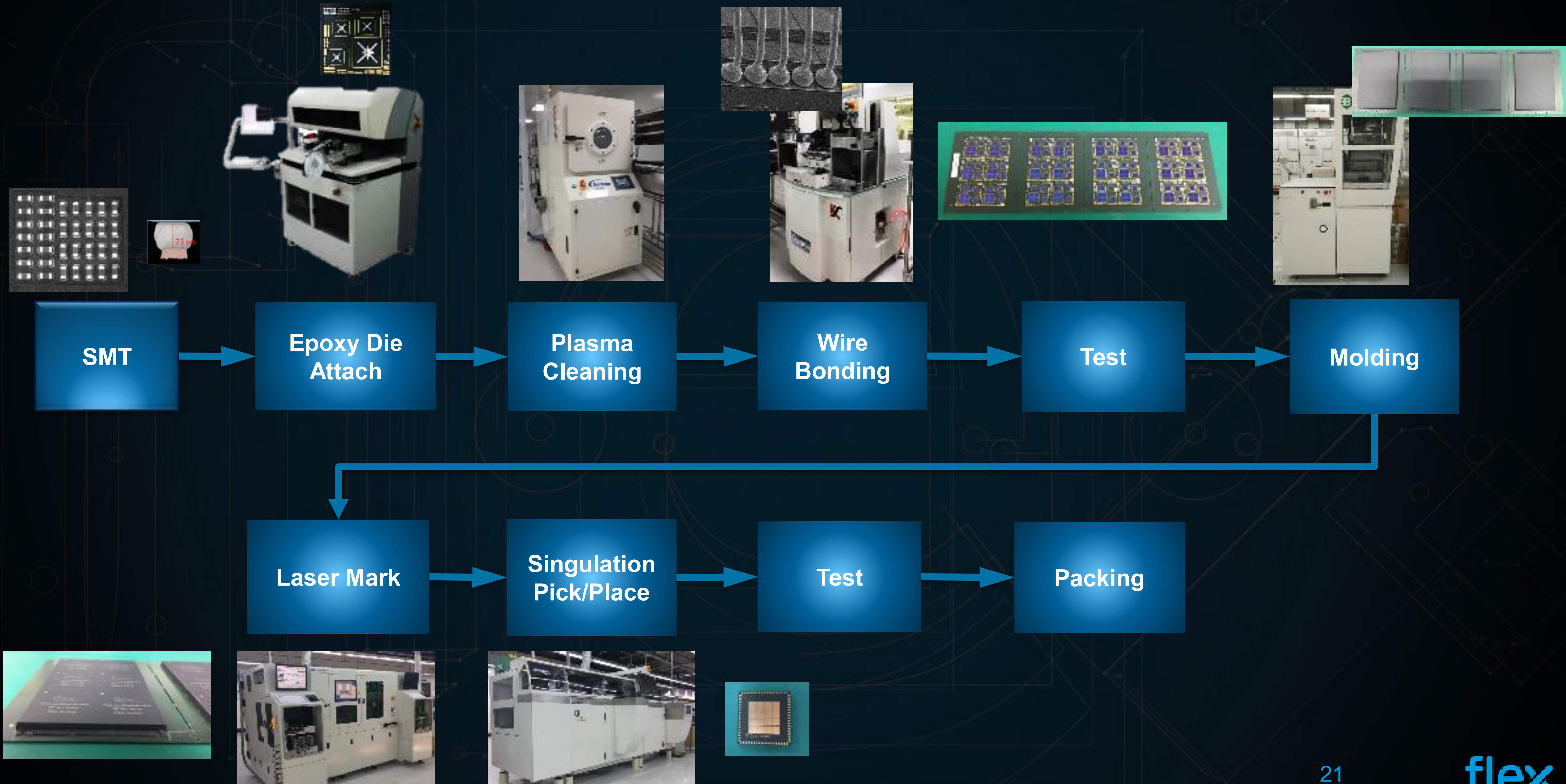
ASSEMBLY PROCESSES
- *High Density SMT*
- *Wire Bonding*
- *Flip Chip*
- *Die Stacking*
- *Underfill (CUF/MUF)*
- *Transfer Molding*
- *Ball attach*
- *EMI shielding*
- *Marking / Singulation*

RELIABILITY & FAILURE ANALYSES
- *JEDEC, MIL REL tests*
- *Comprehensive failure analyses*

TEST
- *Structural / Functional*
- *RF / Digital*
- *Diagnostics / FA*
- *System level test (SLT)*
- *Tester / Handler / Fixture*

SiP Processes



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Bump on Trace (2003 paper)

Assembly Processes for

Flip Chips on Substrates

STUDY PROVIDES NEW DATA ON ASSEMBLY OF SOLDER FLIP CHIP DEVICES.

BY DAVID A. GEIGER, JONAS SJOBERG, PATRICK WONG AND DONGKAI SHANGGUAN

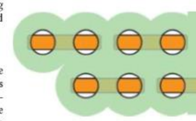

Figure 1. Area array land pattern

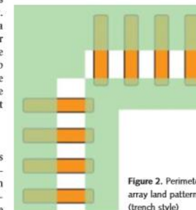

Figure 2. Perimeter array land pattern (trench style)

www.apmag.com November 2003

Advanced Packaging

Inline PoP

San Jose Lab (2002)

Production (2003)

IEEE IEMT Paper (2003)

Package Stacking in SMT for 3D PCB Assembly

David Geiger, Dongkai Shangguan, Samuel Tam, and Dan Rooney
Flextronics
San Jose, CA, USA

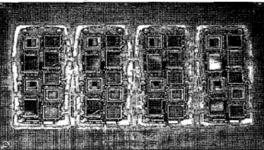

Figure 1: Test Vehicle

2003 IEEE/CPMT/SEMI Int'l Electronics Manufacturing Technology Symposium

Method of Providing a RF Shield of an Electronic Device (Filed 2008; Granted 2011)

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(12) United States Patent
Joshi

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(45) Date of Patent: Jul. 5, 2011

(54) METHOD OF PROVIDING A RF SHIELD OF AN ELECTRONIC DEVICE

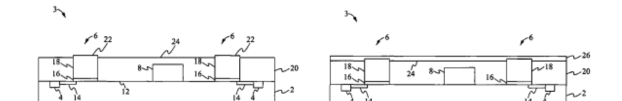
(75) Inventor: Rajeev Joshi, Cupertino, CA (US)

(73) Assignee: Flextronics AP, LLC, Broomfield, CO (US)

(21) Appl. No.: 12/221,256

(22) Filed: Jul. 31, 2008

29 Claims, 4 Drawing Sheets



2000

2010

2016

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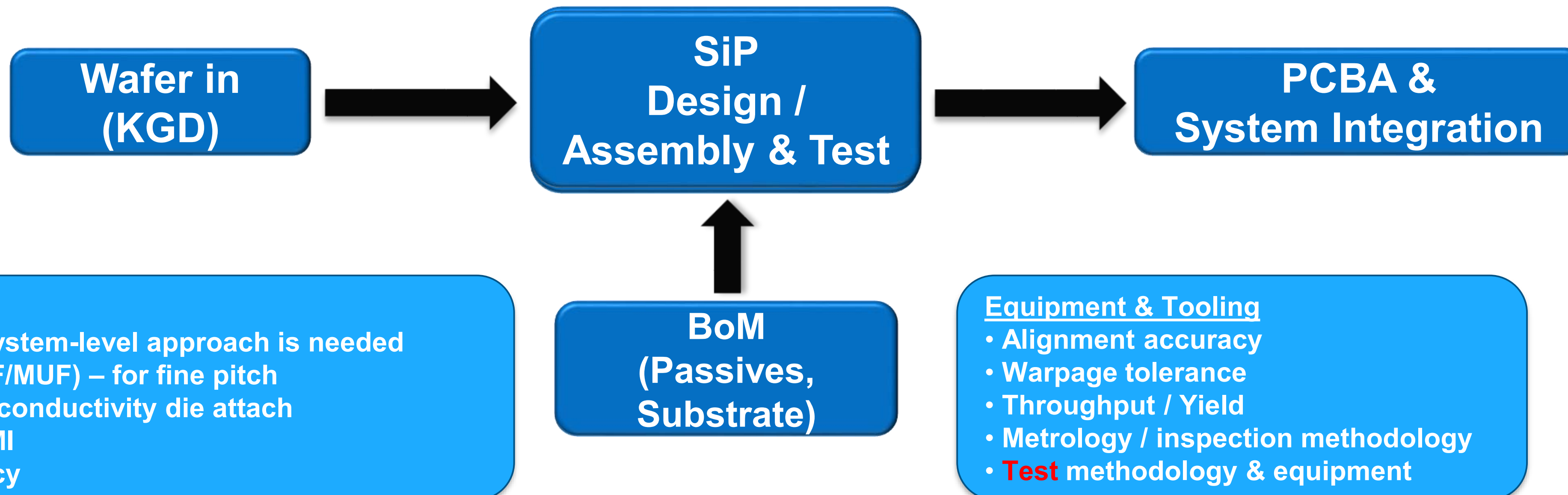
Supply Chain Focus Areas (examples)

Design
- EDA tools & design guidelines
  - Cross domain, multi-physics
- Architecture & partition
- Silicon-Package-PCB co-design
- Electrical: SI/PI/EMI
- Thermal: high density, heat flow path, space constrain, transient
- Mechanical: stress during assembly process and usage, warpage
- Reliability
- System level total optimization

Value Chain
- Cost (system cost, TCOO)
- KGD…Tolerance stack-up
- Multiple IC vendors
- Process flow & partition
- Inter-operability
- Infrastructure
- Standards & specifications
- Convergence, Integration, and Business Model



Materials
- Warpage: a system-level approach is needed
- Underfill (CUF/MUF) – for fine pitch
- High thermal conductivity die attach
- Conformal EMI
- High frequency

Equipment & Tooling
- Alignment accuracy
- Warpage tolerance
- Throughput / Yield
- Metrology / inspection methodology
- Test methodology & equipment

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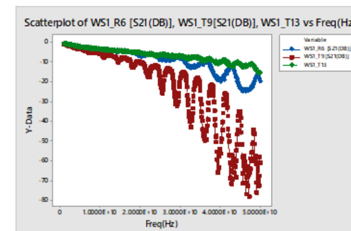
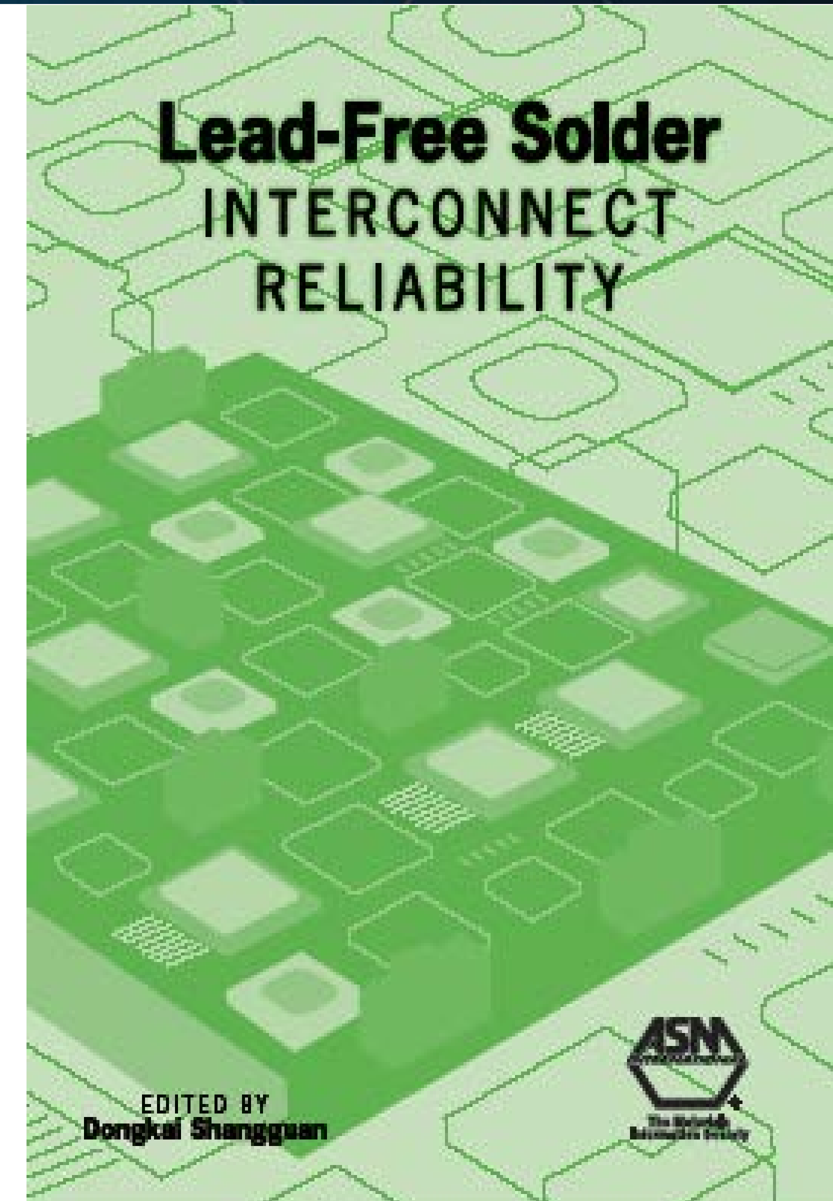
Reliability ~ Miniaturization

- Smaller solder interconnects – more susceptible to thermomechanical failures
- Higher current density – electromigration
- Tighter spacing – solder extrusion, whiskering, …
- Importance of the interface as the solder volume decreases - Interfacial IMC's
- Heterogeneous integration and diversity of packaging methods (devices, materials, interfaces) in the same module – more complex (often interactive) reliability failure modes and mechanisms
- Process yield
- Electrical – cross talk, EMI……in the 5G era
- Thermal



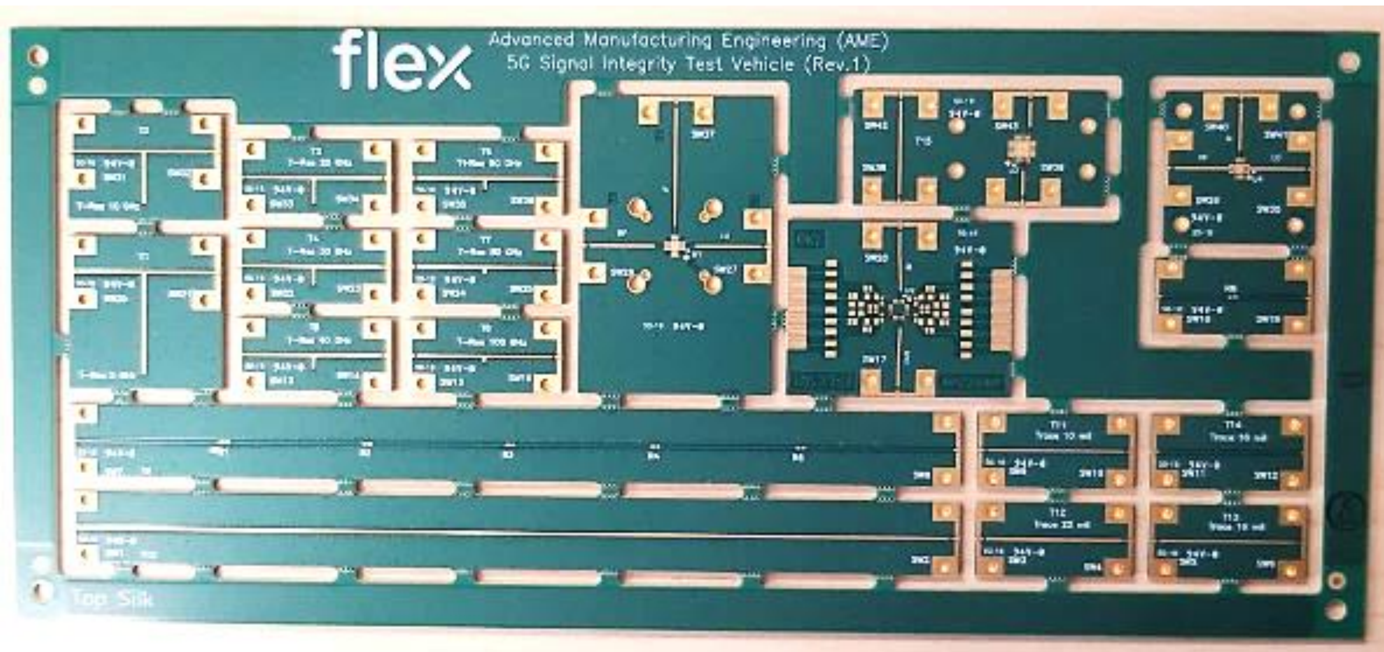


High Frequency Applications

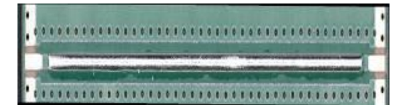
Signal Integrity vs. No-Clean Residue

– No-clean flux residue becomes a concern when products operate at high frequency, as it can provide an alternate path to signals

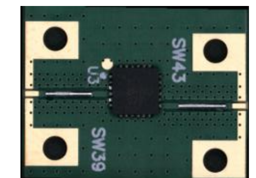
- **Initial study (2003): up to 15GHz**
- **New study (2019): up to 50GHz**



- Trace Designs
  - Different Length
  - Different Width
  - Solder Mask vs. Solder
  - Traces with 0Ω Resistors



- Components
  - T-Resonator
  - Band Pass Filter
  - Wideband Mixer
  - Low Noise Amplifier

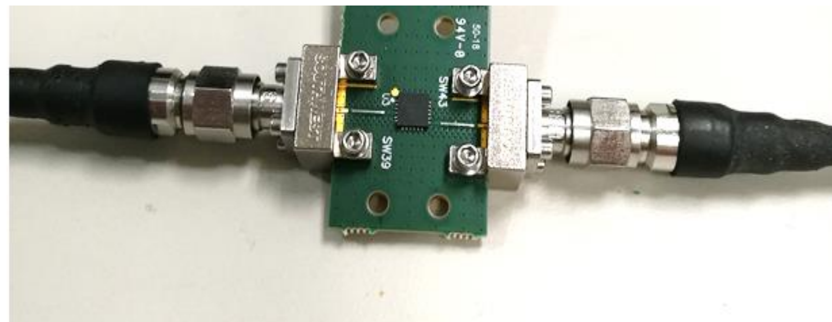


- Process Variables
  - Water Soluble
  - No Clean
  - Cleaning No Clean Residue
  - Humidity Testing

Signal Integrity vs. No-Clean Residue

- **Response Functions: Insertion Loss**
  - An insertion loss is considered significant in this study if
    - > 10% change in the signal integrity performance, or
    - or 2dB

Vector Network Analyzer (VNA)



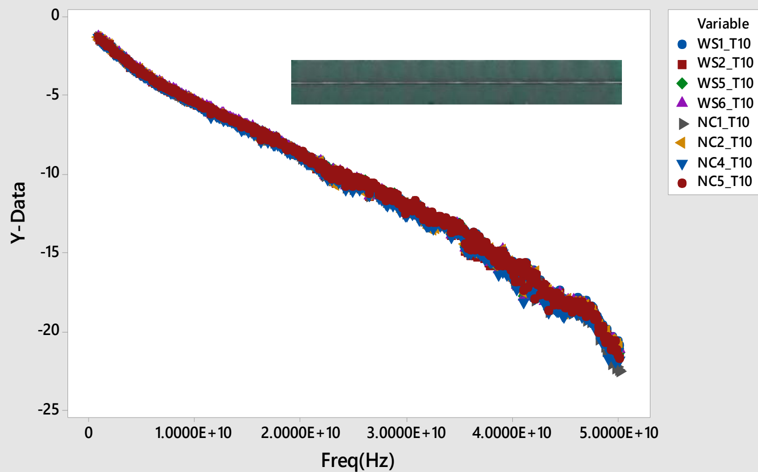
Example of a Device Under Test (DUI)

- DoE
- GR&R
- Data analysis

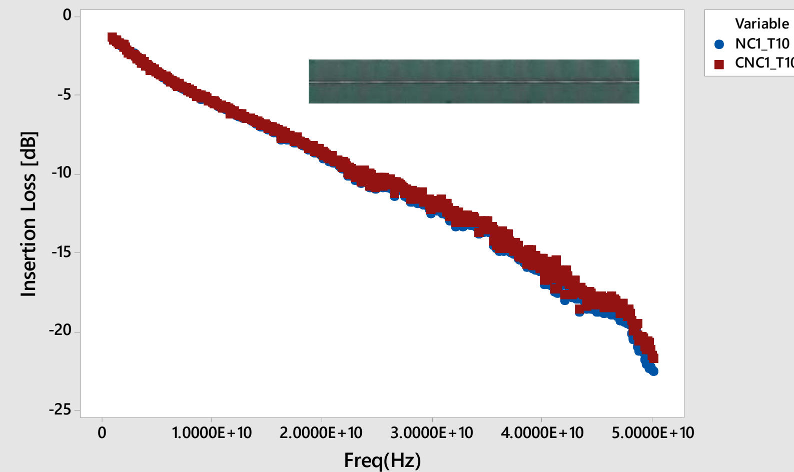
Signal Integrity vs. No-Clean Residue

Preliminary Results (examples)

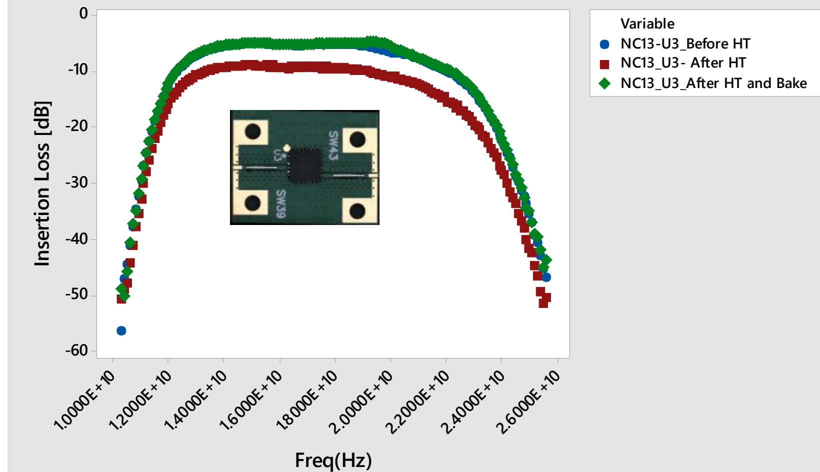
WS vs. NC



Before and After NC Residue Cleaning



85ºC/85%R. H for 168 hours



- The effect of no-clean residue on signal performance was relatively small and insignificant as compared to other variables such as frequency, design and moisture.
- Higher frequency can result in higher loss, depending on the component design. Wider trace would help to lessen the signal loss when the product operates at high frequency.
- Moisture can be a critical factor resulting in high signal insertion loss and affecting the signal integrity performance.

(Nguyen, Geiger, Shangguan, 2019)

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Flexible Electronics SiP

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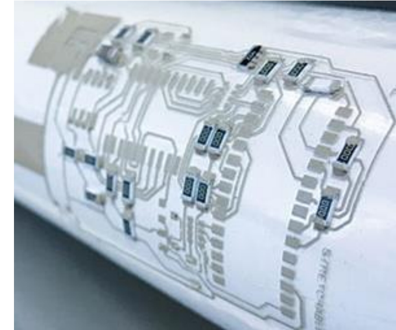
Flexible Hybrid Electronics

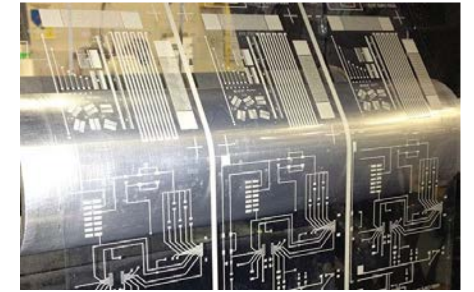
Rigid PCB/Assembly

Flexible Printed Circuit

Flexible Hybrid Electronics (FHE)



All Printed Electronics



(From various sources)

Benefits of printed electronics

- Flexible/Stretchable/Conformable
  - Electronics on curved shapes/3D objects
- Additive
- Low cost high volume production
- Lightweight
- Bio-compatible

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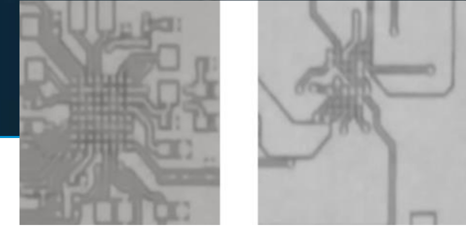
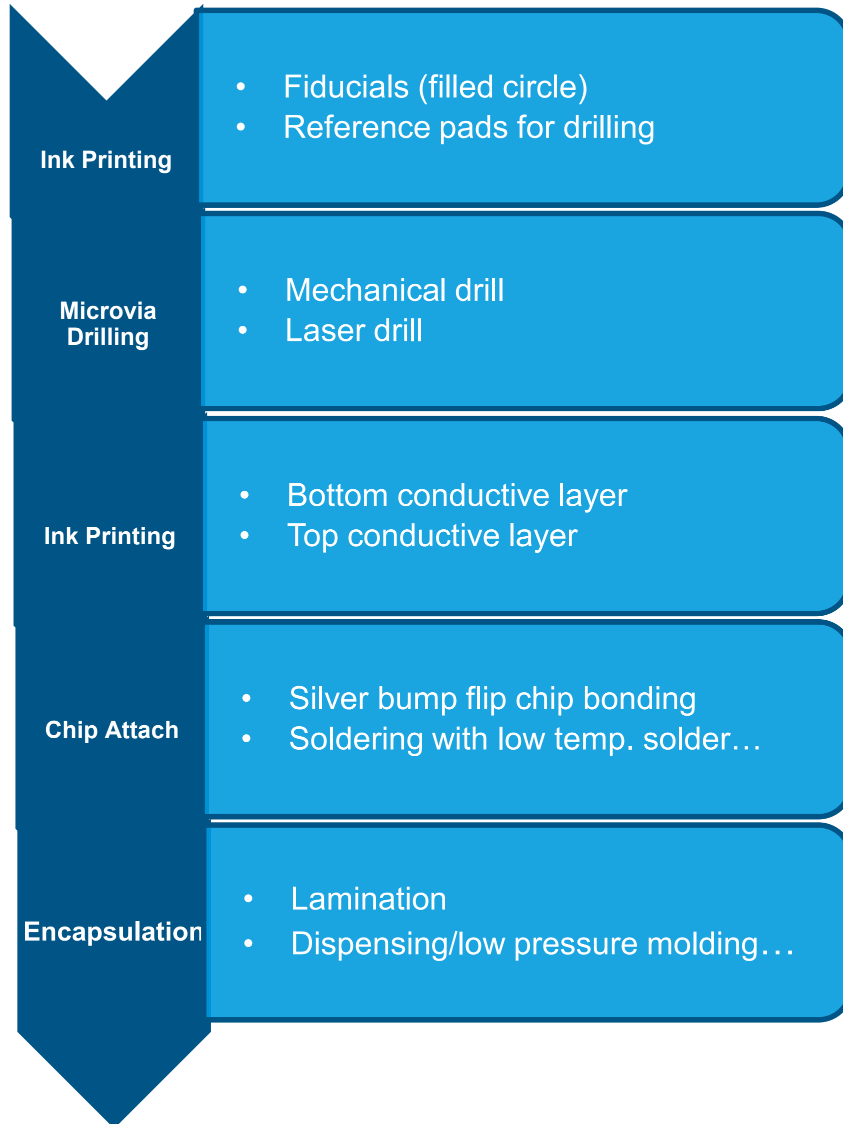
Process Flow





Substrates

- Compatibility with conductive ink
- Mechanical properties: Flexibility / Stretchability / Conformability
  - Low elastic modulus, high elongation
  - Ability to recover from bending, stretching, twisting, or other deformation
- Compatibility: Temperature; Chemical resistance; Electrical;…
- Cost: PI > PC > TPU > PET

Conductive ink

- Resistivity, esp. for power and high frequency applications
- Mechanical properties: Flexibility, stretchability, creasability/foldability
- Process capability: thixotropy, low cure temperature, working life, solderability

Dielectric ink

- Electrical properties: Insulation resistance, dielectric breakdown voltage
- Mechanical properties: Flexibility, stretchability, creasability/foldability
- Process capability: low cure temperature/UV, working life, printing quality
- Reliability: waterproof, high temp./high humidity, sweat resistant

Printing methods

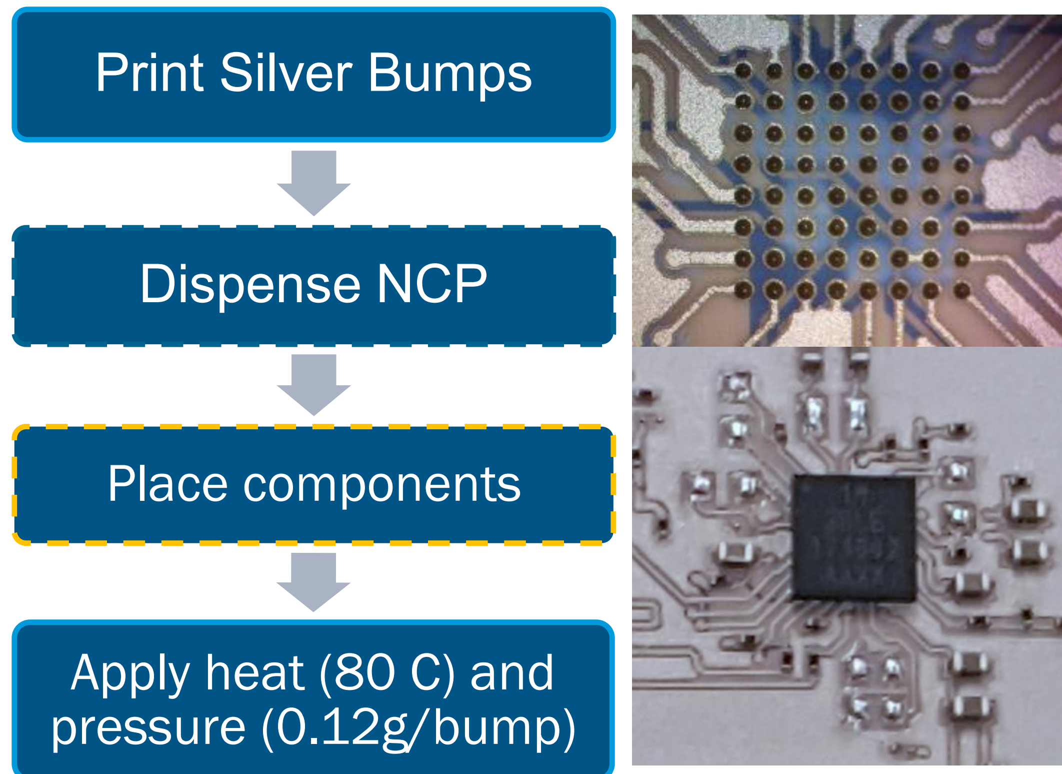
- Screen printing, gravure, flexography, inkjet, aerosol…

Multi-layer interconnect structure

- Conductive ink/dielectric ink build up
- Micro vias and hole filling

Component Attach

- **Thin chip (<50um thickness) pick & place**
- **Compatibility with conventional assembly process**
  - Solderable ink / Low temperature solder
  - Heat/pressure if ACF/ACP bonding



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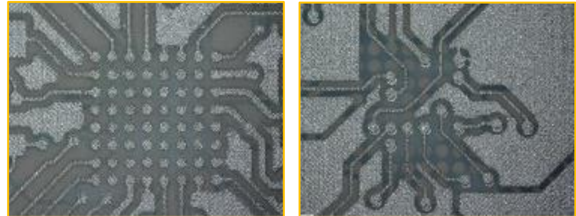
Printed Flexible Electronics SiP
IOT Module Platform

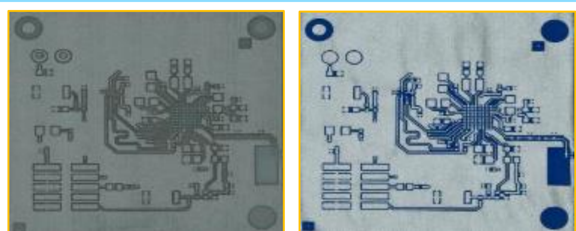
FINE LINE INK PRINTING



TOP SIDE — BOTTOM SIDE

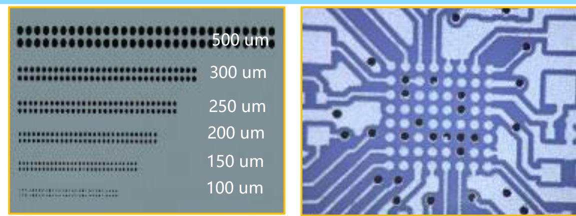
- 64 IO's
- 0.4mm Pitch
- 250um diameter
- 100um line width
- 100um spacing

FLEXIBLE & STRETCHABLE SUBSTRATE



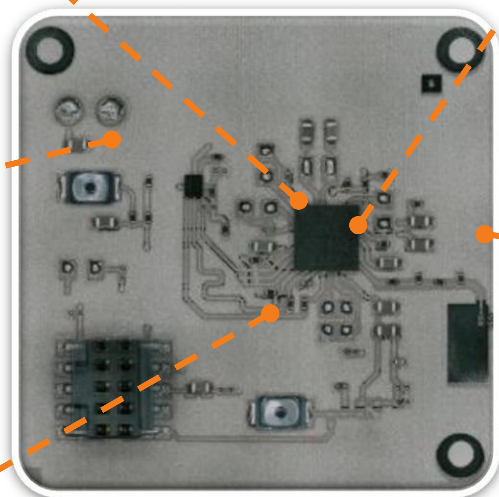
PET — TPU

MECHANICAL DRILLING MICRO VIAS



Filled micro vias with conductive adhesive

- *150 um diameter*
- *250 um diameter*

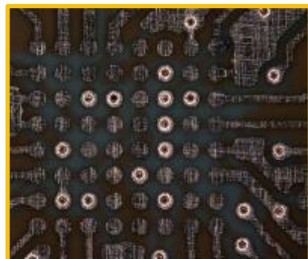


SOLDERABLE INK w/ LOW TEMP SOLDER

Require fixture with top cover before reflow

FLEXIBLE COPPER CLAD TECHNOLOGY

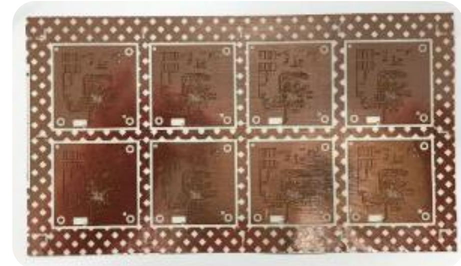
Micro vias with 50um diameter



Flexible IOT Module Platform

- Ultra low power platform with Bluetooth LE capability
  - Low power MCU + Bluetooth LE (plus chip antenna)
  - Integrated with accelerometer
- Flexible hybrid technology with multilayer interconnect structure with printed ink
- Flexible copper clad technology

Test vehicle for copper clad on high temperature flexible substrate



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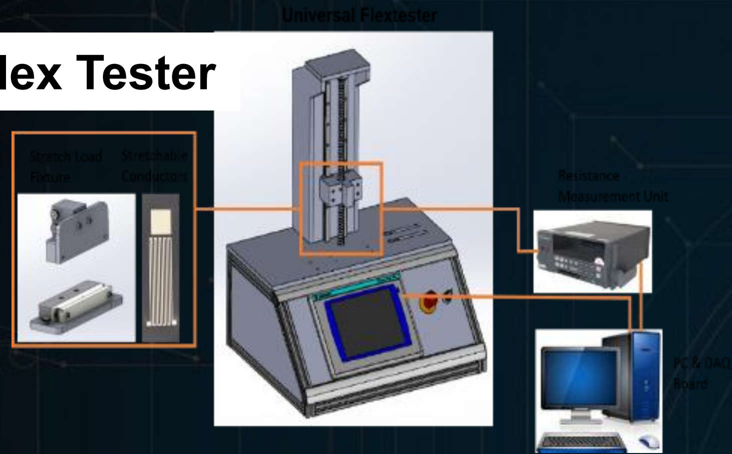
Reliability Testing - FHE

Universal Flex Tester



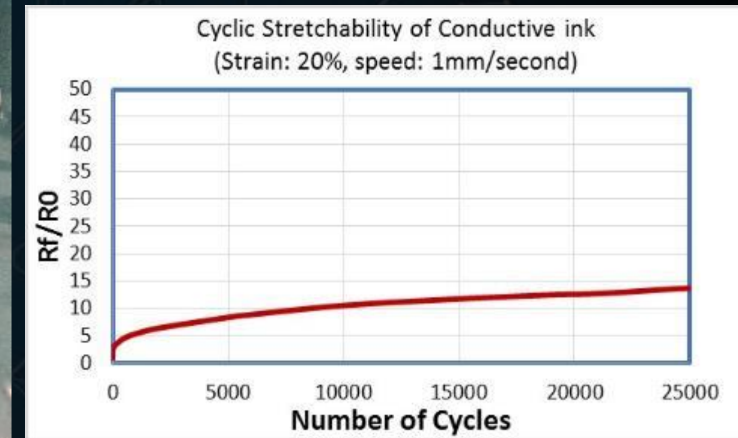
IPC 9204: Flexibility Testing of Printed Electronics

The universal tester can do 9 different tests:

1. Stretchability Testing
2. Variable Radius Bending Test
3. Sliding Plate Flexibility Test
4. Variable Angle Bend Test
5. Variable Diameter Rolling Test
6. Multi Modal Torsion Test
7. Free Arc Bend Test
8. Multi Mode Bend Test
9. Compression Crush Test

Test Coupon

Printed Ink Stretchability



First cycle stretchability

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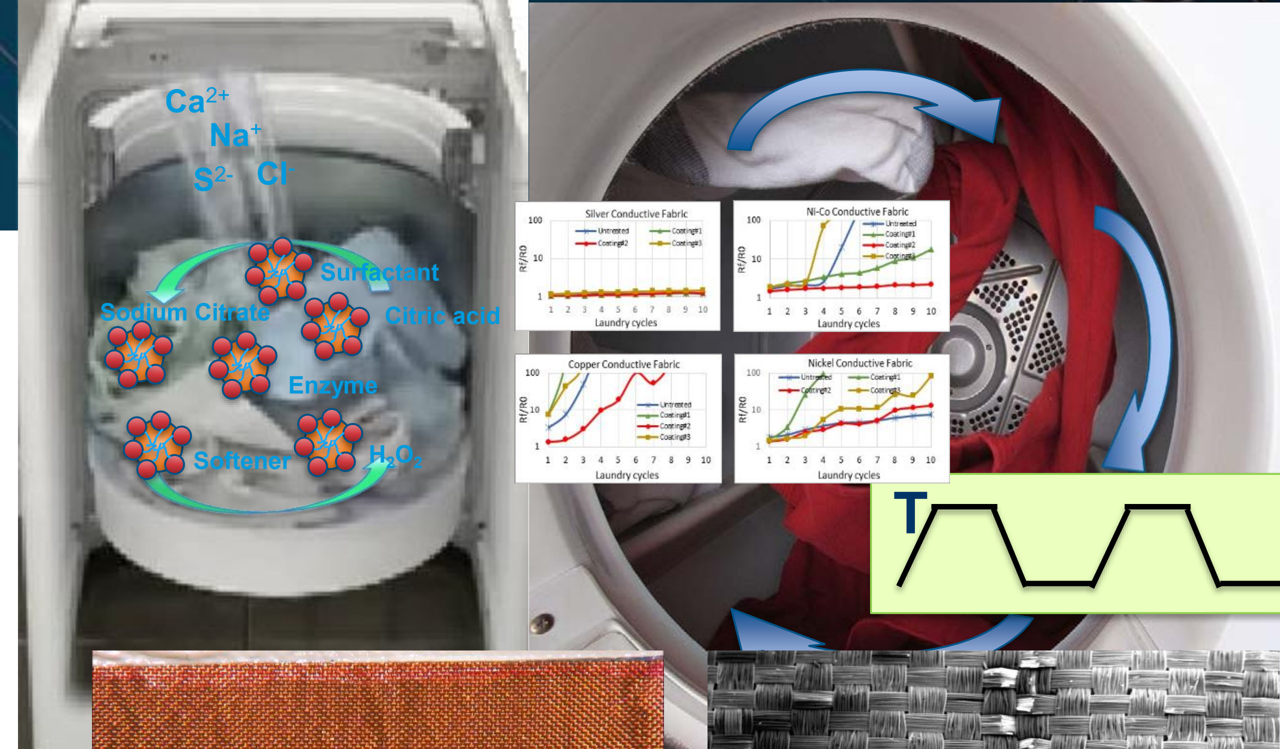
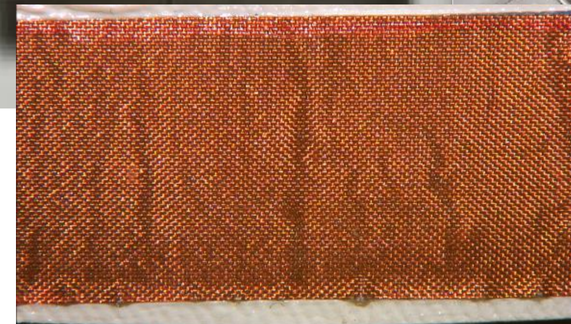
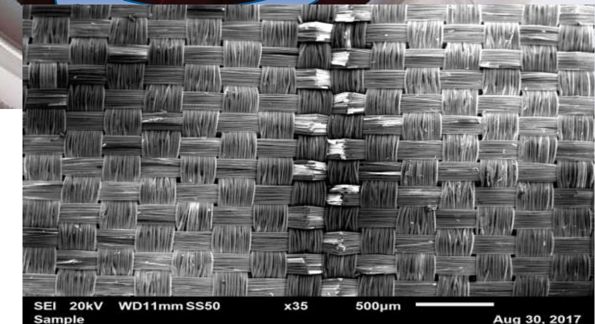
Launderability of E-Textiles

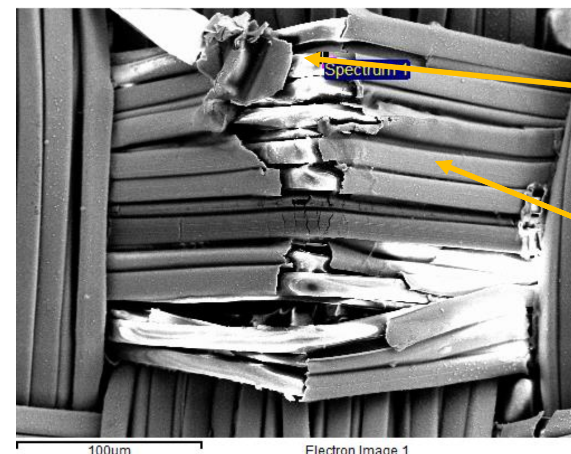
- **Chemical**
  - Water
  - Impurities
  - Detergent
  - Bleach
  - Softener
- **Mechanical**
  - Water flow
  - Abrasion
  - Agitation
  - Tumbling
  - Crumpling
  - Torsion
  - Bending/folding
- **Thermal**
  - Temperature
  - Temp. swing

- 10 cycles of washing and drying performed
- Resistance of the conductive fabrics shows increase with laundry cycles. The level of increase depends on the type of fabric:
  - Performance ranking: Silver fabric>nickel fabric~cobalt fabric>copper fabric
- With water resistance coatings, resistance of the conductive fabrics continue to show increase with laundry cycles
  - Coating#2 shows certain improvement, especially with Ni-Co and copper fabrics









Element	Weight%	Atomic%
C K	67.46	73.84
O K	31.61	25.97
Cu K	0.93	0.19

Element	Weight%	Atomic%
C K	35.61	70.93
O K	4.25	6.35
Cl K	0.27	0.18
Cu K	59.87	22.54

- What are the factors affecting the e textile launderability performance?
- What are the mechanisms causing the degradation of e textile materials during laundry (e.g. metal leach into water)?
- What are the design rules to make e textiles robust and laundry proof?

(Liu, Li, Shangguan et al, 2018)

Summary

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Cost Effective Solutions

Design → **Process Development** → **Test Development** → **Proto & NPI** → **Volume Manufacturing**

Design

- **Platforms** – each optimized for a sub-segment of the market (Modular – Leverageable)
- Package architecture & configuration optimized for cost & yield WB vs. FC vs. WLCSP
- Substrate – layer count, panelization, L/S, …
- Cost optimized options – CUF vs. MUF
- **Design for Cost**

Process Development

- Process options
- Qualified materials
- Optimized supply chain

Test Development

- Test equipment
- Handler
- Parallelism / Throughput & cycle time

Proto & NPI

- Tooling cost
- KGD

Volume Manufacturing

- Line configuration & equipment utilization
- Cycle time
- Quality & first pass yield
- LEAN
- Automation

Total cost optimization - throughput product life cycle

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Summary: SiP Value Proposition

Product

Performance, cost, form factor, reliability

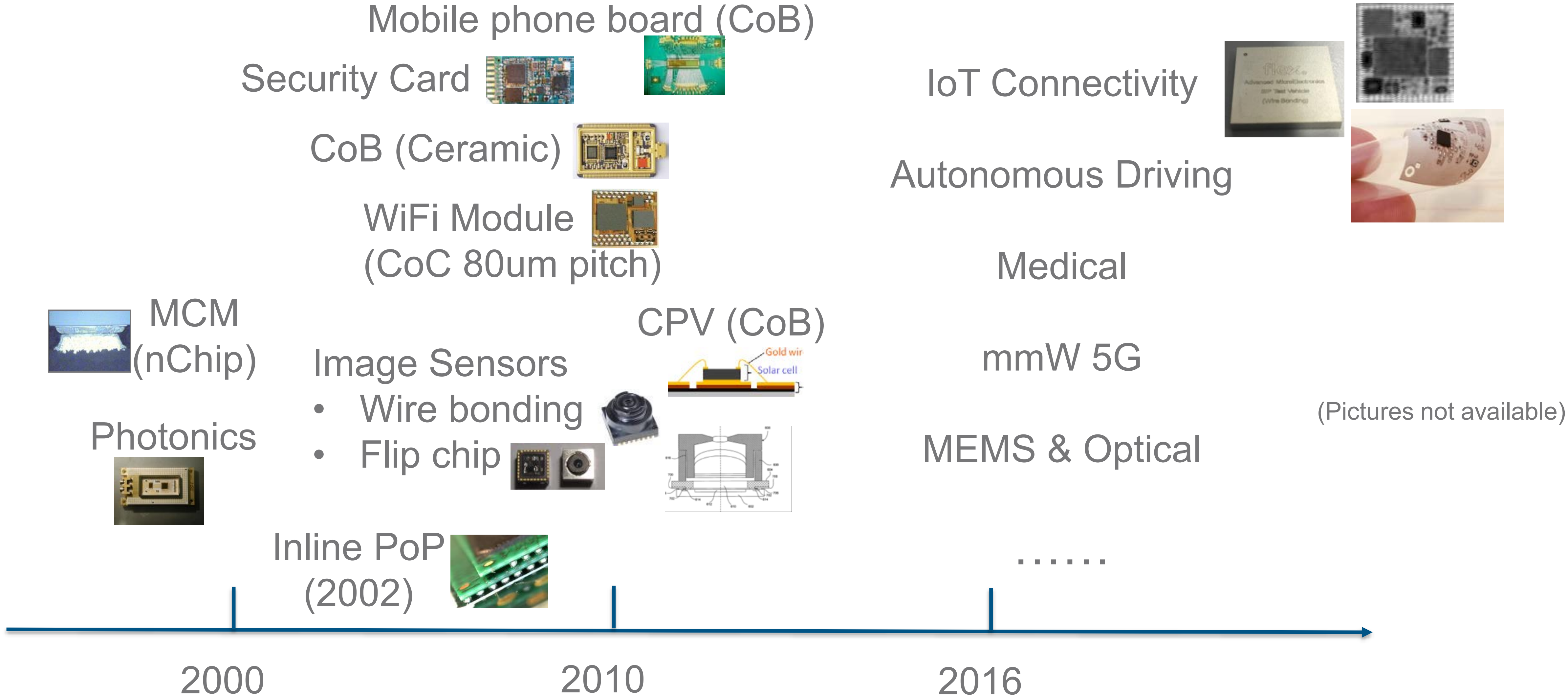
Technology

Heterogeneous Integration, Modularization, Functional Densification & Miniaturization

- **Industry-leading technology portfolio for SiP**
  - Advanced SiP Design capabilities
    - System level expertise – across market segments
  - Advanced manufacturing capabilities for SiP: rigid, flex
  - Reliability; High frequency
- **One stop turnkey solution**
  - System miniaturization, package design, process & test, proto / NPI / HVM
  - Microelectronics packaging, PCBA, System
  - Sketch to Scale
- **Optimized technology platforms & packaging configurations across market segments**
- **Flexible business models**
- **Low / medium / high volume manufacturing, global footprint & operational excellence**
- **Advanced supply chain solutions & lower total manufacturing cost**

SiP Applications (examples)

Very diverse in technology and in applications



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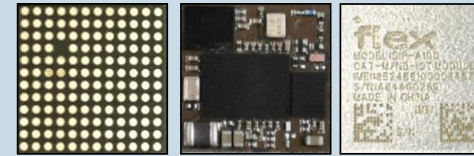
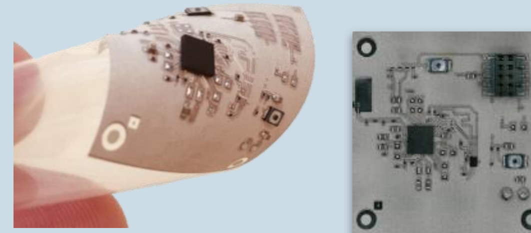
SiP Development Platforms for IoT

Program	Description	
Cellular	Smallest Cellular IoT Connectivity Module on the market - Optimized LTE CAT-M1 & NB-IoT (NB1) modem - Integrated GNSS engine - Integrated MCU with memory - Single-SKU with global RF coverage	 10mm x 10mm
BLE	Smallest IoT Sensing Module - Ultra low-power MCU - Optimized Bluetooth 5.0 Low Energy (BLE) radio - Built-in BLE antenna inside the SiP - Integrated sensors: 3-axis accelerometer & IR-based temperature sensor	 11mm x 12mm
FHE	Flexible IoT Development Platform - MCU + BLE + Antenna + Sensor - Solderable Ink with low temp solder - Flexible copper clad technology	

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Thank You