IEEE/EPS Chapter Lecture
Silicon Valley Area (SCV, SF, OEB)

Recent Advances and Outlook for Heterogeneous Integration

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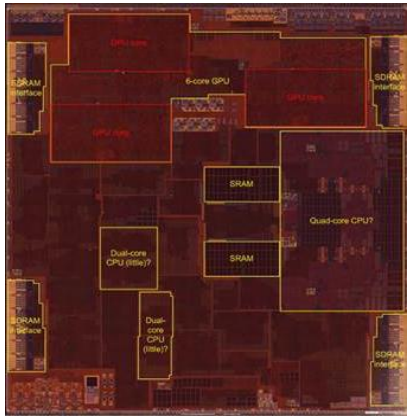
CONTENTS

Moore's Law - Apple's Application Processors (AP): A10, A11, A12, and A13

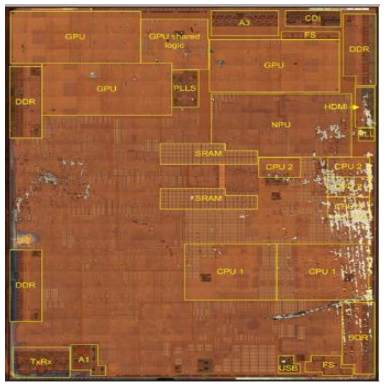
A10



A10 consists of:

- 6-core GPU (graphics processor unit)
- 2 dual-core CPU (central processing unit)
- 2 blocks of SRAMs (static random access memory), etc.
- 16nm process technology
- Transistors = 3 billion
- Chip area ~ 125mm^2

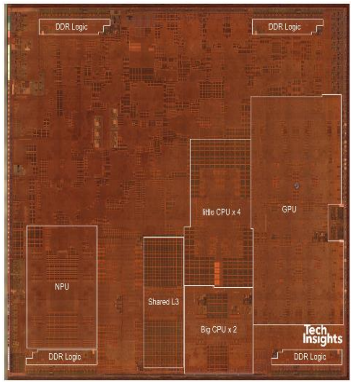
A11



A11 consists of:

- More functions, e.g., 2-core Neural Engine for Face ID
- Apple designed tri-core GPU
- 10nm process technology
- Transistors = 4.3 billion
- Chip area ~ 89mm^2

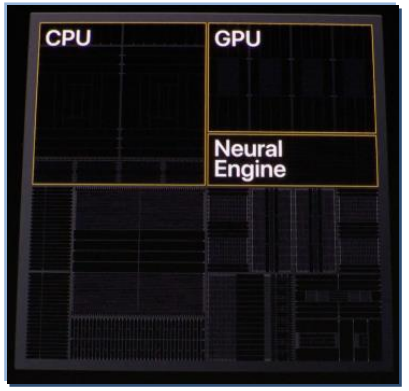
A12



A12 consists of:

- Eight-core Neural Engine with AI capabilities
- Four-core GPU (faster)
- Six-core CPU (better performance)
- 7nm process technology
- Transistors = 6.9 billion
- Chip area = 83mm^2

A13

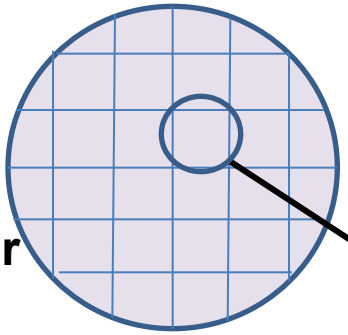


A13 consists of:

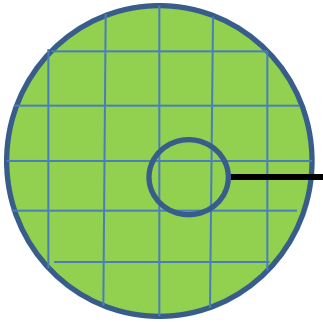
- Eight-core Neural Engine with Machine Learning
- Four-core GPU (20% faster > A12)
- Six-core CPU (20% faster and 35% save energy > A12)
- 7nm process technology with EUV
- Transistors = 8.5 billion
- Chip area ~ 100mm^2 (9.26mmx10.8mmm)

Definition of Heterogeneous Integration (SiP)

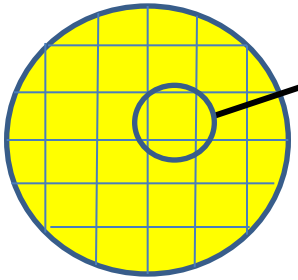
- Chip-1
- FAB-1
- 7nm
- 12”-wafer

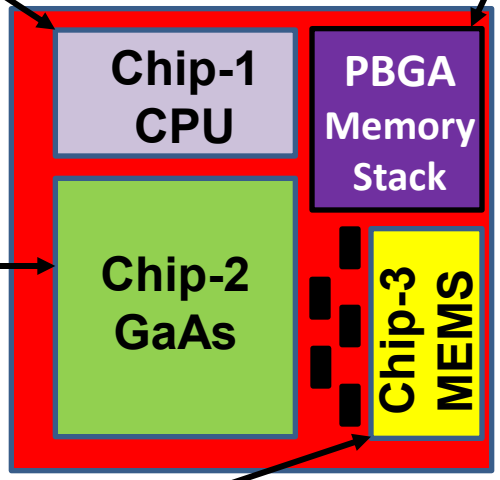


- Chip-2
- FAB-2
- 64nm
- 8”-wafer



- Chip-3
- FAB-3
- 100nm
- 6”-wafer





- Time-to-market
- Less IP issues
- Flexibility
- Low cost alternative than SoC
- Optimized signal integrity and power

Heterogeneous integration uses packaging technology to integrate dissimilar chips, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

Heterogeneous Integration vs. Moore's Law

Why Heterogeneous Integration?

This is because of the end of the Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. Heterogeneous integration is going to take some of the market shares away from SoC.

What are Heterogeneous Integration for?

For the next five years, we will see more of a higher level of heterogeneous integration, whether it is for:

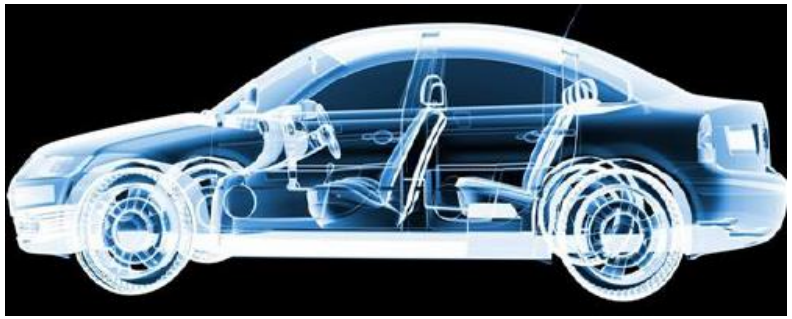
- **Time-to-market**
- **Performance**
- **Form factor**
- **Power consumption**
- **Cost**

Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on Silicon Substrate (TSV-less Interposers)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

Amkor Automotive SiP

- Large singulated body SiP
- Infotainment & ADAS
- Autonomous driving
- Computers in a car
- Increasing trend in designs

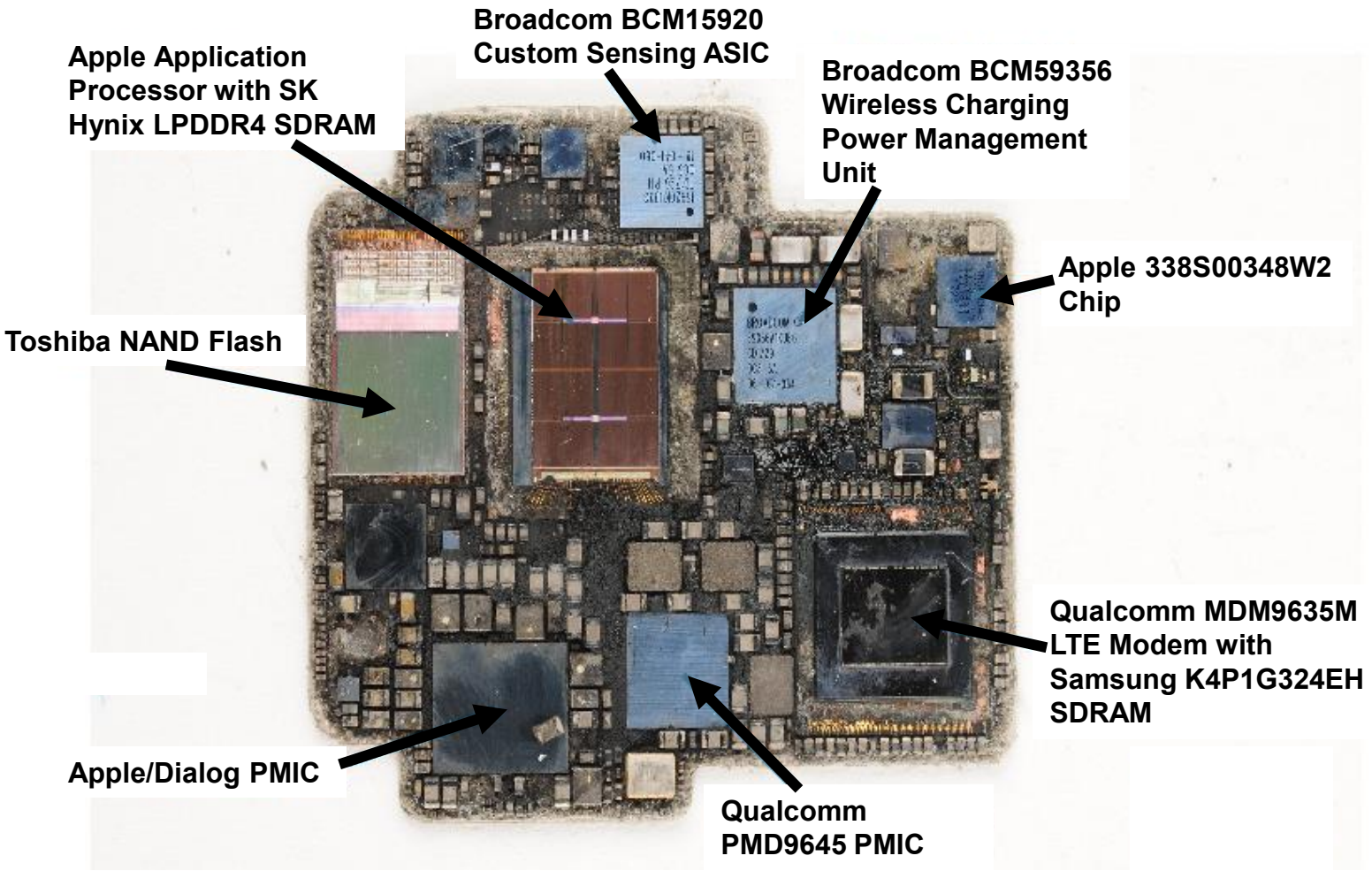


42.5 x 42.5 mm, Infotainment, Processor + DDR

55 x 72 mm, Network Switch, ASIC + Memory

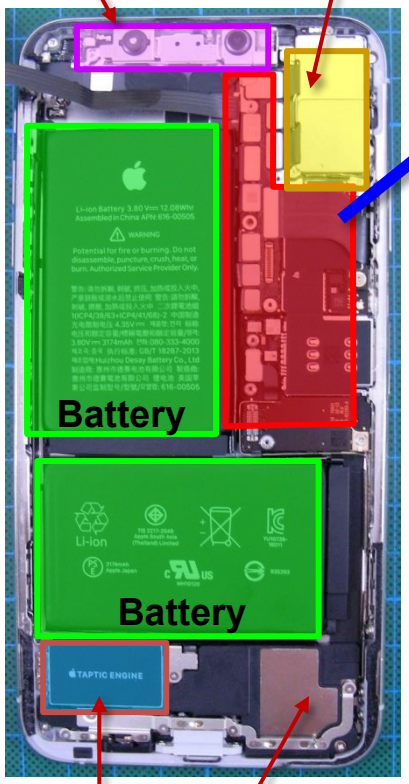
Heterogeneous Integration on organic-substrate

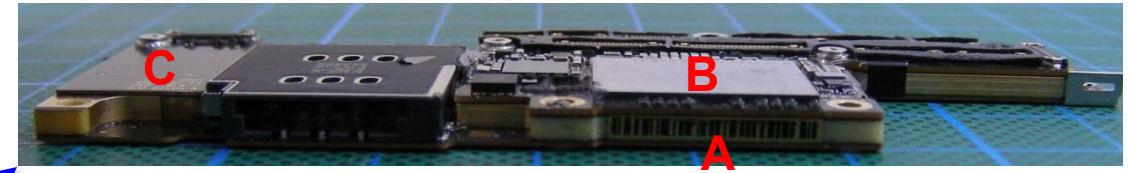
The Apple Watch is SiP and was Assembled by ASE (Universal Scientific Industrial – Shanghai)

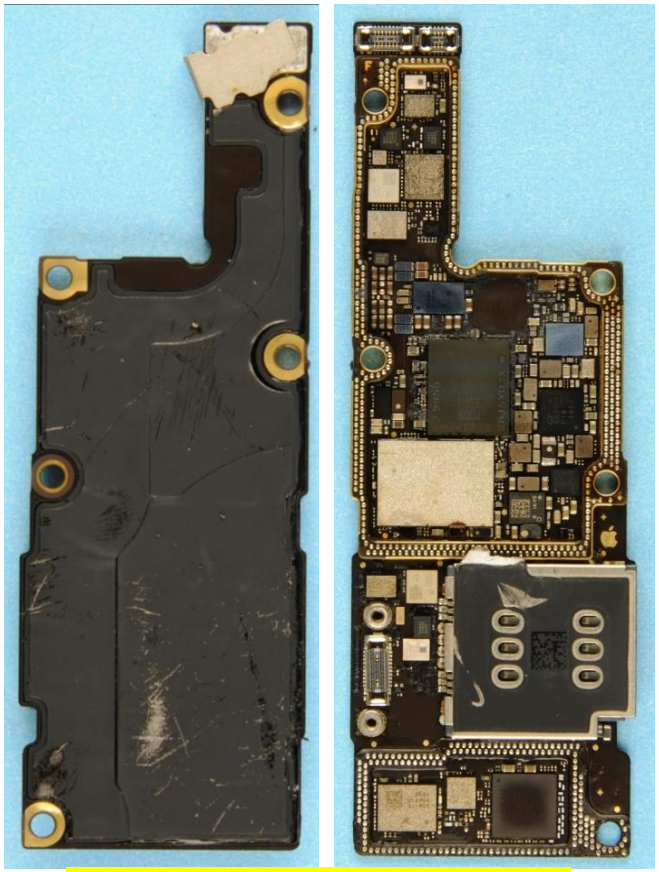


Heterogeneous Integration on Organic-Substrate

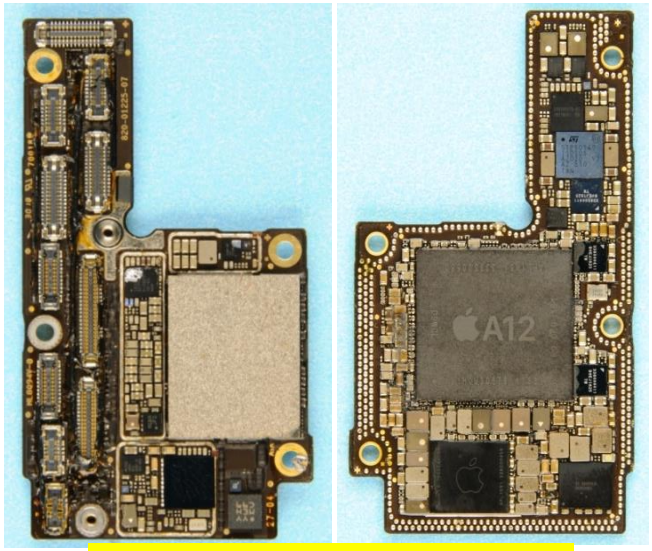
Three Substrate-Like PCBs in iPhone XS and XS Max



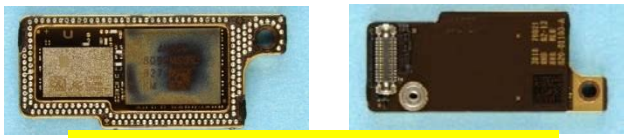




A: Rear PCB
(1-sided assembly)

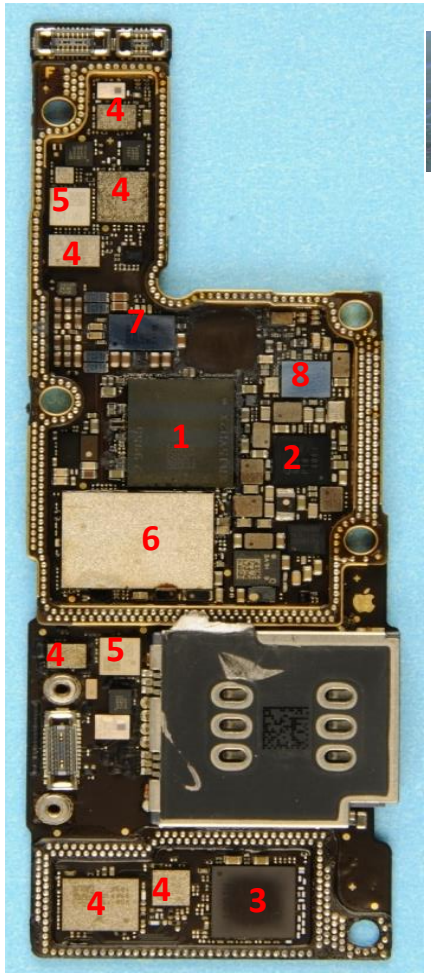


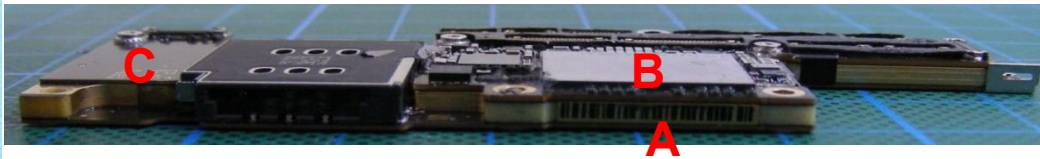
B: Front PCB1
(2-sided assembly)



C: Front PCB2
(2-sided assembly)

SiP in the Rear PCB of iPhone XS and XS Max



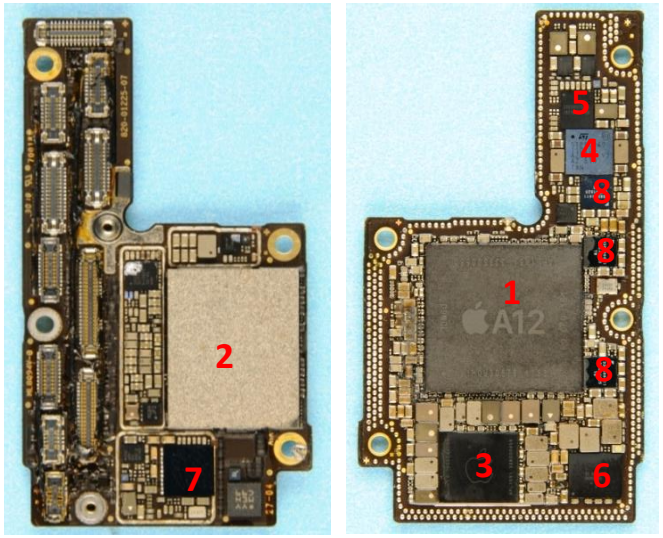


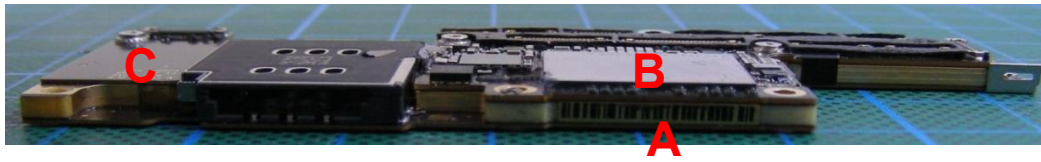
[1] Intel Baseband Chipset
[2] Intel PM IC
[3] Intel RF Transceiver
[4] Skyworks RF FEM
[5] Murata RF FEM (front-end module)
[6] USI WiFi/BT Module
[7] Broadcom Wireless Charger
[8] NXP NFC Controller

Rear PCB (A)

- 8L HDI, 4mSAP layers, 16cm^2
- Single-Sided Assembly
- Baseband, RF, WiFi/BT
- All components face inward

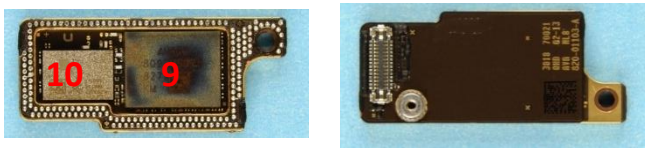
SiPs in the Front PCB1 and Front PCB2





Front PCB 1 (B)

- 10L HDI, 6 mSAP layers, 10cm^2
- Double-Sided Assembly
- A12 CPU, Memory, Connectors
- A12 CPU faces inward



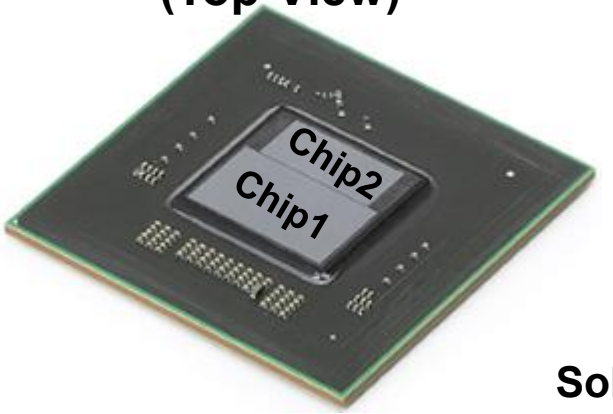
Front PCB 2 (C)

- 6L HDI, 2 mSAP layers, 2cm^2
- Double-Sided Assembly
- RF FEM, Connectors
- RF FEM face inward

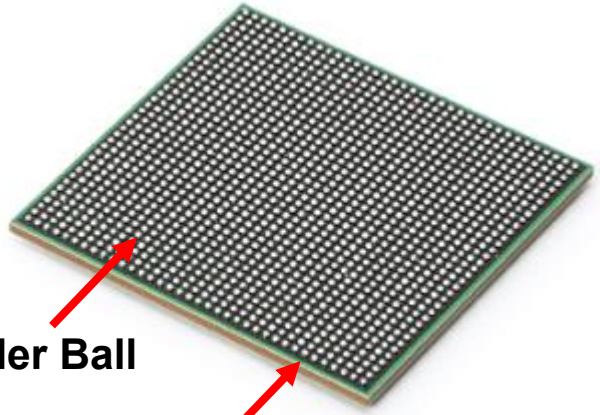
[1] Apple A12 Chipset
[2] Flash Memory
[3] Power Manager
[4] ST Power Manager
[5] Power Manager
[6] TI Battery Charger
[7] Audio Codec
[8] Audio Amplification
[9] Avago RF FEM
[10] Skyworks RF FEM

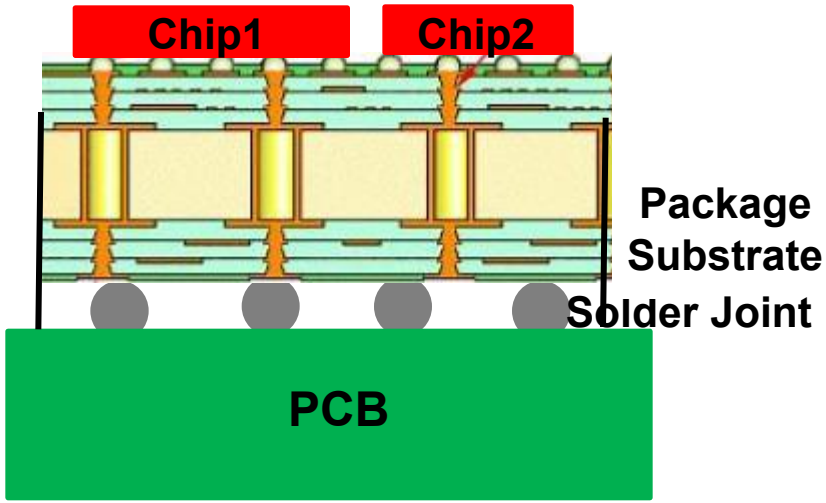
Heterogeneous Integration (Flip Chip) on Organic Substrate (2D IC Integration)

2D IC Integration
(Top-View)

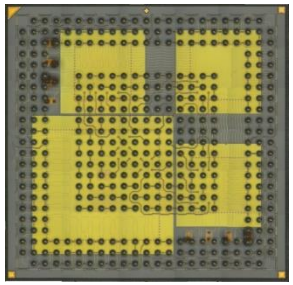


2D IC Integration
(Bottom-View)

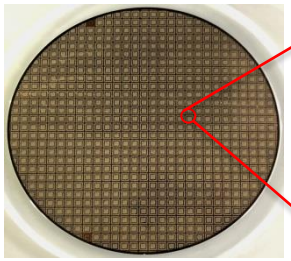




Heterogeneous Integration of 4 Chips and 4 Capacitors (Fan-Out) on PCB (2D IC Integration)



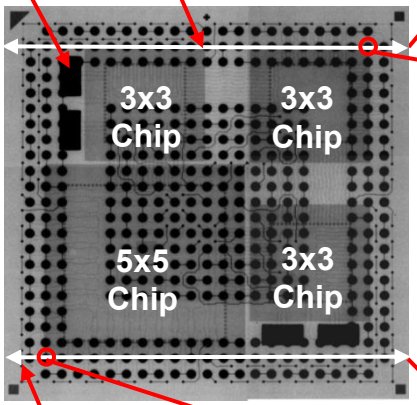
300mm

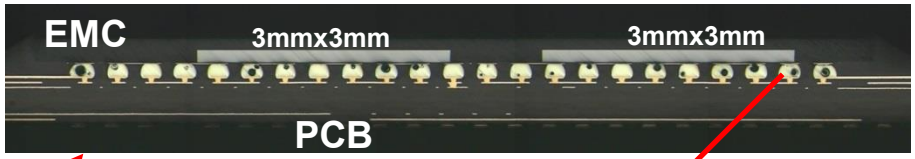


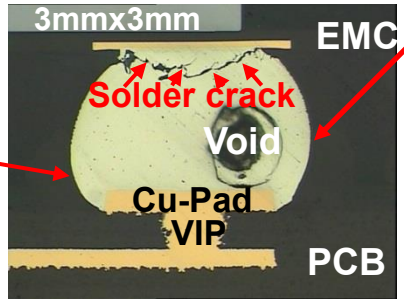
Reconstituted Wafer

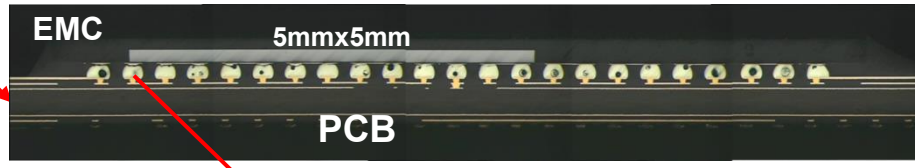
Capacitor

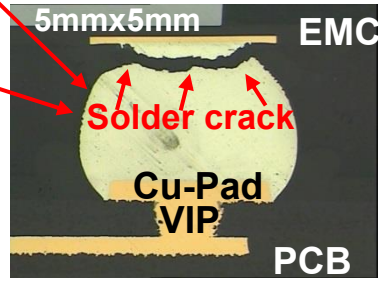
Cross Section



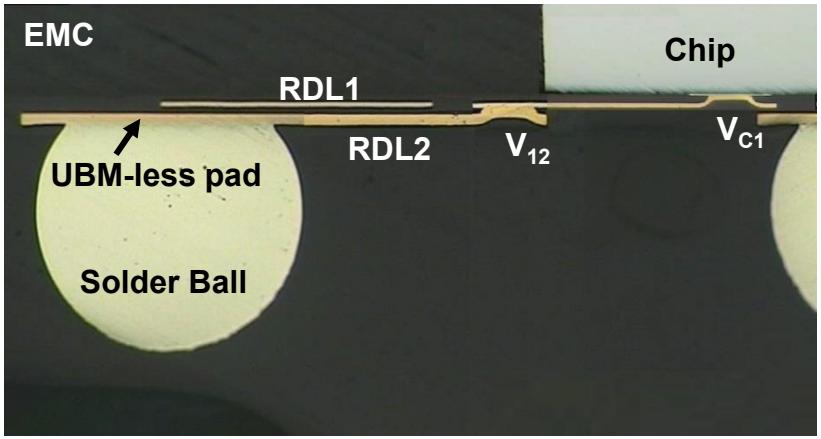








Cross Section

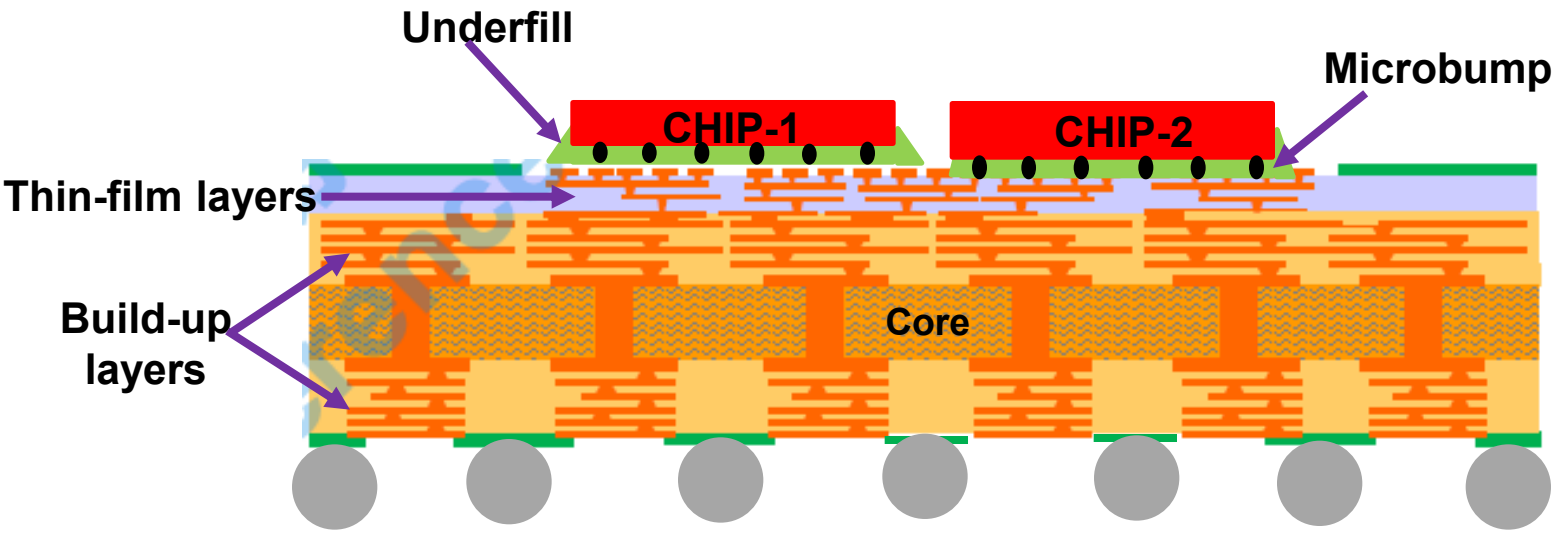


Thermal Cycling Test Results

IEEE Trans. CPMT
2018, pp. 1544-1560

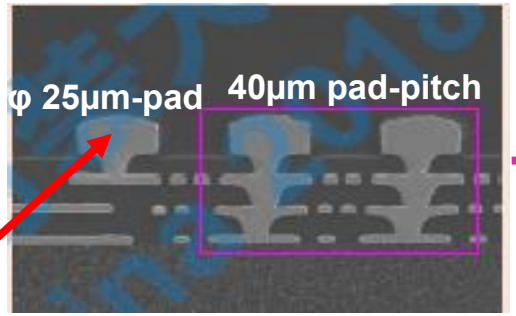
ASM DOW HUAWEI INDIUM JCET jcap 江阴长电先进封装有限公司 JIANGYIN CHANGDIAN ADVANCED PACKAGING CO., LTD. **Unimicron**

Shinko's i-THOP Substrate for Heterogeneous Integration (2.1D IC Integration)

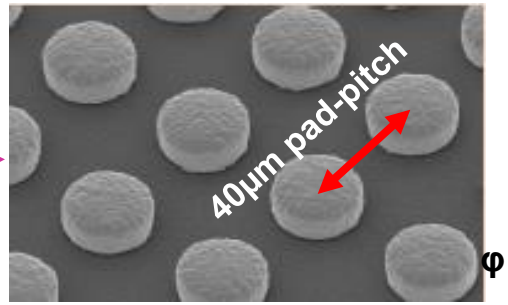


i-THOP (integrated thin-film high density organic package)

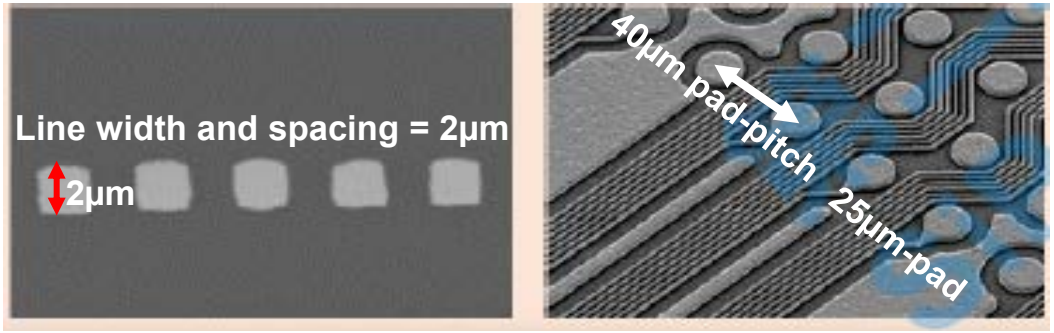
Shinko's i-THOP Substrate

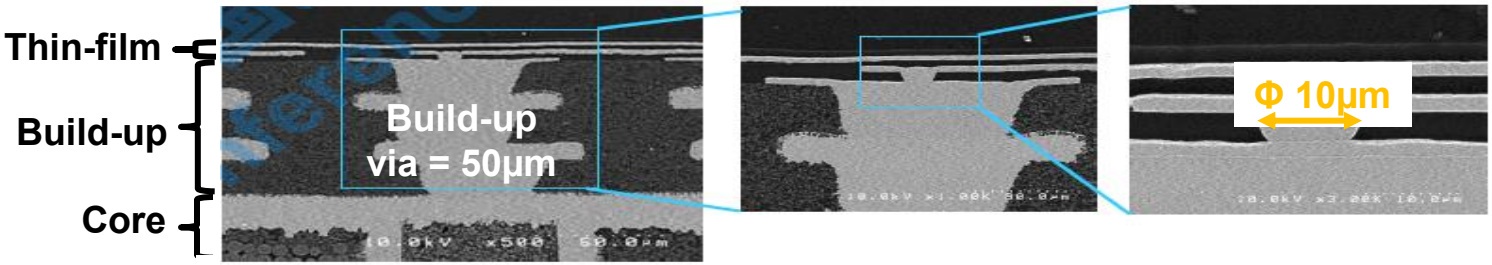


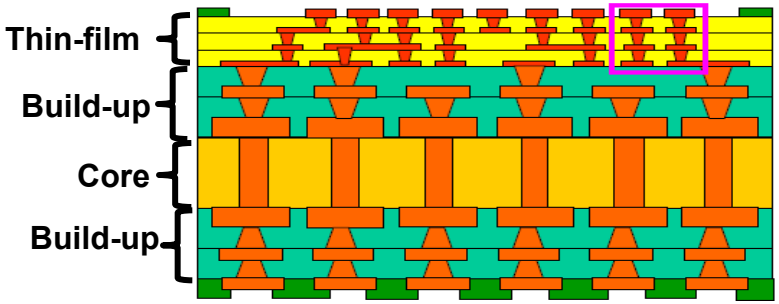
Cu-pad thickness = 11.8μm



φ 25μm Cu-pad



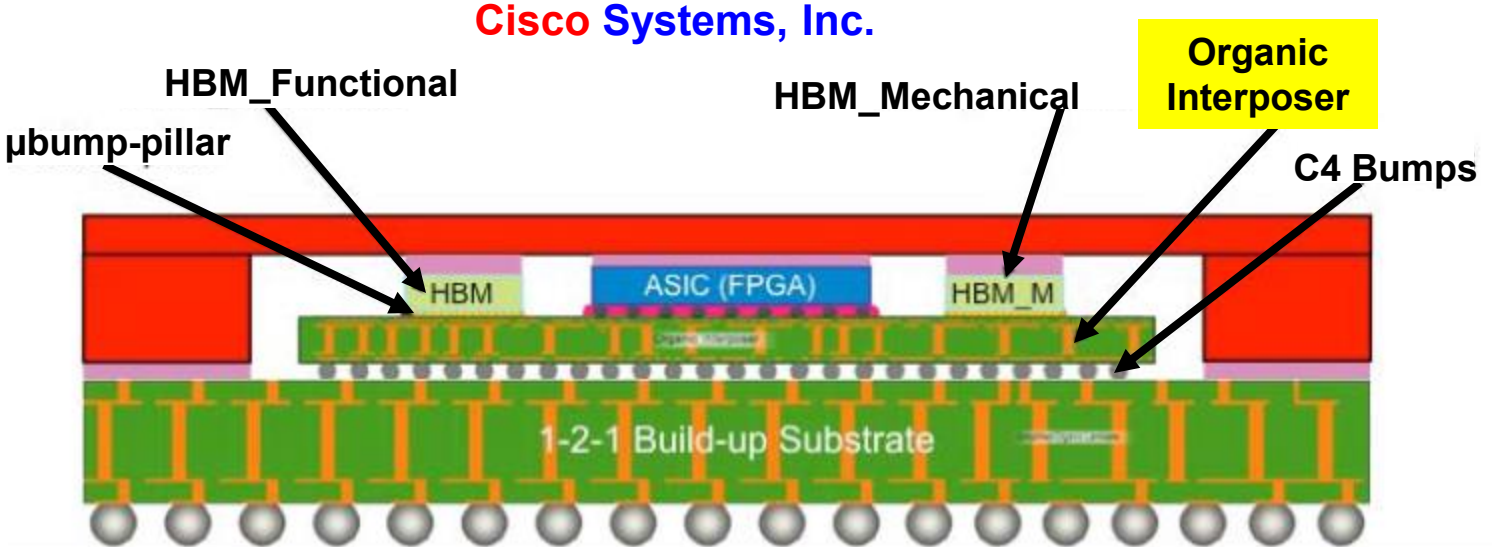


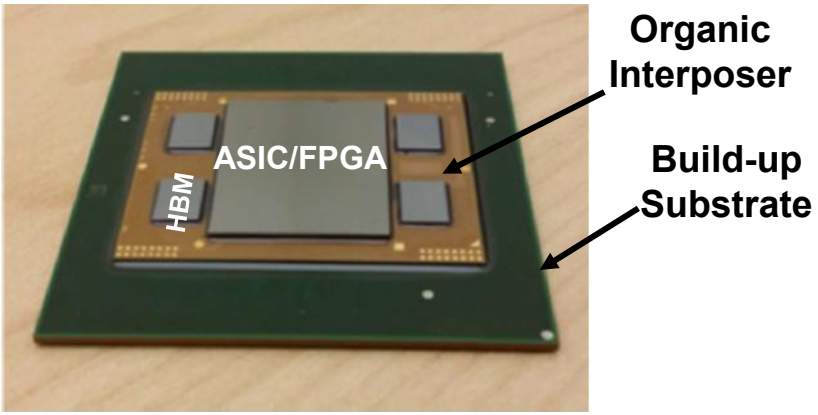


Lau, PDC, ECTC2015

3D SiP with Organic Interposer for ASIC and Memory Integration (2.3D IC Integration)

Li Li, Pierre Chia, Paul Ton, Mohan Nagar, Sada Patil, Jie Xue
Cisco Systems, Inc.



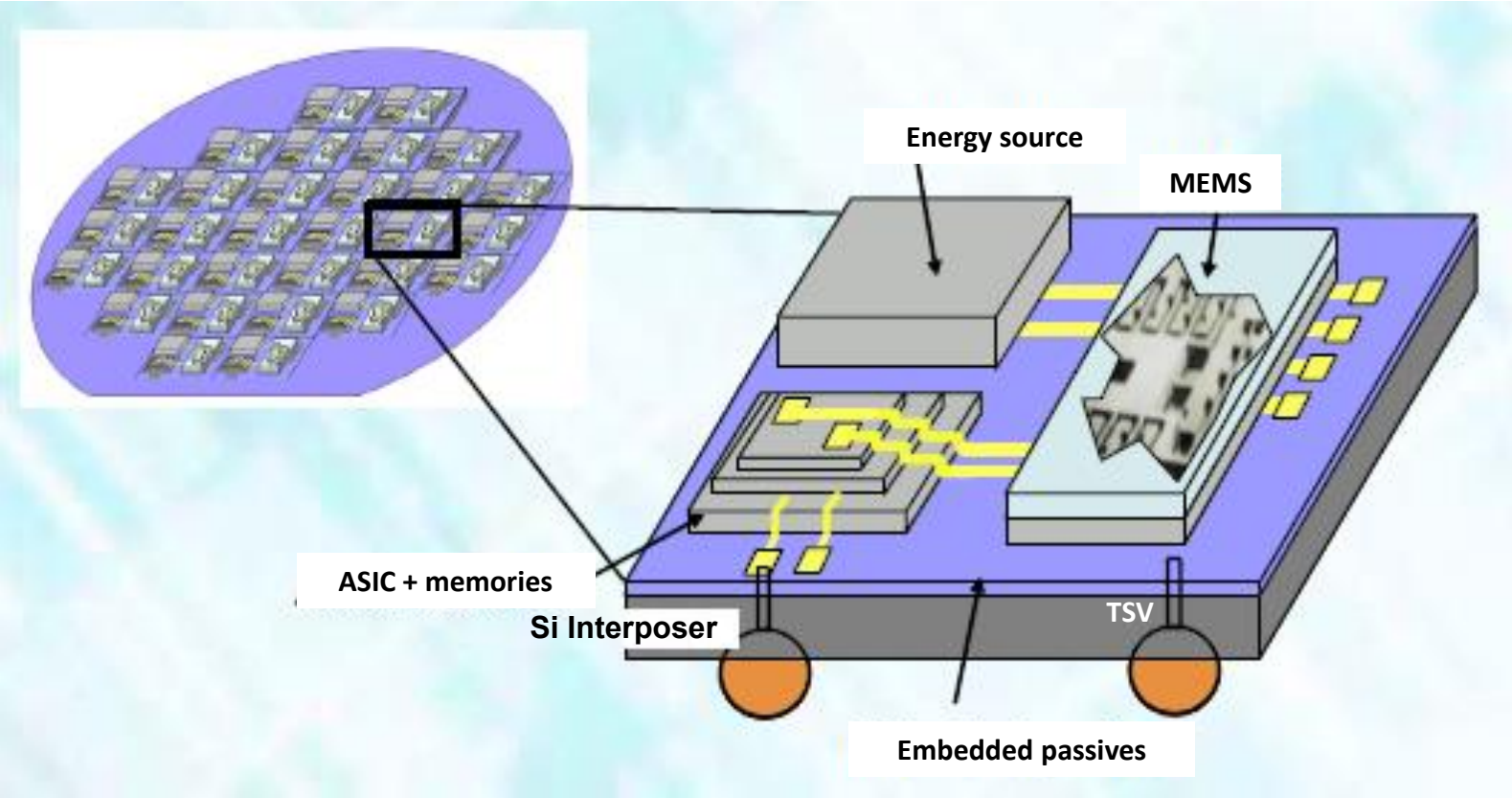


Heterogeneous Integration on Organic-Substrate

Classification of Heterogeneous Integrations

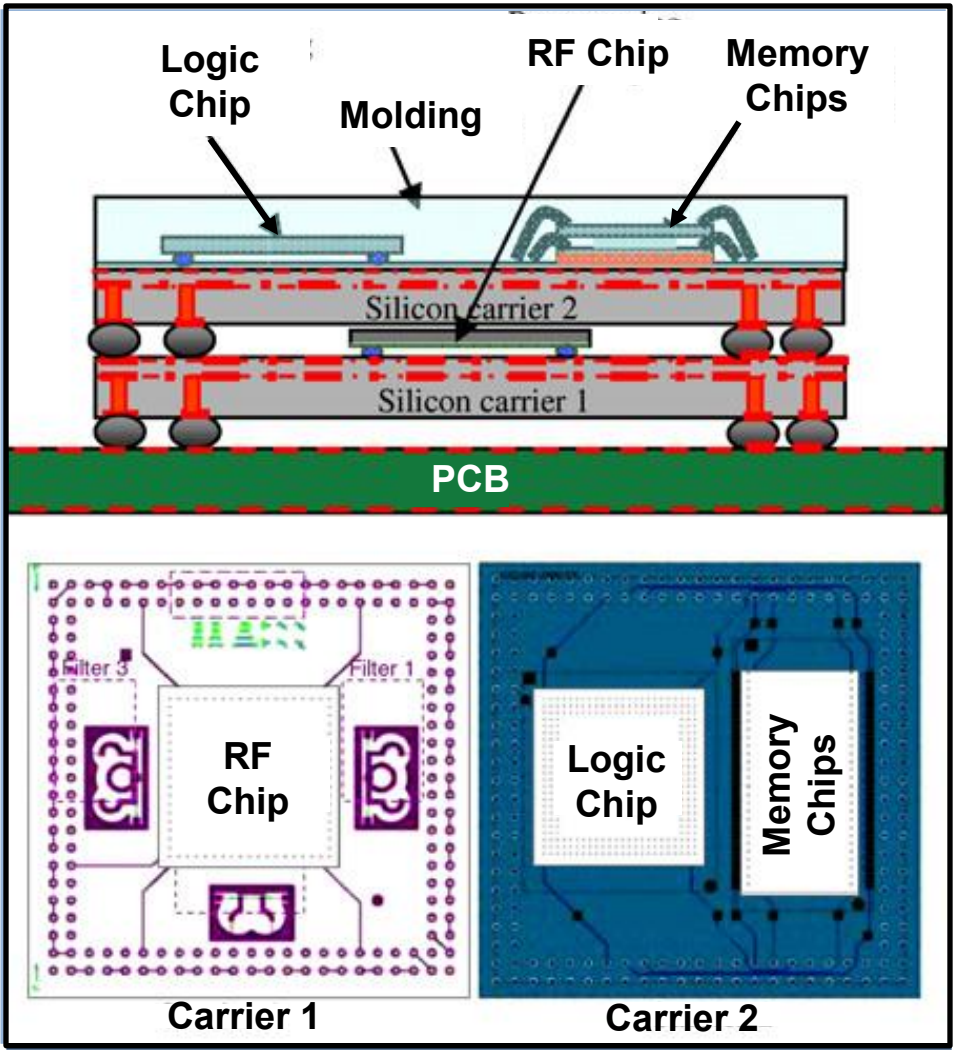
- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on Silicon Substrate (TSV-less interposers)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

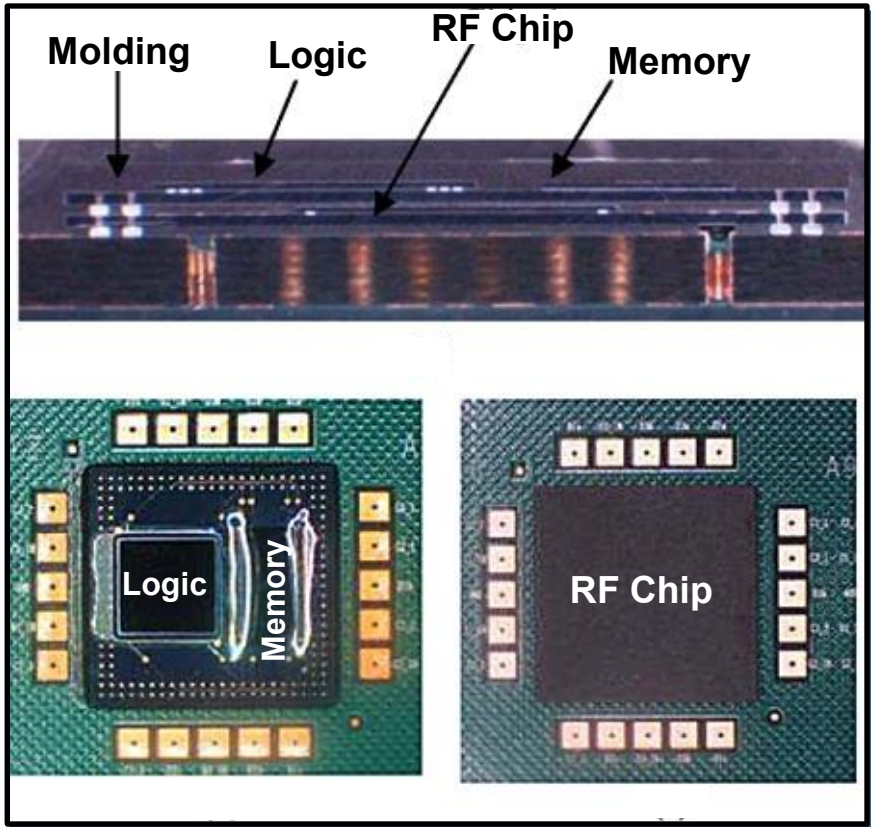
Leti's Heterogeneous Integration: System-on-Wafer (SoW) (2.5D IC Integration)



Heterogeneous Integration on Si-substrate (TSMC called this: CoWoS)

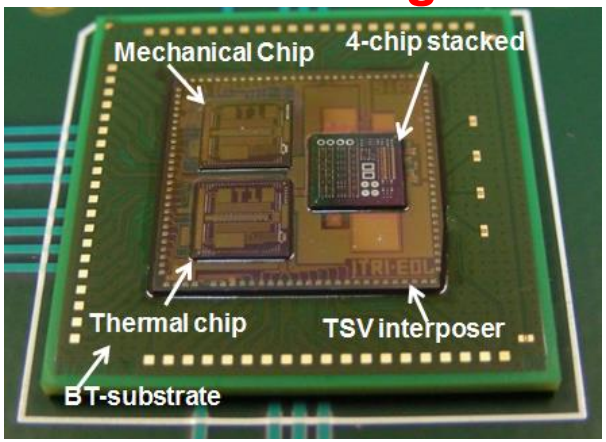
IME's Heterogeneous Integration of RF Chip, Logic chip, and Memory chips

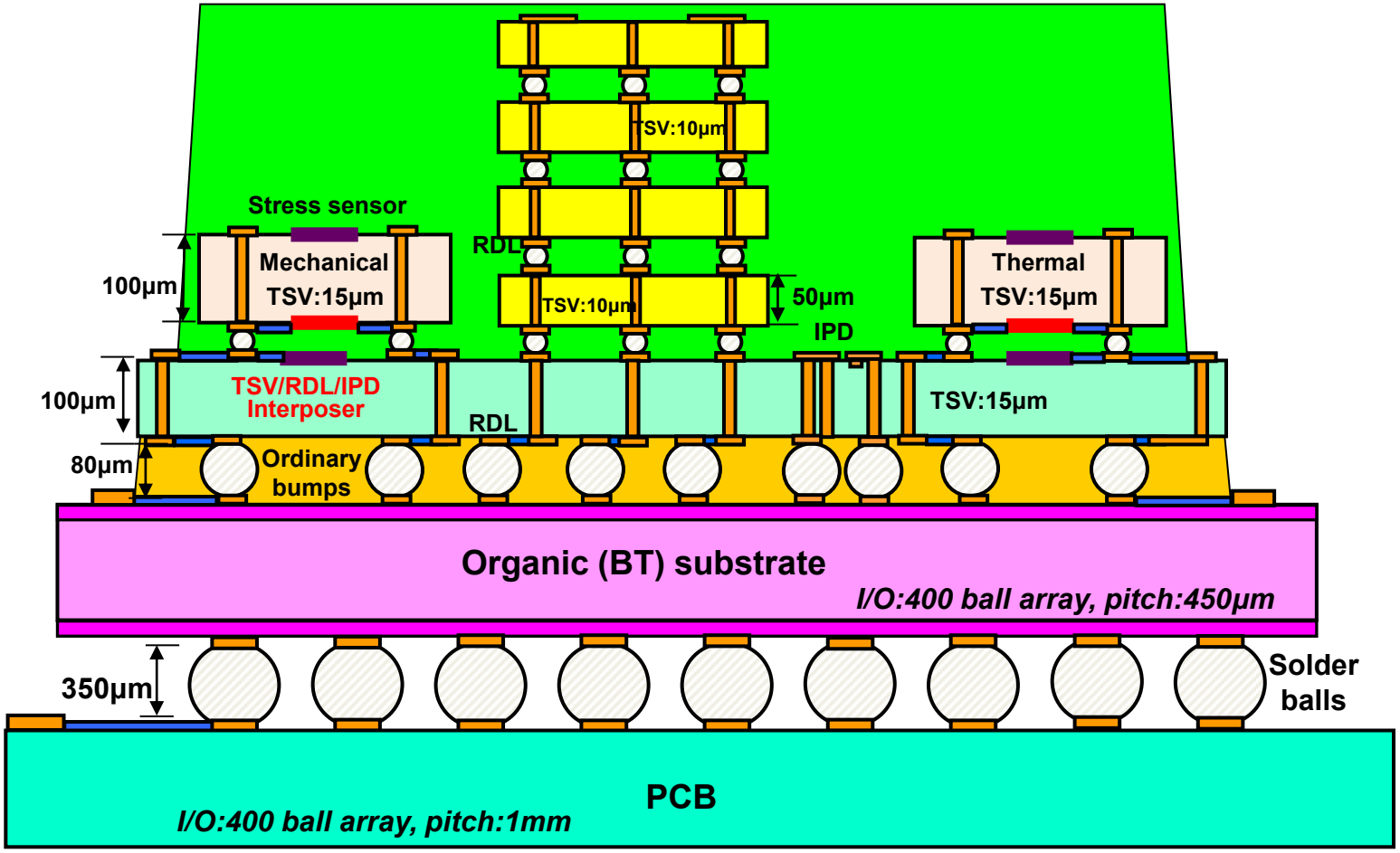




IEEE Trans. on CPMT, 2010.

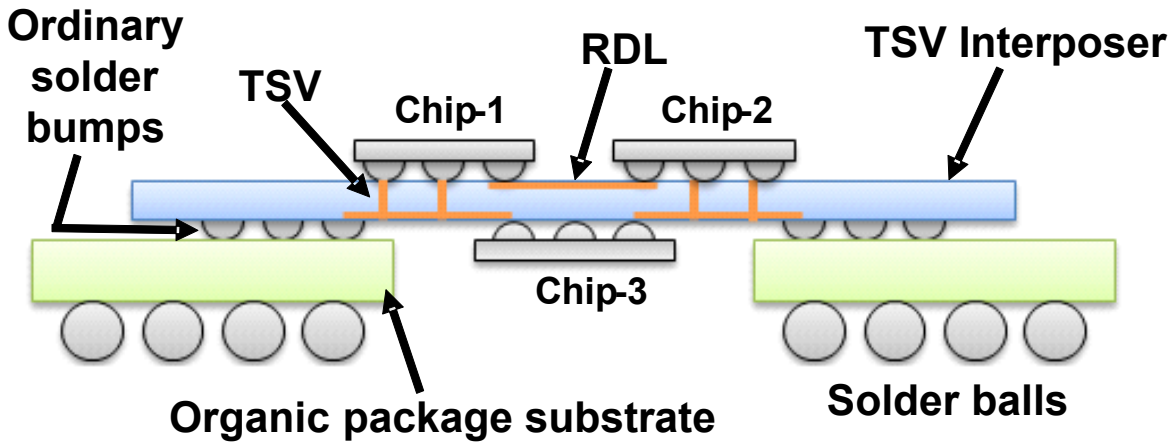
ITRI's 2.5D IC Integration

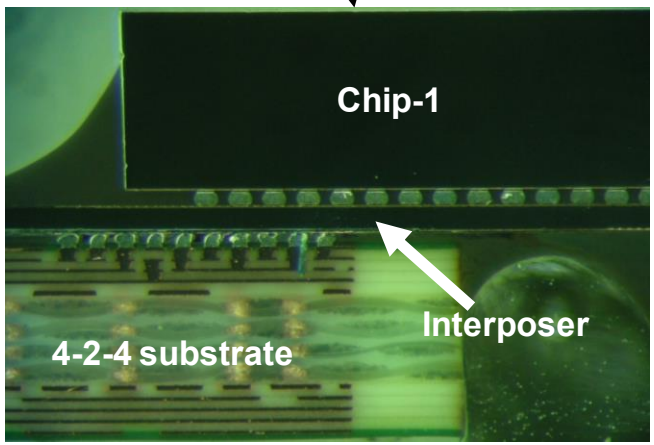


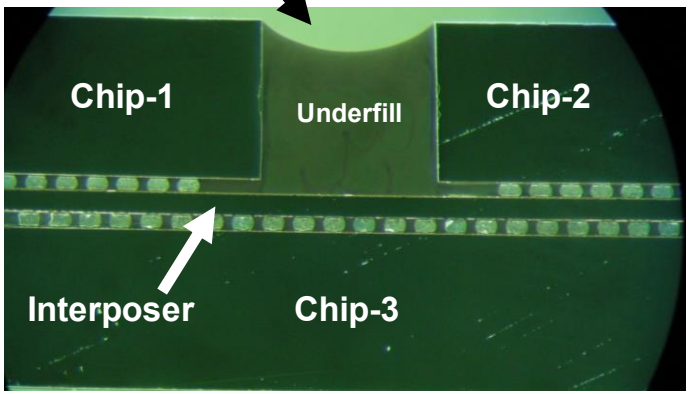


IMAPS Trans. 2011.

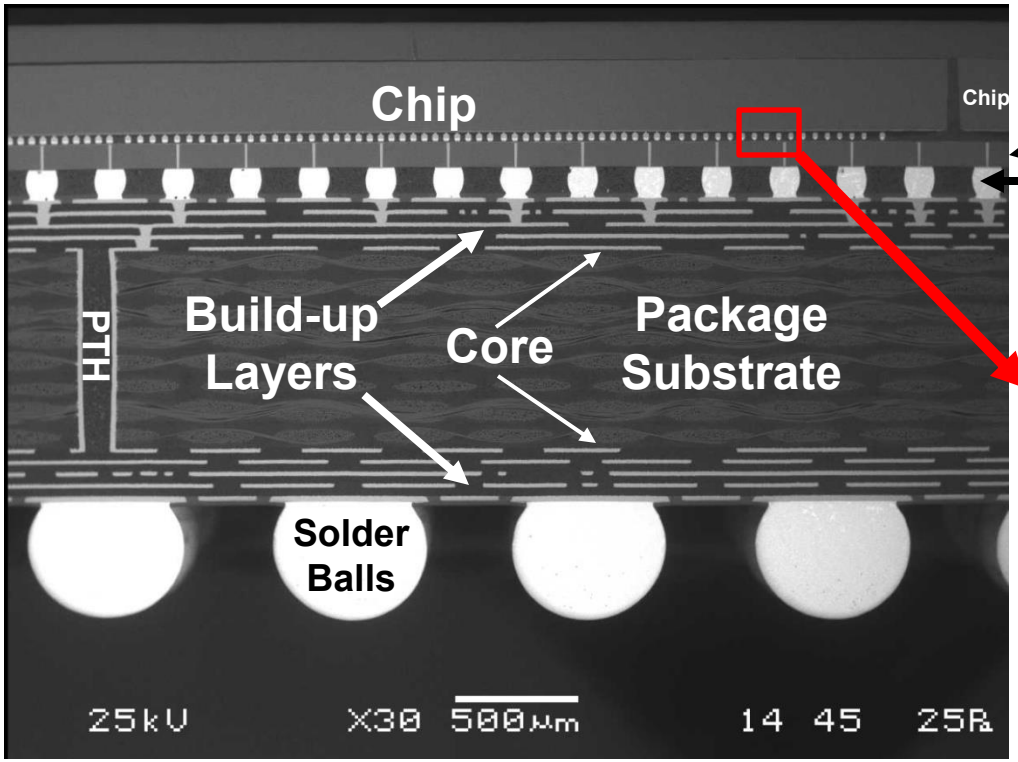
ITRI/Rambus' Heterogeneous Integration of Chips



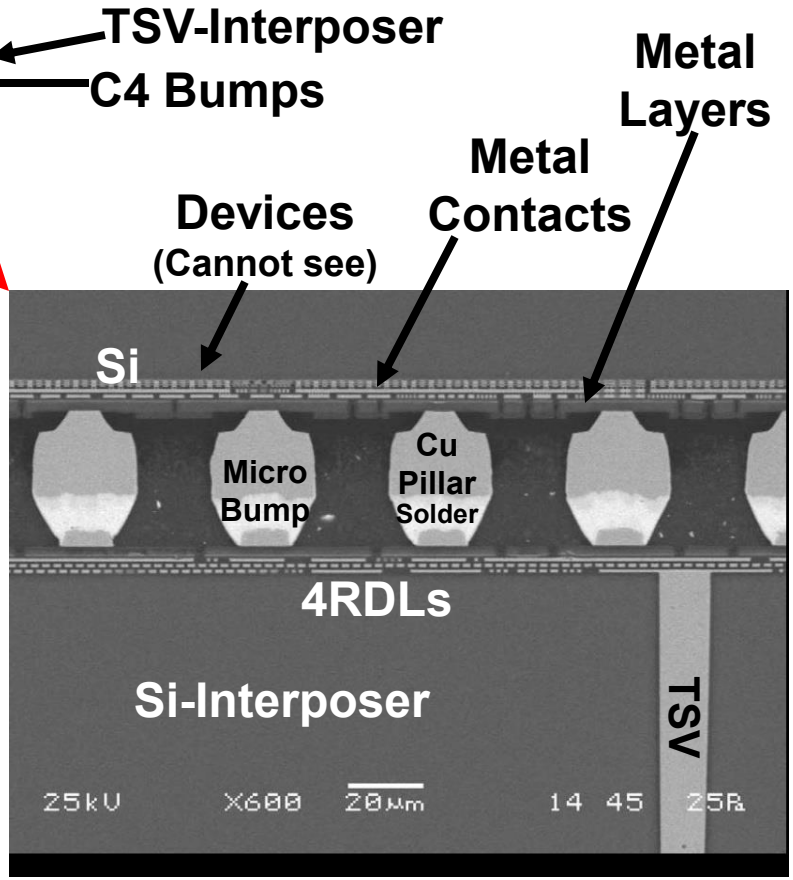




Xilinx/TSMC's 2.5D IC Integration with FPGA



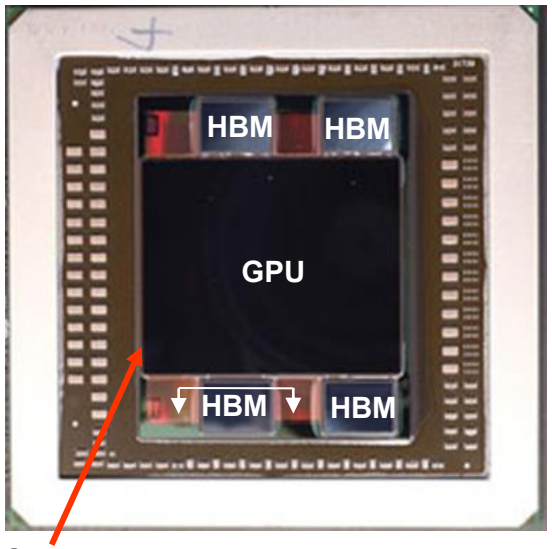
CoWoS
(chip on wafer on substrate)

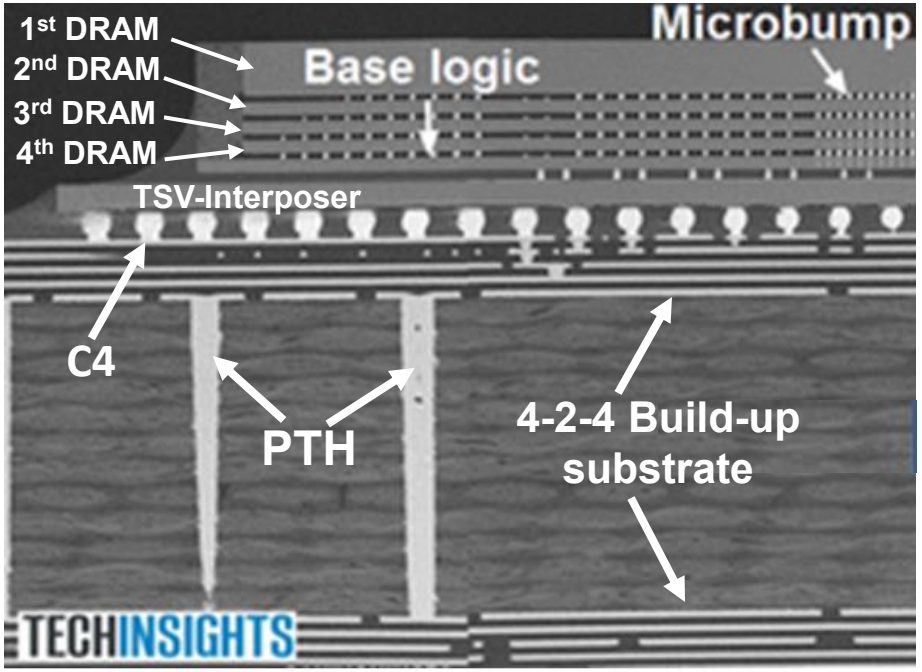


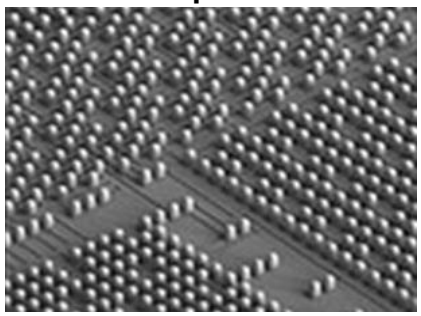
Homogeneous Integration on Si-substrate

- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

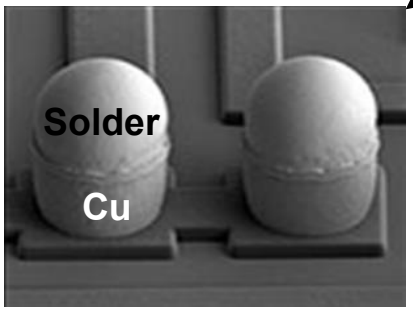
AMD's GPU (Fiji), Hynix's HBM, and UMC's Interposer

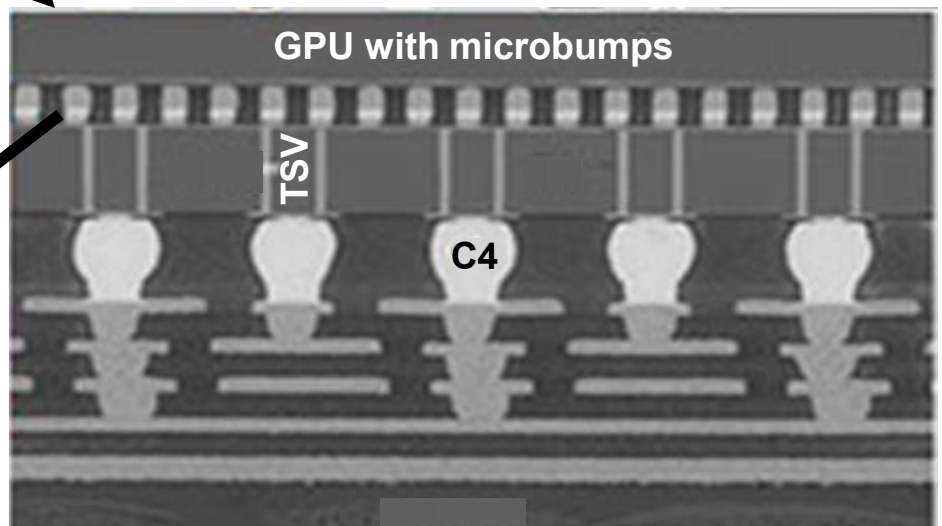






Cu-Pillar with solder Cap





TSV-Interposer

Build-up organic substrate

Lau, PDC, ECTC2016

TSMC's CoWoS-2

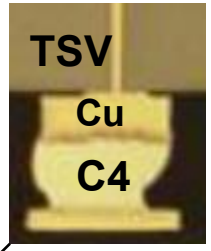
µSolder Joints

µSolder Joints

Memory Cube

TSV

Cu-C4 Solder Joints



SoC
CPU/GPU/FPGA/ASIC

Logic

RDLs

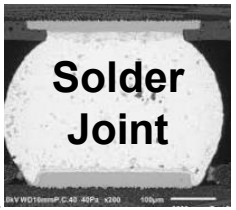
TSV

TSV-interposer

C4

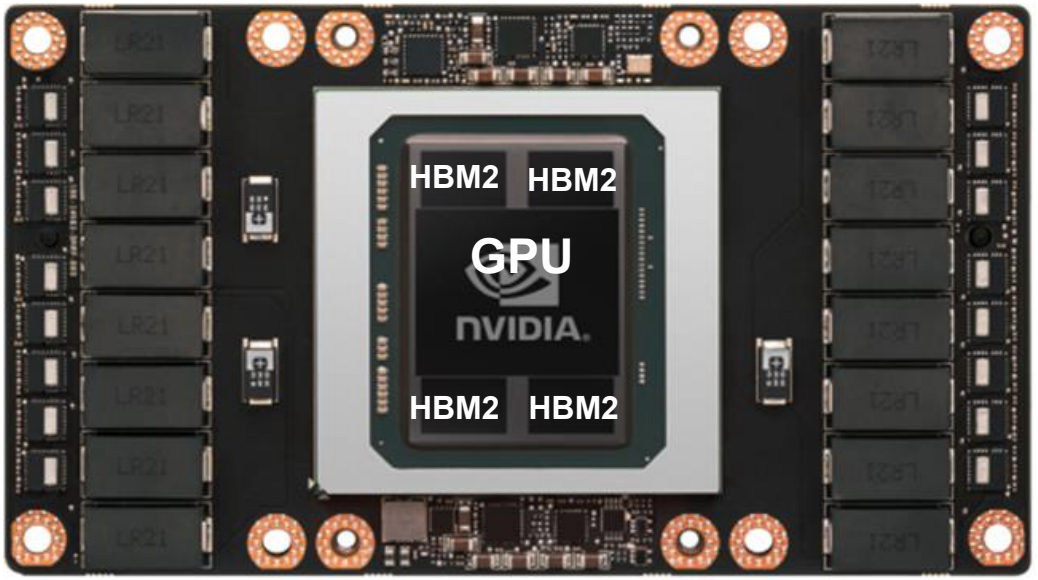
Cu

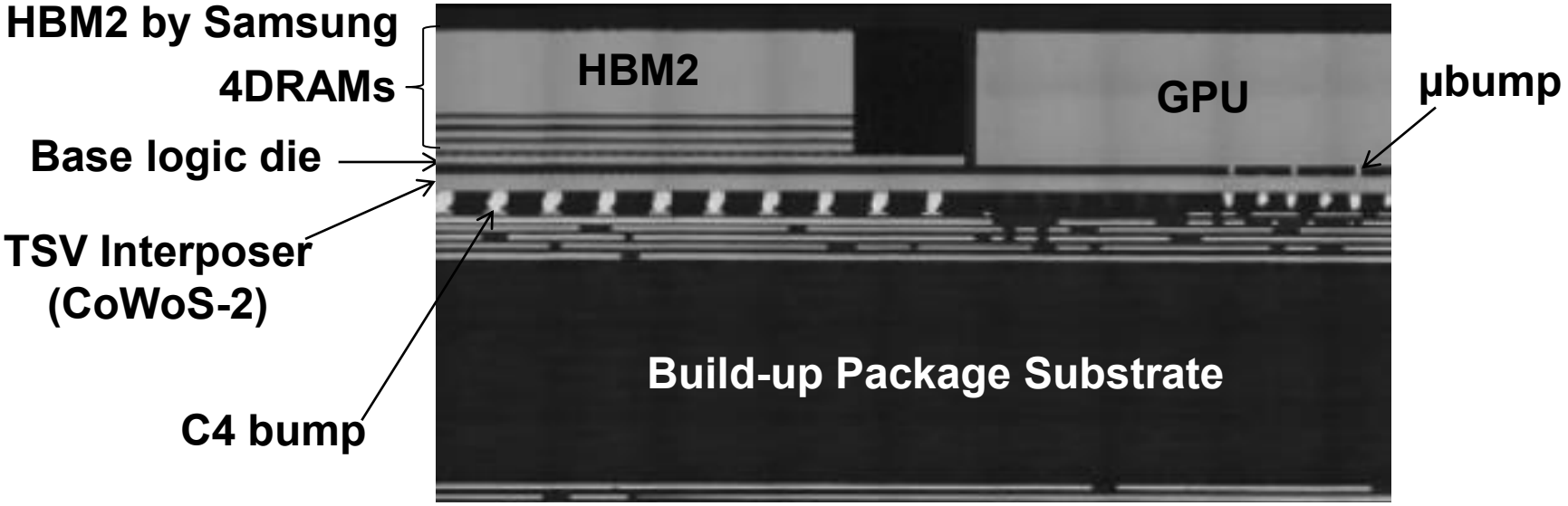
Build-up Package Substrate



PCB

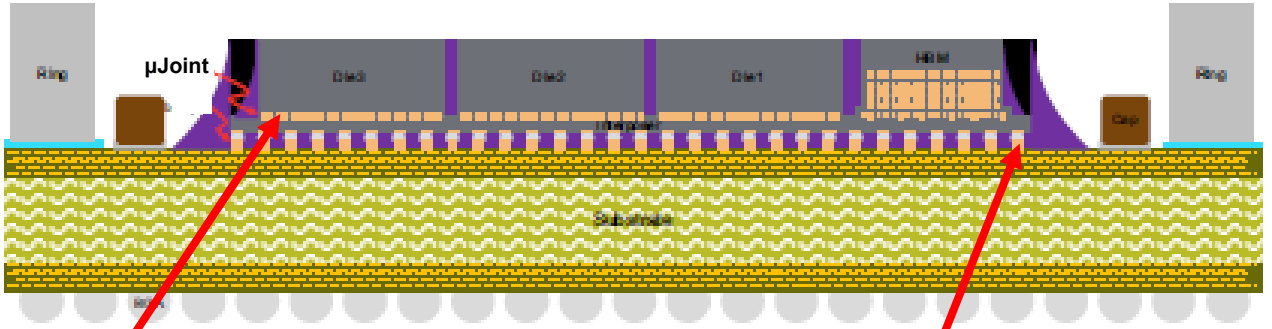
NVidia's P100 with TSMC's CoWoS-2 and Samsung's HBM2



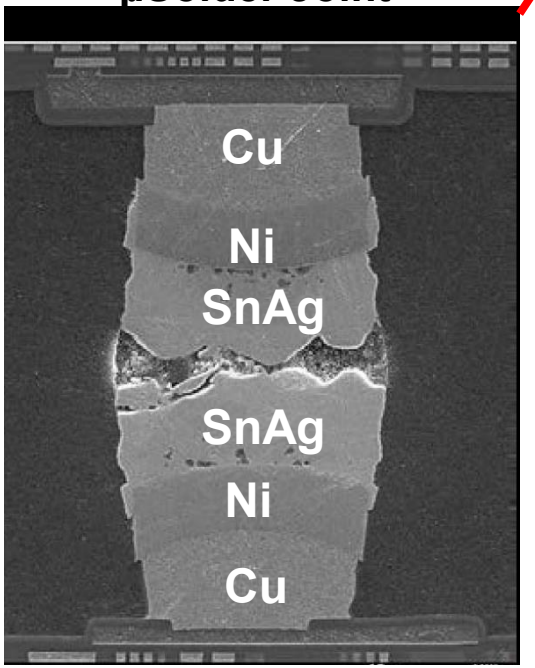


Heterogeneous Integration on Si-Substrate

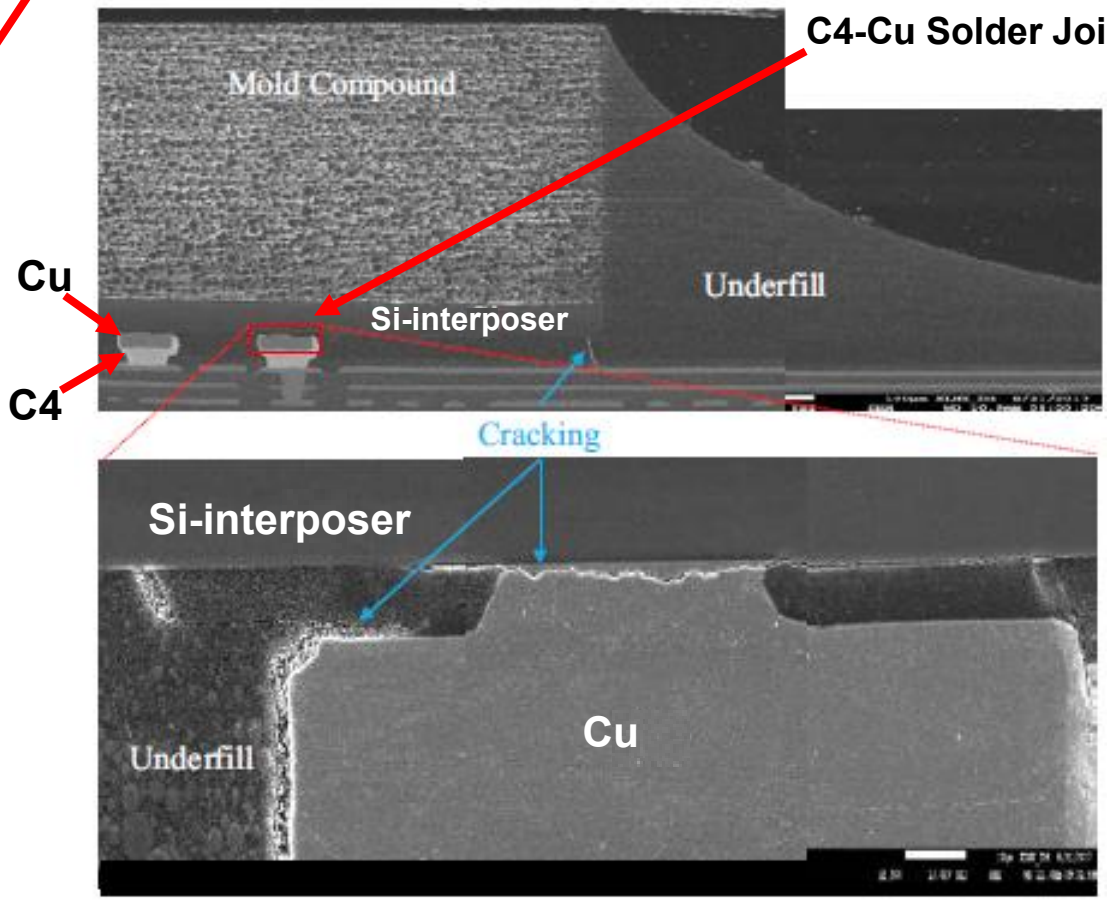
Xilinx's HPC Applications Driven by AI and 5G



µSolder Joint

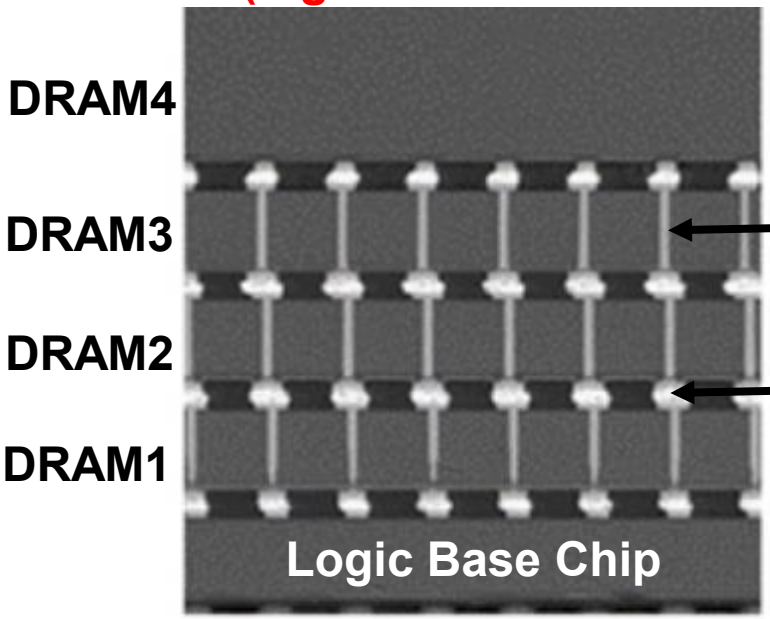


C4-Cu Solder Joint

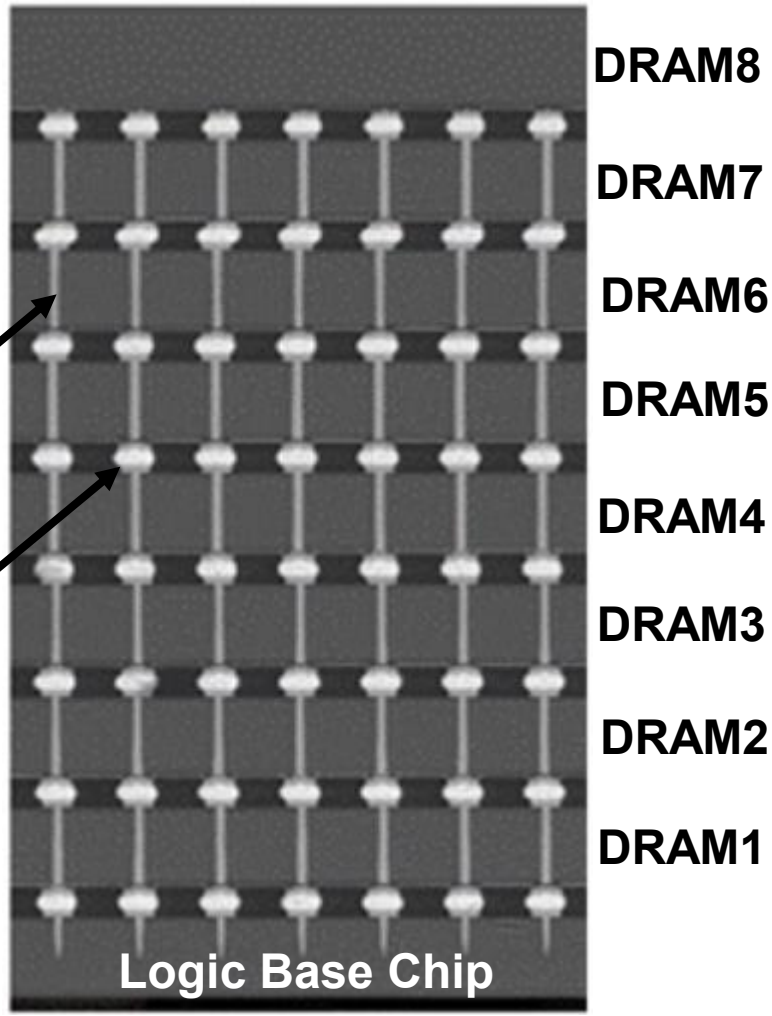


3D IC Integration

HBM (high bandwidth memory)



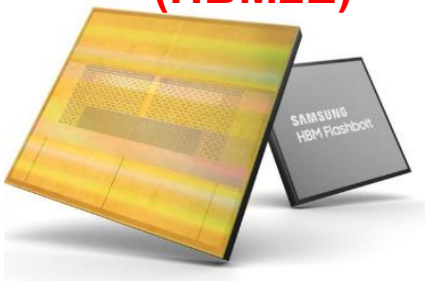
HBM2



TSV

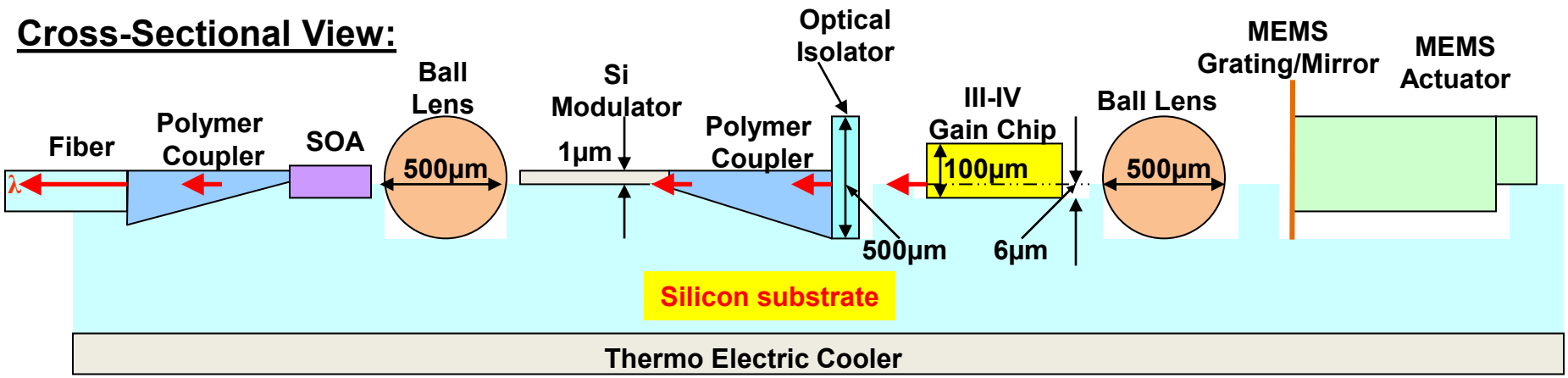
μSolder Joint

HBM2 Evolutionary (HBM2E)

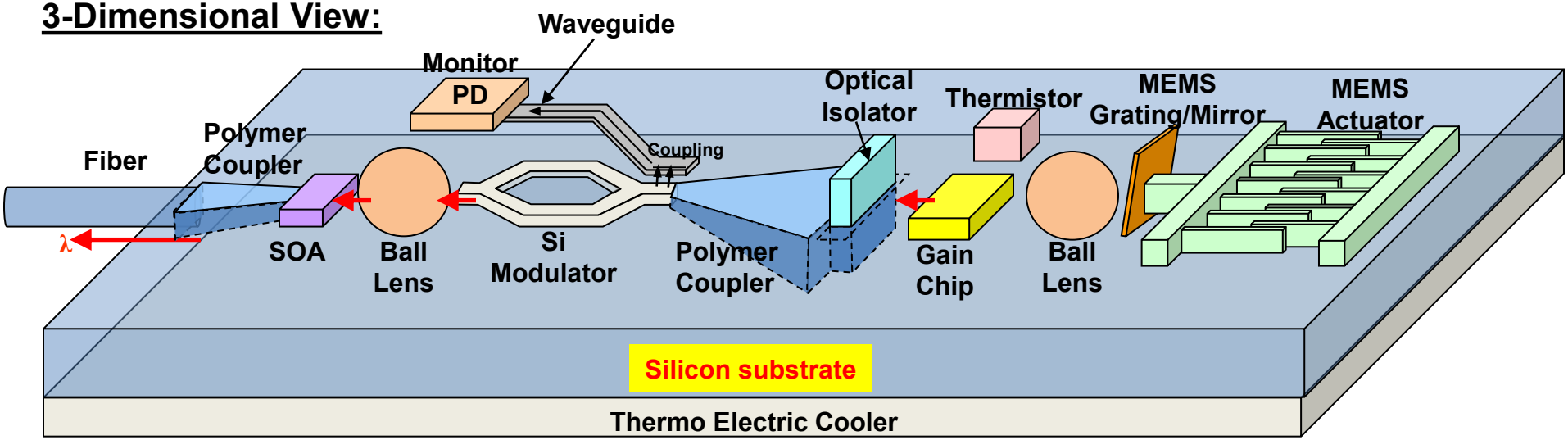


IME's MEMS Based Tunable Laser Source, Gain Chip, and Si-Modulator on Si-Substrate

Cross-Sectional View:



3-Dimensional View:

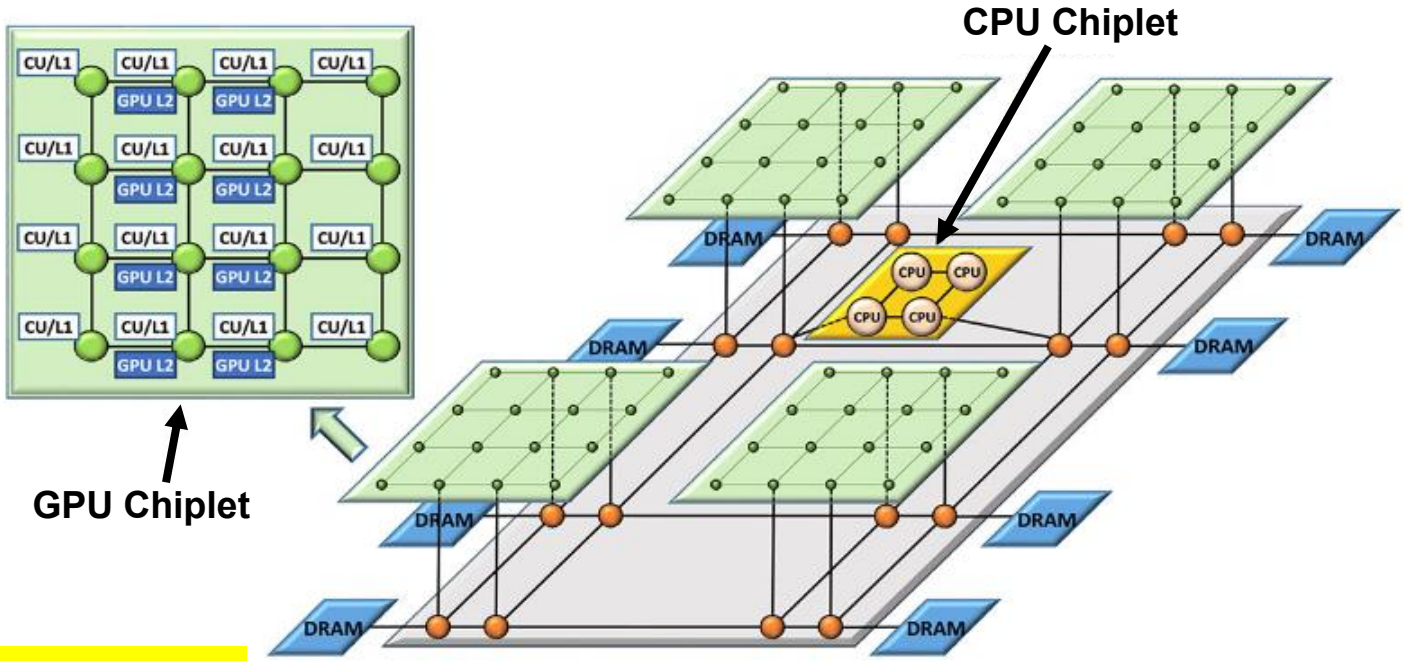


Heterogeneous Integration on Silicon Optical Bench

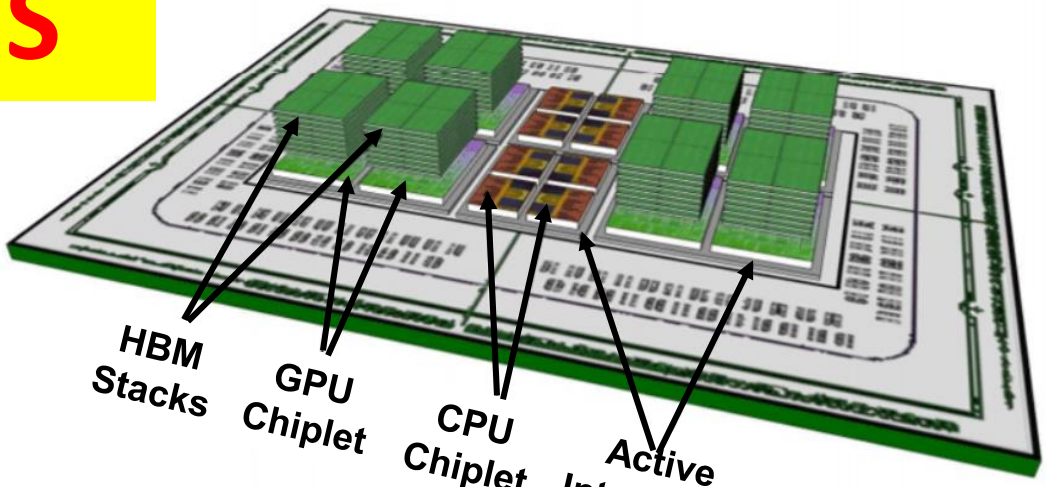
IME, 2007

Lau, PDC, ECTC2016

AMD: A Future System might Contain a CPU Chiplet and Several GPU Chiplets all Attached to the same Piece of Network-Enabled Silicon – Heterogeneous Integration



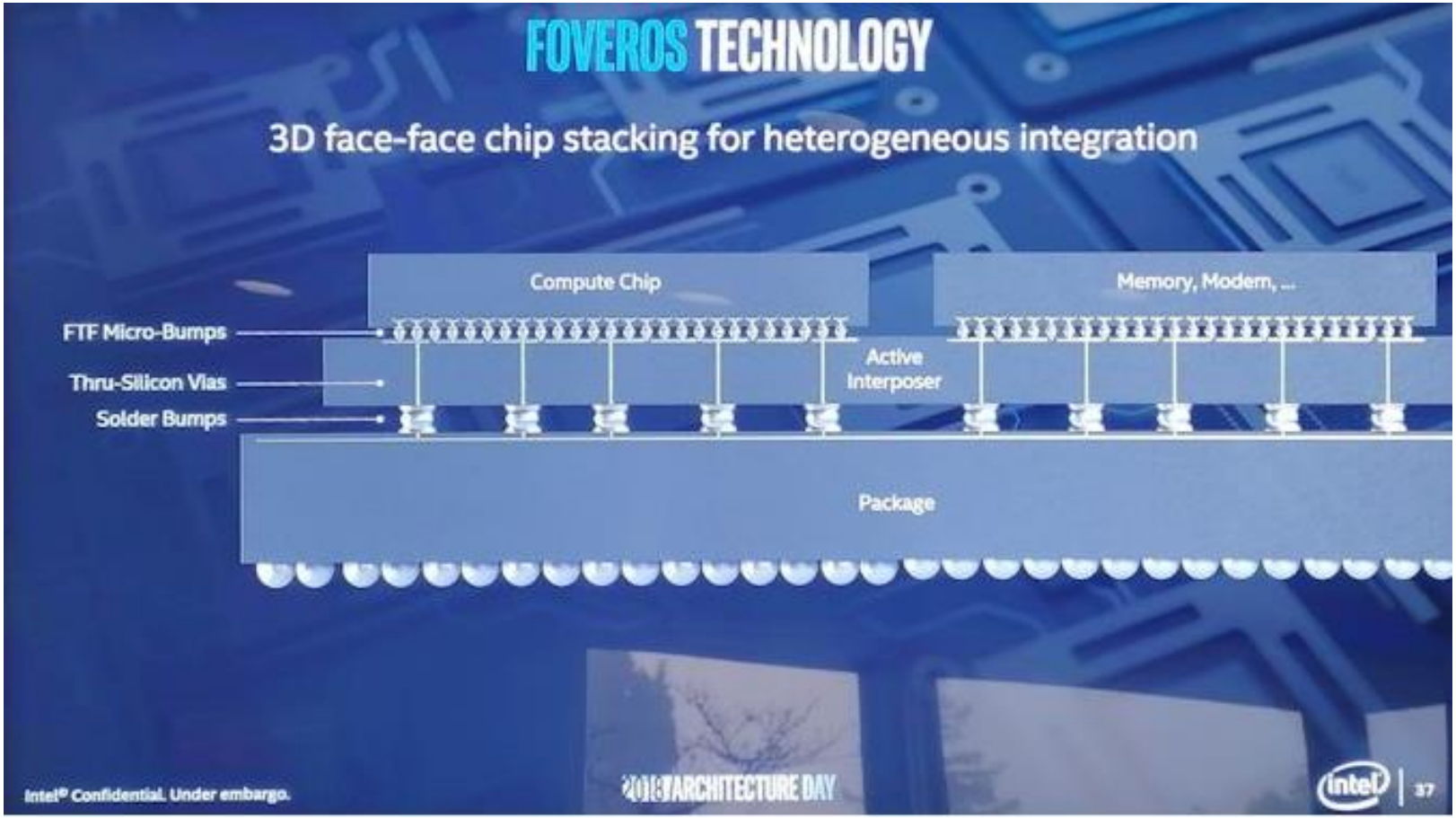
CHIPLETS



Intel's FOVEROS Technology

The key difference between the 2.5D IC Integration (CoWoS) and the FOVEROS is:

- **The TSV-interposer for 2.5D IC integration (CoWoS) is a passive interposer (a dummy piece of silicon)**
- **The TSV-interposer for FOVEROS is an active interposer (with devices), just like a chip**

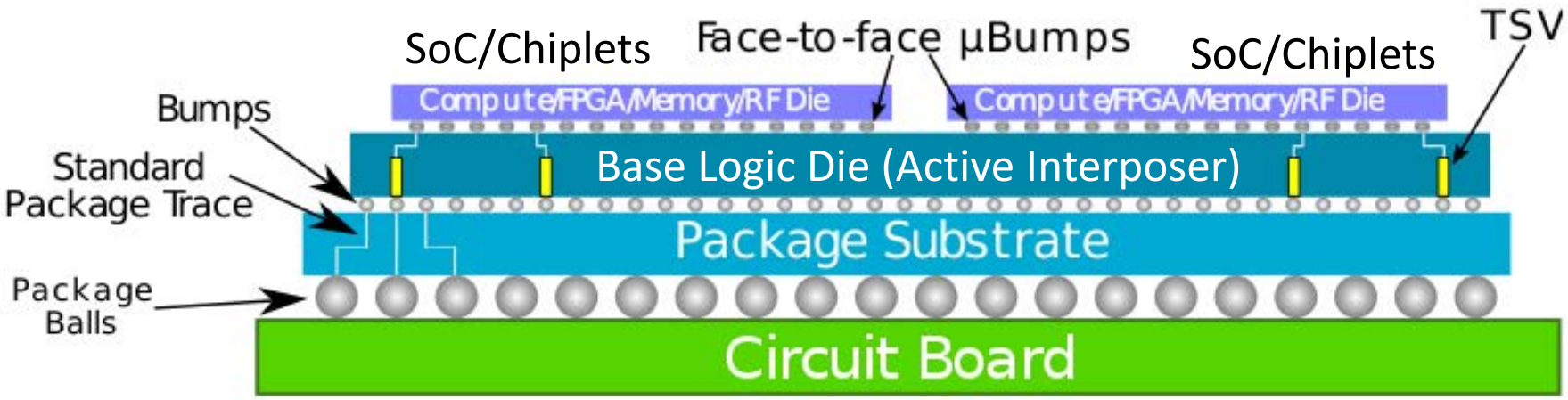


FOVEROS (it is Greek for awesome)

December 2018

Intel's FOVEROS Technology

The SoC/chiplets and the base logic die can be face-to-face by thermal compression bonding with non-conductive film or paste

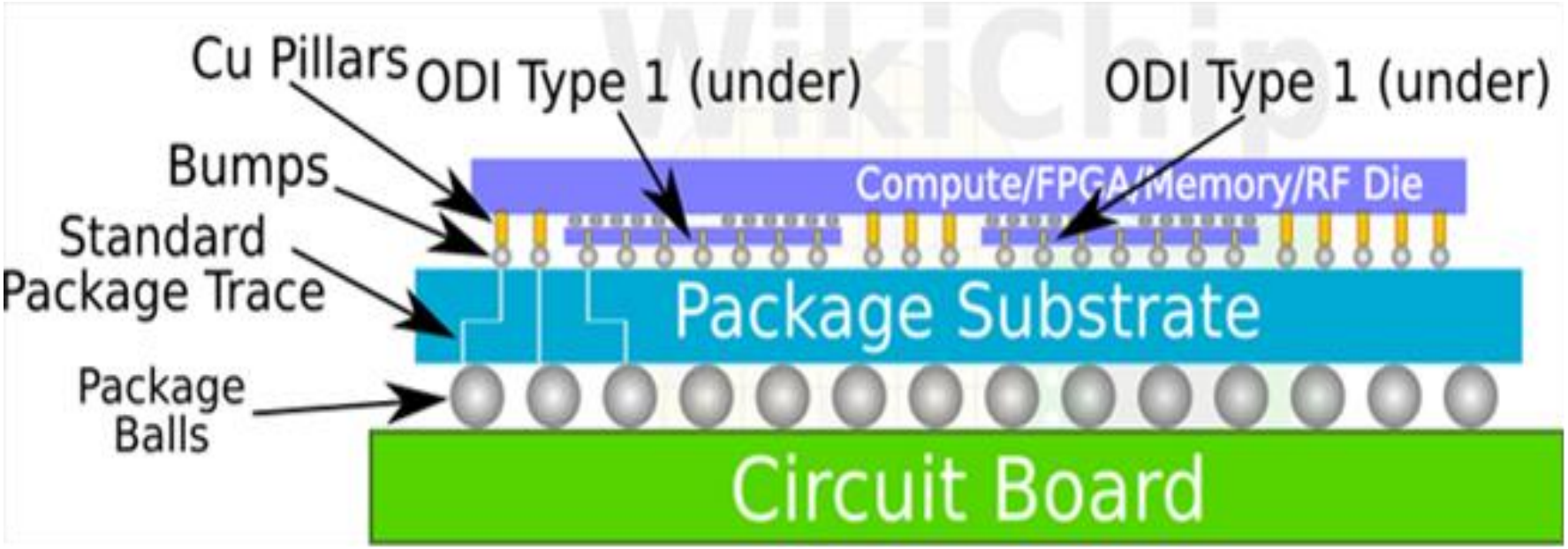


ODI (Omni-Directional Interconnect) TYPE-1

- First of all, it should be emphasized that the "bridge" is not buried in the organic substrate.
- Also, the bridge is not a piece of dummy silicon (like EMIB) but with devices, just like a semiconductor chip with TSVs.

TYPE-1

The bridges (chips) with TSVs are underneath the big chip (e.g., CPU, GPU, FPGA,..). The bridges are not buried in the organic package substrate.

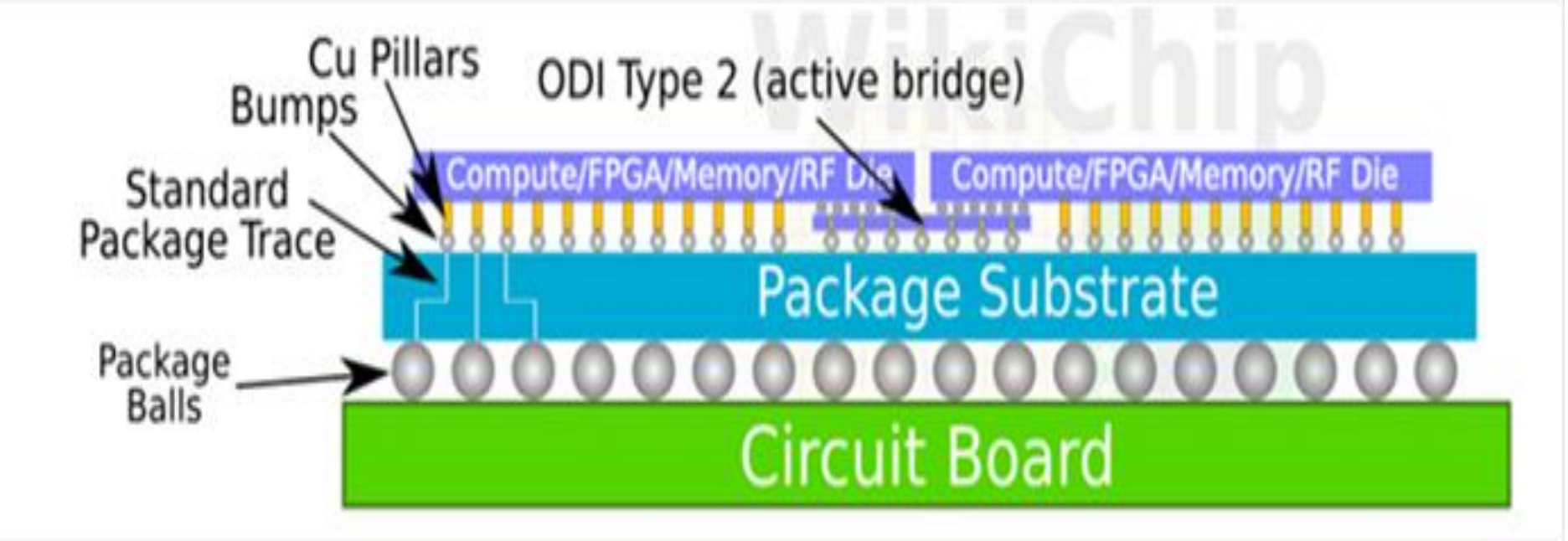


ODI (Omni-Directional Interconnect) TYPE-2

- First of all, it should be emphasized that the "bridge" is not buried in the organic substrate.
- Also, the bridge is not a piece of dummy silicon (like EMIB) but with devices, just like a semiconductor chip with TSVs.

TYPE-2

The bridge (chip) with TSVs is underneath and connecting the two big chips (e.g., CPU, GPU, FPGA, …). The bridge is not buried in the organic package substrate. They called it Type 2.

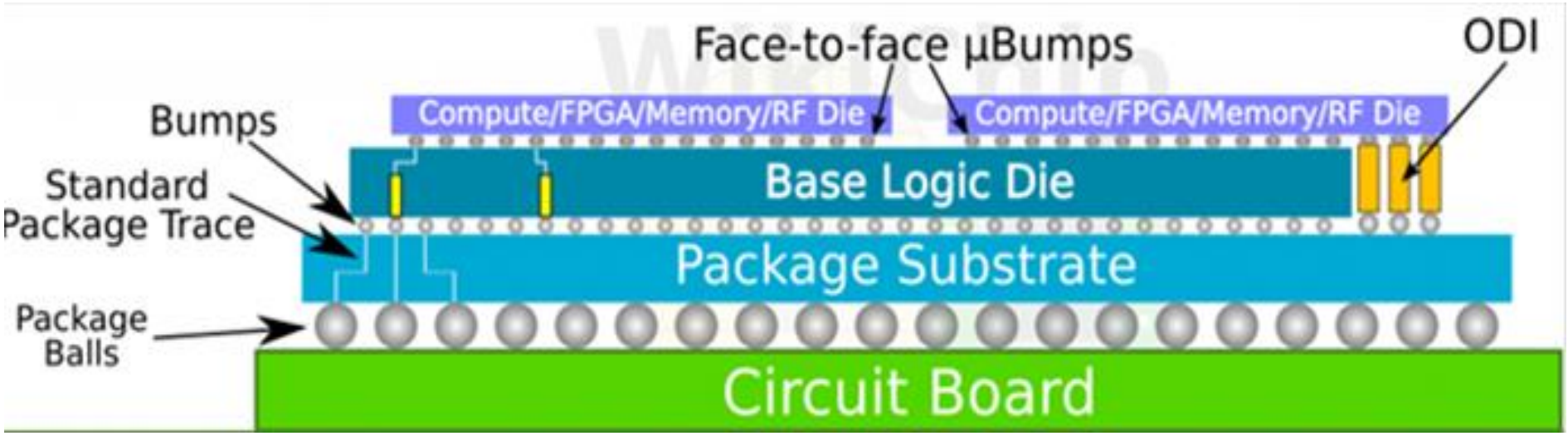


ODI (Omni-Directional Interconnect) TYPE-3

- First of all, it should be emphasized that the "bridge" is not buried in the organic substrate.
- Also, the bridge is not a piece of dummy silicon (like EMIB) but with devices, just like a semiconductor chip with TSVs.

TYPE3

The base logic chip with TSVs is considered as the active bridge and connecting the two big chips (e.g., CPU, GPU, and FPGA…). This is a special case of Type 2.



Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on Silicon Substrate (TSV-less Interposers)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

US 20140070380A1

(19) **United States**

(12) **Patent Application Publication**

Chiu et al.

(10) **Pub. No.: US 2014/0070380 A1**

(43) **Pub. Date: Mar. 13, 2014**

(54) **BRIDGE INTERCONNECT WITH AIR GAP IN PACKAGE ASSEMBLY**

(76) Inventors: **Chia-Pin Chiu**, Tempe, AZ (US); **Zhiguo Qian**, Chandler, AZ (US); **Mathew J. Manusharow**, Phoenix, AZ (US)

(21) Appl. No.: **13/610,780**

(22) Filed: **Sep. 11, 2012**

Publication Classification

(51) **Int. Cl.**

H01L 23/495 (2006.01)

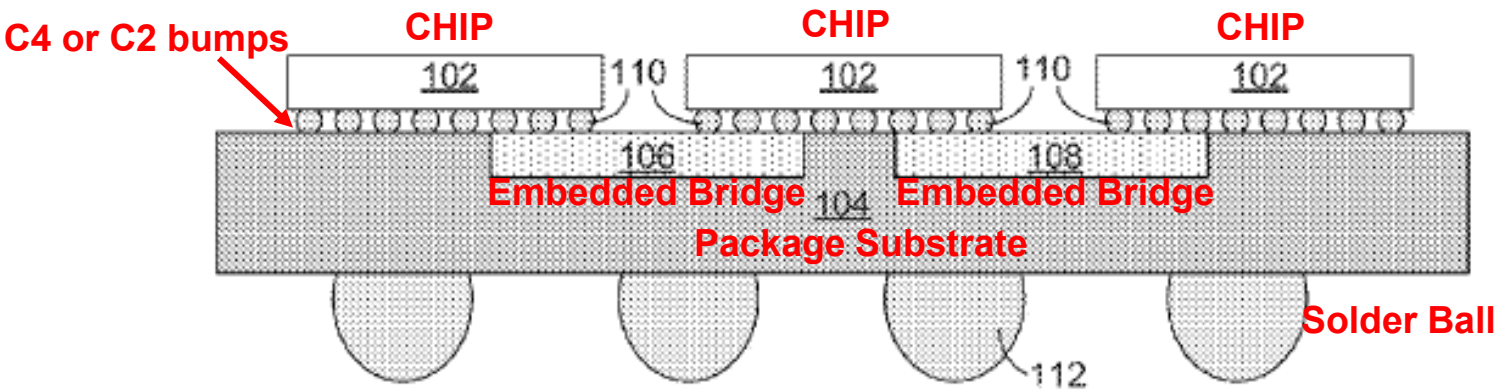
H01L 21/60 (2006.01)

(52) **U.S. Cl.**

USPC **257/666**; 438/107; 257/E21.506; 257/E23.052

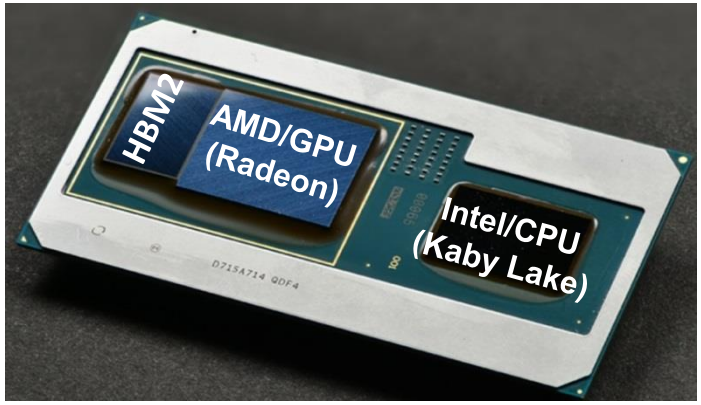
(57) **ABSTRACT**

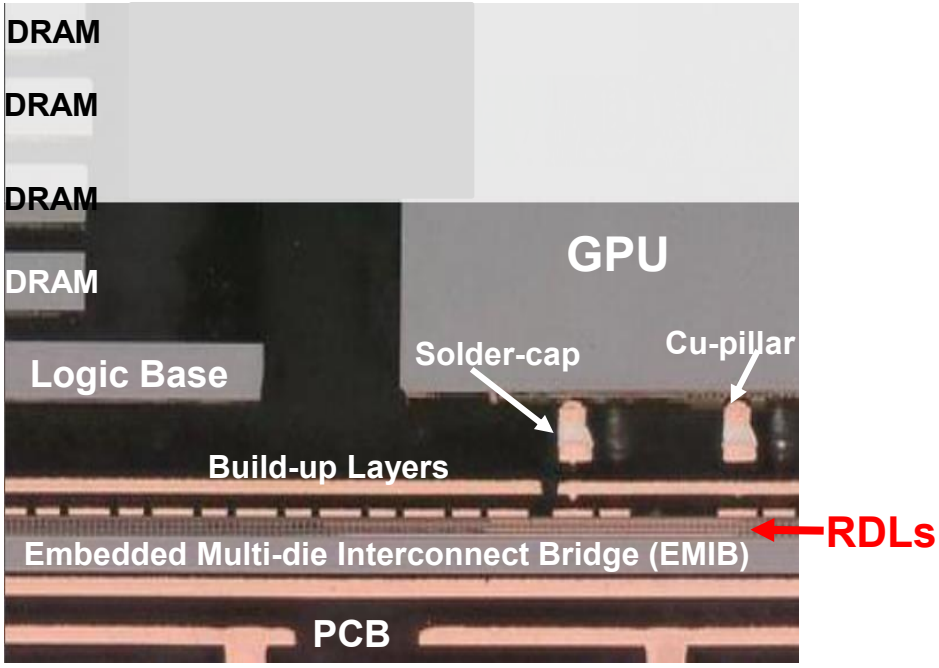
Embodiments of the present disclosure are directed towards techniques and configurations for a bridge interconnect assembly that can be embedded in a package assembly. In one embodiment, a package assembly includes a package substrate configured to route electrical signals between a first die and a second die and a bridge embedded in the package substrate and configured to route the electrical signals between the first die and the second die, the bridge including a bridge substrate, one or more through-hole vias (THVs) formed through the bridge substrate, and one or more traces disposed on a surface of the bridge substrate to route the electrical signals between the first die and the second die. Routing features including traces and a ground plane of the bridge interconnect assembly may be separated by an air gap. Other embodiments may be described and/or claimed.

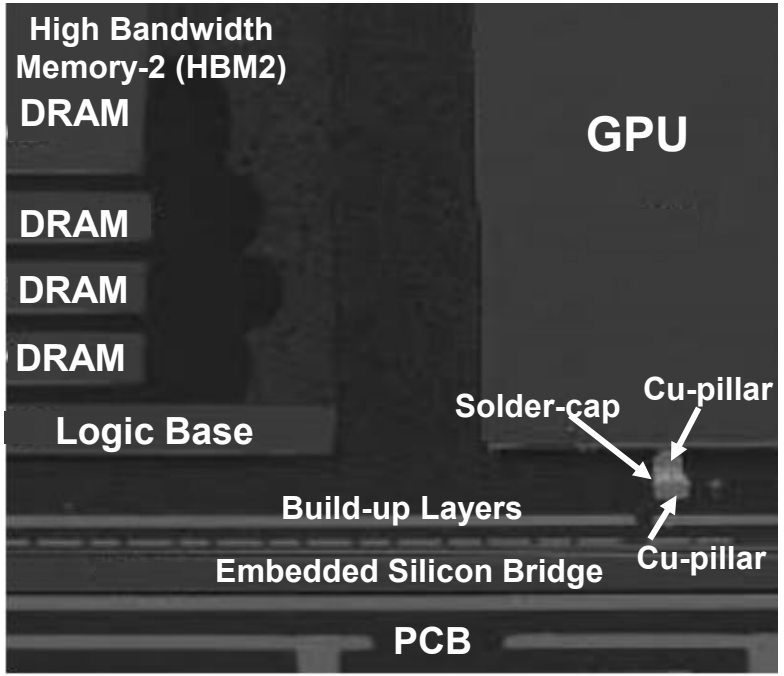


Embedded Multi-die Interconnect Bridge (EMIB)

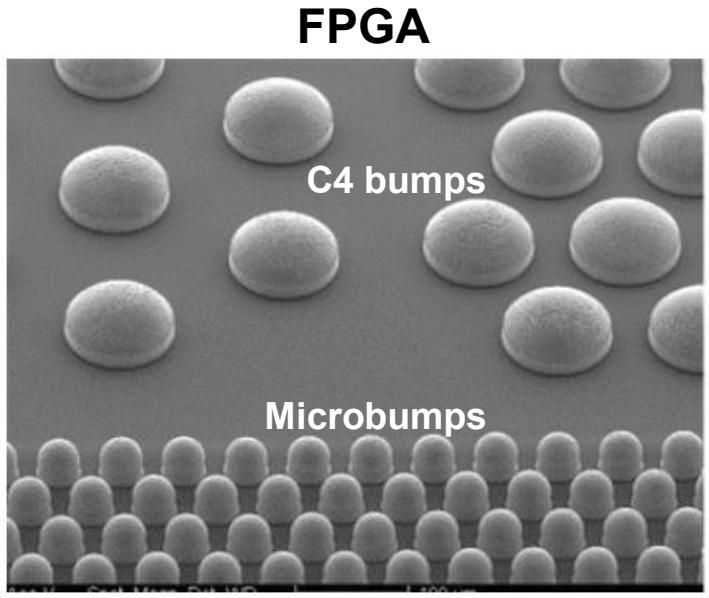
Heterogeneous Integration: Intel's CPU (Kaby Lake) and AMD's GPU (Radeon)

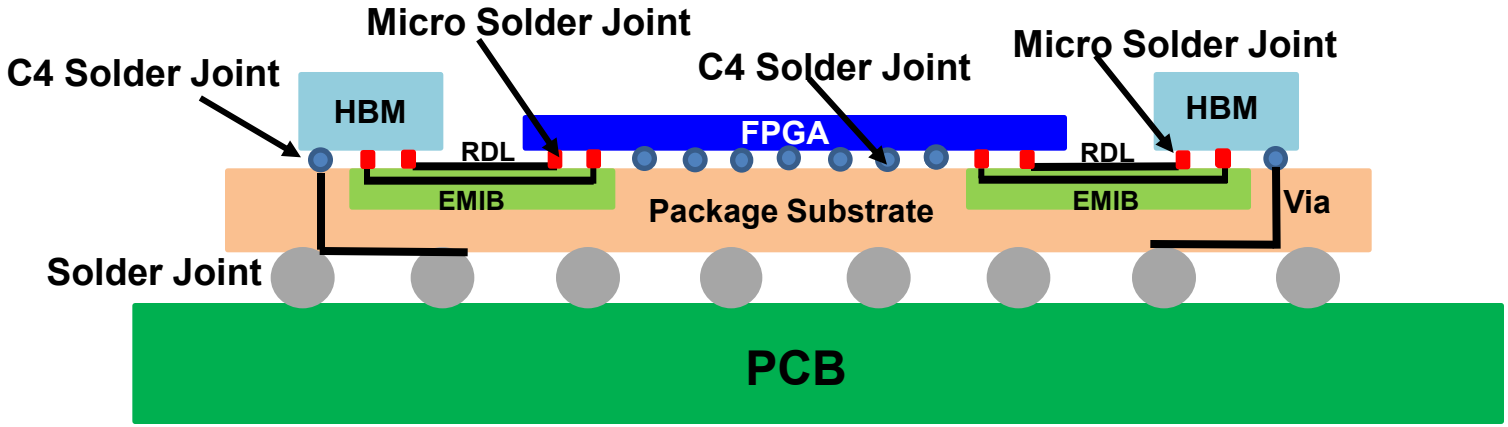






Intel's FPGA (Agilex) with EMIB





Advances in Temporary Carrier Technology for High-Density Fan-Out Device Build-up

Arnita Podpod, Alain Phommahaxay, Pieter Bex, John Slabbekoorn, Julien Bertheau, Abdellah Salahouelhadj, Erik Sleeckx, Andy Miller, Gerald Beyer and Eric Beyne1
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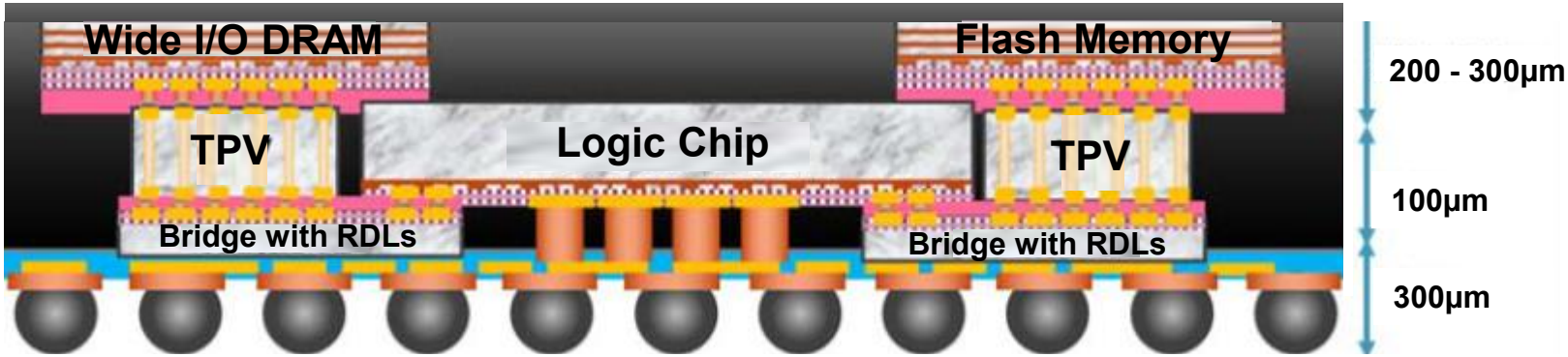
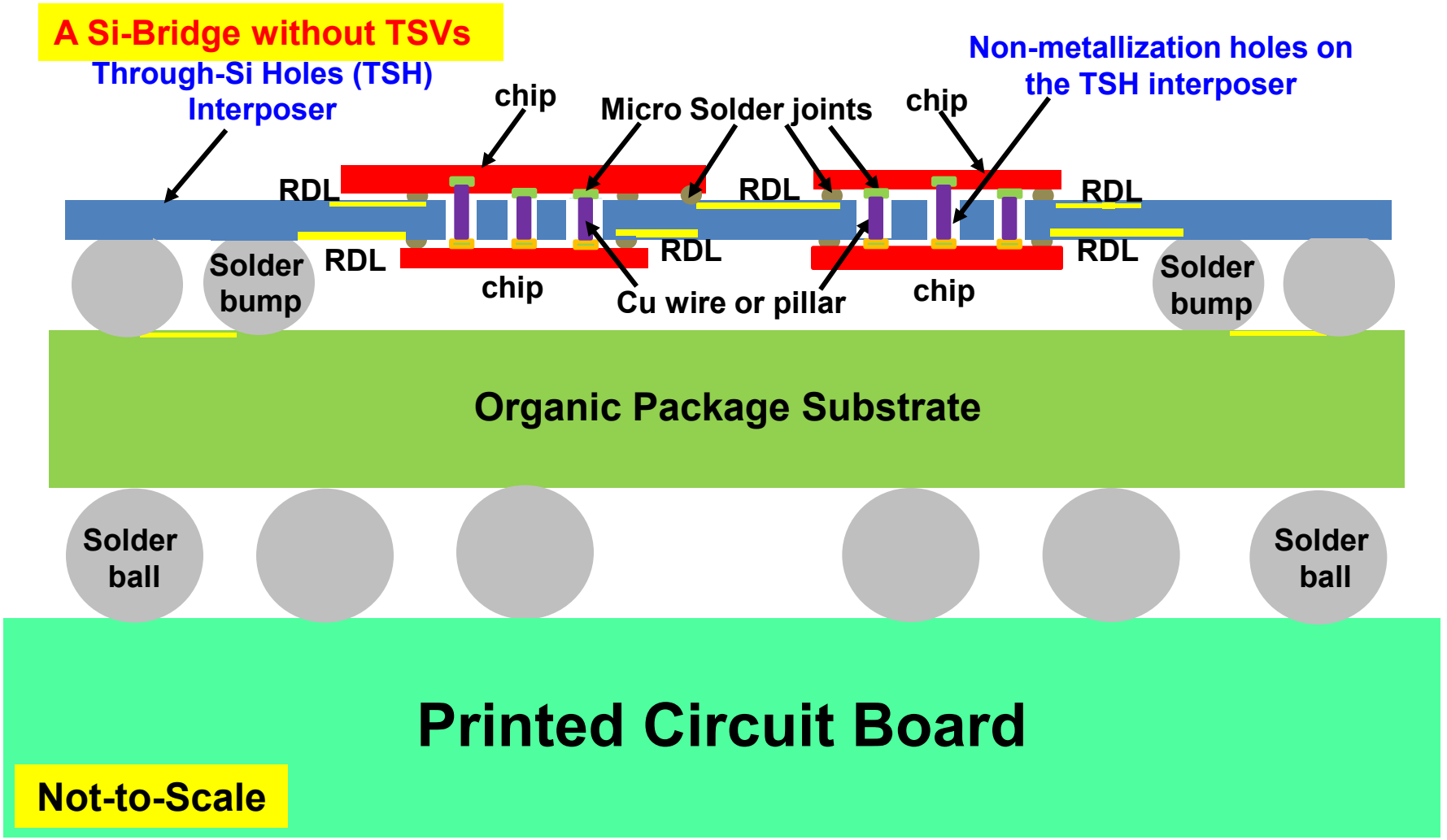
BRIDGE + Fan-Out (RDLs)



- No TSVs on Devices Chips
- TPV is a piece of Si with TSVs

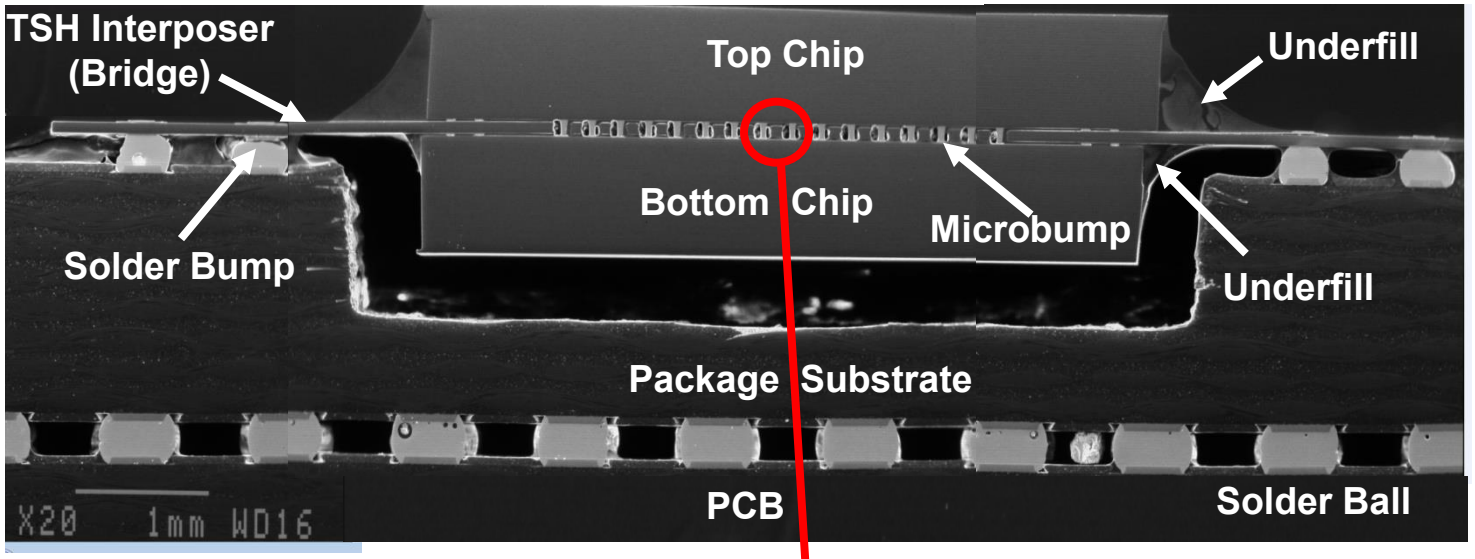
IRTI's Heterogeneous Integration which Consists of a TSH Interposer (Bridge) Supporting Chips with Cu pillars on its Top Side and Chips with Solder Bumps on its Bottom Side

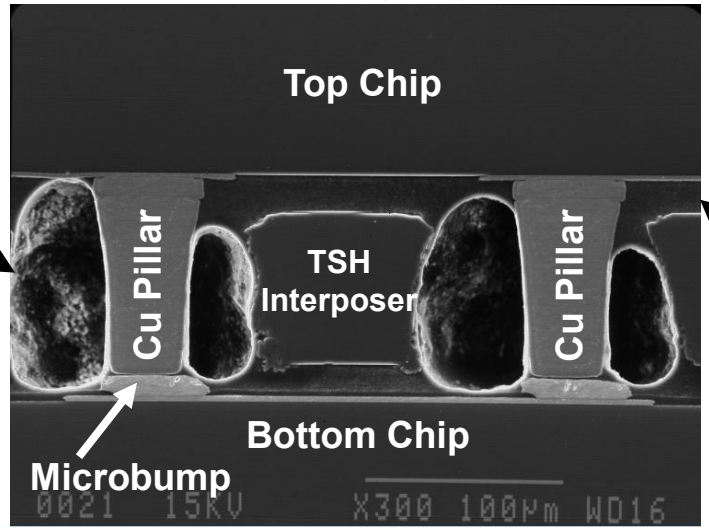


Underfill is needed between the TSH interposer and package substrate. Underfill may be needed between the TSH interposer and chips.

IEEE/ECTC 2013, also,
IEEE Trans. CPMT 2014

SEM image showing a cross-section of the heterogeneous integration which consists of the top chip, TSH interposer (bridge), bottom chip, package substrate, and PCB





IEEE/ECTC 2013, also,
IEEE Trans. CPMT 2014

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- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions

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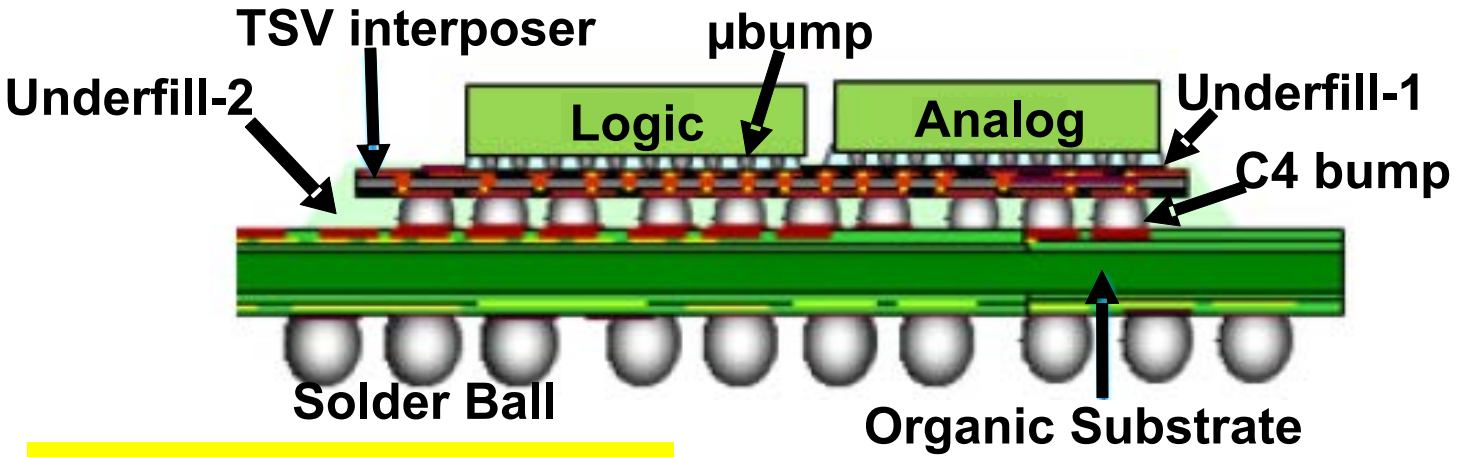
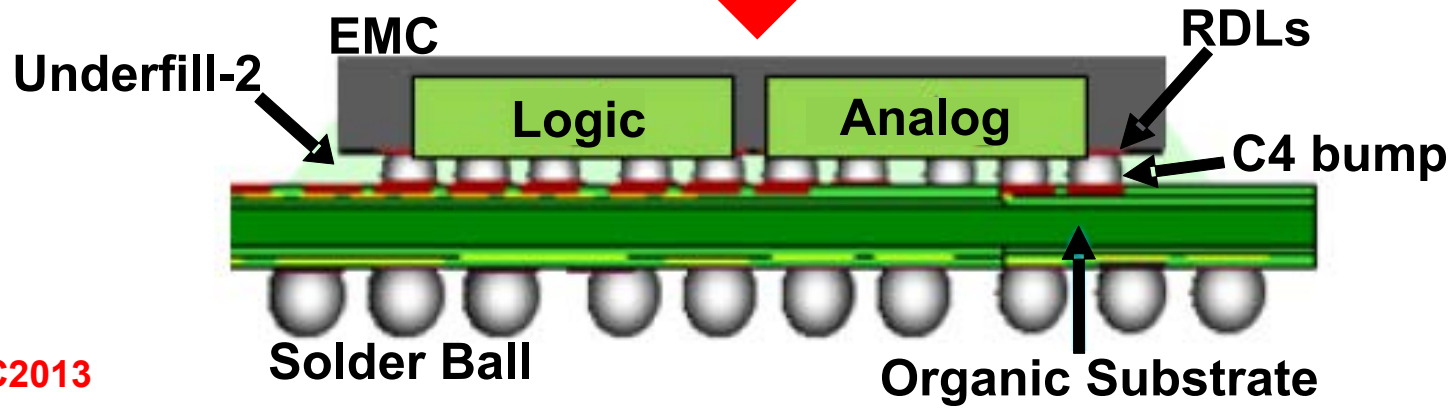


- The µbump, underfill-1, and TSV-interposer are eliminated.
- The RDLs are made by fan-out technology.



Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

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Advanced Semiconductor Engineering (ASE), Inc.
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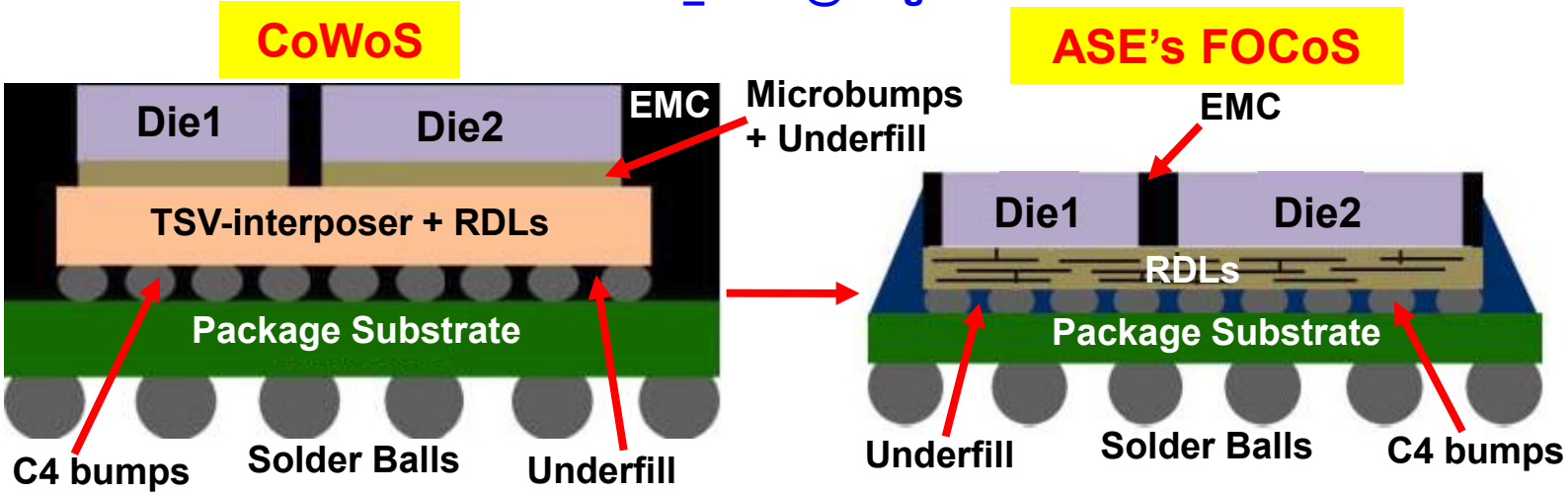
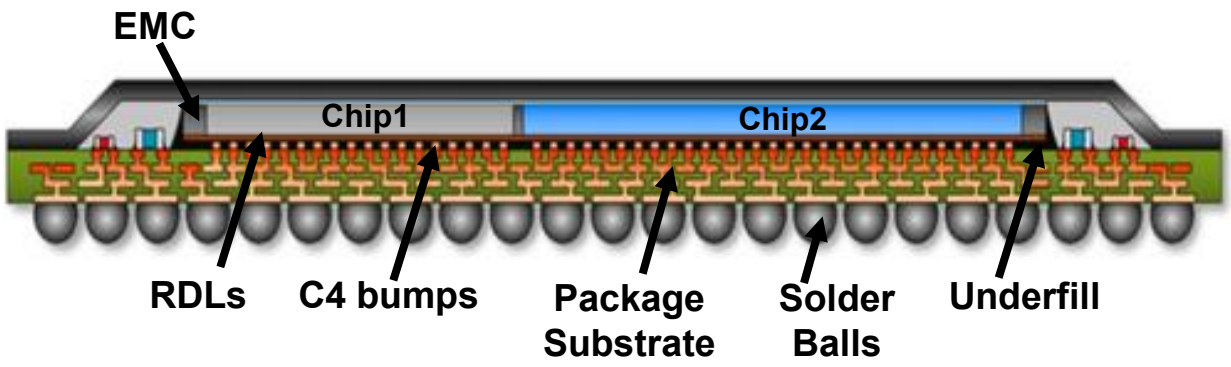
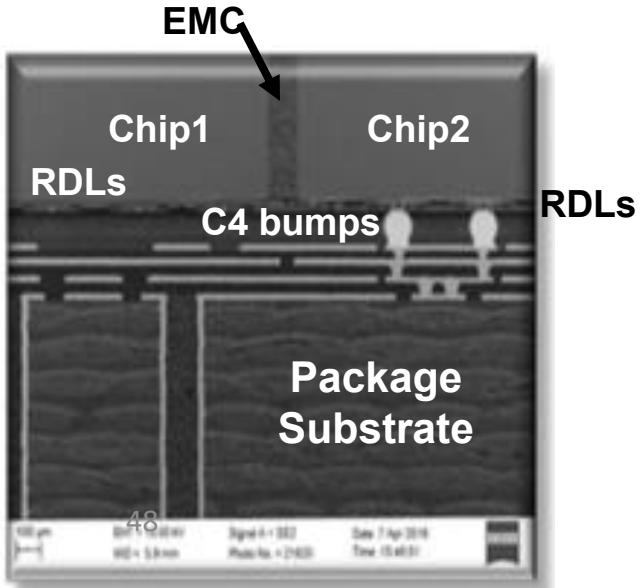
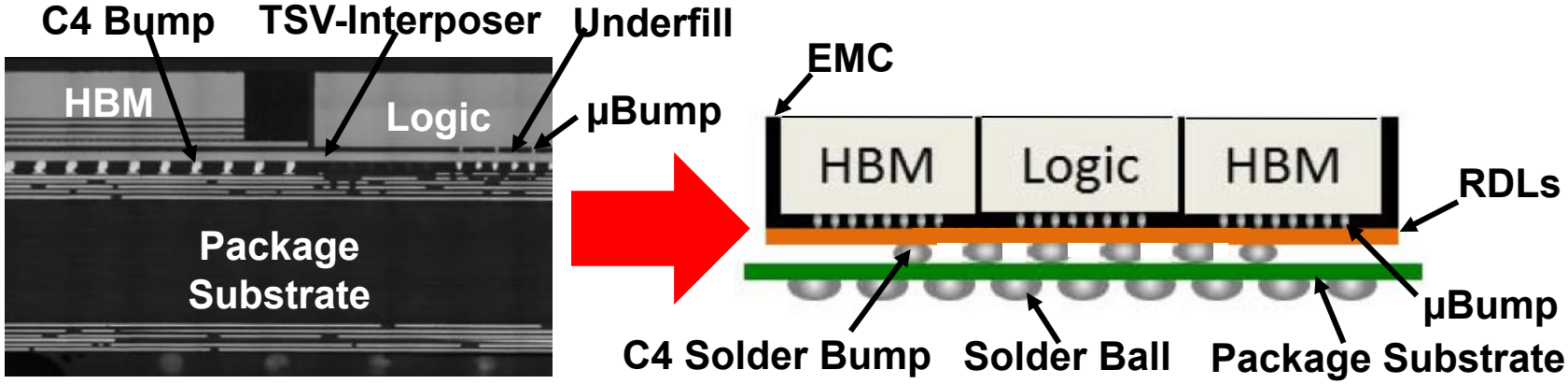




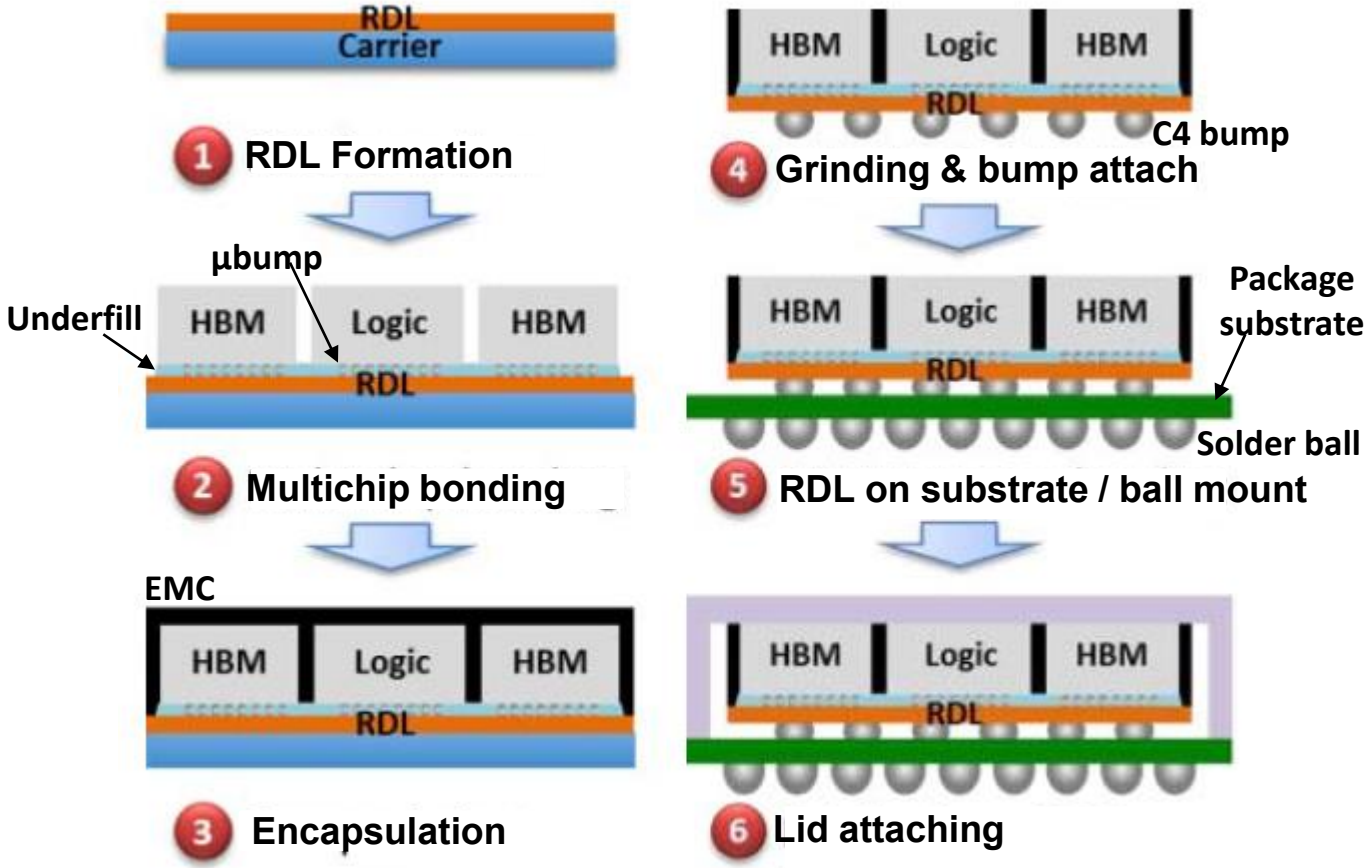


Samsung's Si-less RDL Interposer for Heterogeneous Integrations

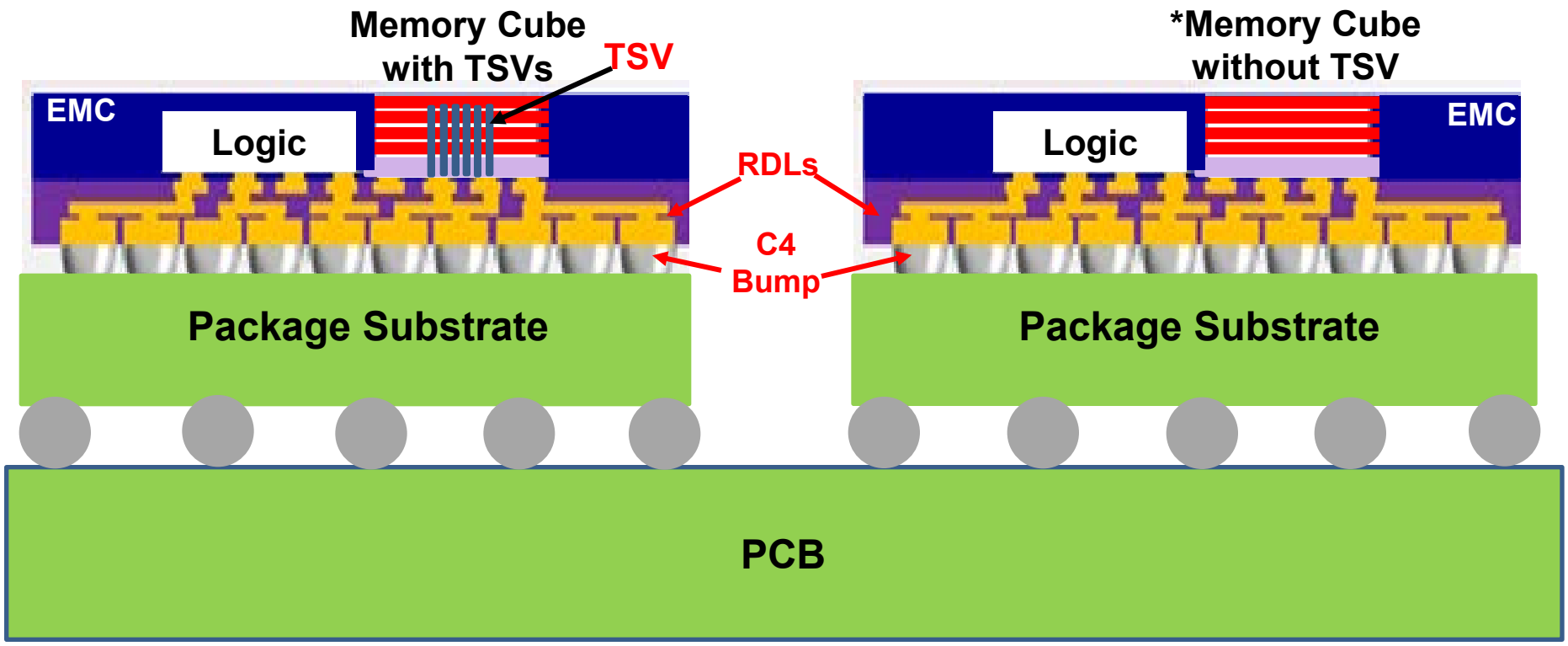
(a)



(b)



TSMC's TSV-less Interposer (InFO_MS) for Heterogeneous Integrations



InFO_MS (Integrated Fan-Out with Memory on Substrate)

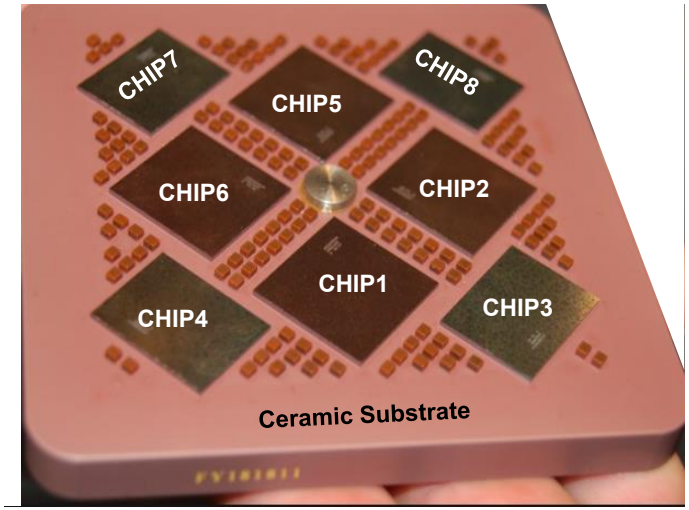
InFO_oS (Integrated Fan-Out on Substrate)

March 2019

Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on Silicon Substrate (TSV-less Interposers)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

MCM (Multichip Module) on Ceramic Substrate



MCM on Ceramic Substrate

IBM 9121 TCM
(Thermal Conduction Module)

- TCM weighs 2.2Kg
- Contains up to 121 chips about 8-10mm square
- Each chip has a spring-loaded Cu piston to remove heat
- Up to 10W dissipation per chip
- Up to 600W dissipation per TCM

  Ceramic substrate has:
  - 63 layers
  - Up to 400m of wirings
  - Up to 2 million vias
- 5Kg air-cooled heatsink to remove heat from TCM

SUMMARY and RECOMMENDATIONS

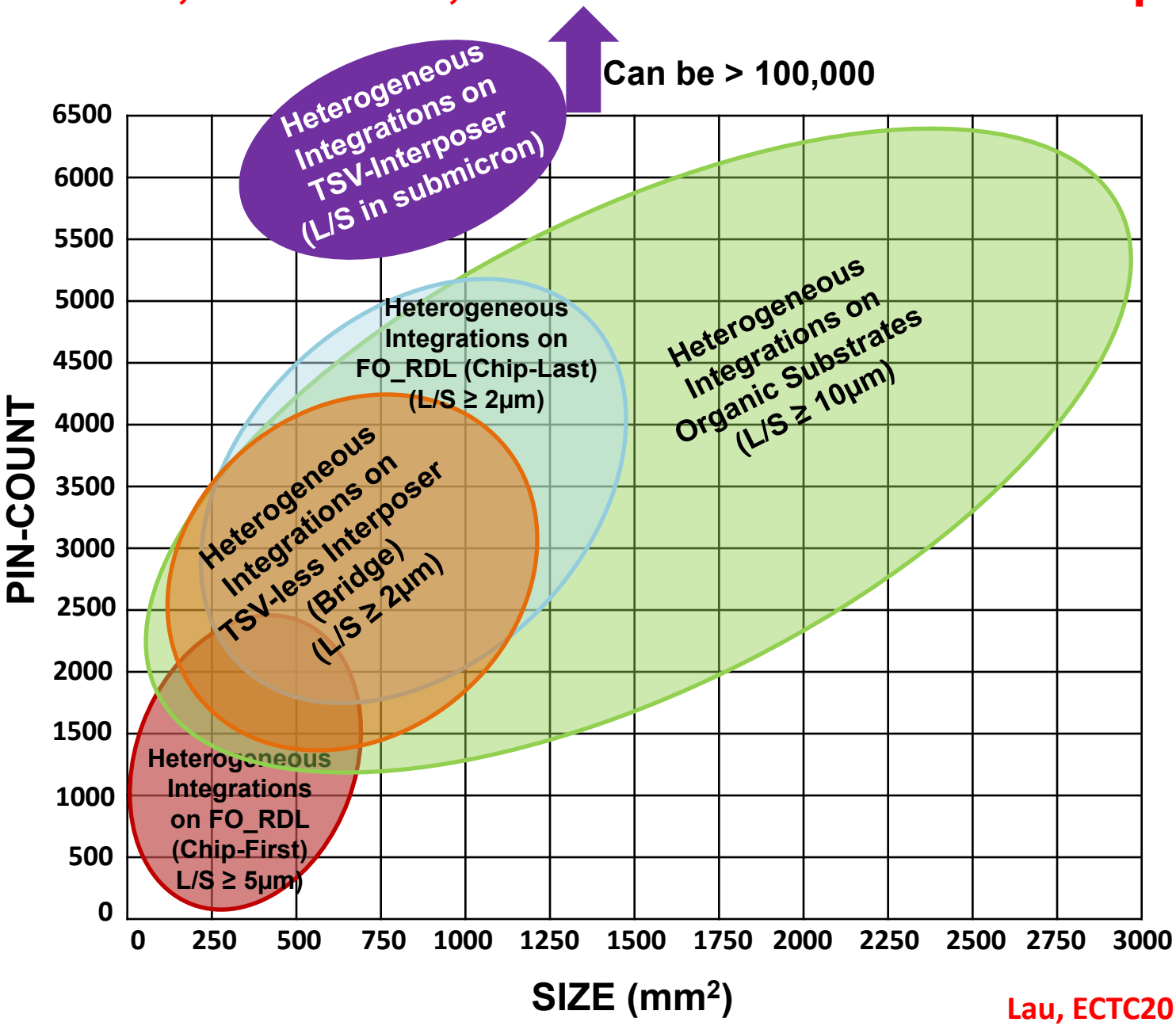
In the next few years, we'll see more of a higher-level of heterogeneous integrations, whether it is for:

- **time-to-market**
- **performance**
- **form factor**
- **power consumption**
- **signal integrity**
- **cost**
- **etc.**

SUMMARY and RECOMMENDATIONS

- In order to promote the heterogeneous integrations, standards are necessary! The Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS) is heading into the right direction.
- EDA (electronic design automation) tools for automating system partitioning and design are desperately needed for complex heterogeneous integration systems.
- Heterogeneous integrations is classified as:
  (1) heterogeneous integrations on organic substrates
  (2) heterogeneous integrations on silicon substrates (TSV-interposers)
  (3) heterogeneous integrations on silicon substrates (TSV-less interposers)
  (4) heterogeneous integrations on fan-out RDL substrates
  (5) heterogeneous integrations on ceramic substrates
- 75% of the heterogeneous integrations will be on organic substrates. (Actually most are SiPs).
- 25% of the heterogeneous integrations will be on other substrates such as silicon (TSV-interposers), silicon (TSV-less interposers), fan-out RDLs, and ceramic.
- How to select different types of heterogeneous integrations? It depends on the applications. The most important indicator (selection criterion) is the metal line width and spacing of the RDLs for the substrates being used for the heterogeneous integrations.

Heterogeneous Integration on Various Substrates with Different Sizes, Pin-Count, and Metal Line Width and Spacing



Lau, ECTC2017 , PDC

Thank You Very Much for Your Attention!