Open Domain Specific Architecture

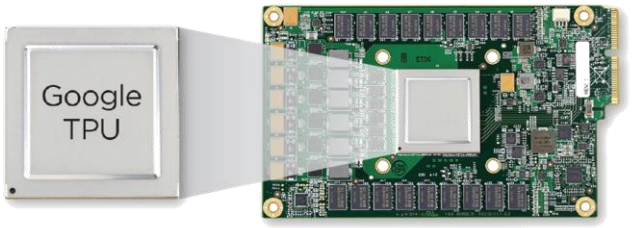
Bapi Vinnakota
Sub-project lead representing an active community of contributors from over 25 companies

Broadcom

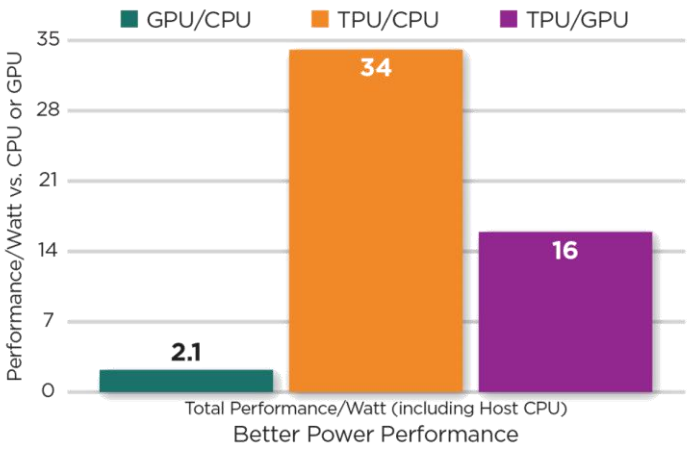
Outline

- Introduction to the ODSA
- Activities, results and roadmap
- **We need your help!**

End of Moore's Law => Accelerators



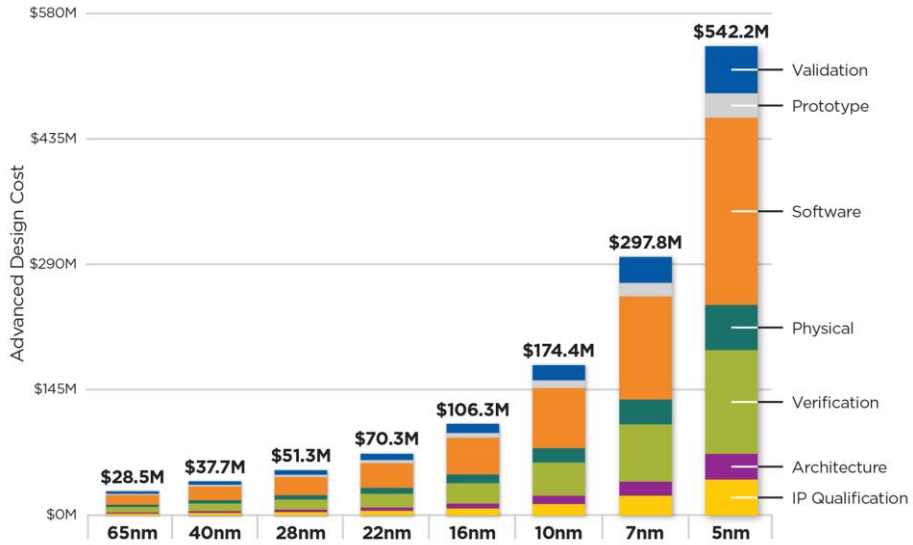
Domain-Specific for Machine Learning and AI



Google TPU vs. CPU and GPU

Source: "An in-depth look at Google's first Tensor Processing Unit (TPU)," Google Cloud, May 2017

- Server-attached devices for compute-intensive workloads
  - Programmable, not hardwired, tailored to a domain
  - 5-10X power performance improvement
  - Challenge: ASIC development costs for a targeted market



ASIC development costs

Consume. Collaborate. Contribute.

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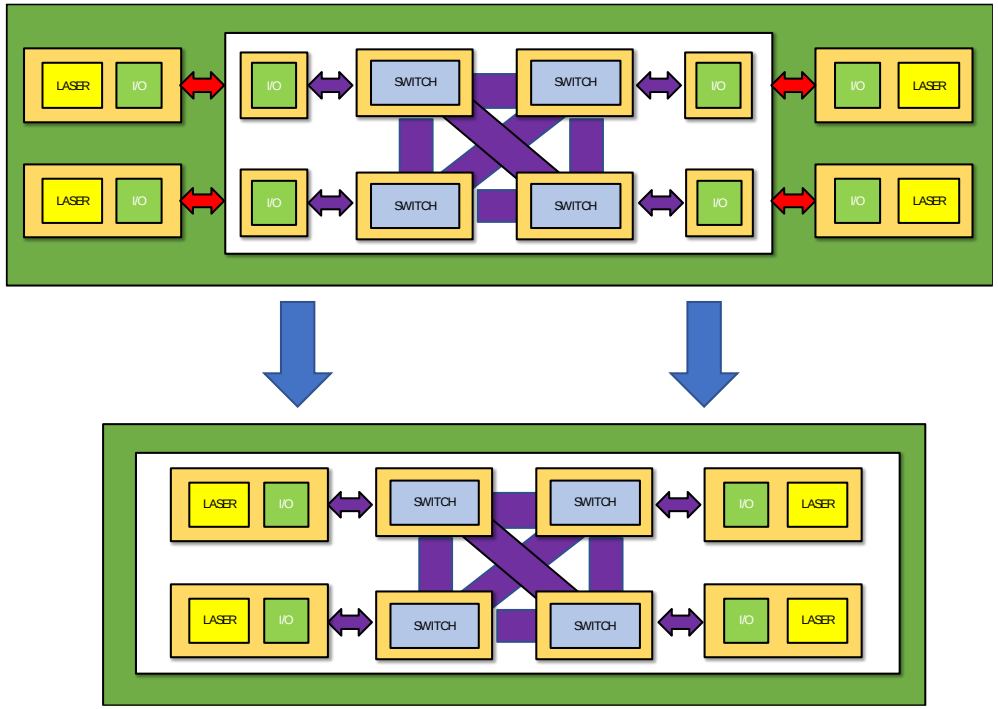
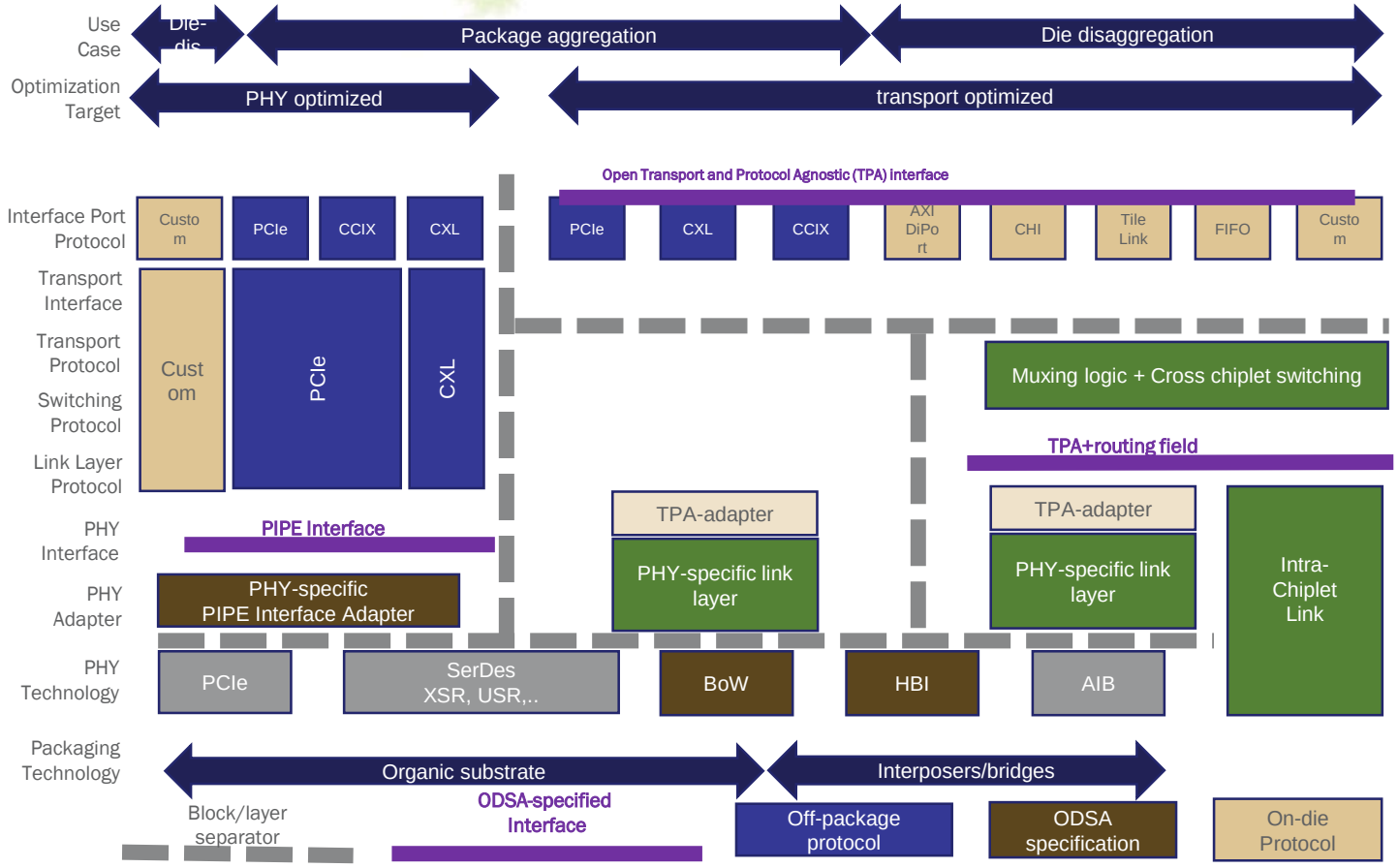
Chiplets

- Create an integrated product across multiple die
  - Optimize a function for a process node
  - Economical approach to large die
  - Reuse IP as hard IP
- Need a die-to-die interface, physical and logical
  - Physical – optimized for on-package
  - Logical – need a protocol
- Today: proprietary vertically integrated D2D interfaces



ODSA D2D Interface

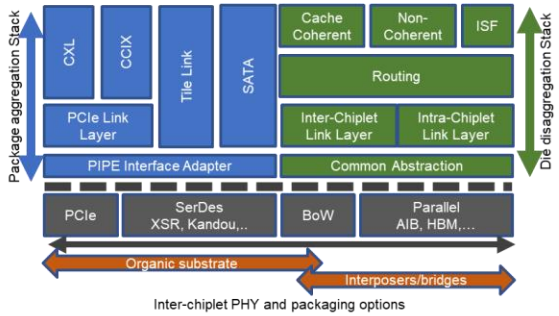


Open with abstraction layers

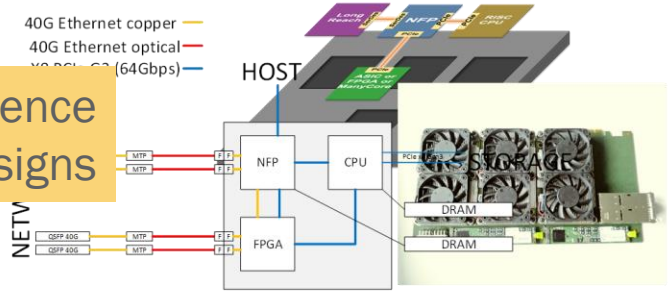
- Open logic, Open PHY evolve separately
- Reuse protocols, minimize “new”
- Multiple options to make chiplets, market will choose

ODSA Charter

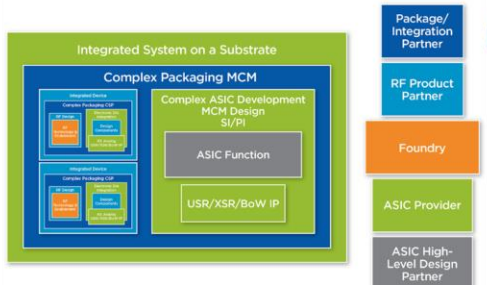
Open D2D Interface



Reference Designs

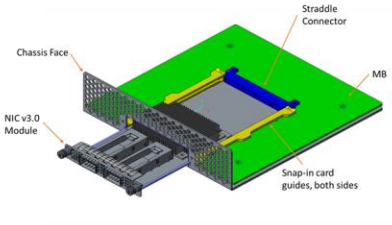


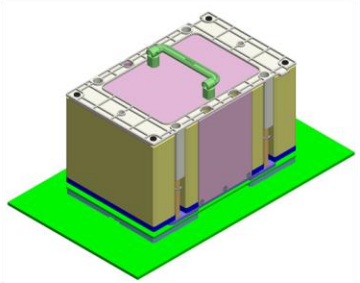
Reference Workflows

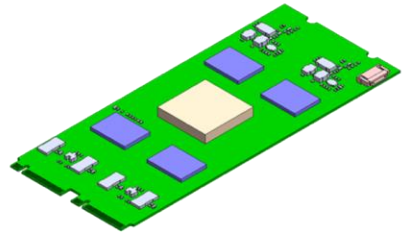


Integrate best in class chiplets from multiple vendors

Chiplet Marketplace







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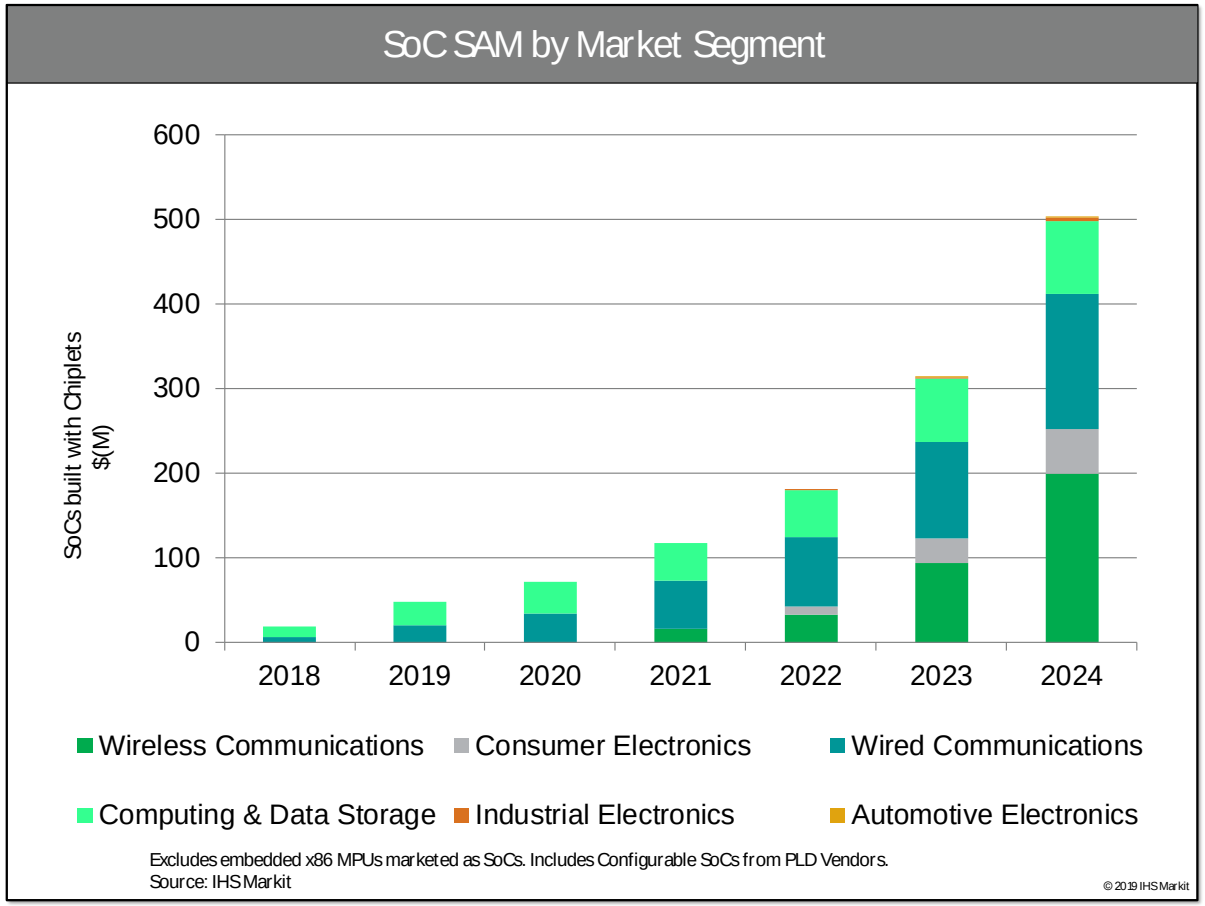
Transformative Market Opportunity: The Tip of the Spear

- Independent research from IHS Markit
- Four (4) segments for chiplets analyzed (SoCs, MPU, GPU, PLD (FPGA/CPLDs)
- Six Verticals (wireless, wireline, consumer, computing, industrial, automotive)

Subset of IHS Markit Data:
- System on a Chip (SoC) segment
- **Conclusion**: Immediate opportunity for chiplets and an open interface

Tip of the spear !!!



Attendees and Participants:

Attendance and/or participation do not imply corporate endorsement

Semi Vendors
IP providers, EDA
Service providers

Tools, Manufacture,
Design, Test,
Integration

Systems vendors,
End users, ISVs,
Service Providers

Started 11/2018 with 7 companies
Started as an Open Compute Project activity in 03/2018
Workshops at Global Foundries, Samsung, Intel, IBM, Facebook

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ODSA Workstreams

Workstream	Leader	Participants	Objective
PHY Layer	Robert Wang	IBM, XILINX, KANDOU BUS, SYNOPSYS, MARVELL	PCIe PIPE adapter
Bunch of Wires	Mark Kuemerle	MARVELL, XILINX, SYNOPSYS, KEYSIGHT TECHNOLOGIES, Google, IBM, SiFive	Low cost D2D PHY
CDX	Jawad Nasrullah	zGlue, ANSYS, Advanced Semiconductor Engineering, Inc., AyarLabs, cadence, SYNOPSYS	Chiplet design exchange
Business	Sam Fuller	NXP, facebook, Microsoft Azure, AyarLabs	Chiplet workflow
PoC hardware	JP Balachandran	CISCO, facebook, Achronix Data Acceleration, Lattice, NXP	PoC board design
PoC software	Kevin Drucker	facebook, samtec, MACOM, NETRONOME, zGlue	Application/Infra software
Link layer	Open	XILINX, NXP, intel	ODSA Stack
Open HBI	Kenneth Ma	XILINX	High perf D2D PHY

https://www.opencompute.org/wiki/Server/ODSA

Consume. Collaborate. Contribute.

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Significant Results

- First fully open physical and logical D2D interfaces, available in 2020
  - New open Bunch of Wires interface. Low development cost, very flexible
  - PIPE adapter to carry PCIe/CXL over BoW PHYs
  - NXP DiPort protocol to disaggregate
- Proof of concept flexible software development platform

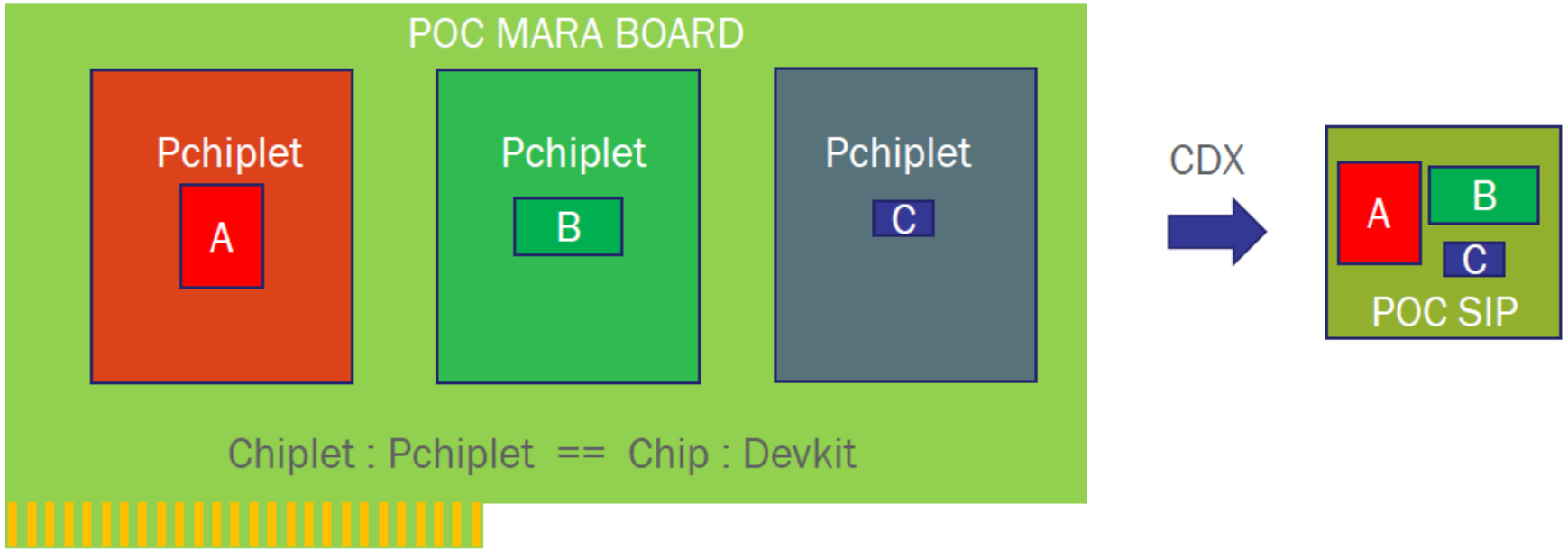
Where we need help

- Developing the protocol stack
- Packaging and physicals
- Test

CDX Subgroup Charter

Jawad Nasrullah, zGlue
Facebook workshop, Dec. 2019

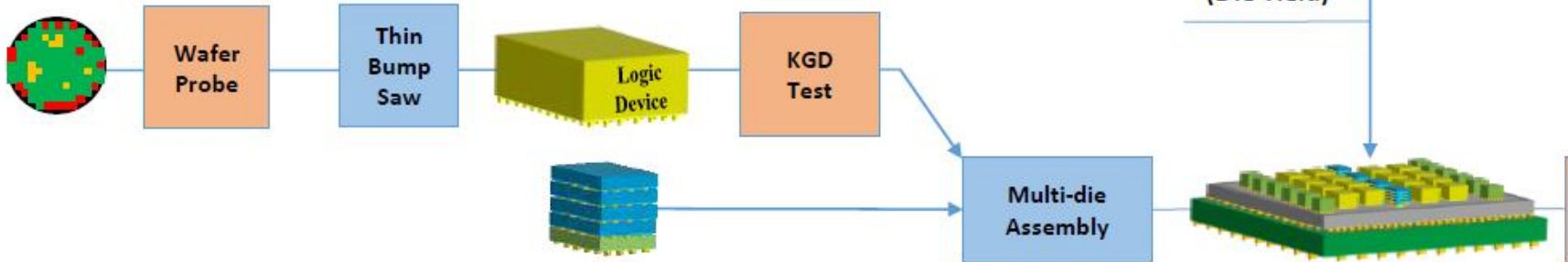
1- Chiplet Machine Readable Description Format Standardization
2- Chiplet Catalog
3- Pchiplet-to-SIP conversion flow



Tomorrow (circa 2020)

Dave Amstrong, HIR Facebook workshop, Dec. 2019

HETEROGENEOUS INTEGRATION ROADMAP



$(\text{Die Yield})^N$

- What is a "system"
- Key on/Key off test
- Software test

Final Test at Temp & Speed

System Level Test

Highest Quality devices with the Lowest Cost

- Fine pitch probing
- Thermal extremes
- Wide bandwidth contacting issues
- Photonic probe alignment challenges
- No end in site to # probes (probe force!)
- Low I/O drive strength

- Die level test becoming critical
- High power levels
- Automatic thermal control required
- Wide bandwidth contacting
- Thinned die handling
- TSV probing (?)
- Low I/O drive strength

- Partial assembly test providing value
- Large part thermal management
- Temporary thermal contact
- Crazy high power levels
- Temporary fiber align/attach

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

In brief…

- Open physical and logical D2D chiplet interface for best in class products
- Rapid growth, in interest, activities and results – we're just getting started
- We really could use your help in packaging and test
- Join the contributors from: Achronix, AnalogX, ANSYS, ASE, Avera Semi, Ayar Labs, Broadcom, Cadence, Cisco, Facebook, Ferric, IBM, IEEE HIR, Intel, Kandou, Keysight, Lattice, Macom, Marvell, Microsoft, Netronome, NXP, On Semi, Samtec, Sarcina, Synopsys, Tamind, Xilinx, zGlue