# Chiplets On the Rise

## *2020 Heterogeneous Integration Roadmap Symposium*

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# The Case for Chiplets



*"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."* [1]

Gordon E. Moore

[1]3rd Page of Moore's 1965 paper, "Cramming more components onto integrated circuits"

(intel)

# *Chiplets on the Rise:*
# Early Days and the Mother of Invention

# Chiplets on the Rise: Early Days

## Intel to make 14-nm FPGAs for Altera

By [Rick Merritt](#)  02.26.2013

SAN JOSE, Calif. – Intel Corp. will build FPGAs for Altera Corp. using its 14-nm FinFET process technology in a deal that turns up the heat on TSMC in foundry and Xilinx high-end FPGAs.

*Source: EE Times*

**Digital focused PDK & Intel EMIB**

## Altera and Intel Extend Manufacturing Partnership to Include Development of Multi-Die Devices
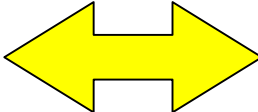
**Collaboration Will Optimize Integration of 14 nm Tri-Gate Stratix 10 FPGAs with Heterogeneous Technologies into a Single System-in-a-Package**

San Jose and Santa Clara, Calif., March 26, 2014 – Altera Corporation (Nasdaq: ALTR) and Intel Corporation today announced their collaboration on the development of multi-die devices that leverage Intel's world-class package and assembly capabilities and Altera's leading-edge programmable logic technology.

*Source: Intel*

# Arria 10 Legacy

Arria 10 on TSMC 20nm, the generation preceding Stratix 10 on Intel 14nm



= Thousands of wires between Core & Transceiver Columns:
  *Data Tx, Rx*
  *Clocks*
  *Configuration*
  *Control*

Arria 10 die image source: IEEE CICC, "Arria 10 Device Architecture," Tyhach et al

**Transceiver Column**

**Transceiver Column**

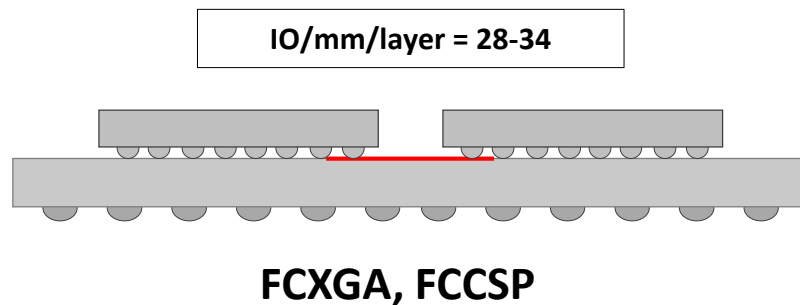**Programmable Logic Core (Advanced Logic Modules)**
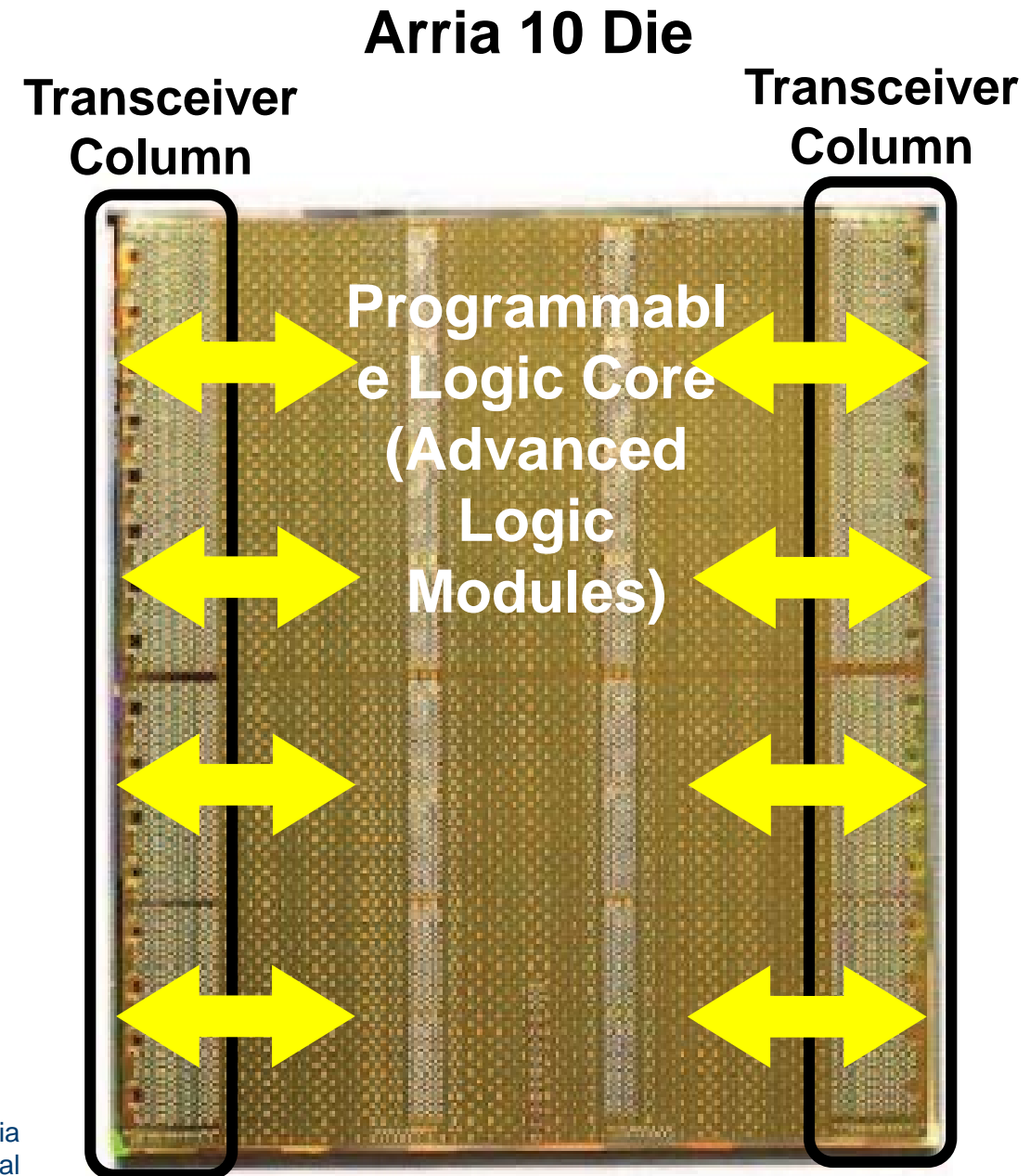
# The Necessities of Stratix 10

## Historical Challenges of 2013

- **Die Disaggregation**: How to separate a Monolithic FPGA into chiplets?

- **Heterogeneous Integration**: How to integrate Transceiver chiplets built on TSMC 20nm with the Intel 14nm main die?

# High-Density Packaging
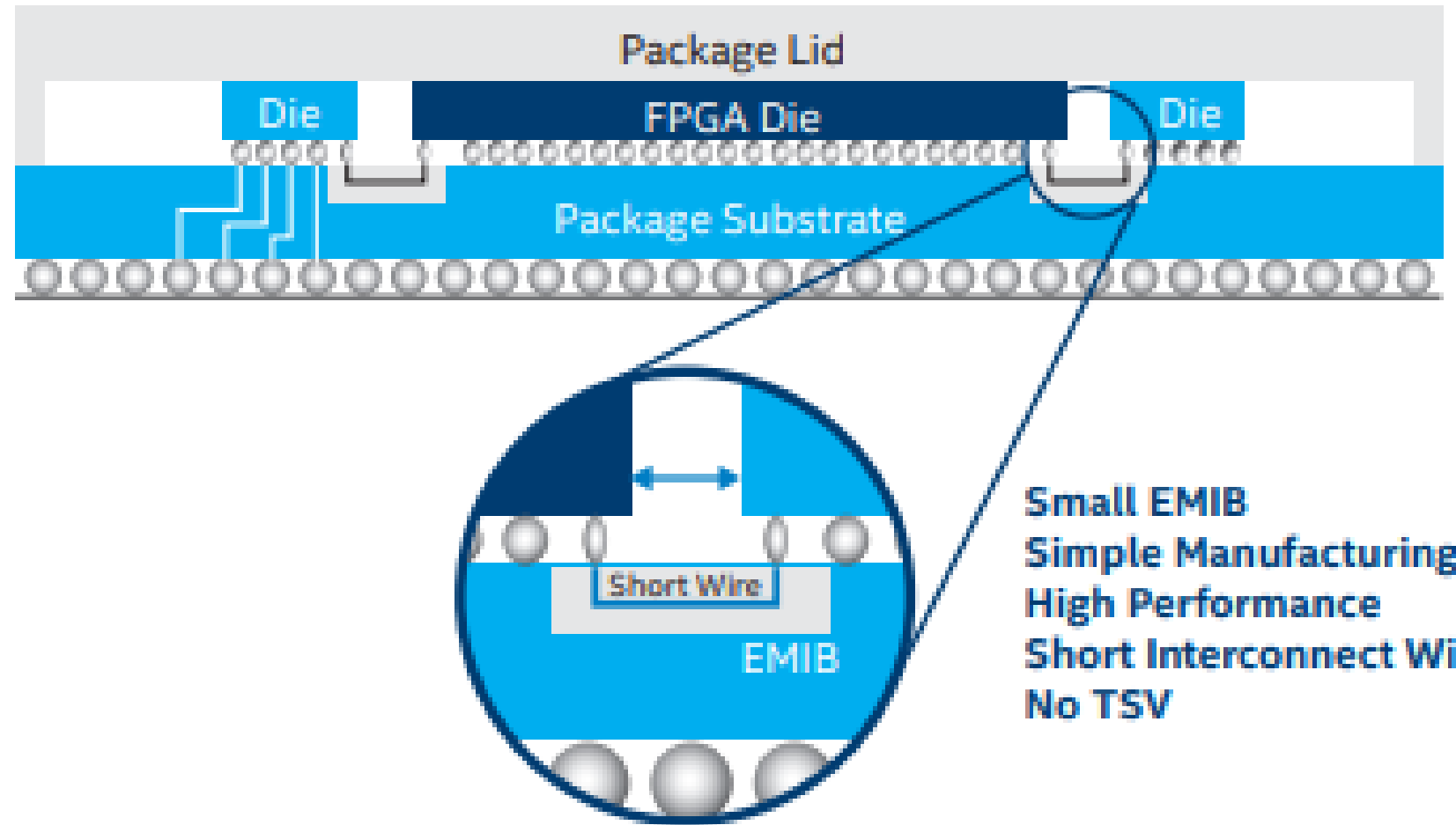
**Standard Flip-Chip Packaging Technology**

**High-Density Packaging Technology**

IO/mm/layer = 28-34

**FCXGA, FCCSP**

EMIB

IO/mm/layer = 250

Silicon Interposer
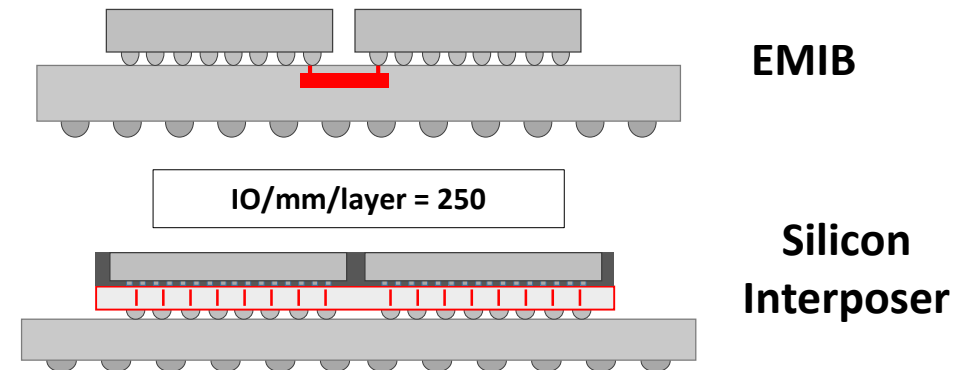
*High-density packaging technology provides 7-8x IO density increase*

# Intel Embedded Multi-die Interconnect Bridge (EMIB)

## Intel® Stratix® 10 FPGAs and SoCs with Intel EMIB

Package Lid

Die

FPGA Die

Die

Package Substrate

Short Wire

EMIB

- Small EMIB
- Simple Manufacturing
- High Performance
- Short Interconnect Wire
- No TSV

# AIB Die-to-Die Physical Interface

**AIB:** Common chiplet wide parallel physical interface

- **A**dvanced **I**nterface **B**us (AIB)
- AIB is a clock-forwarded parallel data transfer like DDR DRAM
- Advanced Packaging with a 2.5D interposer like CoWoS* or EMIB
- AIB is PHY level: OSI Layer 1
- Build protocols like AXI*-4 or PCI Express* on top of AIB
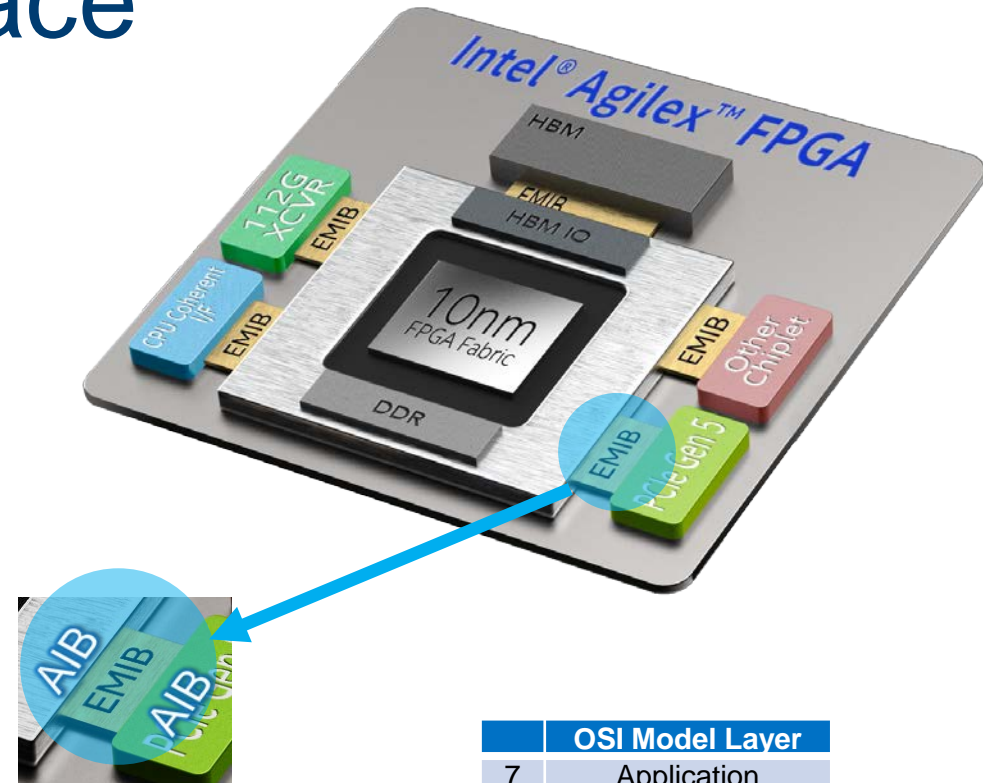


| | OSI Model Layer |
|---|---|
| 7 | Application |
| 6 | Presentation |
| 5 | Session |
| 4 | Transport |
| 3 | Network |
| 2 | Data Link |
| 1 | Physical |

AIB

# Early Days and the Mother of Invention Takeaways

**Advanced packaging technology enabled new thinking about SoC microarchitecture**

- Die disaggregation

- Heterogeneous integration

- Die-to-die interface with high bandwidth and low latency gives near-monolithic performance

# *Chiplets on the Rise:*
# Intel's FPGA Transceiver Leadership

News Byte

February 26, 2018

# INTEL SHIPS INDUSTRY'S FIRST 58G PAM4-CAPABLE FPGA BUILT FOR MULTI-TERABIT NETWORK INFRASTRUCTURE AND NFV
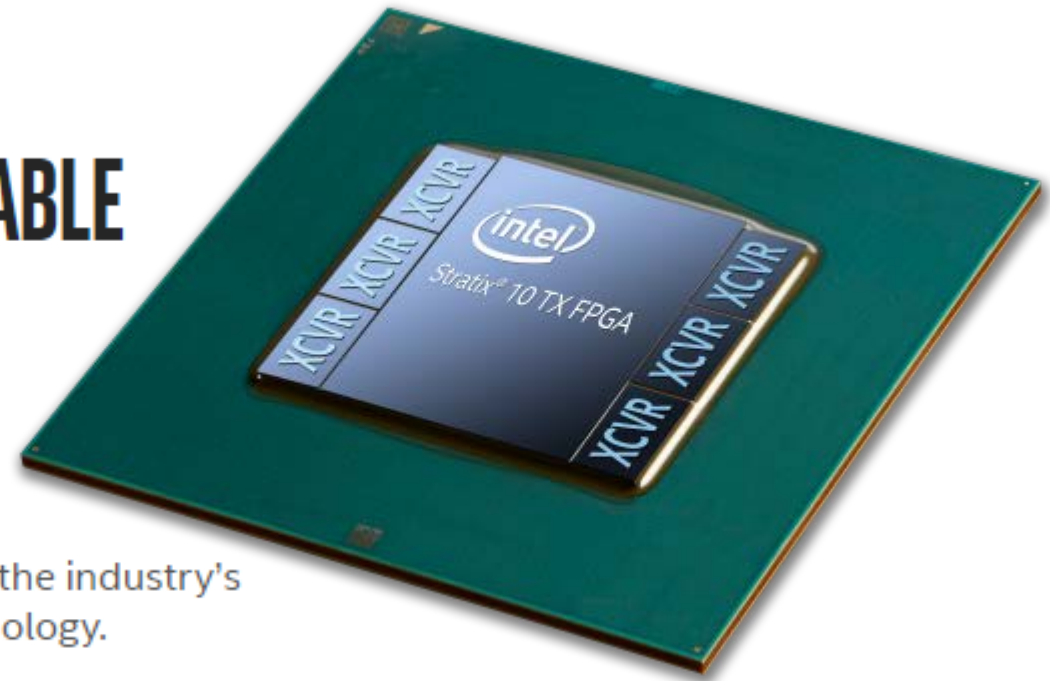
Intel today announced it has begun shipping its Intel® Stratix® 10 TX FPGAs, the industry's only field programmable gate array (FPGA) with 58G PAM4 transceiver technology.

**Mid 2015:** Altera started a parallel development for a new transceiver chiplet

Had to mechanically and electrically drop-in with the same Stratix 10 main die – *seeds of standardization*

First 56Gbps transceivers in the FPGA industry, first 56Gbps product at Intel

# Intel's FPGA Transceiver Leadership Takeaways

Able to add powerful new capability to an existing SoC

Chiplet approach allowed organizational flexibility in execution: parallel team did not defocus main die team

Released this mid-life kicker to Stratix 10, ahead of cycle with the next FPGA development

"In CHIPS, we're working with Intel on some of their integration strategies … so that you can do that composable design."

DARPA's ERI director Bill Chappell

**What is CHIPS?**

CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic

Tomorrow – Modular

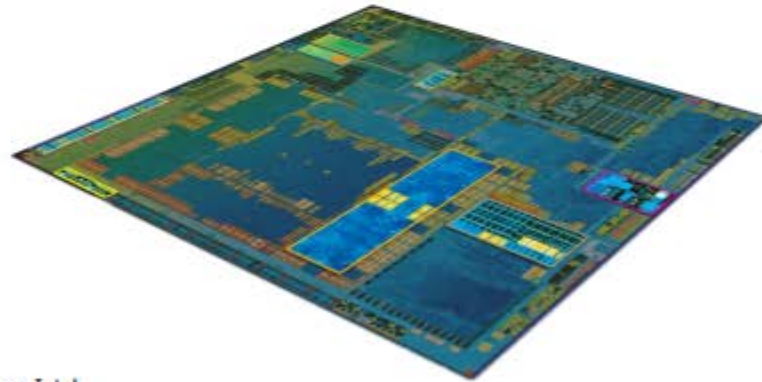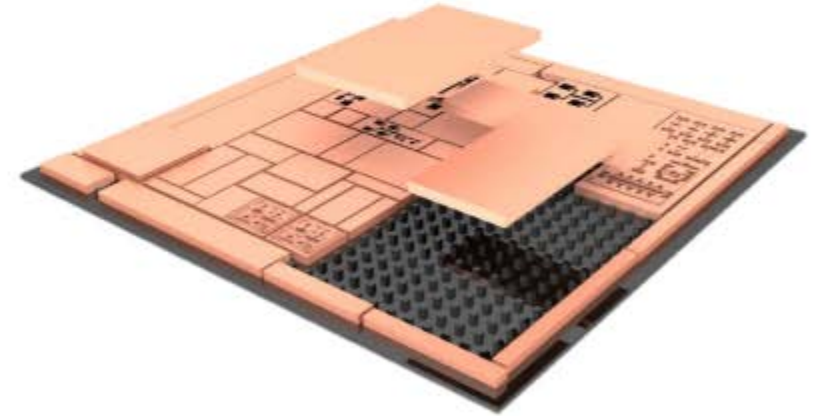Image: Intel

CHIPS is focused on creating modular IP – not new IP!

# Plug and Play Standard: AIB Die-to-Die Interface

*IEEE Spectrum 7/2018:* "Intel CTO Mike Mayberry says that Intel will provide its Advanced Interface Bus (AIB) royalty-free."

Chiplets (die assembled into a Multi-Chip Package) need a standard interface for reuse and interoperability: **AIB**

AIB adopted by US Government DARPA CHIPS performers over competing SERDES concepts

- Fundamental to the US Government's Heterogeneous Integration strategy

Purpose is to grow an ecosystem of interoperating chiplets
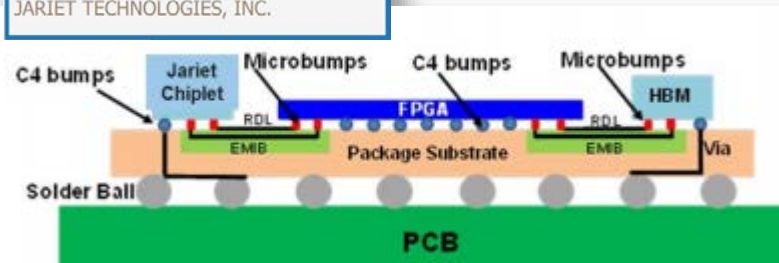
## AIB Promoters Agreement Organizations

Ayar Labs
The Boeing Company
Cadence Design Systems Inc.
eSilicon Corporation
Georgia Tech Research Corp.
Intel Corporation
Intrinsix Corp.
Jariet Technologies, Inc.
Lockheed Martin Corporation Advanced Technology Laboratories
National Technology & Engineering Solutions of Sandia, LLC
North Carolina State University
The Regents of the University of Michigan
Synopsys, Inc.

# Chiplets Kickstarted by DARPA



**ERI** ELECTRONICS RESURGENCE INITIATIVE
**S U M M I T**
**2018** | SAN FRANCISCO, CA | JULY 23-25

**CRAIG HORNBUCKLE**
CHIEF TECHNOLOGY OFFICER
JARIET TECHNOLOGIES, INC.



**High level of RF/Digital Integration in 14LPP SOC**
- 4x ADC/DAC macrocells
- Per-channel digital pre-processing (~40M gates/channel)
- **Standardized AIB low-power in-package parallel interface**

## Ayar Labs Selected as Optical Solution Partner for Intel's DARPA PIPES Project and Announces Customer Sampling Program

*Company will demonstrate latest solution at Supercomputing 2019 Conference as a core innovation to drive Moore's Law benefits for the next decade and beyond*

November 18, 2019 10:00 AM Eastern Standard Time

SANTA CLARA, Calif.--(BUSINESS WIRE)--Ayar Labs is pleased to announce that it's been selected as Intel's optical I/O solution partner for their recently awarded DARPA PIPES research project.

In the first phase of the project, the Ayar Labs TeraPHY™ chiplet will be co-packaged with an Intel FPGA using the AIB (Advanced Interconnect Bus) interface.

18

# AIB Public Specification and Hardware Open Source
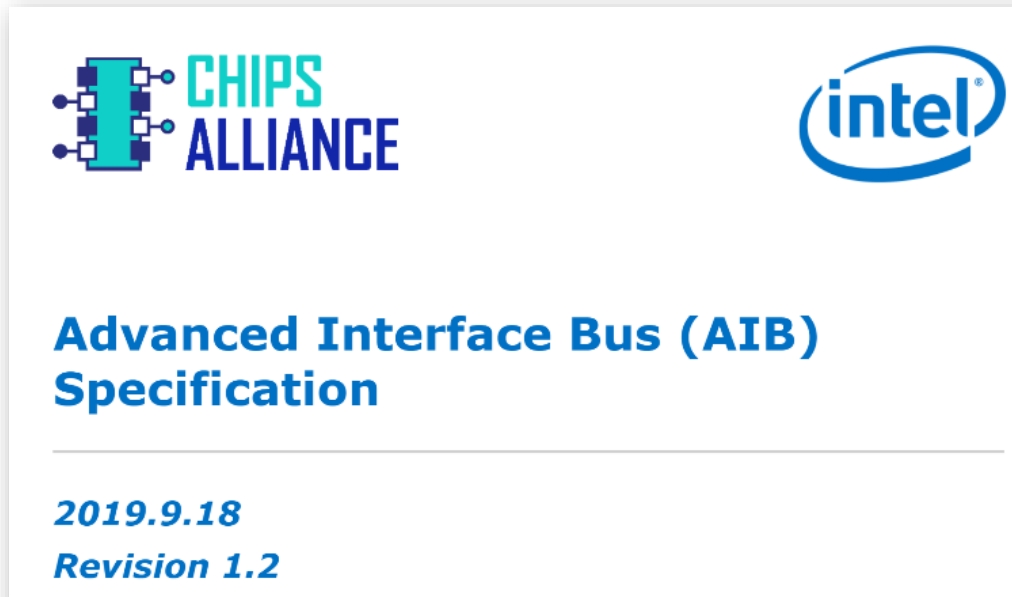


**AIB Public Specification includes:**
- Electrical specs, bump array mechanicals, data/clock/ control signal definitions, reset handshaking, JTAG
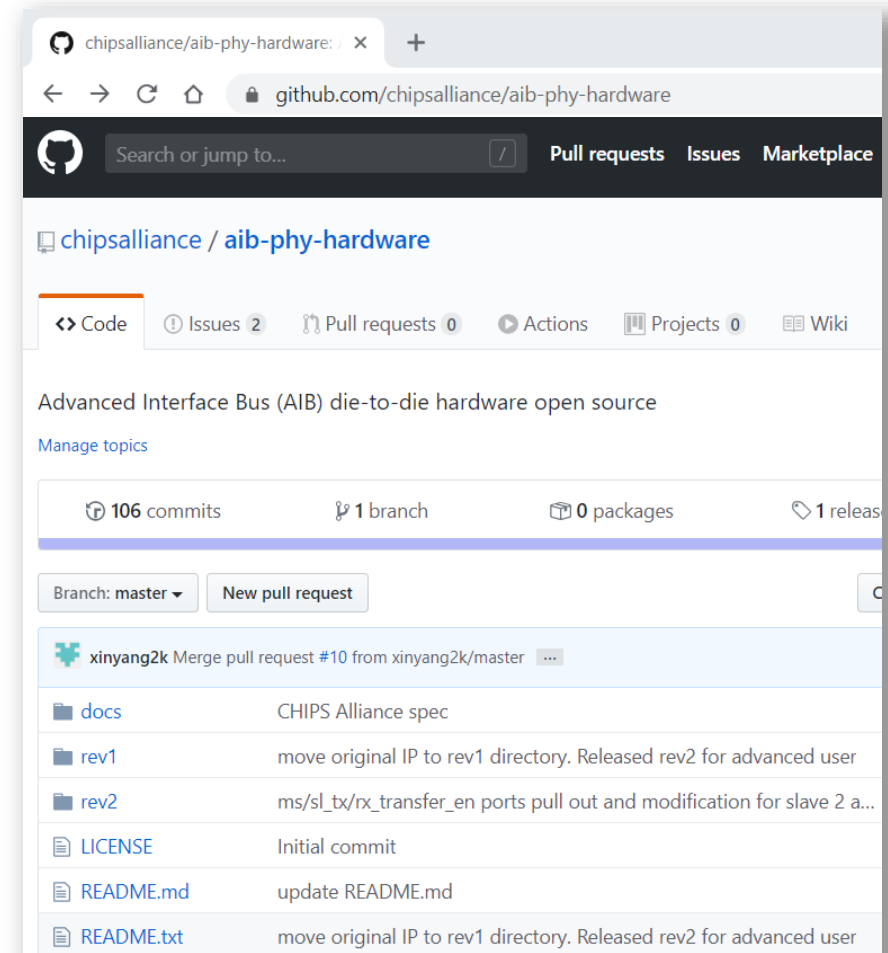
**AIB Open Source Hardware on GitHub**
- Register transfer level (RTL), netlists, generic cell library
- Purpose: **reduce development cost**

Available at https://github.com/chipsalliance/aib-phy-hardware

# DARPA CHIPS and Standardization Takeaways

Government stepped in when industry could not make a standard on its own

DARPA Leadership inspired us to develop not-originally-planned benefits: hardware open source

# *Chiplets on the Rise:*
# Chiplet Ecosystem

intel

# Growing AIB-Based Chiplet Ecosystem

Chiplets in production with Intel® Stratix™ 10 FPGAs
- L-Tile 17G SERDES, H-Tile 28G SERDES, E-Tile 58G SERD

New chiplets with Intel® Agilex™ FPGAs
- F-Tile 112 Gbps serializer /deserializer (SERDES)
- P-Tile PCI Express* (PCIe) Gen4
- R-Tile PCIe Gen5 and Compute Express Link* (CXL)
- Custom intellectual property (IP) via Intel® eASIC™

Industry adoption
- Jariet Technologies 64Gsamples/s ADC/DAC chiplet
- Ayar Labs photonics chiplet
- *Others coming soon*
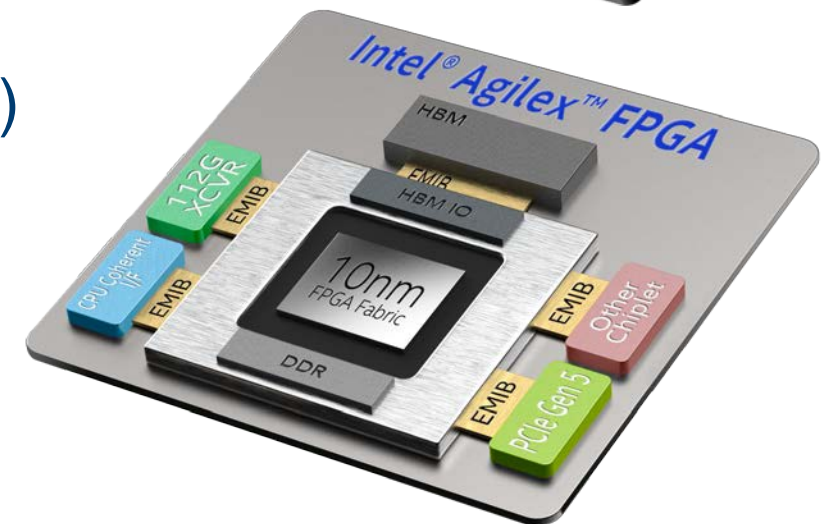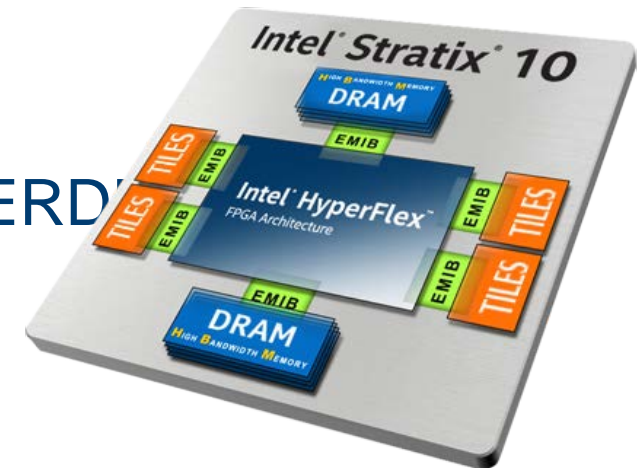
# Intel and CHIPS Alliance

Intel joined the CHIPS Alliance in December 2019

With Intel contributing AIB as a royalty-free CHIPS Alliance specification and CHIPS Alliance hardware open source project, the industry benefits from the CHIPS Alliance objectives[1]:

*"The mission of the CHIPS Alliance is to develop high-quality, open source hardware designs relevant to silicon devices and FPGAs."*

*"By creating an open and collaborative environment, CHIPS Alliance shares resources to lower the cost of development."*
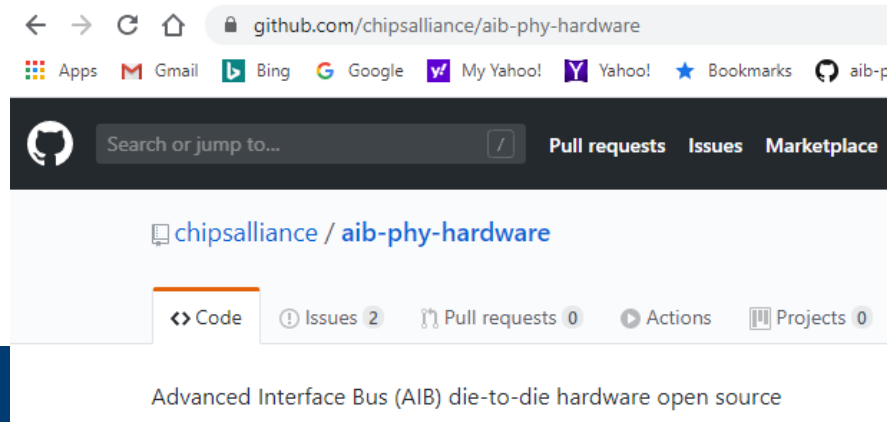
CHIPS Alliance Members[1]:
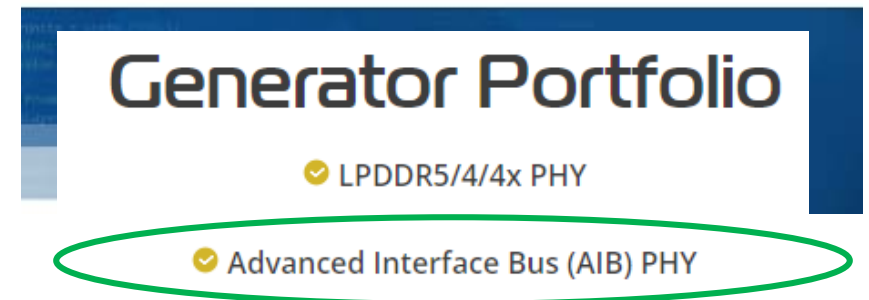
# Chiplet Ecosystem Must Have #1: PHY IP

***Excellent progress on AIB PHY IP:***

- AIB Open Source enhancements: multi-chip simulation testbenches, both SoC and chiplet interfaces
- AIB IP announced from eSilicon and Blue Cheetah Analog Design
- Research into Automated Physical Design Generation to reduce process porting costs



eSilicon

SAN JOSE, Calif., Sept. 22, 2019 (GLOBE NEWSWIRE) -- eSilicon, a leading provider of FinFET ASICs, market-specific IP platforms and advanced 2.5D packaging solutions, announced today its 7nm high-bandwidth interconnect (HBI™)⁺ physical interface (PHY) IP is available to be licensed for inclusion in customer designs. This special-purpose hard IP block delivers a high-bandwidth, low-power and low-latency

- AIB Plus compliant: Intel Advanced Interface Bus (AIB) version 1.1

BLUE CHEETAH
ANALOG DESIGN

**Generator Portfolio**

- ✓ LPDDR5/4/4x PHY
- ✓ Advanced Interface Bus (AIB) PHY

← → C ⌂  🔒 github.com/chipsalliance/aib-phy-hardware

▦ Apps  M Gmail  ▷ Bing  G Google  y! My Yahoo!  Y! Yahoo!  ★ Bookmarks  ⬡ aib-p

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📖 chipsalliance / **aib-phy-hardware**

<> Code    ⊙ Issues 2    ⑂ Pull requests 0    ▶ Actions    ▥ Projects 0

Advanced Interface Bus (AIB) die-to-die hardware open source

# Chiplet Ecosystem Must Have #2: Availability of Advanced Packaging Technology

***Need generally available Advanced Packaging Technology!***

"Large" business opportunity is needed to interest providers of Advanced Packaging Technology

How can the semiconductor packaging industry reduce the barriers?

- Could you be the "MOSIS" of packaging?
  - *MOSIS is a multi-project wafer provider that lowers the per-project cost of masks*
- Could you offer MCP design and prototypes for under $100K?
- Could you make a Google-type offer?

# Chiplets on the Rise Summary

Advanced packaging technology inspired new thinking about SoC microarchitecture

Chiplets enable faster system development serving a broader range of applications

General availability of advanced packaging technology → stronger chiplet ecosystem → better value we can provide