

**IEEE EDS DISTINGUISHED LECTURER TALK****Organized by IEEE Singapore Rel/CPMT/ED Chapter and co-hosted by  
Microelectronics Centre, Nanyang Technological University****“More Moore and More than Moore Meeting for 3D”**

Speaker : **Prof Simon Deleonibus**  
**CEA-LETI, France**

Date : **14 February 2011, Monday**

Time : **2pm – 3pm**

Venue : **Executive Seminar Room, Block S2.2 (S2.2-B2-53), NTU**

Map : <http://www3.ntu.edu.sg/eee/map/car-jb-com.html>

Admission : Free

**ABSTRACT**

Nanoelectronics linear scaling appeals new 3D integration schemes in order to continue Moore's law. Unique opportunities exist to increase the devices performances, system complexity and reduce power consumption of mobile, handheld objects. New design and functional architectures will be possible by mixing logic and memory devices to save power consumption and introduce new applications by using neuromorphic or bio inspired approaches. Devices other than CMOS can be cointegrated with CMOS to interface the outside Multiphysics world (MEMS, sensors and actuators, RF devices, power devices,...) allowing new functionalities. 3D Wafer Level Packaging and System on a Wafer allow these new routes.

**ABOUT THE SPEAKER**

MSc and PhD in Applied Physics from Paris University, in 1979 and 1982 respectively.

- Since 2008, he is Chief Scientist (Directeur Scientifique) at LETI watching at the Silicon Technologies Research (850 researchers).

- From 1999 to 2008, he was Director of the Electronic Nanodevices Laboratory (60 researchers). He managed several Industrial, National and European funded projects.

- From 1996 to 1999, he managed the Ultimate CMOS project.

- He joined LETI (CEA) in 1986 as a device engineering and process modules development expert for CMOS and Flash memories applications.

- He joined Thomson Semiconducteurs (Grenoble) in 1981 as a development and transfer to production process integration engineer.

- Published papers or submitted: more than 550 (conferences and journals; 60 invited) .

- Editor of 1 book (WSPC). Guest editor of 1 Special issue of SSE. Author of 10 book chapters.

- Editor of IEEE Transactions on Electron Devices.

- Editor of European Physical Journal - EPJ Applied Physics

- He owns 30 patents: among them the initial patent on contact plug principle, widely used as a standard process by the semiconductor industry.

- With his team, he realized the first 20nm gate length MOSFET, world's smallest transistor in June 1999.

- International Conference program Committees. European Chair and Member of the VLSI Technology Symposium (from 2000 to 2006). Member of the 1998 and 1999,2004 and 2005 International Electron Devices Meeting (IEDM) program committee. Member of the ESSDERC program committee since 2000 and Responsible for the ESSDERC2005 Tutorials. Member of the Program and Steering Committees of 5 International Conferences sponsored by IEEE and the Electrochemical Society. Member of the International Technology Roadmap of Semiconductors(ITRS). Member of the Board of Directors of the Nanosciences Foundation. Member of the European Research Council Engineering Panel. Since 1998, he lectures on microelectronics devices physics and technology and nanosciences at different Institutions and Universities, in France and Worldwide.

- Fellow of the IEEE

- Research Director of French CEA

- IEEE Distinguished Lecturer

- “Chevalier de l'Ordre National du Mérite” Decree of French Presidence

- Recipient of the “2005 Grand Prix de l'Académie des Technologies - Prix Chéreau Lavet”

- Recipient or co-recipient of 10 Best Papers Awards obtained at International conferences,among them IEDM 2009

- Member of the Electrochemical Society; Member of the Materials Research Society