

IEEE / NTU TALK

Organized by IEEE Singapore Rel/CPMT/ED Chapter and
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Nanyang Technological University

“DESIGNING FOR ELECTROMIGRATION RELIABILITY”

Speaker : **Dr Vincent M Dwyer**
Loughborough University, UK

Date : **2 March 2011, Wednesday**

Time : **4:30pm**

Venue : **LT 9, Block NS4, NS4-04-39, NTU**

Map : <http://maps.ntu.edu.sg/maps#q:lt%209>

Admission : Free

ABSTRACT

Electromigration (EM) failure in VLSI circuits is so serious a problem that the main manufacturers of IC Design software have now developed CAD tools to help prevent such problems arising. At its simplest, the process maximum-current J_{max} is compared to the current density J_{EM} which will produce EM failure, at a fixed probability level, when extrapolated to operational conditions. This statement requires the estimation of J_{EM} from accelerated laboratory conditions and involves the implicit assumption that failure times are distributed lognormally. As the analysis becomes more sophisticated the short length effect is also included. Lines shorter than some critical value are unable to develop sufficient stress for failure; consequently these lines are immortal and may be removed from any reliability analysis. More sophisticated analysis derives expected current densities on each line, compares that to J_{EM} , and increases the linewidth if necessary. For signal lines, which carry bi-directional current as nodes are first charged from V_{DD} and then discharged to V_{SS} , EM analysis is done variously on the basis of either the RMS or the peak value of the extracted current. This talk will look at the manner in which these facts are related through EM models, the commonalities of various models, and the manner in which their predictions impacts on EM reliability analysis.

ABOUT THE SPEAKER

Dr Vincent M Dwyer is originally from Manchester in the UK. He attended Cambridge University as an undergraduate in Mathematics and received his doctorate in Theoretical Surface Physics from the University of York. After periods at Trinity College, Dublin (Eire) and at Warwick University in the UK he joined the Department of Electronic and Electrical Engineering at Loughborough University, where he is now a Reader in Electronic Devices.

He has published over 70 academic papers on a variety of topics. A major area has been the reliability and physics of failure of VLSI devices and circuits where his studies have included Electrostatic Discharge (ESD) and Electrical Overstress (EOS) damage, and more recently Electromigration.