

# 4<sup>TH</sup> ELECTRONICS PACKAGING TECHNOLOGY CONFERENCE (EPTC 2002)

10 - 12 December 2002

Grand Copthorne Waterfront Hotel Singapore

## FINAL PROGRAMME

ORGANIZED BY:



IEEE Reliability/CPMT/ED  
Singapore Chapter

TECHNICALLY CO-SPONSORED BY:



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## FOREWORD

The organising committee welcomes you to the 4<sup>th</sup> Electronics Packaging Technology Conference (EPTC 2002) at the Grand Corphorne Waterfront Hotel, Singapore. This conference is organised by the Reliability/CPMT/ED Chapter of the IEEE Singapore Section and is technically co-sponsored by the IEEE CPMT Society and IMAPS. It is organised in cooperation with ASME Singapore Section, Institute of Materials Research and Engineering, Institute of Microelectronics, Nanyang Technological University, National University of Singapore and Singapore Institute of Manufacturing Technology.

The EPTC is an international conference dedicated to advances, research, development and applications of electronic components, assemblies and systems. This year, we have more than 80 quality technical papers to be presented in 19 sessions by engineers and scientists from 16 countries. These papers will address key issues on lead free solders, electrical and thermal modeling, design for high performance electronics, MEMS and optical component packaging, materials and processes, interconnection technologies and reliability. As befitting the growing stature of the conference, we have put in place six technical sub-committees comprising local and international researchers in the relevant areas to assist us in the review process. We are privileged to have Dr. Rao Tummula and Dr. Werner Weber to deliver the 2 conference keynote addresses. For the first time, we are introducing the Poster Session to offer delegates a unique opportunity to interact with the authors in an informal atmosphere. As part of our growth toward a leading electronics packaging technology conference, the EPTC 2002 will offer its proceedings to you both in print and on CD-ROM. 4 one-day short courses are offered prior to the technical sessions to provide avenues for specific area of technology interest. The conference also features a one-day table-top exhibition for companies to showcase some of the latest products and services on offer.

We are delighted to have IEEE CPMT Society to hold its leadership workshop and IEEE CPMT TC-12 to hold a one-day workshop on Electrical Design of Advanced Packaging and Systems in conjunction with EPTC 2002. With such strong support and endorsement from the international community, including the International Advisory Board, we are confident that EPTC is truly realising its vision to be a leading international electronics packaging technology conference for the Asia Pacific region.

The organizing committee would like to thank the authors, speakers, exhibitors, sponsors and members of the technical sub-committees for your contribution and participation. We are grateful to the delegates for making an extraordinary effort to attend the conference during this period of challenging business outlook and to our organizations for their support in making this conference possible.

We trust that you will find EPTC 2002 to be enjoyable and a rewarding experience for you.

Charles Lee  
General Chairman

Toh Kok Chuan  
Technical Programme  
Co-Chairman

Mahadevan K. Iyer  
Technical Programme  
Co-Chairman

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Yogendra Joshi, *Georgia Institute of Technology, USA*  
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Mihai Rotaru, *Institute of Microelectronics*

## GENERAL INFORMATION

### NAME TAG

The name tag is your identification to gain entry to all events of EPTC 2002 and MUST be worn at all times.

### LANGUAGE

The official language of the conference is English.

### SECRETARIAT ON-SITE AND OPENING HOURS

Please note that the EPTC 2002 Secretariat will be located at Flamingo, Level 3, Grand Copthorne Waterfront Hotel from 10 to 12 December 2002. The opening hours are:

10 December 2002: 8.00am to 5.30pm  
11 – 12 December 2002: 7.30am to 6.00pm

### AUTHOR'S ROOM AND OPENING HOURS

The Author's Room is located at the Flamingo, Level 3, Grand Copthorne Waterfront Hotel from 10 to 12 December 2002. The opening hours are:

10 December 2002: 10.00am to 5.30pm  
11 – 12 December 2002: 10.00am to 6.00pm

### SECRETARIAT

EPTC 2002 is organised by the IEEE Reliability/CPMT/ED Singapore Chapter and managed by the EPTC 2002 Secretariat. All correspondence should be addressed to:

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Website: <http://ewh.ieee.org/soc/cpmt/singapore/eptc2002>

### CONFERENCE VENUE

Grand Copthorne Waterfront Hotel  
392 Havelock Road, Singapore 169663  
Tel: (65) 6733 0880  
Fax: (65) 6737 8880  
Website: <http://www.grandcopthorne.com.sg>

## PROGRAMME OVERVIEW

### SHORT COURSES: 10 December 2002, Tuesday

0830 – 0900 hrs	Registration: Level 3 Foyer			
0900 – 1700 hrs (inclusive of Lunch and two Coffee Breaks)	<b>SC1: Integrated Passives Technologies: Design, Materials &amp; Processing</b> Room: Galleria II	<b>SC2: Active Optical Components for Telecom &amp; Data Applications</b> Room: Galleria III	<b>SC3: Wafer Level Chip Scale Packaging Technologies: Application of Solders &amp; Solder Alternatives</b> Room: Swallow	<b>SC4: Lead Free Solder Materials &amp; Reliability Performance</b> Room: Cardinal
Instructor(s):	Dr Swapan Bhattacharya, <i>Georgia Institute of Technology, USA</i>	Dr Torsten Wipiejewski, <i>Agility Communications, USA</i>	Dr John Lau, <i>Agilent Technologies, USA</i>	Dr John Pang, <i>Nanyang Technological University, Singapore</i> and Dr Andreas Schubert, <i>Fraunhofer Institute, Germany</i>

### CONFERENCE DAY 1: 11 December 2002, Wednesday

0730 – 0830 hrs	Registration: Level 4 Foyer		
<b>Plenary Session</b>	Room: Grand Ballroom 1, Level 4		
0830 – 0845 hrs	Conference Opening Address by EPTC 2002 General Chairman Charles Lee, <i>Infineon Technologies Asia Pacific</i>		
0845 – 0930 hrs	<b>Keynote Address: High Density Packaging in 2010 and Beyond</b> Rao R. Tummala, <i>Georgia Institute of Technology, USA</i>		
0930 – 1015 hrs	<b>Keynote Address: Ambient Intelligence - Key Technologies in the Communication Age</b> Werner Weber, <i>Infineon Technologies AG, Germany</i>		
1015 – 1045 hrs	Coffee Break		
<b>Technical Sessions</b>	Track 1 Room: Galleria II & III, Level 3	Track 2 Room: Cardinal, Level 3	Track 3 Room: Swallow, Level 3
1045 – 1225 hrs	Session A1 - MP2: <b>Lead Free Solders</b>	Session A2 - AP4: <b>RF/HF Challenges</b>	Session A3 - QR1: <b>Reliability/ Failure Analysis I</b>

1225 – 1335 hrs	Lunch: Grand Ballroom 1, Level 4		
1335 – 1515 hrs	Session B1 - MP1: <b>Advanced Materials</b>	Session B2 - AP1: <b>MEMS Packaging</b>	Session B3 - QR2: <b>Reliability / Failure Analysis II</b>
1515 – 1600 hrs	Coffee Break		
1600 – 1740 hrs	Session C1 - MP3: <b>Solders and Adhesives</b>	Session C2 - AP3: <b>Optical Components</b>	Session C3 - TE2: <b>Electrical Design &amp; Test</b>
1830 – 2100 hrs	Conference Banquet cum Talk Room: Lyrebird, Level 3		

### TABLETOP EXHIBITION: 11 December 2002, Wednesday

1000 – 1830 hrs	Level 3 Foyer
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### CONFERENCE DAY 2: 12 December 2002, Thursday

<b>Technical Sessions</b>	Track 1 Room: Galleria II & III, Level 3	Track 2 Room: Cardinal, Level 3	Track 3 Room: Swallow, Level 3
0845 – 1050 hrs	Session D1-IA3: <b>Manufacturing Technologies</b>	Session D2 - AP2: <b>Modules and Integration</b>	Session D3 - TE1: <b>Electrical Performance / Signal Integrity</b>
1050 – 1200 hrs	Coffee Break / P1: Poster Session / Networking Session Level 3 Foyer		
1200 – 1325 hrs	<b>Luncheon Talk: Educational Modules Over the Internet: A Demonstration</b> Paul Wesling, <i>CPMT/Hewlett Packard Co., USA</i> Room: Grand Ballroom 1, Level 4		
1325 – 1530 hrs	Session E1 - IA1: <b>Interconnects I</b>	Session E2 - TE3: <b>Package Thermal Modeling</b>	Session E3 – MS2: <b>Modeling &amp; Simulation II</b>
1530 – 1600 hrs	Coffee Break		
1600 – 1740 hrs	Session F1 - IA2: <b>Interconnects II</b>	Session F2 - TE4: <b>Thermal Management</b>	Session F3 – MS1: <b>Modeling &amp; Simulation I</b>
1740 – 1800 hrs	Presentation of Outstanding Papers and Closing Level 3 Foyer		

**SHORT COURSE 1: Integrated Passives Technologies: Design, Materials & Processing**  
*Dr Swapan Bhattacharya, Georgia Institute of Technology, USA*

**Course Outline:**

- Embedded/integral passives - Descriptions and definitions
- Why Integral/Embedded passives?
- Electronic system packaging needs (SIA, NEMI, ITRI, Industry perspectives)
- Benefits of integration of passive components
  - Design and Modeling of passives
  - Materials approaches for realization of embedded capacitors, resistors, and inductors in MCM-C, MCM-D, MCM-L and MCM-L/D technologies
- Integral passives research and development activities around the world
  - Integral passives and MEMS research at the Packaging Research Center, Georgia Tech
- University and industry prototypes
- Commercialization paths and issues
  - Economic and technical viability - integral vs. discretized
  - Challenges: Design, modeling, fabrication, characterization and testing
  - The future of embedded passives

**SHORT COURSE 2: Active Optical Components for Telecom & Data Applications**  
*Dr Torsten Wipiejewski, Agility Communications, USA*

**Course Outline:**

- Introduction: modern optical transmission systems
- Laser diodes: basic design and operation
  - Optical gain in semiconductors
  - Fabry-Perot laser diodes (structure and fabrication, performance)
  - Distributed Feedback (DFB) lasers (properties and applications)
  - Vertical-cavity surface-emitting lasers (VCSELs at 850nm, 1300/1550nm)
  - Tunable lasers (tuning scheme, applications)
  - Laser diode packaging (wavelength monitoring)
- Modulators: different types and speed limitations
  - Mach-Zehnder modulator
  - Electro-absorption modulator (chirp performance)
- Photodetectors: the receiving side of a transmission system
  - Pin photodiodes (responsivity and bandwidth limitation)
  - Avalanche photodiodes (gain and noise performance)
  - Other photodetectors (MSM, heterodyne detection)
- Integration: technical challenges and economic boundary conditions
  - Types of integration and limitations
  - Laser diode and electro-absorption modulator
  - Outlook on future developments

**SHORT COURSE 3: Wafer Level Chip Scale Packaging Technologies: Application of Solders & Solder Alternatives**

*Dr John Lau, Agilent Technologies Inc, USA*

**Course Outline:**

- Critical Issues of WLCSPs
- Lead-free soldering activities in Europe, Asia, and USA.
- Criteria, development approaches, and varieties of alloys and properties of lead-free solders.
- Physical, mechanical, chemical, electrical, and soldering properties of lead-free solders.
- Chip (wafer) level interconnects with lead-free solder bumps – various UBMs.
- Lead-free solder wafer-bumping with micro-ball mounting and paste printing methods.
- Microvia Technologies.
- PCB/substrate with build-up layers connecting through Microvias.
- Lead-free solder-joint reliability of WLCSPs on organic and ceramic substrates.
- Chip (wafer) level interconnects with solderless bumps such as Ni-Au, Au, and Cu; solderless wires such as Cu and Au; and solderless studs such as Au and Cu.
- Adhesives:- isotropic conductive adhesives, anisotropic conductive adhesives, non-conductive adhesives, and reworkable adhesives.
- Design, materials, process, and reliability of various solderless WLCSPs with various adhesives on Flex/PCB/substrate.
- Summary

**SHORT COURSE 4: Lead Free Solder Materials & Reliability Performance**

*Dr John Pang, Nanyang Technological University, Singapore and Dr Andreas Schubert, Fraunhofer Institute, Germany*

**Course Outline:**

- Lead-Free Bulk Solder Mechanical Properties
  - Mechanical properties of lead-free (SnAg, SnCu, SnAgCu) versus SnPb solders, Effect of Temperature and Strain Rate
  - Fatigue properties of lead-free (SnAg, SnCu, SnAgCu) versus SnPb solders, Effect of Temperature and Frequency
  - Creep properties of lead-free (SnAg, SnCu, SnAgCu) versus SnPb solders, Effect of Stress and Temperature
- Lead Free Solder Joint Reliability Tests and Analysis
  - Creep and Stress Relaxation, Bulk versus Joint behavior (SnAg, SnAgCu, and SnPb)
  - Temperature cycle data on FCOB with/without underfills, CSPs and BGAs at different test conditions and solder alloys types
  - Solder-surface finish interactions, intermetallic growth, metallization consumption, intermetallics within the solder, thermo-mechanical properties of the intermetallics.
  - Failure mechanisms related to the solder joints of the new alloys, will creep deformation still play a dominant role for e.g. thermally induced low cycle fatigue?
- Finite Element Analysis and Modeling
  - Material constitutive models - implementation of time and temperature dependent behavior of solders (SnAg, SnAgCu, and SnPb).
  - Life prediction models - Strain-based relations (accumulated creep strain), Energy-based relations (average viscoplastic strain energy dissipated).
  - FEA modeling and simulation of Thermal Cycling Tests (SnAg, SnAgCu and SnPb), Comparison between simulation results and experimental results.

## EPTC 2002 CONFERENCE PROGRAMME

### DAY 1: 11 DECEMBER 2002, WEDNESDAY

0730 – 0830hrs Registration

0830 – 0845hrs Conference Opening Address

0845 – 0930hrs **Keynote Address:** High Density Packaging in 2010 and Beyond  
Rao R. Tummala, *Georgia Institute of Technology, USA*

0930 – 1015hrs **Keynote Address:** Ambient Intelligence Key Technologies in the Communication Age  
Werner Weber, *Infineon Technologies AG, Germany*

1015 – 1045hrs COFFEE BREAK

#### Session A1 - MP2: LEAD FREE SOLDERS

Chairman: John Lau, *Agilent Technologies, USA*

1045hrs A1.1 An Assessment of Lead Free Solder (Sn3.7 Ag0.8Cu) Wettability  
C.K. Chung, F. Mustapha, F. Hua\* and R. Aspandiar\* / *Intel Corporation, Malaysia;*  
*\*Intel Corporation, USA*

1110hrs A1.2 Lead-free Solder Evaluation for Ball Attaché Process  
A. Anand and Y.C Mui / *Advanced Micro Devices, Singapore*

1135hrs A1.3 Lead-Free Semiconductor Packaging  
C.C.M. Beelen-Hendriks, J. Klerk and J.T. van de Water / *Philips, The Netherlands*

1200hrs A1.4 Fretting Corrosion Studies for Lead-Free Alloy Plated Contacts  
J. Wu and M. Pecht / *University of Maryland, USA*

#### Session A2 - AP4: RF/HF CHALLENGES

Chairman: A.C. Cangellaris, *University of Illinois, Urbana-Champaign, USA*

1045hrs A2.1 RFICs Packages Electrical Performance Comparison of both ULTRA-CSP and Standard TSOP  
T. Hsu, K. Chiang and Y.P. Wang / *Siliconware Precision Industries, Taiwan*

1110hrs A2.2 Integrated Circuit Package Band Pass Filter  
Y.P. Zhang and T.Y. Phang / *Nanyang Technological University, Singapore*

1135hrs A2.3 An Original Modeling Process and Technology with Intra-Package Crosstalk Consideration for Compact Array Antennas on the 4G Communications Packages  
A.F. Kamal, C.P. Wong and J.A. Copeland / *Georgia Institute of Technology, USA*

1200hrs A2.4 Design of On-Package Microstrip Antennas for Single-Chip Wireless Transceivers  
Y.P. Zhang / *Nanyang Technological University, Singapore*

#### Session A3 - QR1: RELIABILITY / FAILURE ANALYSIS I

Chairman: John Pang, *Nanyang Technological University*

1045hrs A3.1 Bonding on Cu: A New Stress Evaluation Approach by Raman Spectroscopy  
J. Chen, H.M. Ho, W. Lam, P. Ratchev, S. Stoukatch, E. Beyne, C.J. Vath III\* and I. De Wolf *IMEC, Belgium; \*ASM Technology, Singapore*

1110hrs A3.2 Non-Destructive Analysis on Flip Chip Package with TDR (Time Domain Reflectometry) and SQUID (Superconducting Quantum Interference Device)  
L. Cao, H.B. Chong, J.M. Chin and R.N. Master\* / *Advanced Micro Devices, Singapore; \*Advanced Micro Devices, USA*

1135hrs A3.3 Flip Chip Interfacial Behavior Under Thermal Testing  
Z.W. Zhong, X.Q. Shi\*, K.W. Wong and Z.P. Wang\* / *Nanyang Technological University, Singapore; \*Singapore Institute of Manufacturing Technology, Singapore*

1200hrs A3.4 Solder Imprint Technology: A Reverse Growth of Intermetallic Compound at the Interface to Fix the Brittle Interfacial Fracture of BGA Package Soldered on Ni / Au Plating  
C.K. Chung and K.F. Leong and K.S. Sim / *Intel Corporation, Malaysia*

1225 – 1335hrs LUNCH

#### Session B1 - MP1: ADVANCED MATERIALS

Chairman: Simon Ang, *National University of Singapore*

1335hrs B1.1 Novel Ultra-High Dielectric Constant Polymer Based Composite for Embedded Capacitor Application  
Y. Rao and C.P. Wong / *Georgia Institute of Technology, USA*

1400hrs B1.2 An Effective Method of Characterizing Moisture Desorption of Polymeric Materials at High Temperature  
Y. Shi, A.A.O. Tay, E.H. Wong\* and R. Ranjan\* / *National University of Singapore, Singapore; \*Institute of Microelectronics, Singapore*

1425hrs B1.3 Effect of Mechanochemical Treatment of Supported Catalysts on the CVD Growth of Carbon Nanomaterials  
H. Ryu, H.K. Yu and F. Saito\* / *Korea Institute of Chemical Technology, Korea; \*Tohoku University, Japan*

1450hrs B1.4 Low Temperature (< 100°C) Hydrothermal Synthesis of High K- low Loss BaTiO<sub>3</sub> Films for Integral Capacitors  
D. Balaraman, P.M. Raj. R. Tanikella, P. Kohl, S. Bhattacharya, and R. Tummala / *Georgia Institute of Technology, USA*

#### Session B2 - AP1: MEMS PACKAGING

Chairman: Lim Thiam Beng, *Institute of Microelectronics*

1335hrs B2.1 Role of Bonding Temperature and Voltage in Silicon-to-Glass Anodic Bonding  
J. Wei, Z.P. Wang, H. Xie and F.L. Ng / *Singapore Institute of Manufacturing Technology, Singapore*

1400hrs B2.2 A Study on Hermetic Packaging for Micro-Optical Switch  
Y.F. Jin, Z.F. Wang and Z.P. Wang / *Singapore Institute of Manufacturing Technology, Singapore*

1425hrs B2.3 Packaging of a Fiber Optical MEMS Switch  
Z.F. Wang, W. Cao\*, P. Arulvanan, Y.F. Jin, D.Y. Pan and Z.P. Wang / *Singapore Institute of Manufacturing Technology, Singapore; \* National University of Singapore, Singapore*

1450hrs B2.4 Finite Element Simulation of the Fatigue Behaviour of a MEMS Package  
A. Chng, A.A.O. Tay, K.M. Lim, T.C. Chai\* and Premachandran\* / *National University of Singapore, Singapore; \*Institute of Microelectronics, Singapore*

**Session B3 - QR2: RELIABILITY / FAILURE ANALYSIS II**Chairman: Andreas Schubert, *Fraunhofer IZM, Germany*

- 1335hrs B3.1 Flip Chip Solder Joint Fatigue Life Model Investigation  
A. Yeo, C. Lee and J.H.L. Pang\* / *Infineon Technologies AP, Singapore; \*Nanyang Technological University, Singapore*
- 1400hrs B3.2 In-Situ Reliability Analysis of Solder Joint by Digital Image Correlation  
J.H.L. Pang, X.R. Zhang, Q.J. Liu, F.X. Che, T.H. Low, X.Q. Shi\* and Z.P. Wang\* / *Nanyang Technological University, Singapore; \*Singapore Institute of Manufacturing Technology, Singapore*
- 1425hrs B3.3 Mechanical Response of PCBs in Portable Electronic Products During Drop Impact  
S.K.W. Seah, C.T. Lim, E.H. Wong\*, B.C. Tan and V.P.W. Shim / *National University of Singapore, Singapore; \*Institute of Microelectronics, Singapore*
- 1450hrs B3.4 Reliability Assessment of High Density Multi-Layer Board Assembly Using Shadow Moiré and Luminescence Spectroscopy  
S. Bansal, P.M. Raj, S. Banerji, K. Shinotani\*, S. Bhattacharya, R.R. Tummala and M.J. Lance\*\* / *Georgia Institute of Technology, USA; \*Matsushita Electric Works, Japan; \*\*Oak Ridge National Laboratory, USA*

1515 – 1600hrs COFFEE BREAK

**Session C1 - MP3: SOLDERS AND ADHESIVES**Chairman: Tan Ah Chin, *Micron Semiconductor Asia*

- 1600hrs C1.1 Studies on Moisture-Induced Failure in ACF Interconnection  
W. Zhou, S.W. Low, Y.L. Neo, M.K. Eng and M. Huang / *Micron Semiconductor Asia, Singapore*
- 1625hrs C1.2 Low Temperature Flip-Chip Process Using ICA and NCA (Isotropically and Non-Conductive Adhesive) for Flexible Displays Application  
J. Vanfleteren, B. Vandecasteele and T. Podprocky / *IMEC, Belgium*
- 1650hrs C1.3 Current Loadability of ICA for Flip Chip Applications  
J. Haberland, B. Pahl, S. Schmitz, C. Kallmayer, R. Aschenbrenner\* and H. Reichl / *Berlin Technical University, Germany; \*Fraunhofer Institute Reliability and Microintegration, Germany*
- 1715hrs C1.4 Effects of Gold Layer Thickness on the Characteristics of Flip-Chip Interconnects  
W.S. Chai, M. Gupta, A.A.O. Tay and J.F.J. Caers\* / *National University of Singapore, Singapore; \*Philips Electronics, Singapore*

**Session C2 - AP3: Optical Components**Chairman: Paul Wesling, *Hewlett Packard Co, USA*

- 1600hrs C2.1 Modelling and Optimization of Photonic-Crystal Waveguide Coupling  
A. Popov / *Institute of Microelectronics, Singapore*
- 1625hrs C2.2 Superposition of OADM and Switch via Polarization  
A.J. Whang, S. Liao and S.M. Chao / *National Taiwan University of Science & Technology, Taiwan*
- 1650hrs C2.3 Design for Enhancing Reliability of LC Chip in a 10Gps Optoelectronic Package  
Y. Ma, K. Suharsanam, P. Ramana and E. Ishimura / *Institute of Microelectronics, Singapore; \*Mitsubishi Electric Corporation, Japan*
- 1715hrs C2.4 Low Cost Materials and Processes for OE Packaging  
C. K. Ong, S. Krishnamachari, P. Ramana and T.C. Chai / *Institute of Microelectronics, Singapore*

**Session C3 - TE2: ELECTRICAL DESIGN AND TEST**Chairman: F. Canavero, *Politecnico di Torino, Italy*

- 1600hrs C3.1 A Test Strategy for Nanoscale Wafer Level Packaged Circuits  
D.C. Keezer, J.S. Davis, S. Ang\* and M. Rotaru\* / *Georgia Institute of Technology, USA; \*National University of Singapore, Singapore*
- 1625hrs C3.2 A Novel Twisted Differential Line for High-speed On-chip Interconnections with Reduced Crosstalk  
D.G. Kam, S. Ahn, S. Baek, B. Park, M. Sung and J. Kim / *KAIST, Korea*
- 1650hrs C3.3 Serial Test Interface: A Novel Architecture for Self-Tests of ASICs  
A.A. Kokrady and D. Khanna / *Texas Instruments, India*
- 1715hrs C3.4 Over GHz Frequency Model of Commercial 2mm Hard Metric Connector using On-board Calibration Standards  
S. Baek, B.C. Park, D.G. Kam and J. Kim / *KAIST, Korea*

**DAY 2: 12 DECEMBER 2002, THURSDAY****Session D1 - IA3: MANUFACTURING TECHNOLOGIES**Chairman: James How, *Motorola Electronics*

- 0845hrs D1.1 Rework and Reliability of QFP and BGA Lead-Free Assemblies  
H.G. Sy, P. Arulvanan and P.A. Collier / *Singapore Institute of Manufacturing Technology, Singapore*
- 0910hrs D1.2 Study of Surface Topography in Nanometric Ductile Cutting of Silicon Wafers  
K. Liu, X.P. Li, M. Rahman, X.D. Liu\* and L.C. Lee\* / *National University of Singapore, Singapore; \*Singapore Institute of Manufacturing Technology, Singapore*
- 0935hrs D1.3 Yield Estimation for BGA Assembly  
S.S. Phadnis, K. Srihari and V. Yamunan\* / *State University of New York at Binghamton, USA; \*Texas Instruments, USA*
- 1000hrs D1.4 Statistical Process Control for Solder Deposition and Yield Enhancement  
R. Muthaiyan, V. Barba\* and K. Srihari / *State University of New York at Binghamton, USA; \*Endicott Interconnect Technologies, USA*

**Session D2 - AP2: MODULES AND INTEGRATION**Chairman: Rao Tummala, *Georgia Institute of Technology, USA*

- 0845hrs D2.1 The Development of Enhanced Wafer Level Packaging  
W.C. Lo, L.C. Shen, S.M. Chang, Y.C. Chen, H.T. Hu, J.R. Lin, K.C. Chen and Y.J. Hwang / *APC/ERSO/ITRI, Taiwan*
- 0910hrs D2.2 Integration of Passive and Active Components into Build-Up Layers  
A. Ostmann, A. Neumann\*, J. Auersperg, C. Ghahremani, G. Sommer, R. Aschenbrenner and H. Reichl\* / *Fraunhofer Institute for Reliability and Microintegration, Germany; \*Technical University of Berlin, Germany*
- 0935hrs D2.3 Design and Fabrication of High Aspect Ratio Fine Pitch Interconnects for Wafer Level Packaging  
A.O. Aggarwal, P.M. Raj, R. J. Pratap, A. Saxena and R.R. Tummala / *Georgia Institute of Technology, USA*

1000hrs D2.4 Wafer Level Encapsulation - A Transfer Molding Approach to System in Package Generation  
T. Braun, K.-F. Becker, M. Koch, V. Bader, U. Oystermann, D. Manassis, R. Aschenbrenner and H. Reichl / *Fraunhofer Institute of Reliability and Micro integration, Germany*

**Session D3 - TE1: ELECTRICAL PERFORMANCE AND SIGNAL INTEGRITY**

Chairman: M. Swaminathan, *Georgia Institute of Technology, USA*

- 0845hrs D3.1 Impact of Meshed Ground Planes on Broadband Performance of LTCC  
A.C.W. Lu, W. Fan, L.L. Wai and L. Jin / *Singapore Institute of Manufacturing Technology, Singapore*
- 0910hrs D3.2 Effects of Process Variation on Signal Integrity for High Speed Differential Signaling on Package Level  
S. Ahn, A.C.W. Lu\*, W. Fan\*, L.L. Wai\* and J. Kim / *KAIST, Korea; \*Singapore Institute of Manufacturing Technology, Singapore*
- 0935hrs D3.3 An Asymptotic FEM Analysis for the Electromagnetic Modeling of Interconnects and Integrated RF Passives for SiP and SoC Designs  
T.V. Yioultis, L.B. Proekt and A.C. Cangellaris / *University of Illinois at Urbana-Champaign, USA*
- 1000hrs D3.4 Investigation of Plane-to-Plane Noise Coupling Through Cutout on Multi-layer Power/Ground Planes  
J. Lee, M.S. Yeo\*, M.K. Iyer\* and J. Kim / *KAIST, Korea; \*Institute of Microelectronics, Singapore*
- 1025hrs D3.5 A Hybrid Technique for System-Level Signal Integrity and EMC Assessment  
S. Grivet-Talocia, I.S. Stievano, I.A., Maio and F.G. Canavero / *Politecnico di Torino, Italy*

1050 – 1120 hrs COFFEE BREAK

1050 – 1200 hrs **Session P1: POSTER SESSION**

- P1.1 Analysis of a New BGA THB Failure and Study on its Mechanism  
K.H. Yip and M. Xue / *Infineon Technologies Asia Pacific, Singapore*
- P1.2 Time and Temperature Dependent Mechanical Characterization of Polyimide Materials in Electronic Packaging Application  
C.T. Kuo, M.C. Yip and K.N. Chiang / *National Tsing Hua University, Taiwan*
- P1.3 Design Optimization of Wire Bonding for High Frequency Applications  
A.C.W. Lu, W. Fan and L.L. Wai / *Singapore Institute of Manufacturing Technology, Singapore*
- P1.4 Electroless Plating of Copper and Nickel via a Sn-free Process on Dielectric SiLK<sup>®</sup> Surface  
W.H. Yu, E.T. Kang, K. G. Neoh, Y. Zhang, S.S. Ang and A.A.O. Tay / *National University of Singapore, Singapore*
- P1.5 Packaging Processes using Flip Chip Bonder and Future Directions of Technology Development  
H. Hatanaka / *Toray Engineering Co Ltd, Japan*
- P1.6 Use of Simulation to Improve the Kitting Process at an EMS Provider's Facility  
A. Joshi, S.S. Phadnis, K. Srihari and R. Seeniraj\* / *State University of New York at Binghamton, USA; \*Solectron Corporation, USA*

P1.7 Thermal Optimization of a Miniaturized Camera with Pentium PC Module  
F. Vogel, R. Köthe, Z. Stössel and A. Kiser / *University of Applied Sciences of Central Switzerland, Switzerland*

1200 – 1325hrs LUNCH

**Session E1 – IA2: INTERCONNECTS I**

Chairman: Wang Zhiping, *Philips MDS, China*

- 1325hrs E1.1 The Evaluation of Flip Chip Bumping on Cu/Low-k Wafer  
R.H. Uang, S.M. Chang, T.C. Chen, H.T. Hu, J.R. Lin, K.C. Chen, Y.J. Hwang / *APC/ERSO/ITRI, Taiwan*
- 1350hrs E1.2 Investigation of Cr/Cu/Cu/Ni Under Bump Metallization for Lead-free Applications  
K.C. Chan, Z. W. Zhong\* and K.W. Ong / *MicroFab Technology, Singapore; \*Nanyang Technological University, Singapore*
- 1415hrs E1.3 Bump & Assembly Technologies For Sub-100 Micron Pitch Flip Chip  
C.E. Bauer and F.J. Wu\* / *TechLead Corporation, USA; \*Chipbond Technology Corporation, Taiwan*
- 1440hrs E1.4 Development of Core-Less Substrate for Multi Wiring Layers  
M. Maehara, I. Kato, S. Akimoto, T. Okuma, R. Iino and T. Tsukamoto / *Toppan Printing Co, Japan*
- 1505hrs E1.5 Non-metallurgical Bonding Technology with Super-narrow Gap for 3D Stacked LSI  
M. Umemoto, K. Tanida, Y. Tomita, Tatsuya and K. Takahashi / *ASET, Japan*

**Session E2 - TE3: PACKAGE THERMAL MODELING**

Chairman: John Chai, *Nanyang Technological University*

- 1325hrs E2.1 Transient Thermal Analysis Applied to an IC Package  
R. Mandal, B. Liu and Y.C. Mui / *Advanced Micro Devices, Singapore*
- 1350hrs E2.2 An Algorithm for the Direct Co-Simulation of Dynamic Compact Models of Packages with the Detailed Thermal Models of Boards  
M. Rencz, V. Szekely, A. Poppe and B. Courtois\* / *Budapest University of Technology and Economics, Hungary; \*TIMA Laboratories, France*
- 1415hrs E2.3 Parametric Studies on Temperature Drops in Bare Chip Cooling System  
T. Tomimura / *Kyushu University, Japan*
- 1440hrs E2.4 An Adaptable Compact Thermal Model for BGA Packages  
M. Xie, K.C. Toh and D. Pinjala\* / *Nanyang Technological University, Singapore; \*Institute of Microelectronics, Singapore*
- 1505hr E2.5 Thermal Methodology for Evaluating the Performance of Microelectronic Devices with Non-Uniform Power Dissipation  
T.J. Goh, K.N. Seetharamu\*, G.A. Quadir\* and Z.A. Zainal\* / *Intel Products, Malaysia; \*Universiti Sains Malaysia, Malaysia*

**Session E3 - MS2: MODELING AND SIMULATION II**

Chairman: Andrew Tay, *National University of Singapore*

- 1325hrs E3.1 On the Moduli of Viscoelastic Materials  
X.R. Zhang, J.H.L. Pang, X.Q. Shi\* and Z.P. Wang\* / *Nanyang Technological University, Singapore; \*Singapore Institute of Manufacturing Technology, Singapore*

- 1350hrs E3.2 Calibration of a Piezoresistive Stress Sensor in (100) Silicon Test Chips  
Z.W. Zhong, X. Zhang\*, B.H. Sim, E. H. Wong\*, P.S. Teo\* and \* / *Nanyang Technological University, Singapore; \*Institute of Microelectronics, Singapore*
- 1415hrs E3.3 Drop Impact Test – Mechanics & Physics of Failure  
E.H. Wong, K.M. Lim\*, N. Lee\*, S. Seah\*, C. Hoe\*\* and J. Wang\*\* / *Institute of Microelectronics, Singapore; \*National University of Singapore, Singapore; \*\*Worley Advanced Analysis, Singapore*
- 1440hrs E3.4 Three Dimensional Finite Element Simulation of Wire Looping Process in Wirebonding  
B.H. Ng, A.A.O. Tay and S.H. Ong\* / *National University of Singapore, Singapore; \*National Semiconductor, Singapore*
- 1505hrs E3.5 Predicting Optimal Process Conditions for Flip-Chip Assembly Using Copper Column Bumped Dies  
H. Lu and C. Bailey / *University of Greenwich, UK*

1530 – 1600 hrs COFFEE BREAK

**Session F1 – IA1: INTERCONNECTS II**

Chairman: Mui Yew Cheong, *Advanced Micro Devices*

- 1600hrs F1.1 Direct Au and Cu Wire Bonding on Cu/Low-k BEOL  
P. Banda, H.M. Ho, C. Whelan, W. Lam\*, C.J. Vath III\* and E. Beyne / *IMEC, Belgium; ASM Technology, Singapore*
- 1625hrs F1.2 Fine Pitch Copper Wire Bond Process Development for Dual Damascene Cu Metallized Chips  
M. Sivakumar, V. Kripesh, L.A. Lim\* and M. Kumar\* / *Institute of Microelectronics, Singapore; \*ASM Technology, Singapore*
- 1650hrs F1.3 Process Development for Ultra Low Loop Reverse Wire Bonding on Copper Bond Pad Metallization  
V.P. Ganesh, M. Sivakumar / *Institute of Microelectronics, Singapore*
- 1715hrs F1.4 Fabrication of Fine Wiring Structure by Electrodeposited Polyimide for High Density Packaging and Interconnection  
K. Tokoro\*, H. Nakagawa\*, K. Kikuchi\*, E.S. Jung\*, S. Segawa\*, H. Itatani\* and M. Aoyagi\* / *\*National Institute of Advance Industrial Science & Technology (AIST), Japan; ^PI R&D Co, Japan*

**Session F2 - TE4: THERMAL MANAGEMENT**

Chairman: Chan Poh Keong, *DSO National Laboratories*

- 1600hrs F2.1 Thermal Analysis of IC Package Burn-in Subrack  
N. Khan, D. Pinjala, M.K. Iyer, B. Liu\*, R. Mandal\* and Y.C. Mui\* / *Institute of Microelectronics, Singapore; \*Advanced Micro Devices, Singapore*
- 1625hrs F2.2 Single Current Source Tj Control  
V. Yap, C. Naravane and C.S. Beh / *Advanced Micro Devices, Singapore*
- 1650hrs F2.3 Optimization of Thermal Management Techniques for Low Cost Optoelectronic Packages  
L. Xie, D. Pinjala, K. Sudharsanam, R. Pamidighantam and E. Ishimura\* / *Institute of Microelectronics, Singapore; \*Mitsubishi Electric Corporation, Japan*
- 1715hrs F2.4 Direct Liquid Cooling of a Stacked Multichip Module  
X.Y. Chen, K.C. Toh and J.C. Chai and D. Pinjala\* / *Nanyang Technological University, Singapore; \*Institute of Microelectronics, Singapore*

**Session F3 - MS1: MODELING AND SIMULATION I**

Chairman: Leo Ernst, *Delft University of Technology, The Netherlands*

- 1600hrs F3.1 C\*-parameter Approach to Low Cycle Fatigue Crack Growth of Solders  
C. Kanchanomai, Y. Miyashita\* and Y. Mutoh\* / *Thammasat University, Thailand; \*Nagaoka Univrsity of Technology, Japan*
- 1625hrs F3.2 Design Analysis of Solder Joint Reliability for Stacked Die Mixed Flip Chip and Wirebond BGA  
T.Y. Tee, M. Lim, H.S. Ng, X. Baraton, D. Kaire and Z.W. Zhong\* / *STMicroelectronics, Singapore; \*Nanyang Technological University, Singapore*
- 1650hrs F3.3 On the Effect of Cure-Residual Stress on Flip Chip Failure Prediction  
L.J. Ernst, D.G. Yang, K.M.B. Jansen, C. van't Hof, G.Q. Zhang\* and W.D. van Driel\* / *Delft University of Technology, The Netherlands; \*CFT/Philips, The Netherland*
- 1715hrs F3.4 Toward a Better Understanding of Morphology Changes in Solders Using Phase Field Theories: Quantitative Modeling and Experimental Verification  
D.S. Brodie, A.J. Gunn, W.H. Müller\* and R.L. Reuben / *Heriot-Watt University, Great Britain; \*Technische Universität Berlin, Germany*

1740 – 1800hrs **Outstanding Paper Award Presentation and Conference closing**

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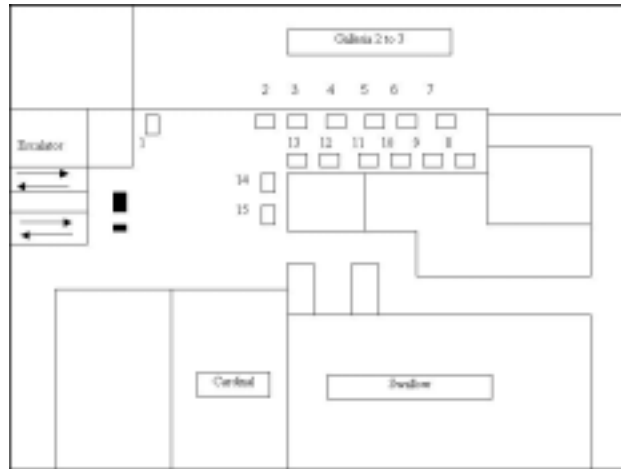
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Table No: 8

# EPTC 2002 TABLE-TOP EXHIBITION LAYOUT PLAN

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1	Infineon Technologies Asia Pacific
2	United Instruments Corporation
4	Bridge Semiconductor Corp.
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