Mixed-Signal Measurement Circuits For Embedded Test Access

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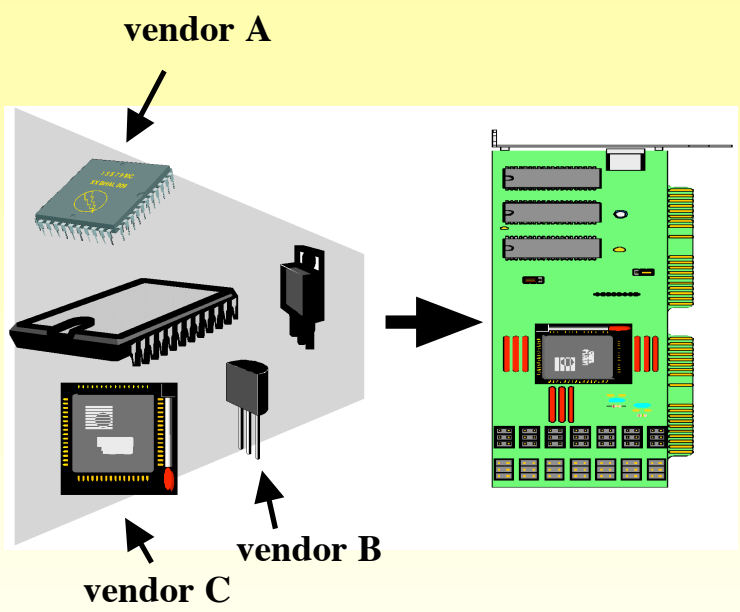
(Presently on leave with DFT MicroSystems)

October 26, 2003

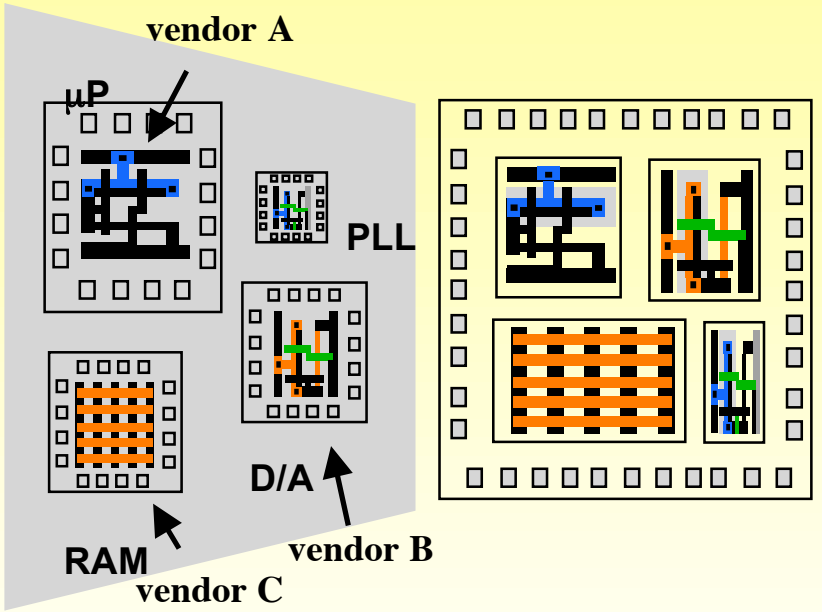
Outline

- Introduction
- On-Chip Instruments
  - Signal Generators
  - Sampling Oscilloscopes
  - Coherent Sampling Test System
  - Time Domain Reflectometry & Transmission
  - Timing Analyzers
- Conclusions

System On-A-Chip / In-A-Package



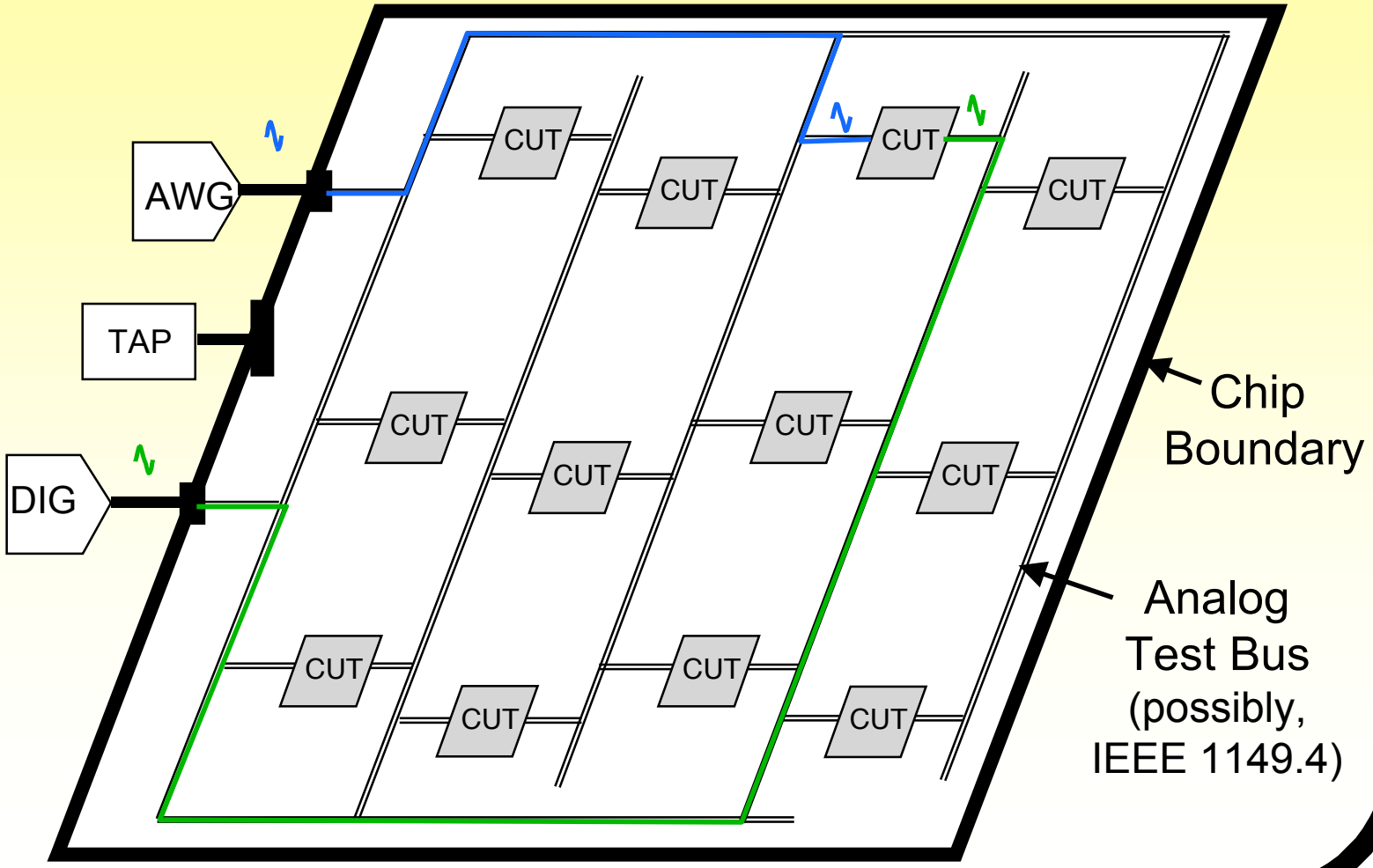
Component-Based Design



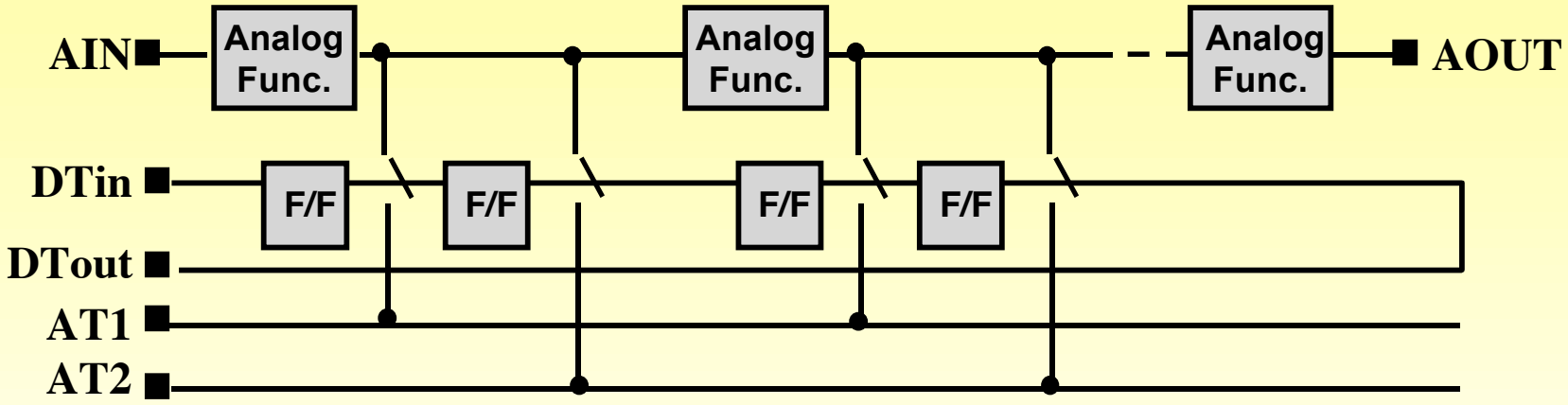
Core-Based Design

- ***More and more components are being integrated into smaller and smaller devices/packages.***
  - ***Gaining test access to ALL components is becoming increasingly more difficult.***

Embedded Test Capability

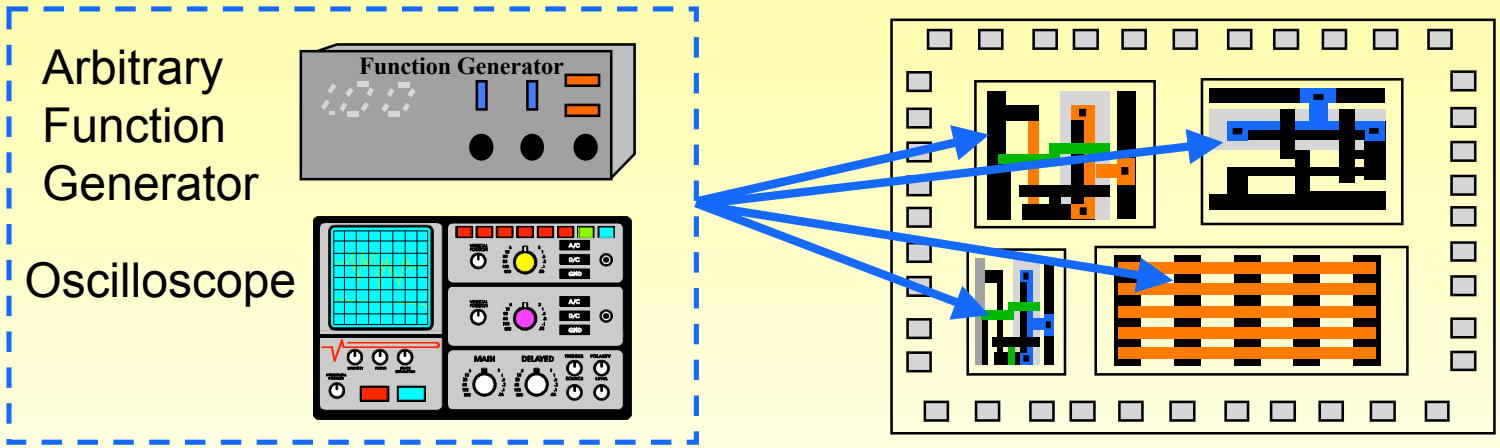


Test Bus / Test Ports



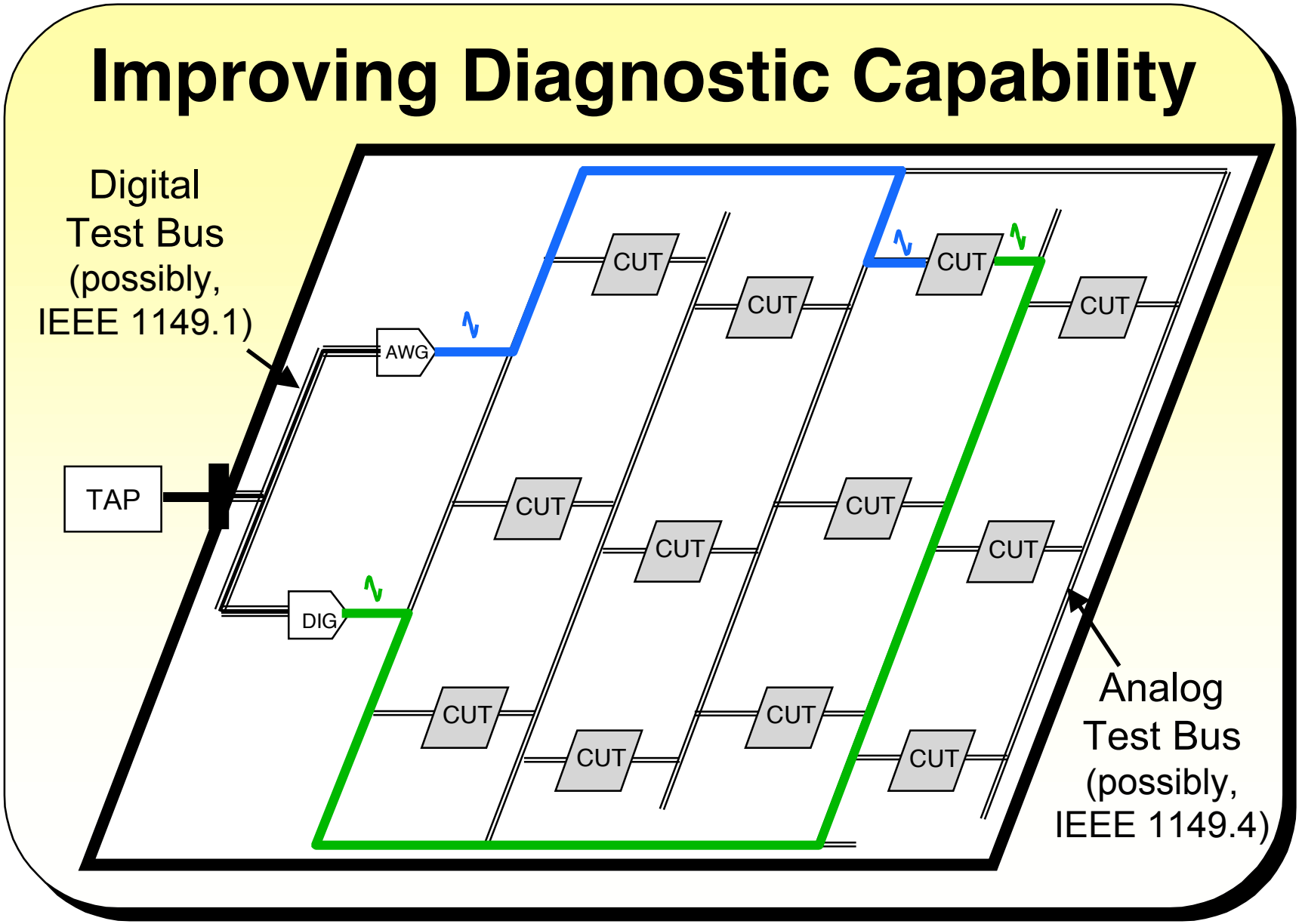
- A test bus provides **observability** and/or **controllability** of internal nodes on an IC/board/system.
- Standardizing the pins of the test port facilitates test set-up and program re-use.
  - IEEE industrial standard (IEEE 1149.4).
- Good analog switches are difficult to realize in advanced CMOS.

Moving Test Instruments Directly On-Chip

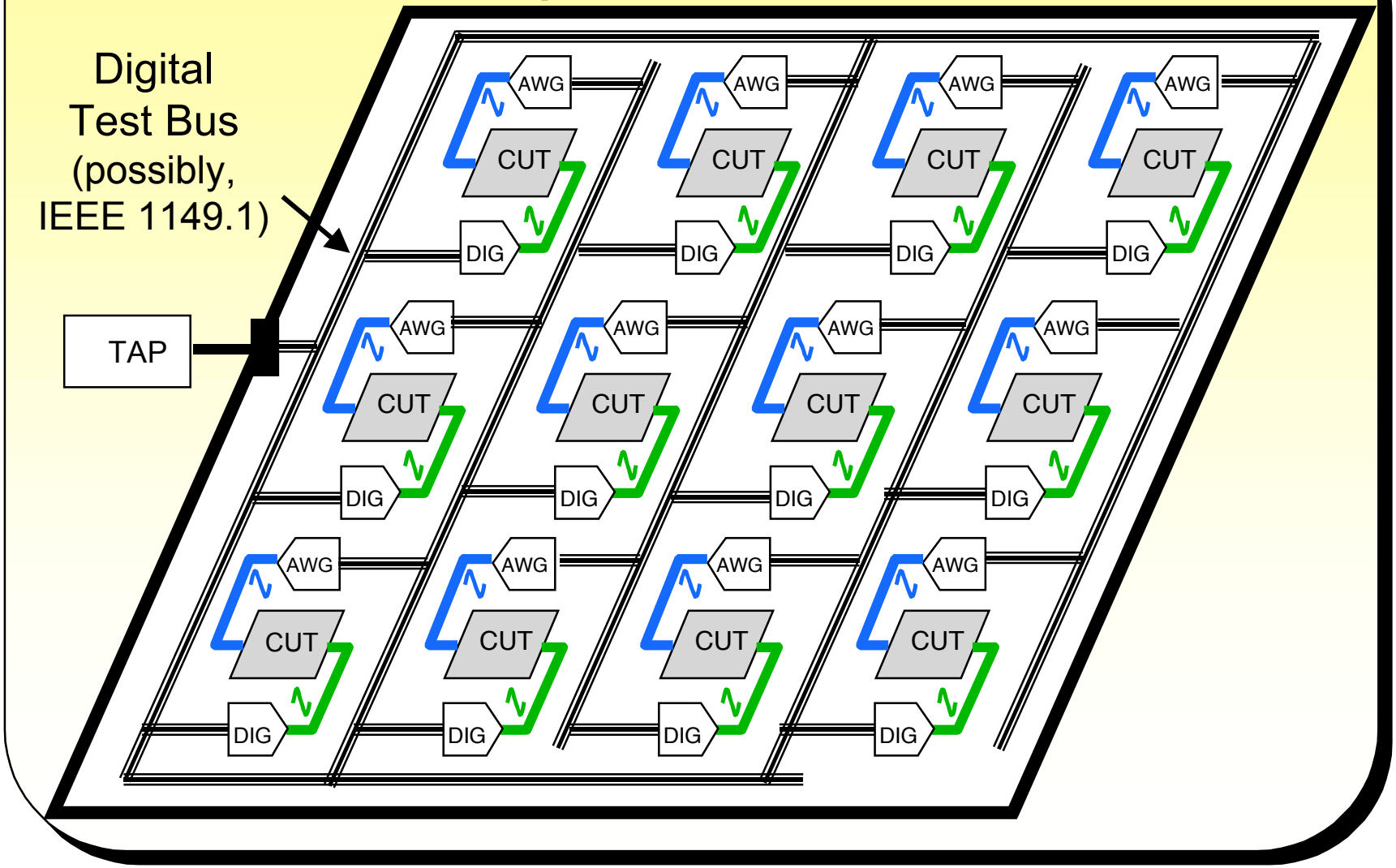


Move the test equipment to the signals-under-test rather than the signals to the test equipment!

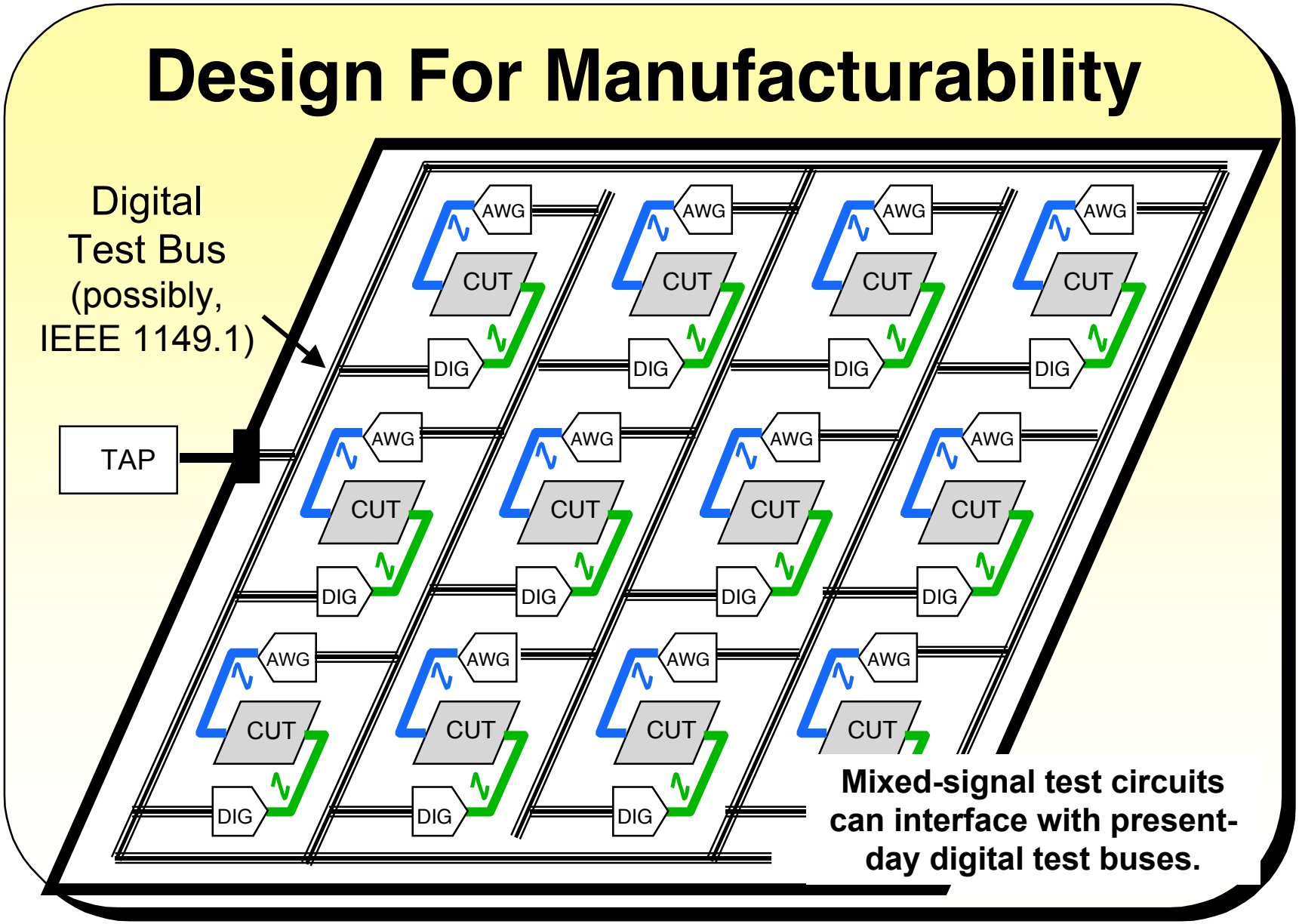
Improving Diagnostic Capability



Improving SOC Test Times



Design For Manufacturability



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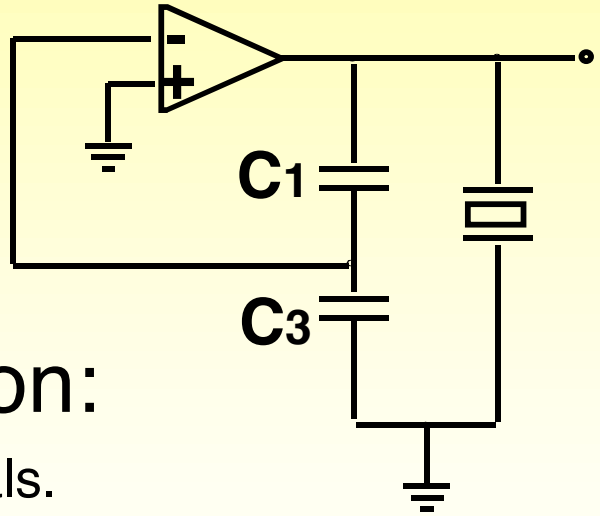
Analog Signal Generation

Conventional Analog Signal Generation:

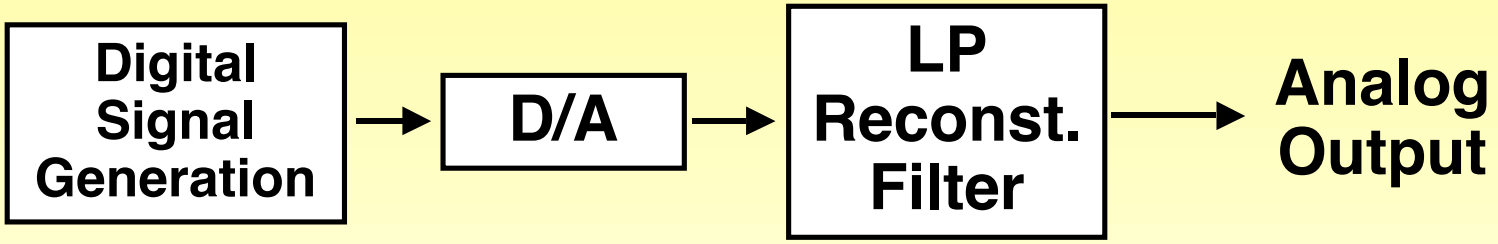
- Tuned oscillator circuits
- Relaxation oscillator circuits



Problem for On-Chip Solution:

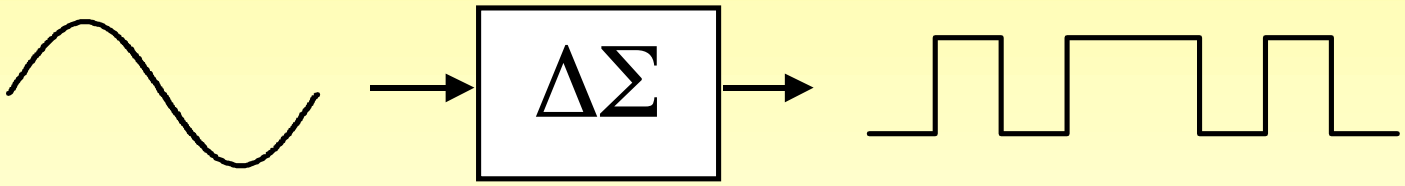
- Low-Q operation unless using crystals.
- Difficult to control amplitude, frequency and multi-tone signals.
- Frequency and amplitude sensitive to absolute value of components.

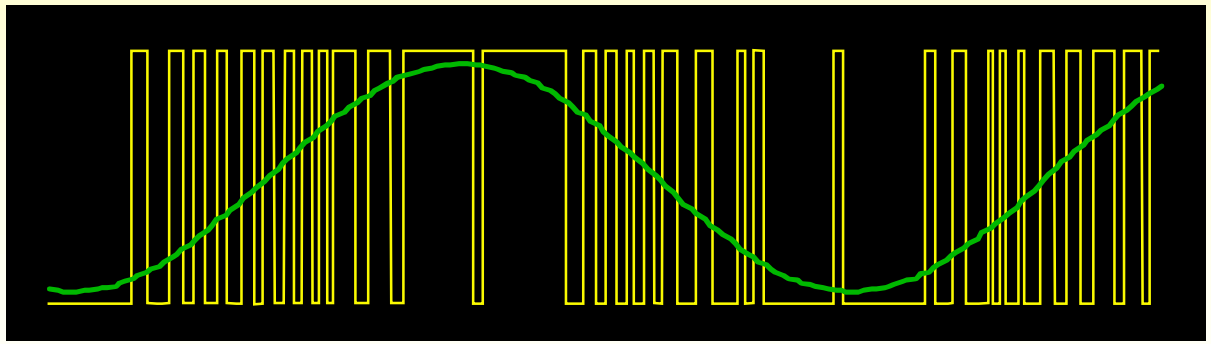
Analog Signal Generation
Using Direct Digital Frequency Synthesis



- A digital signal is numerically created and converted to analog form using a D/A circuit.
- Advantages:
  - Largely digital, stable signal generation and fully programmable (both amplitude and frequency).
  - Frequency set by system or external clock.
  - Coherent measurement system - fastest measurement
- Disadvantages:
  - Large silicon area requirement.

Data Conversion Using Delta-Sigma Modulation

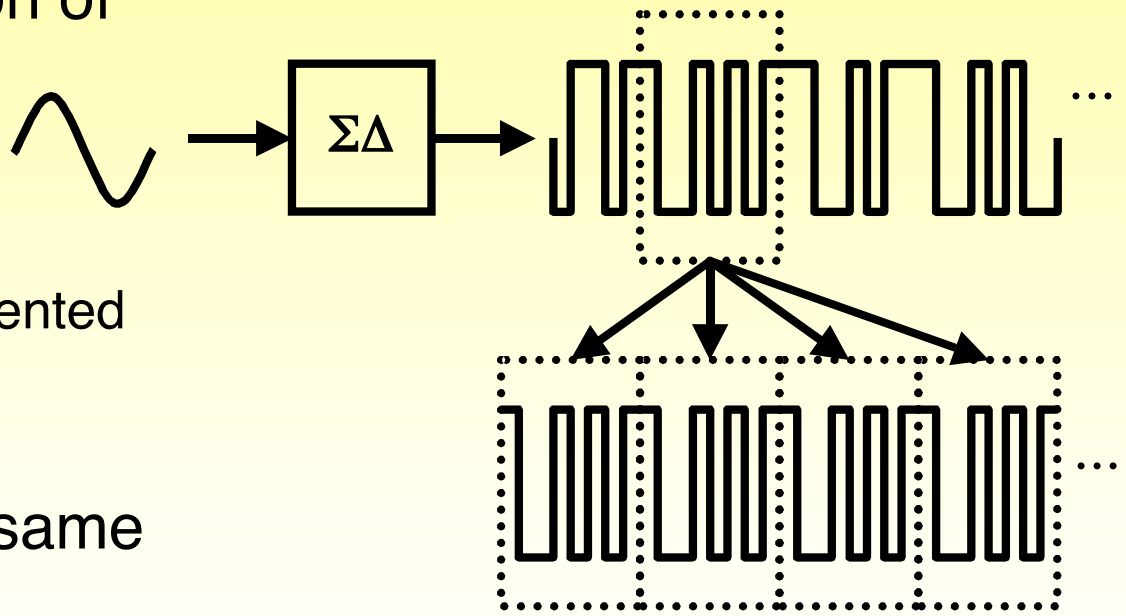




- Delta-sigma modulation converts multi-bit precision signals into a single-bit digital pattern
- Pulse Density Modulation, PDM

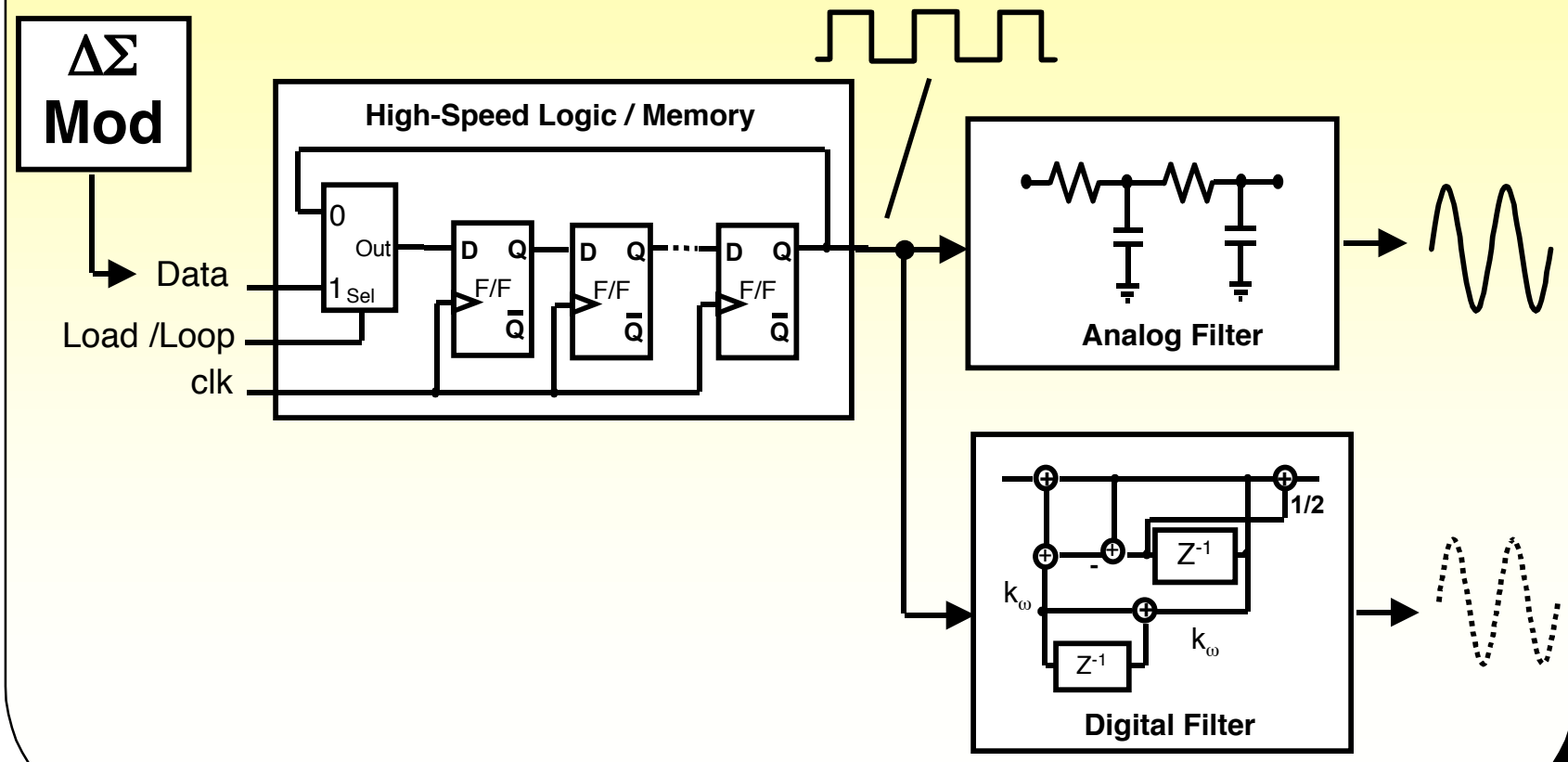
Single-Bit Generation

- Record a portion of a ΣΔ output
- Reproduce it periodically
  - Easily implemented
  - High speed
- Desired Tone, same Frequency and Amplitude as input

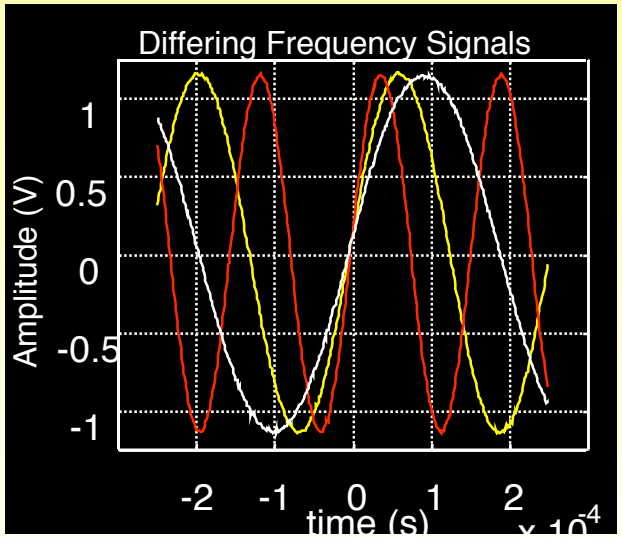


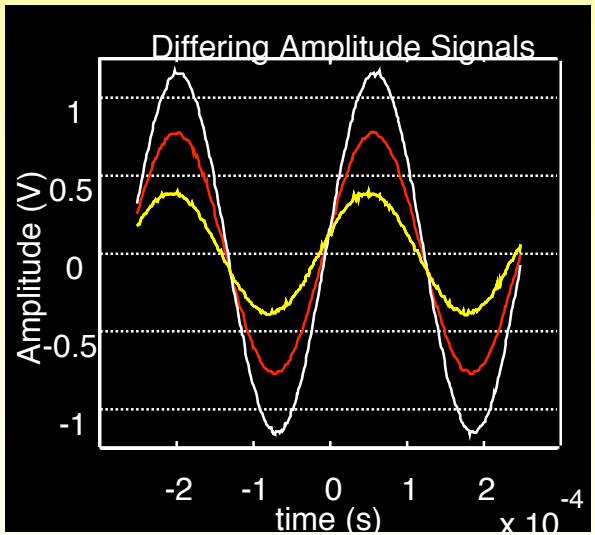
Scan-Chain Generator

Analog & Digital Signals



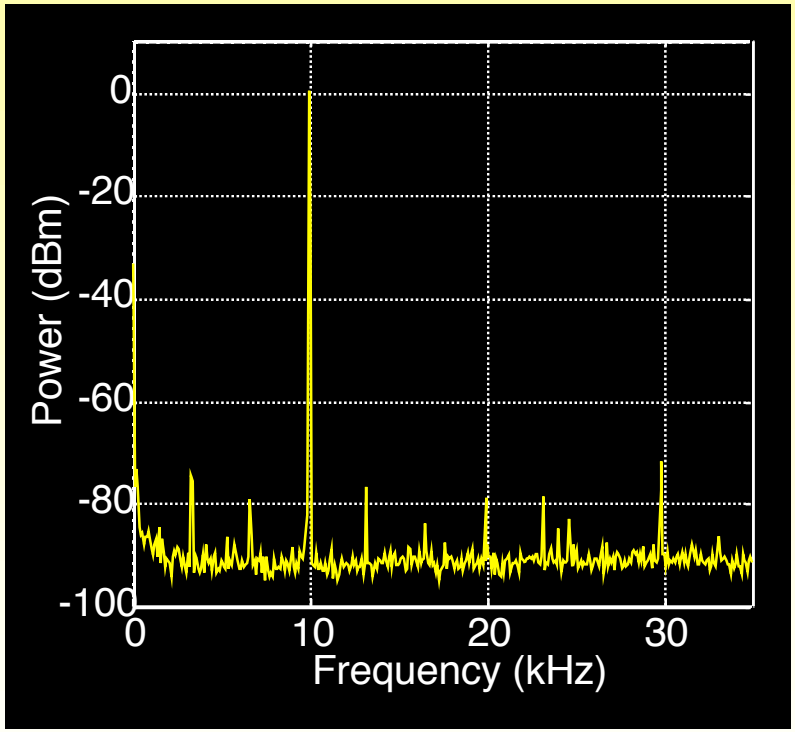
Signal Generation Equations



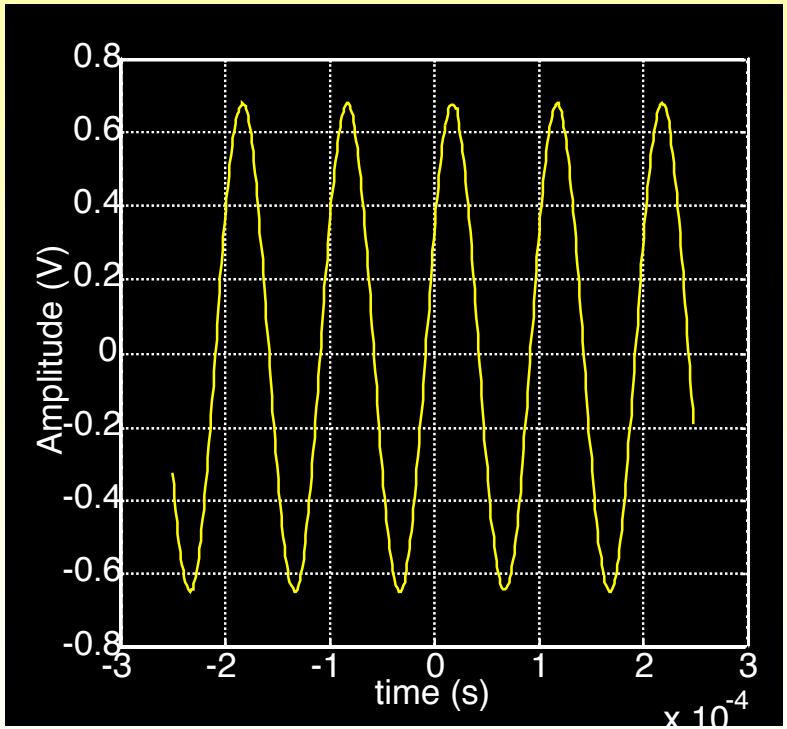


- Both frequency and amplitude of test signal can be controlled by changing the density of 1's and 0's in the digital pattern.

392-Bit Sine Wave



Power Density Spectrum

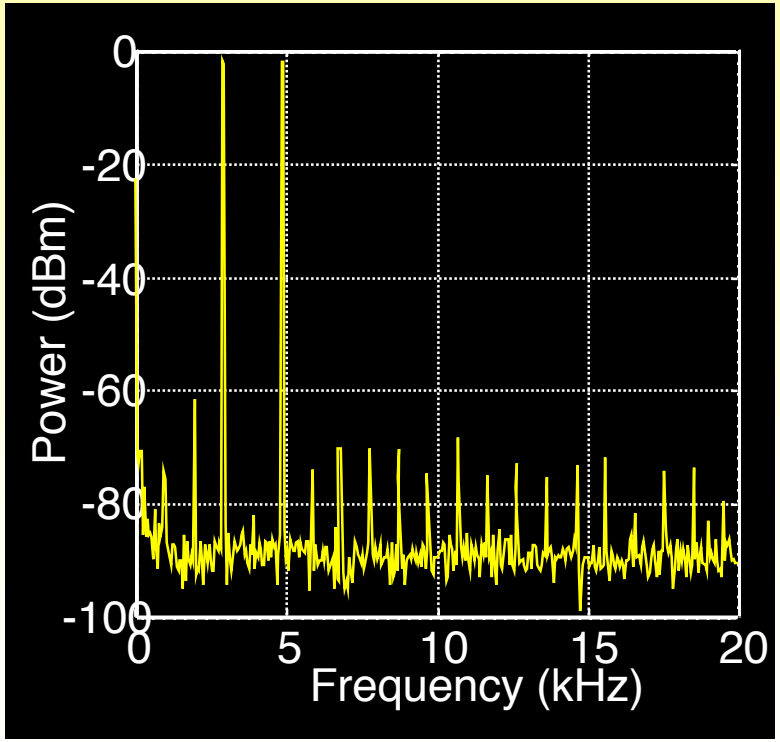


Oscilloscope Trace

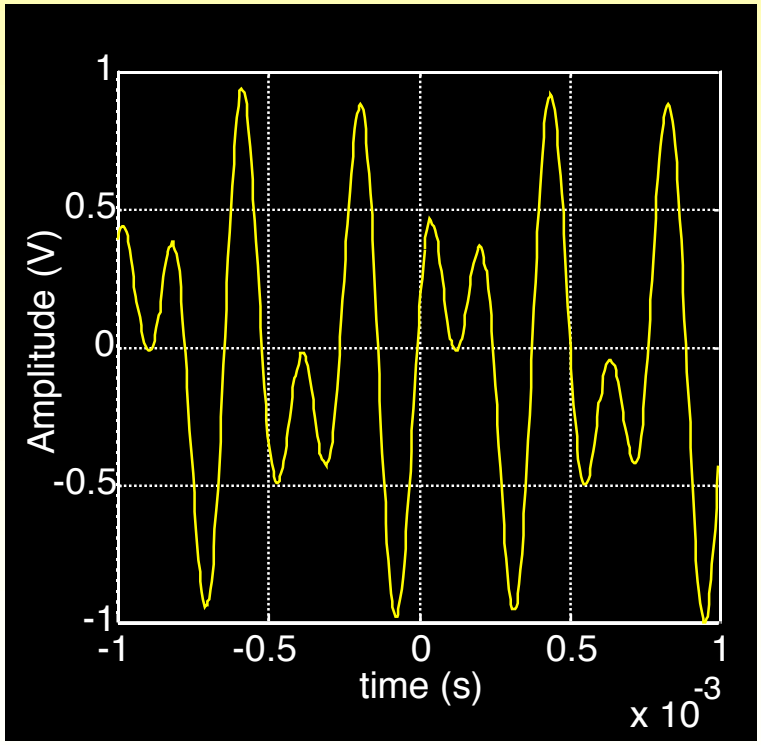
- Go to web-site http://www.macs.ece.mcgill.ca/~roberts/ to download other examples

Multi-Tone Waveform

Two-Tone Frequency Spectrum



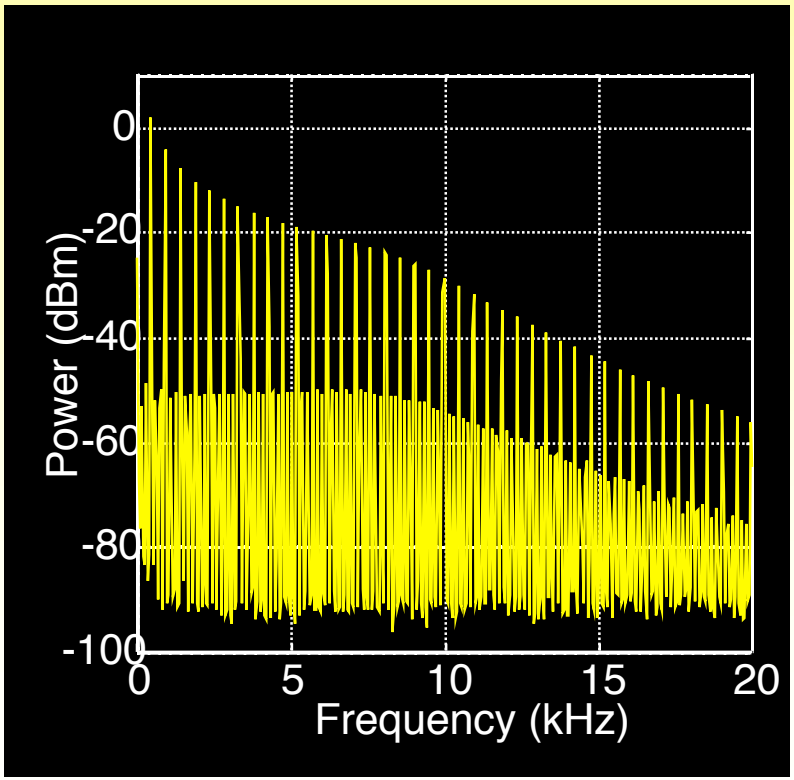
Two-Tone Oscilloscope Trace



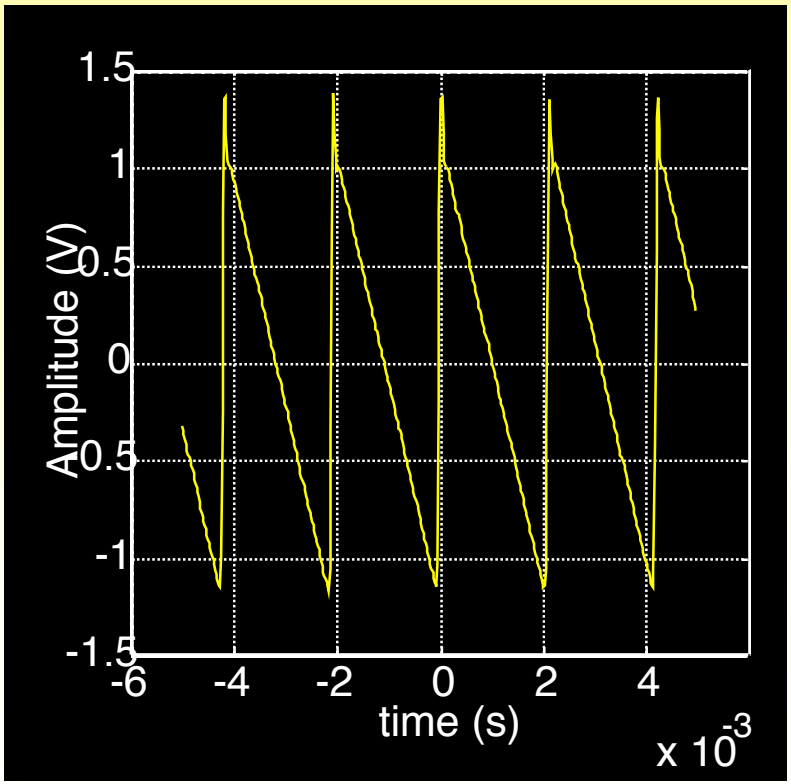
- example of a reconstructed two-tone signal

Sawtooth Waveform

Frequency Spectrum of Sawtooth



Scope Trace of Sawtooth



- 476 Hz sawtooth (infinite-tone) reconstruction

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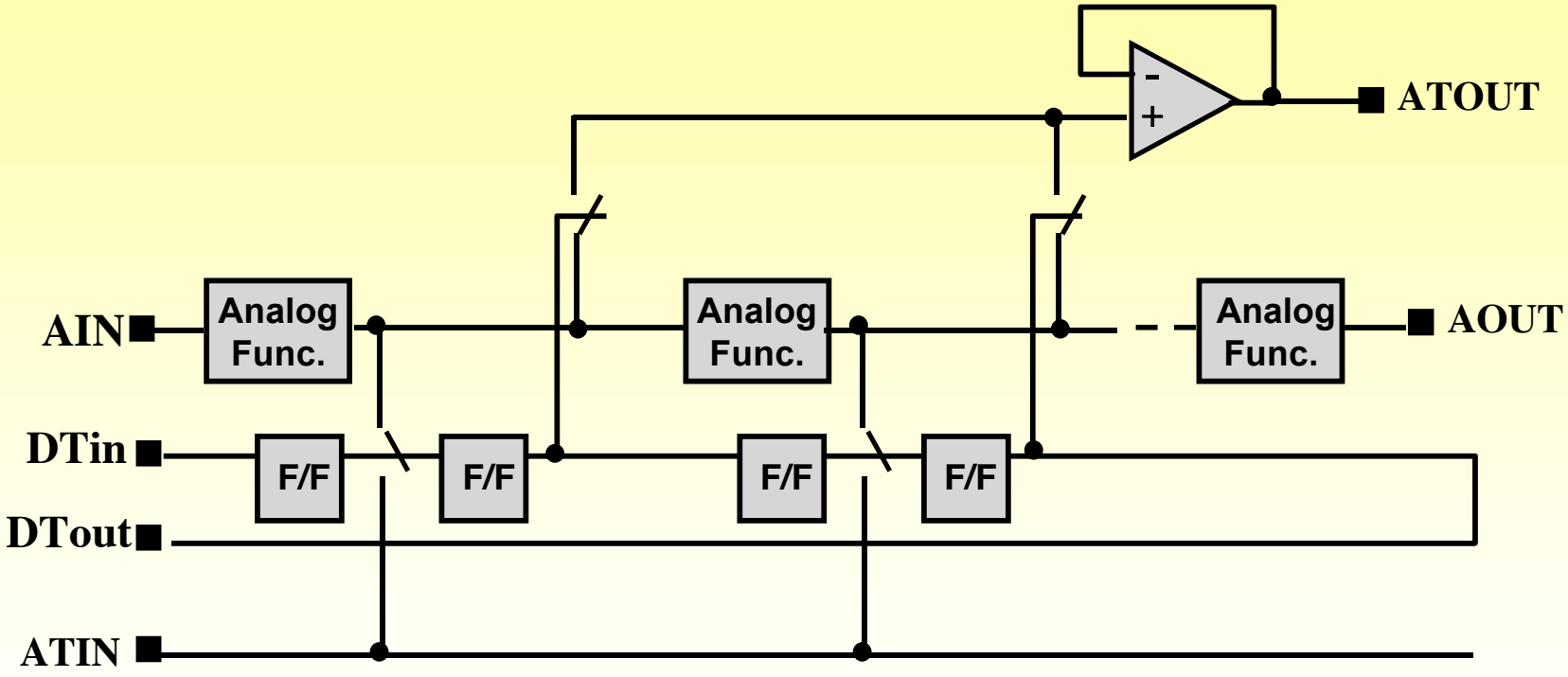
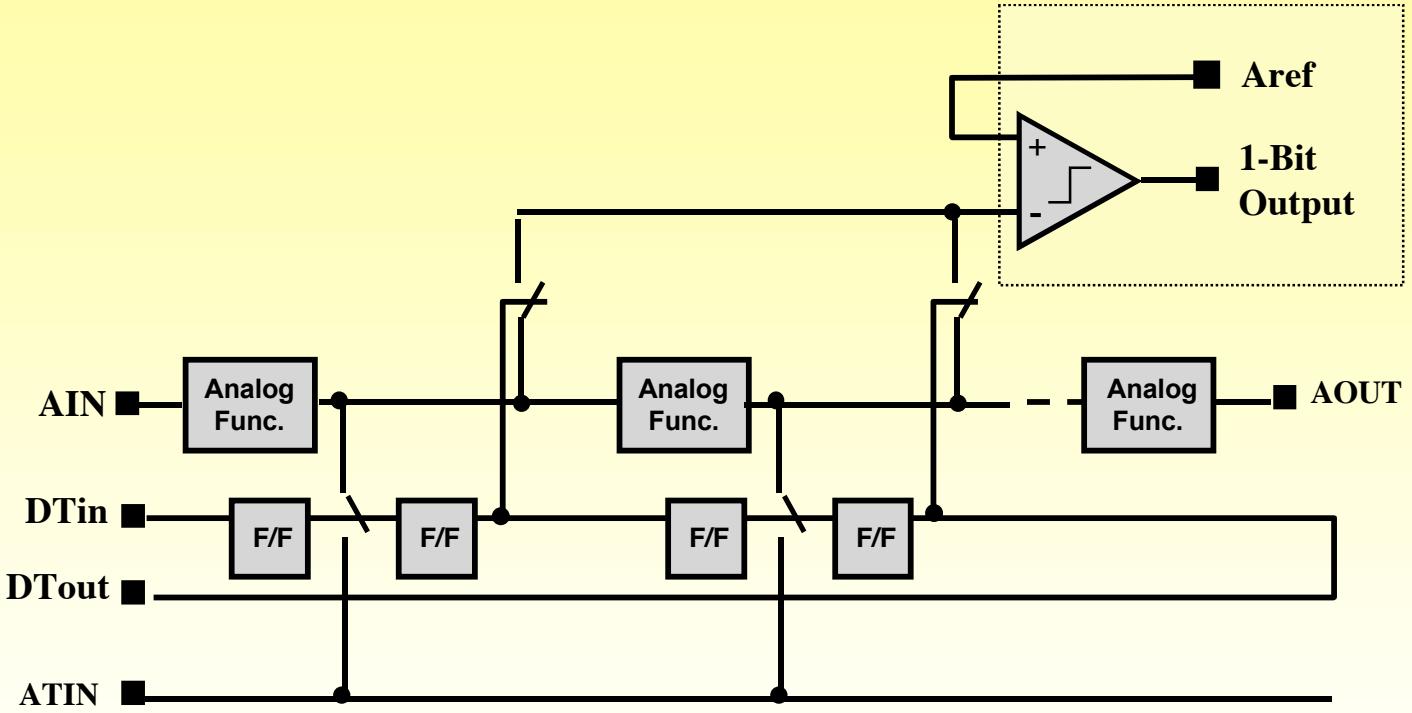
Test Bus With On-Chip Buffers



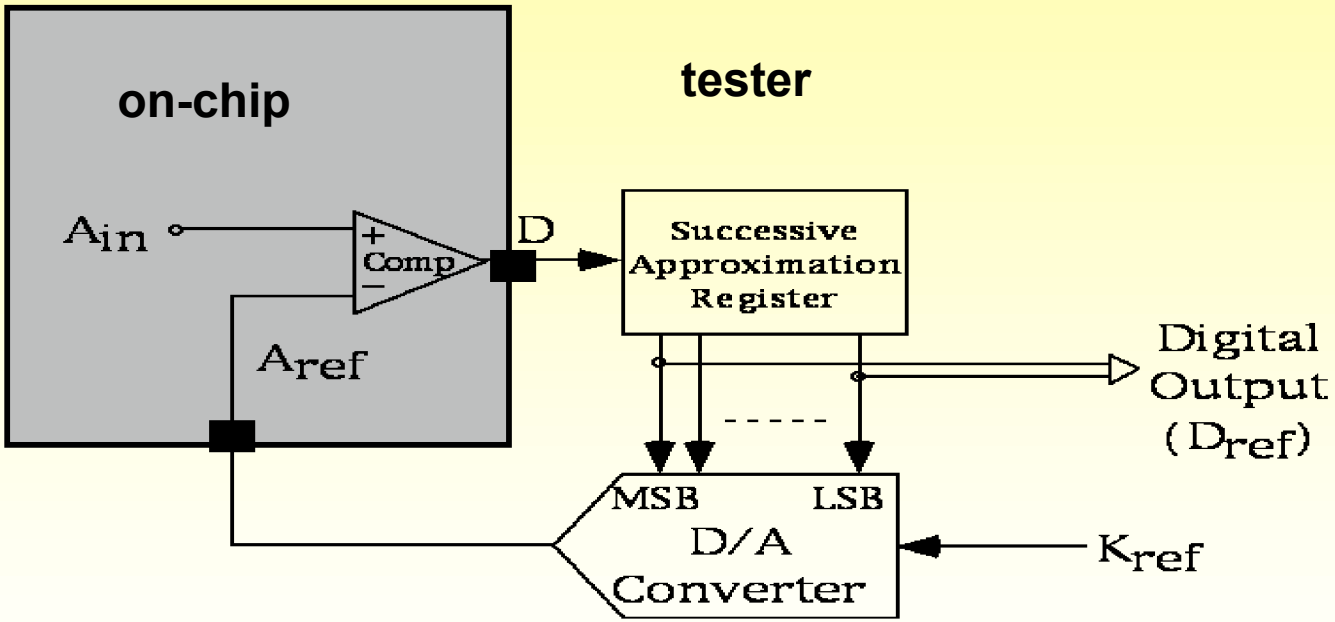
- A test bus often has an on-chip voltage buffer to drive off-chip loads.

Test Bus With On-Chip Comparator



- A test bus can be turn into a sampling oscilloscope by replacing the voltage buffer with a 1-bit comparator.
  - Only digital signals are moved across the chip boundary.

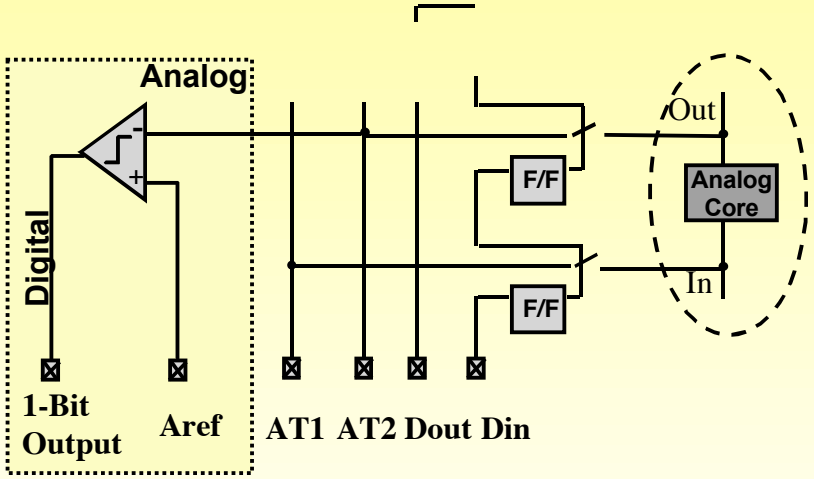
A/D Conversion Algorithm
(successive-approximation process)



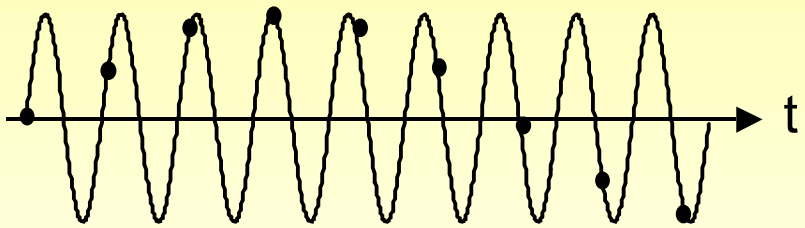
$$A_{in} = K_{ref}\left(\frac{b1}{2^1} + \frac{b2}{2^2} + \frac{b3}{2^3} + ... + \frac{bN}{2^N}\right)$$

On-Chip Oscilloscope

(High-Speed Signals Observed Using Subsampling)



Chip Configured for IEEE1149.1/1149.4 Test Bus



Subsampling Principle

- K. Lostrom, "Early capture for boundary scan timing measurements," Proc. of the International Test Conference, pp. 417-422, Oct. 1996.
- A. Hajjar and G. W. Roberts, International Test Conference, 1998.

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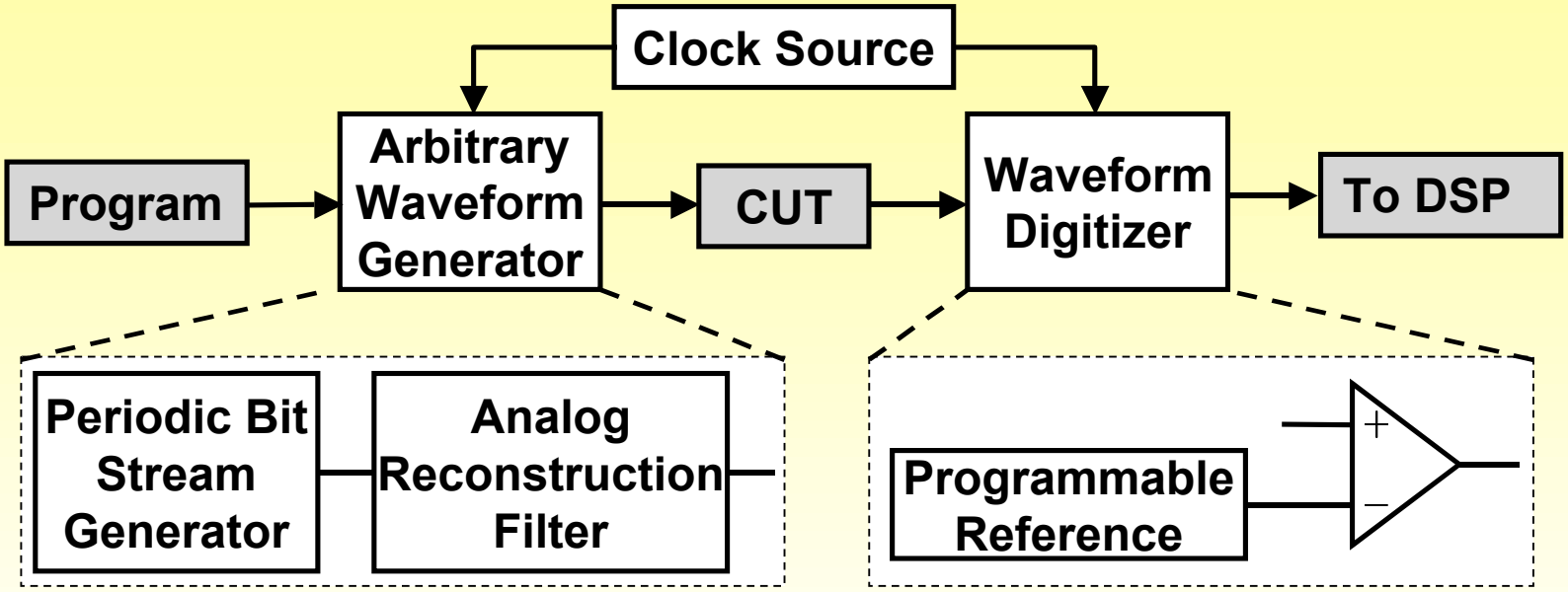
Coherent Test System

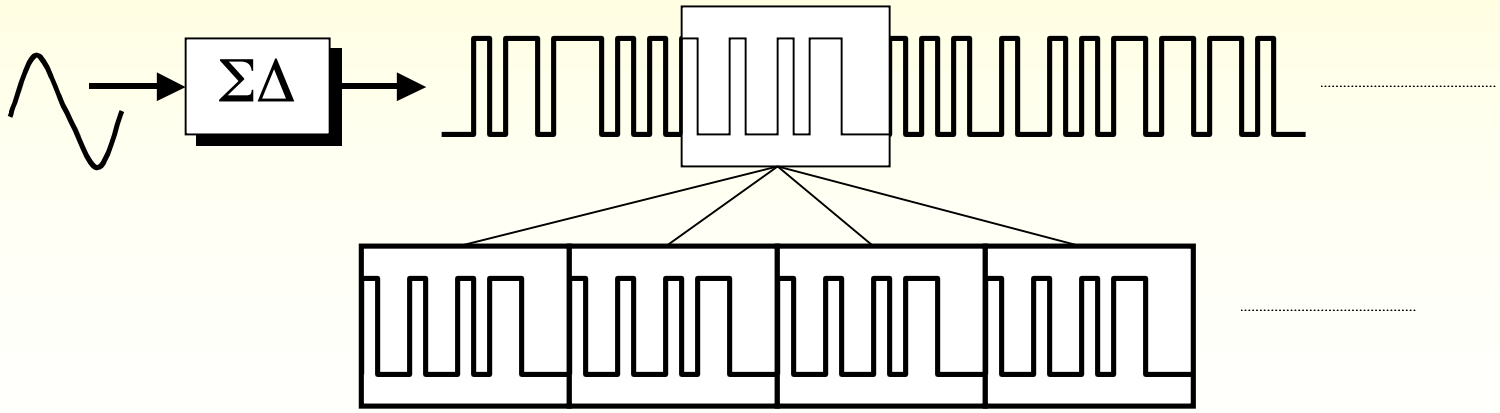


- Functional diagram identical to that of a generic DSP-based test system
- Unified clock guarantees coherence between the generation and measurement subsystems

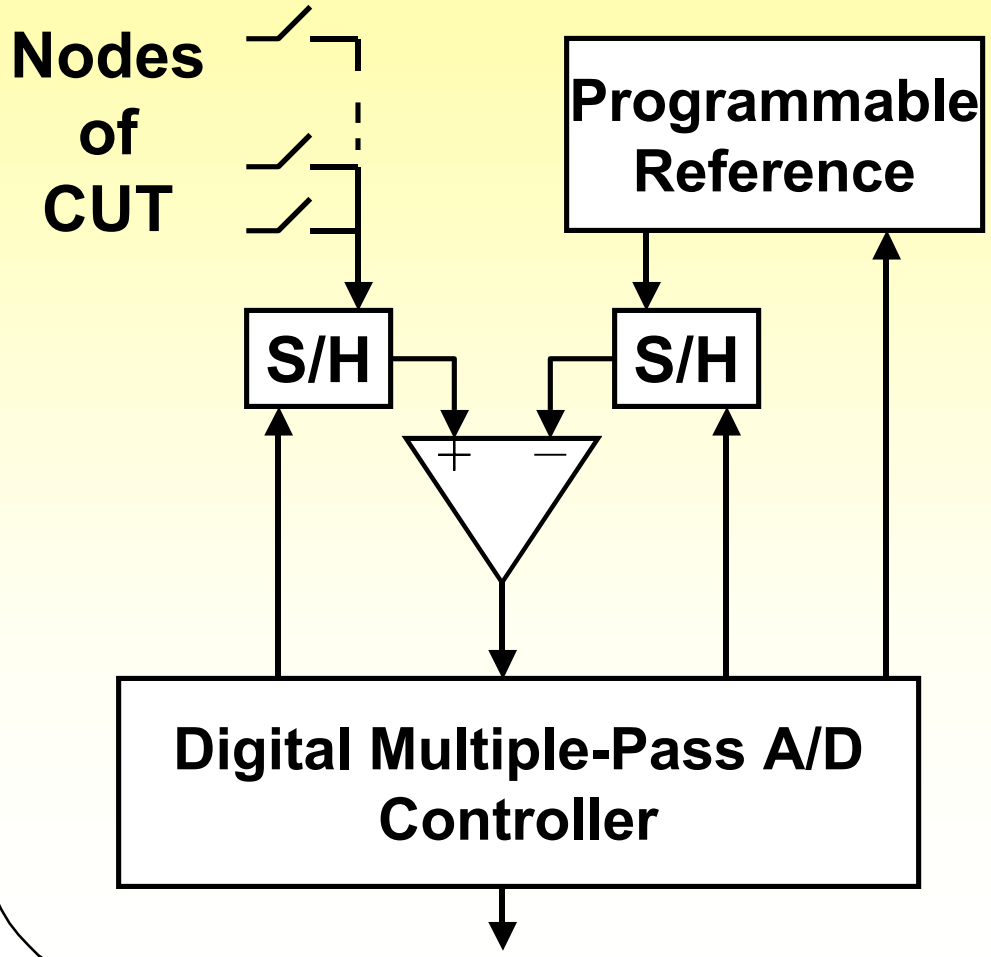
* M. Hafed, N. Abaskharoun and G. W. Roberts, "A 4 GHz Effective Sample-Rate Integrated Test Core for Analog and Mixed-Signal Circuits," IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, pp. 499-514, April 2002.

Signal Generation
Periodic ΔΣ Bit Stream Approach

- Output of ΔΣ modulator is approximated using a short repetitious sequence of bits
- Very short sequences demonstrate high spectral purity analog signals



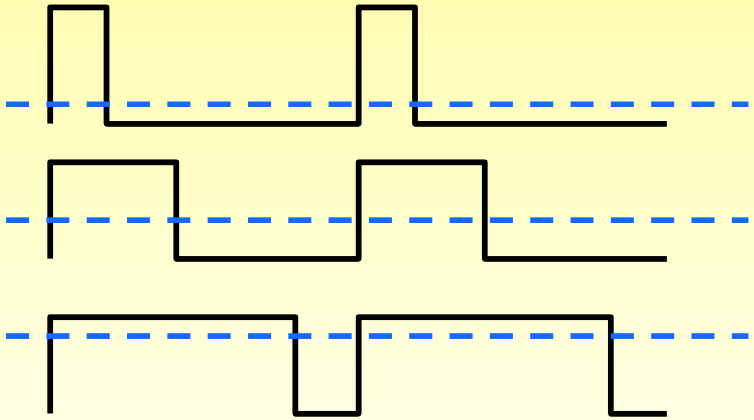
Waveform Digitizer
Implementation

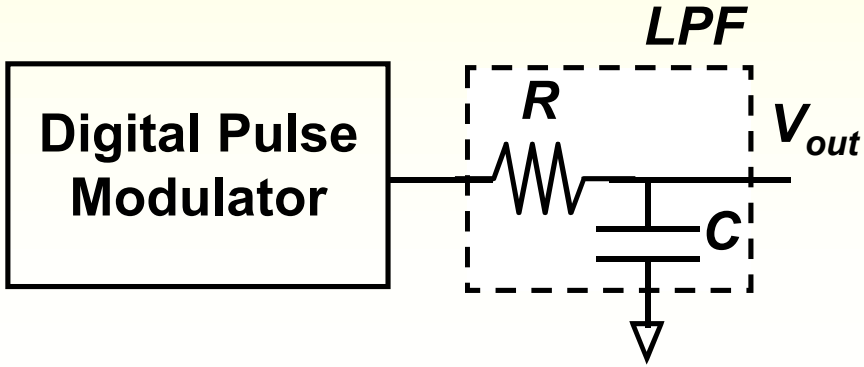


- No Specific requirements on comparator
- S/H decouples sampling rate from comparator conversion rate
- M. Hafed & G. Roberts ITC'2000

Programmable Reference Generator

- DC level is encoded in the average of a finite-length periodic digital bit sequence
- Passive on-chip filter achieves area efficiency, simplicity, and robustness



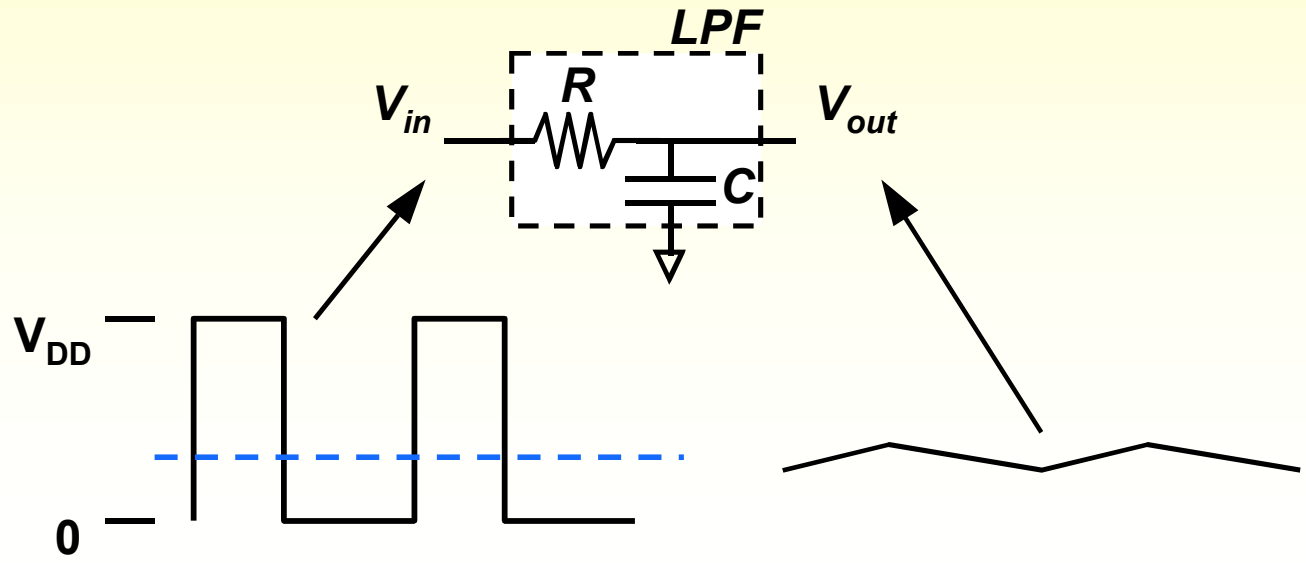


Passive Filtering

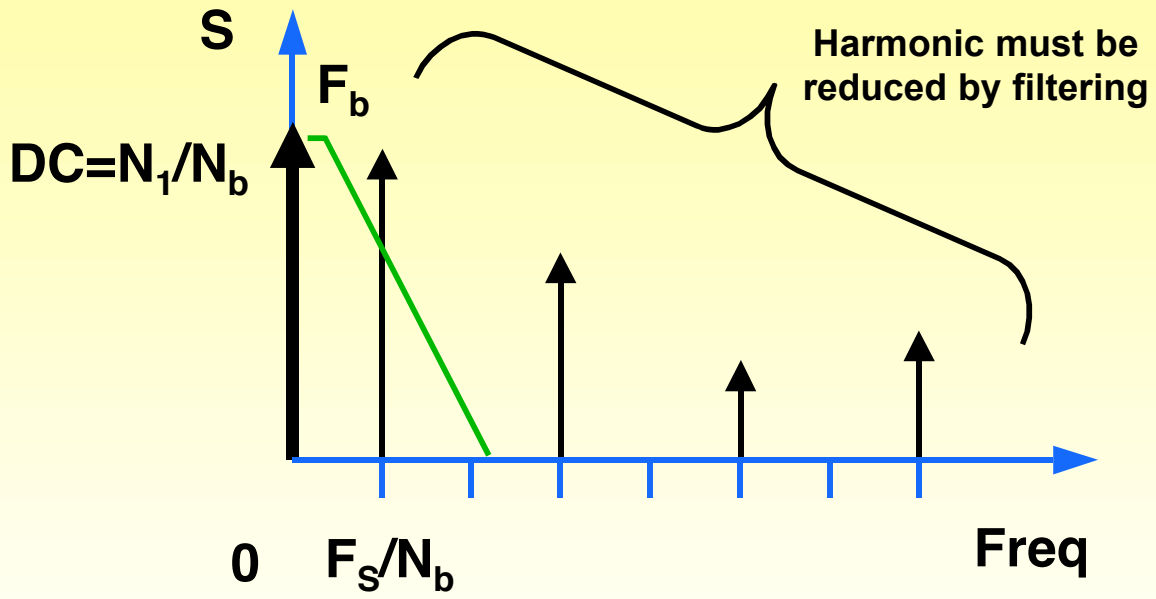
- Passive RC does not alter DC component regardless of the values of R and C:

$$\left|H(f)\right| = \frac{1}{\sqrt{1+\left(2\cdot\pi\cdot f\cdot R\cdot C\right)^2}}$$

- Filter trades off amplitude resolution (allowable ripple) versus speed (settling time)

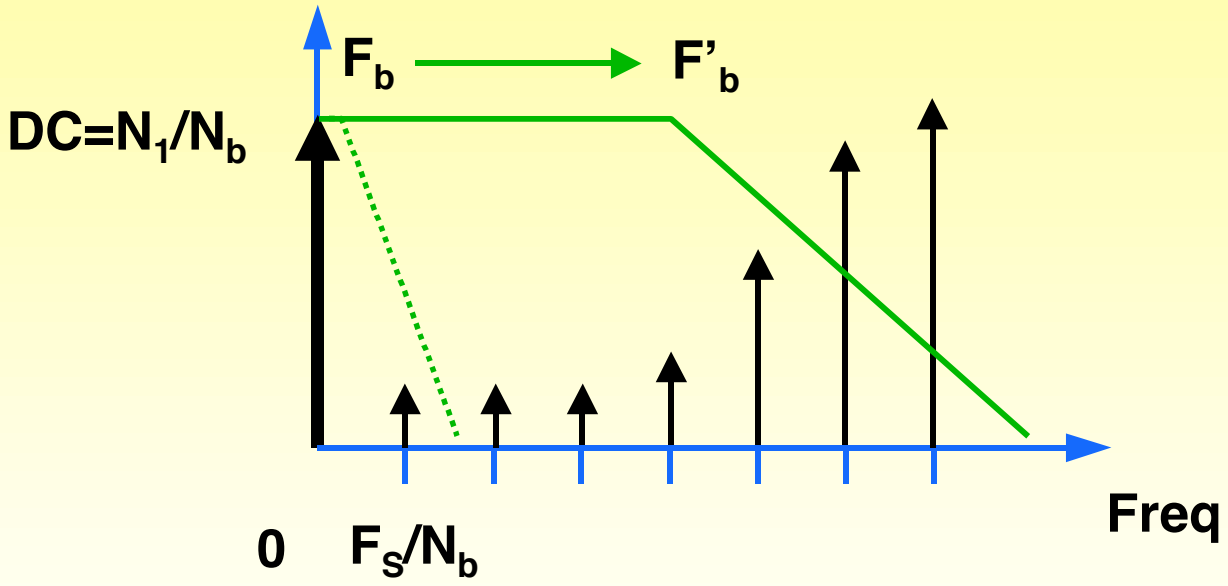


PWM Frequency Domain Description



- The DC tone has a magnitude which is dependent on the ratio of 1's (N_1) to the total number of bits in the digital periodic sequence (N_b).
- The magnitude and distribution of the AC harmonics depend on the sequence of 1's and 0's in the bitstream.

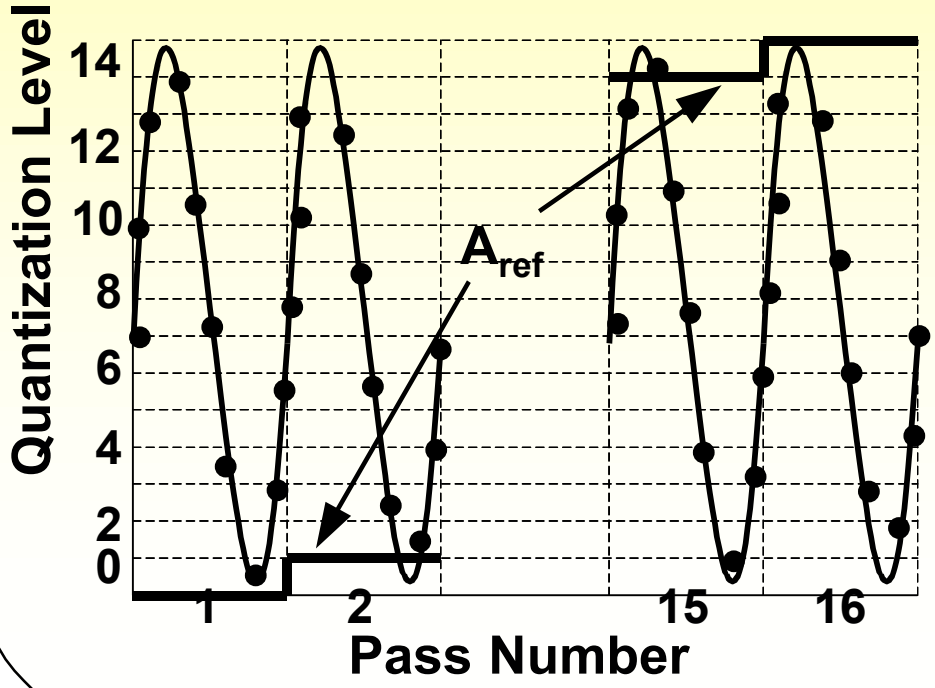
PDM Frequency Domain Description

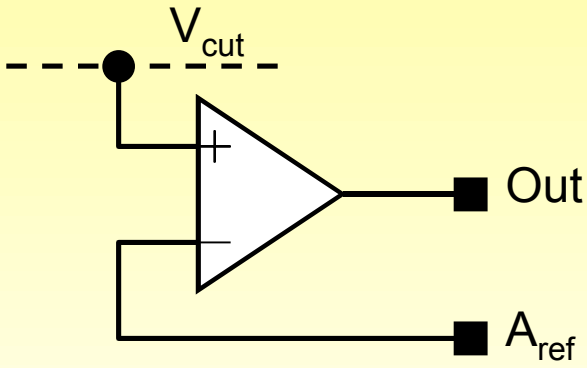


- Using Pulse Density Modulation (PDM) has the effect of pushing most of the harmonic power higher in frequency therefore alleviating the filter requirements.
- DC Patterns can be generated in the exact same way as for the AC signals.

Digitization Using On-Chip Comparators

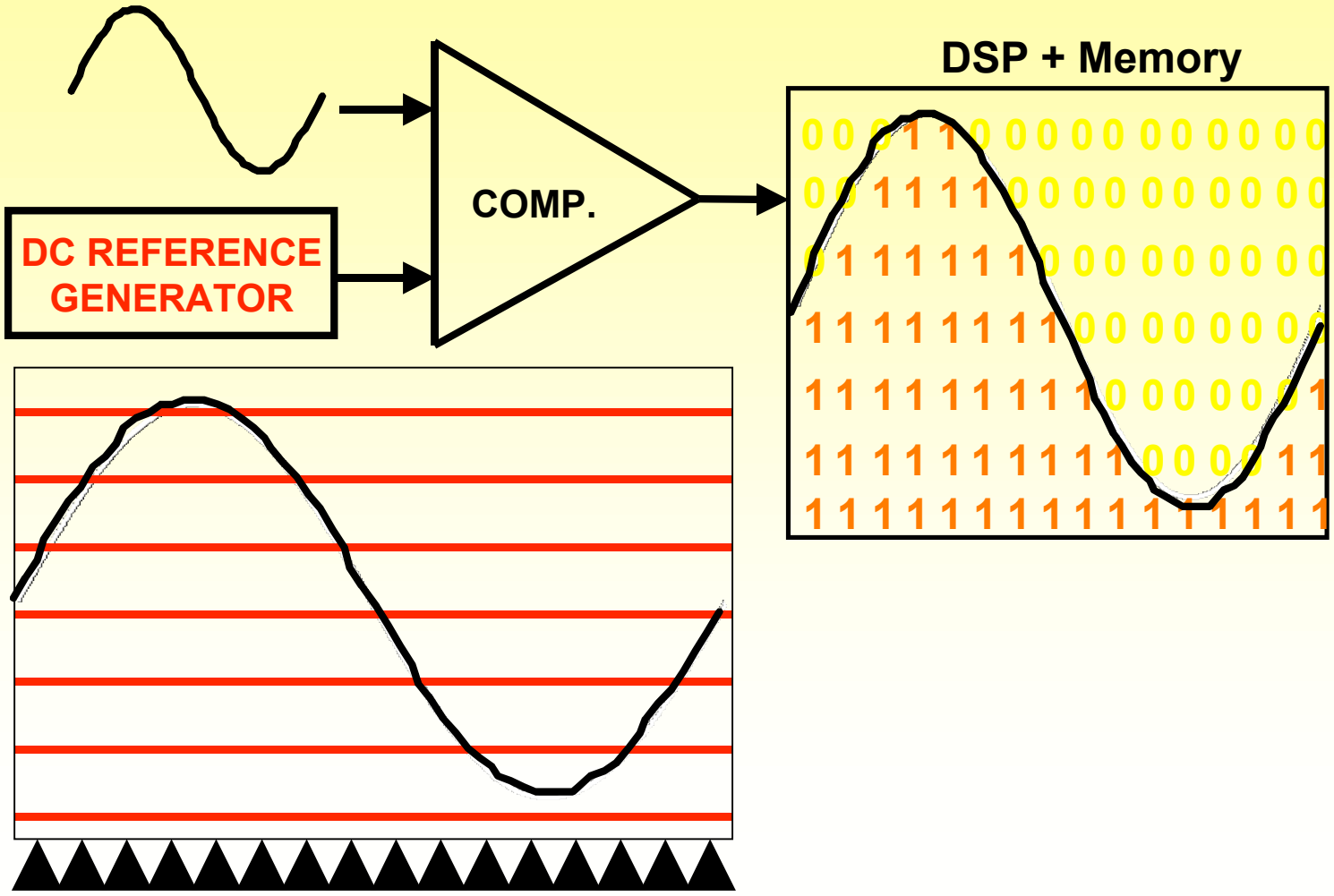
- A_{ref} is successively modified until the quantization level of the sample-under-test is determined



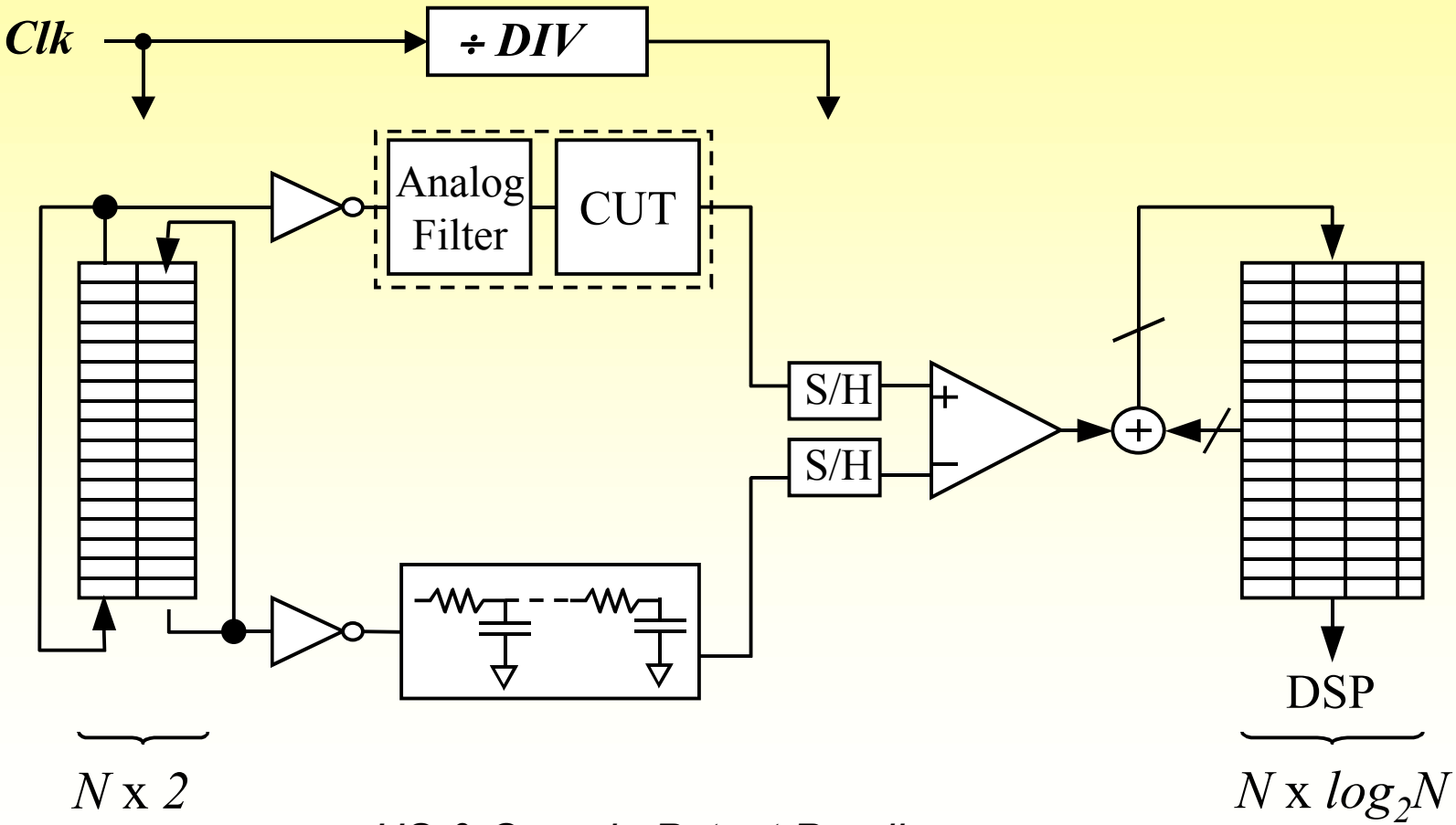


- Inherent sub-sampling operation means high effective sampling rate

Multipass Method



Almost All-Memory Implementation



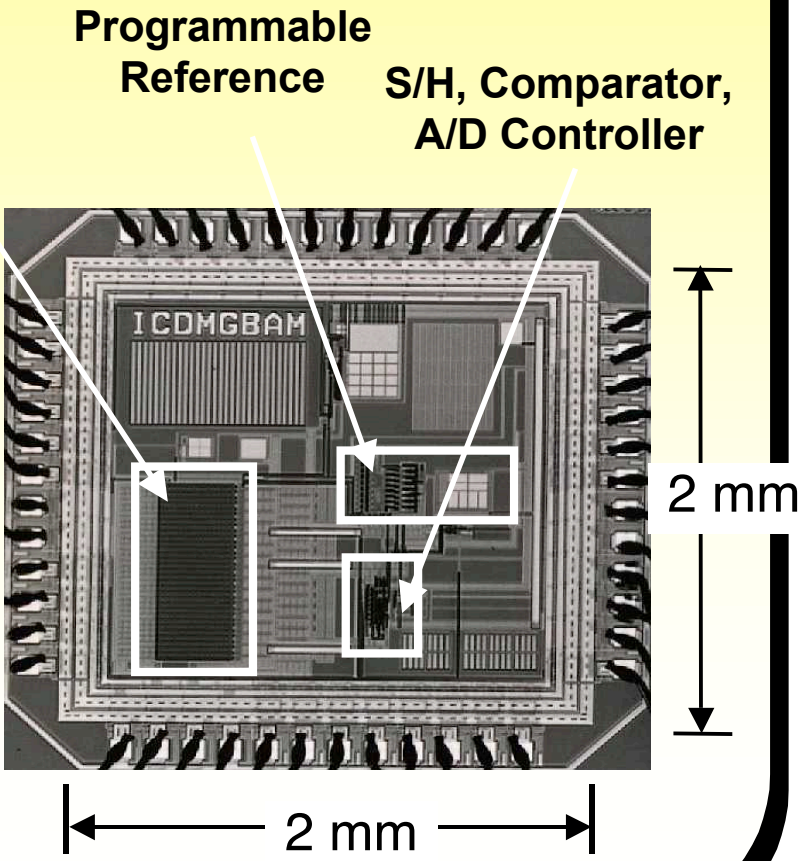
US & Canada Patent Pending

8-Bit, 4 GHz AWG & Digitizer

M. Hafed & G. Roberts CICC'2000, JSCC April 2002

Chip Details

- Technology: 0.35 um, 3.3 V CMOS
- Amplitude Resolution: 8 bits
- Effective Sampling Rate: 4 GHz
- Time resolution (off-chip): 200 ps
- SFDR: 65 dB @ 500 kHz
  40 dB @ 500 MHz

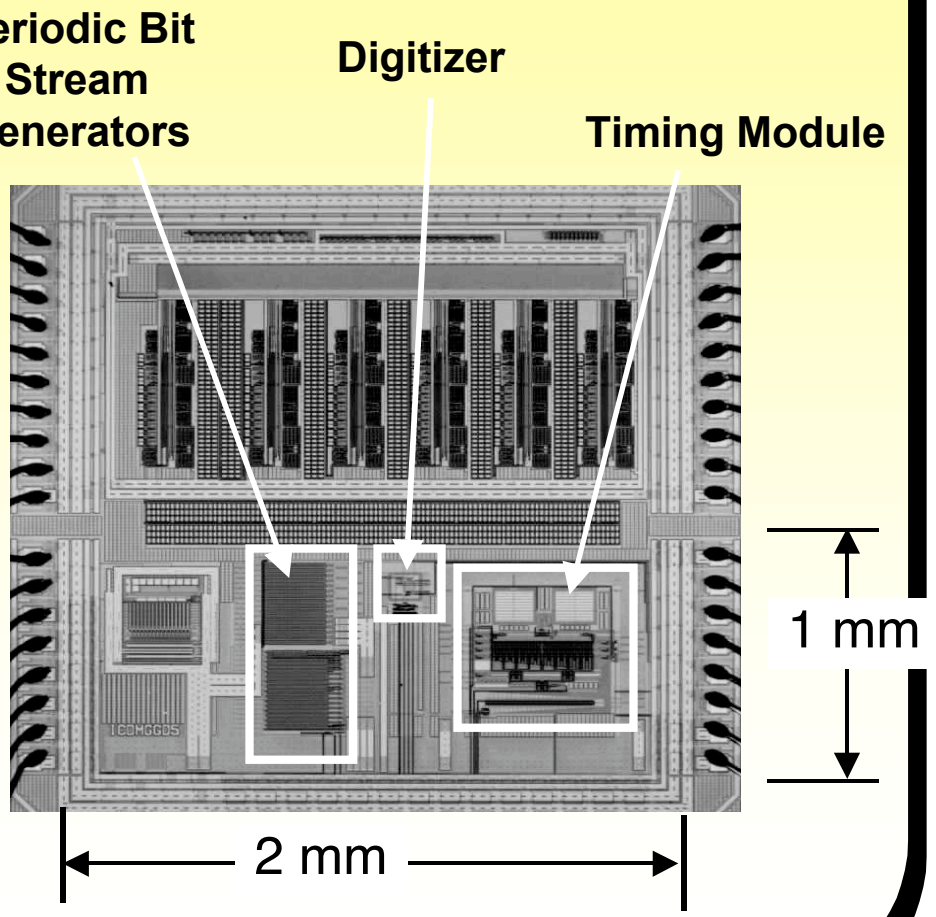


10-Bit, 4 GHz AWG & Digitizer

M. Hafed & G. Roberts / Wireless Test Workshop 2001

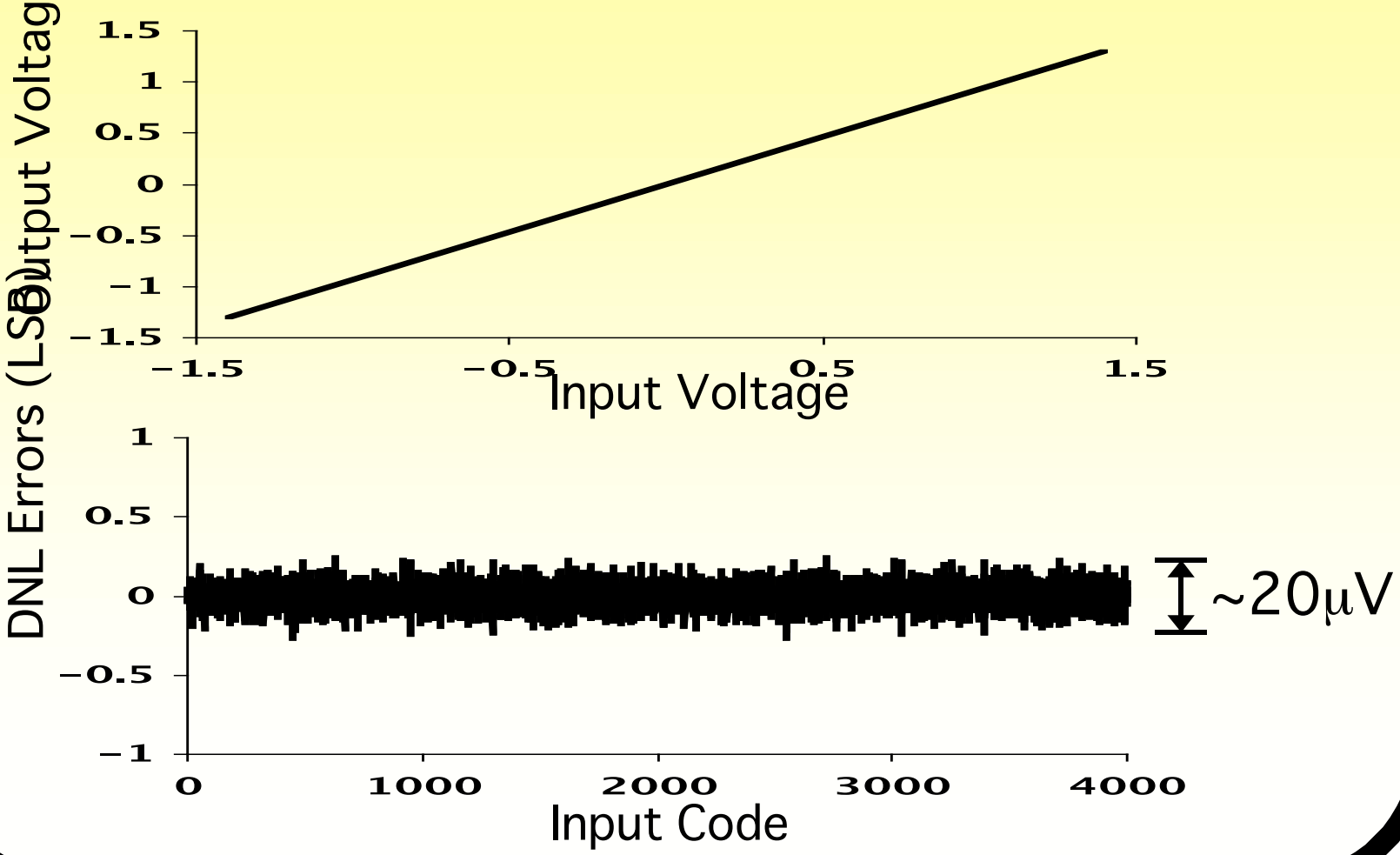
Chip Details

- **Technology: 0.35 um, 3.3 V CMOS**
- **Amplitude Resolution: 10 bits**
- **Effective Sampling Rate: 4 GHz**
- **Time resolution (on-chip): 200 ps**
- **SFDR: 65 dB @ 500 kHz**
  40 dB @ 500 MHz



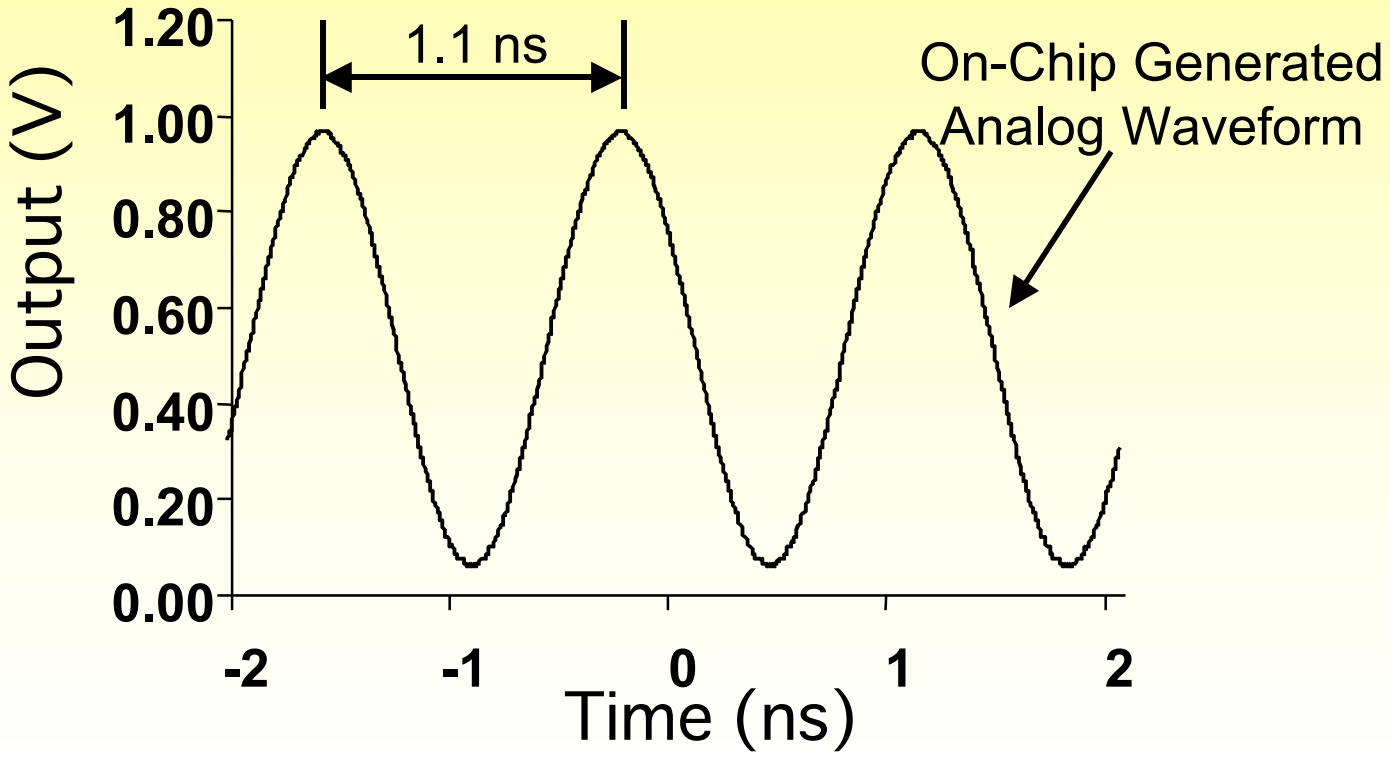
Measured Performance

Curve-Tracer Functionality



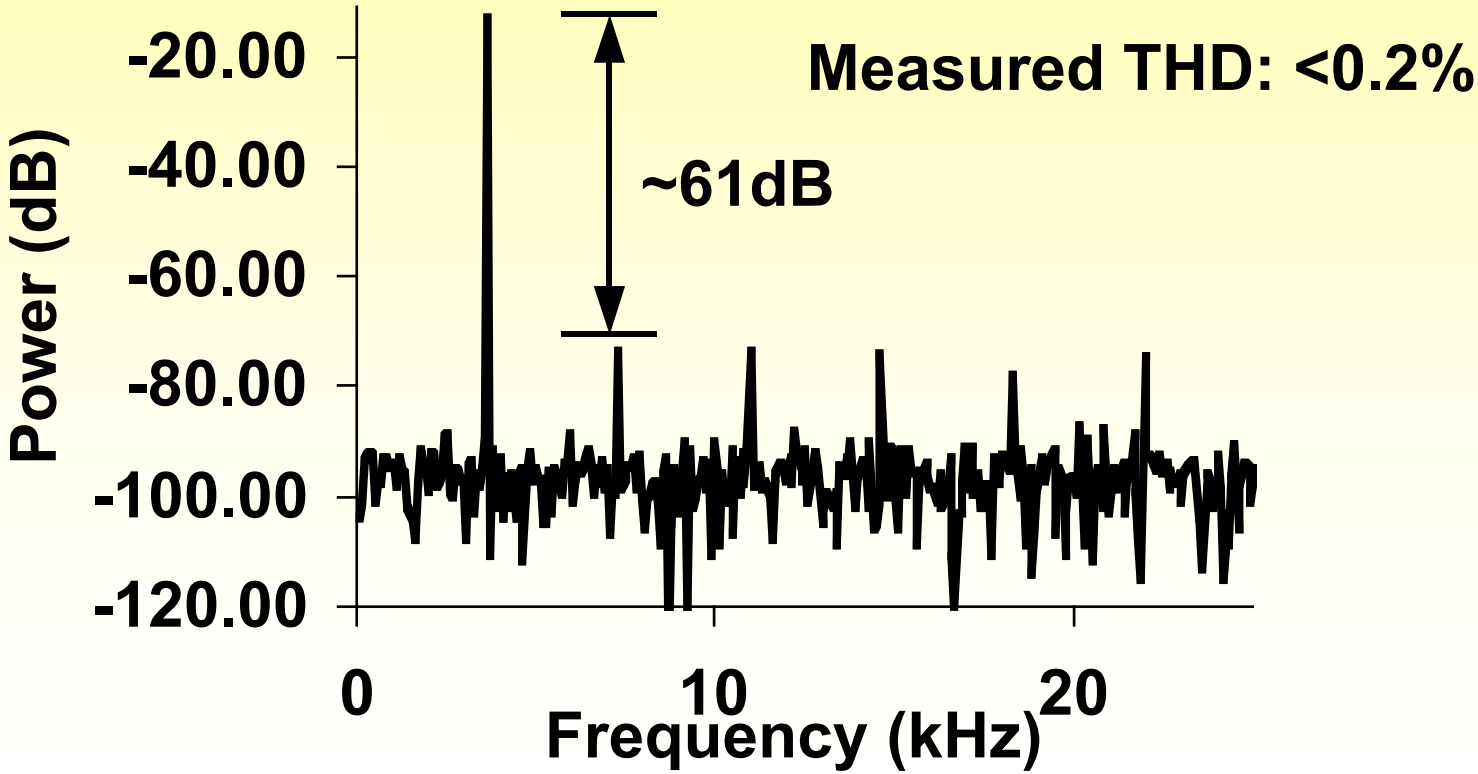
Measured Performance

Oscilloscope-Like Functionality



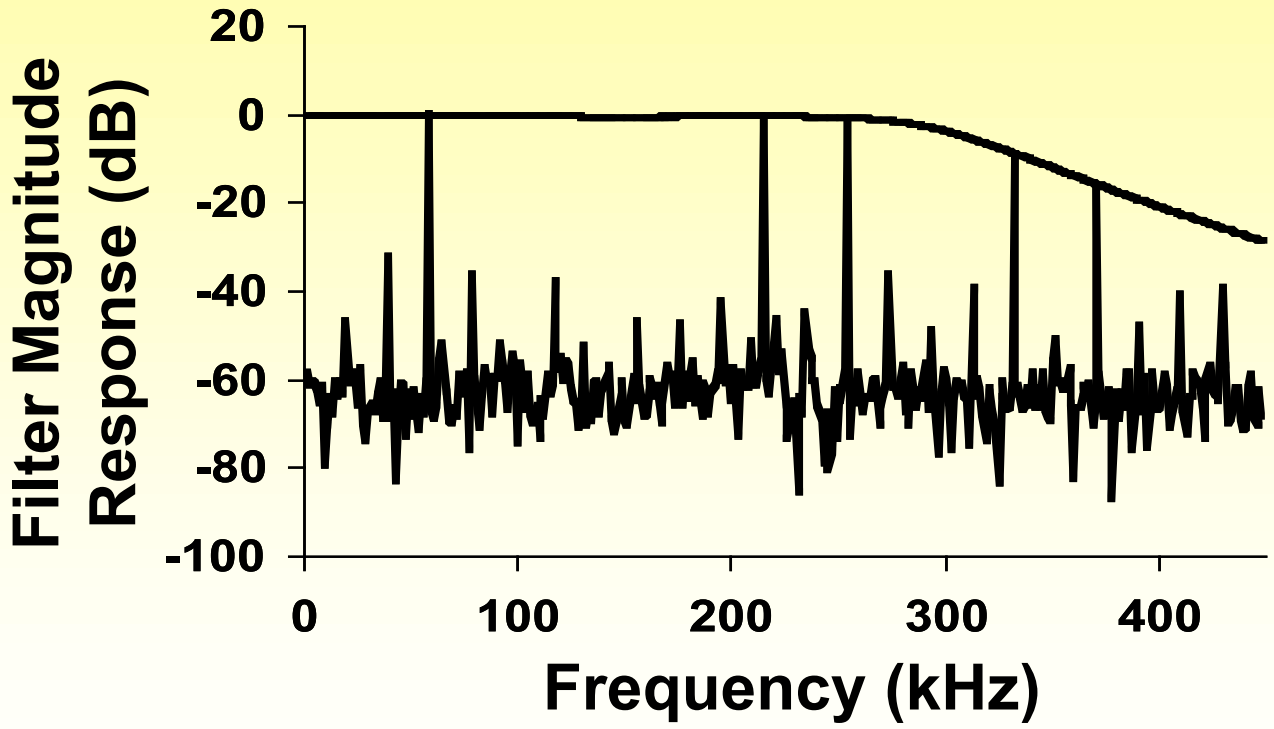
Maximum harmonic error: < 0.01%

Waveform Digitizer
Measured Performance



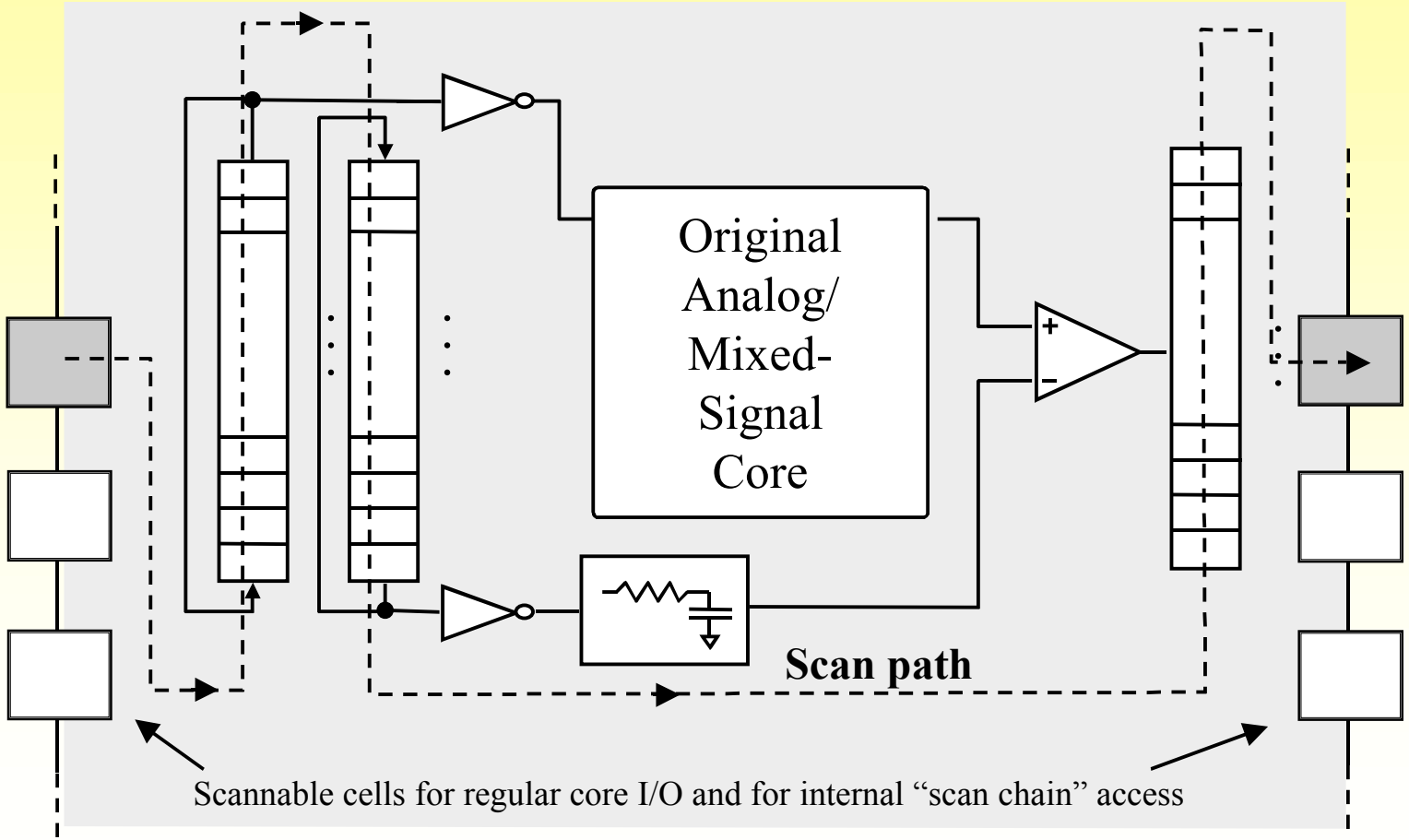
Measurement Capability

Spectrum Analyzer-Like Functionality

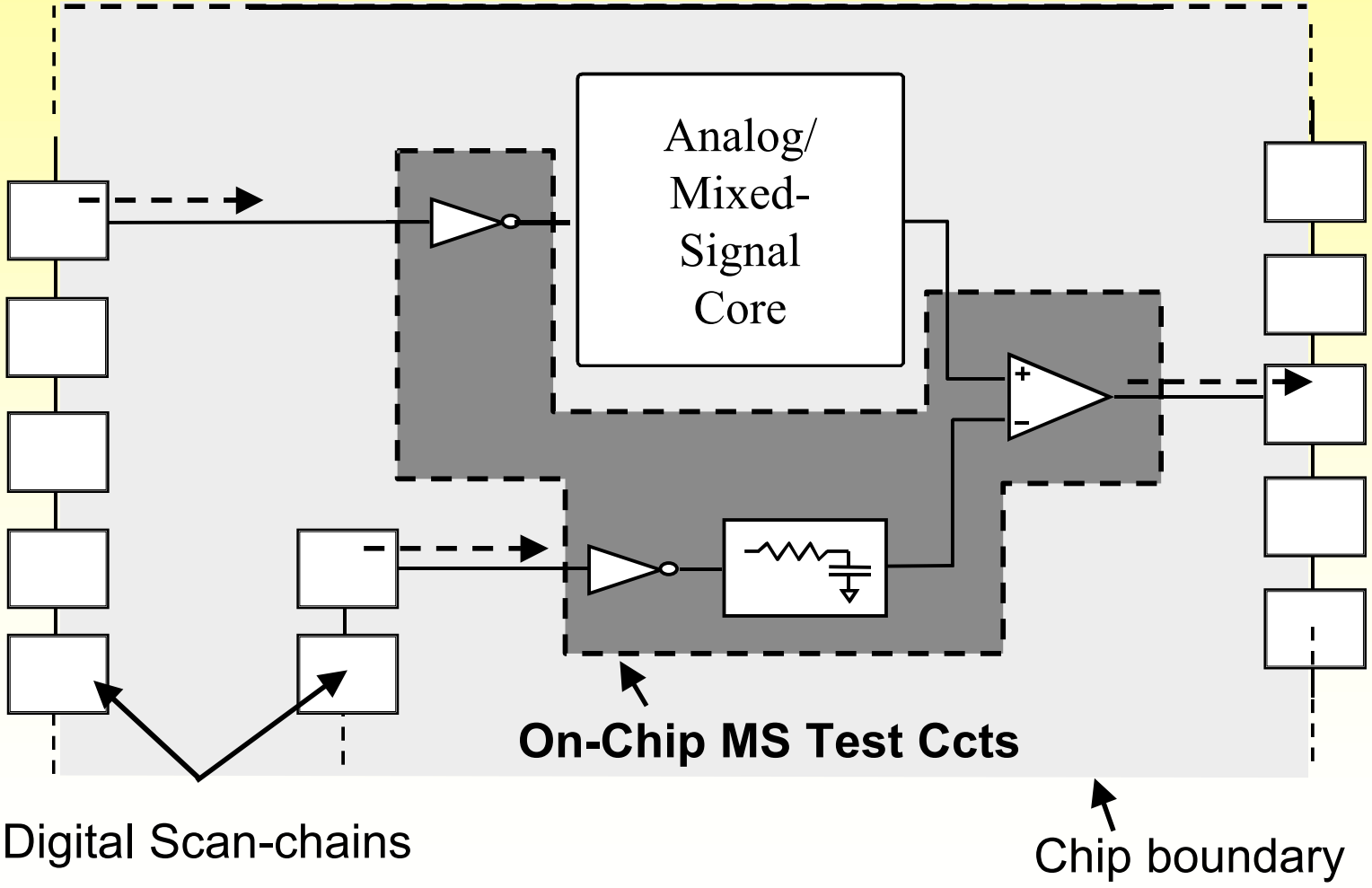


- **On-chip measurement result compared to actual measurement on a HP3588 Spectrum Analyzer**

Interfacing With Off-Chip Eqmt



Moving Scan Chains Off Chip



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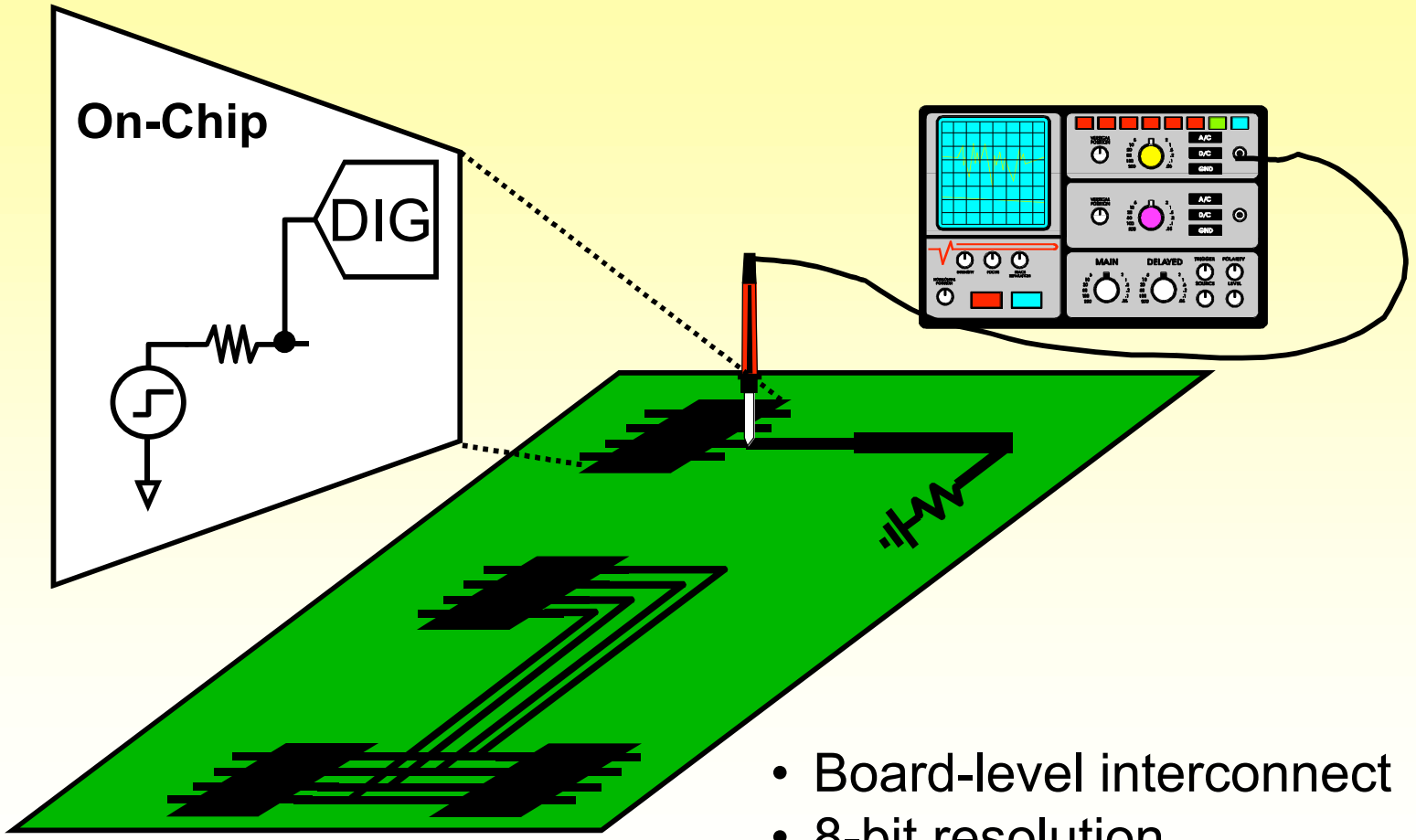
  - Coherent Sampling Test System
  - Time Domain Reflectometry & Transmission
  - Timing Analyzers
- Conclusions

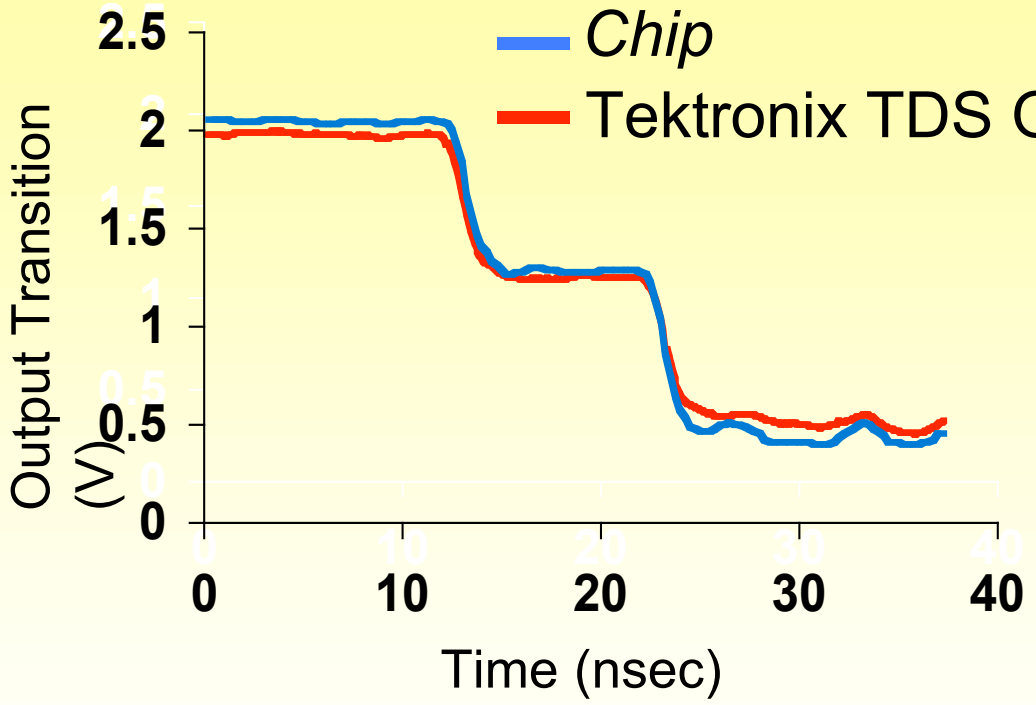
Board Testing: Time Domain Reflectometry

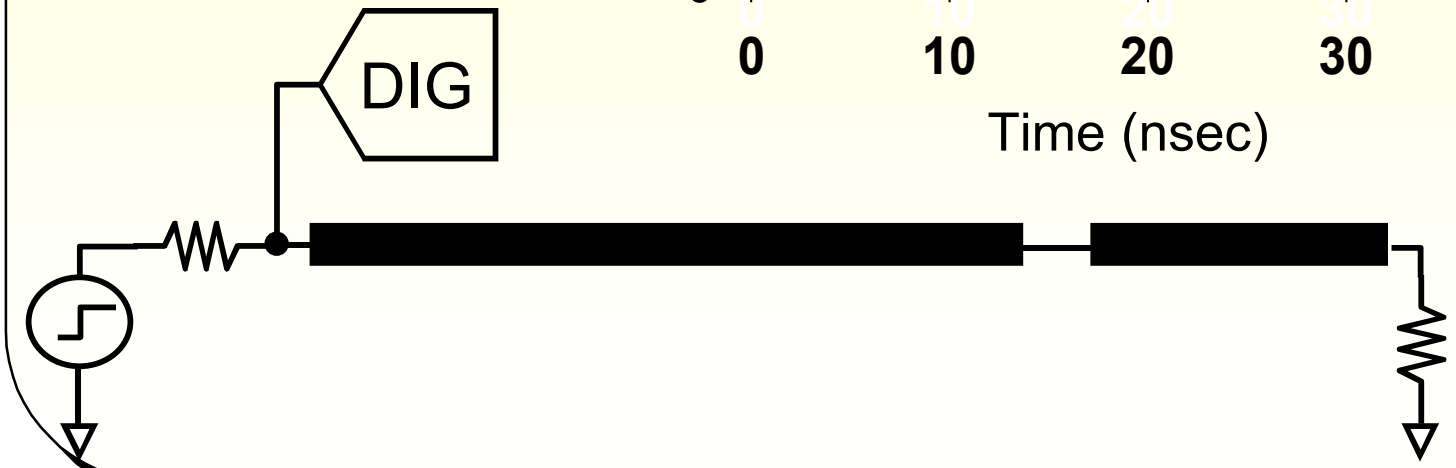


- Board-level interconnect
- 8-bit resolution
- 4-GHz sample rate

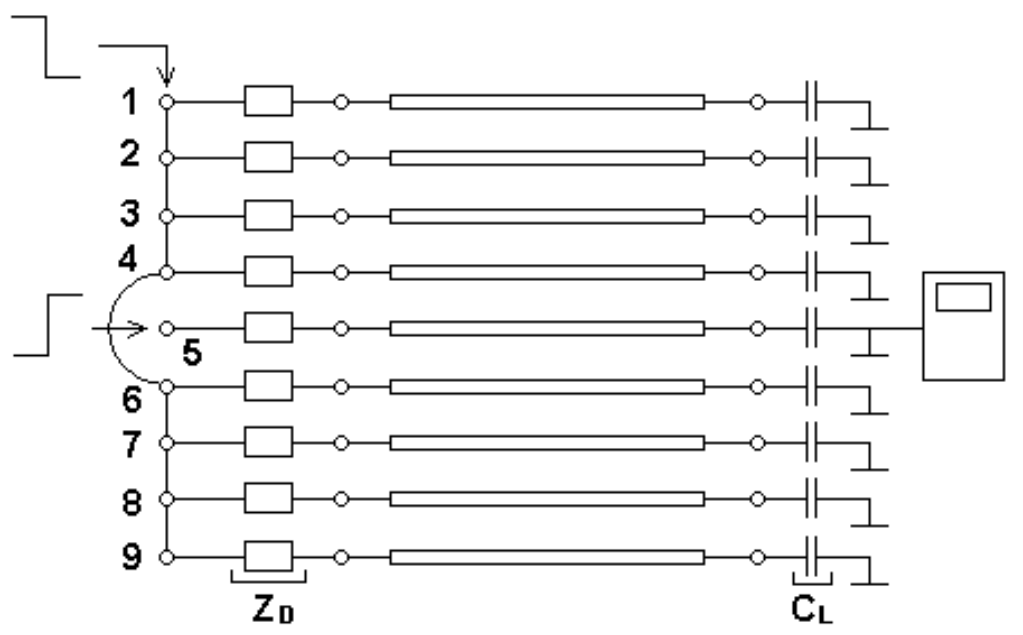
Board-Level TDR at 4 GSample/s

- Board-level interconnect
- 8-bit resolution
- 4-GHz sample rate





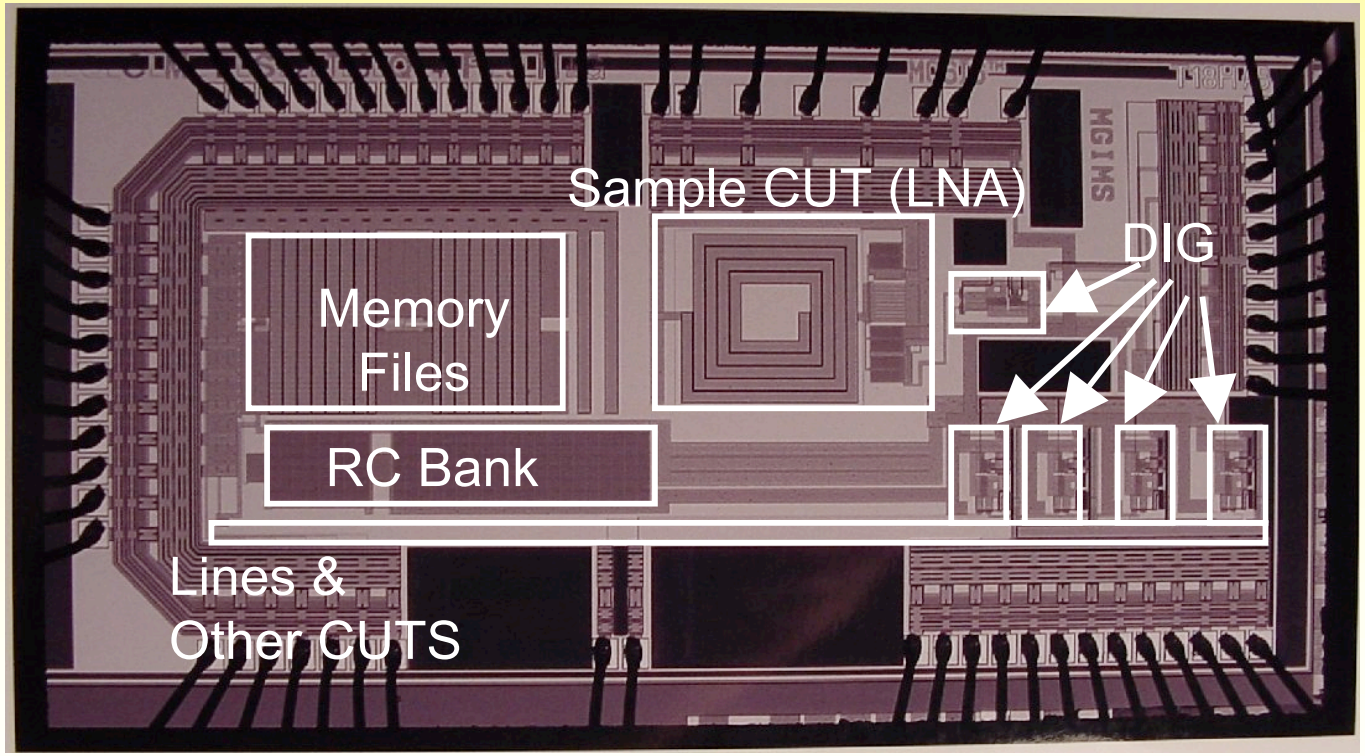
Crosstalk Characterization



- Investigating on-chip crosstalk effects is often performed with a multi-conductor structure using different forms of signal excitation.
  - On-chip behavior is often difficult to obtain due to package parastics and equipment loading effects.

10 GHz Sampling Scope Prototype

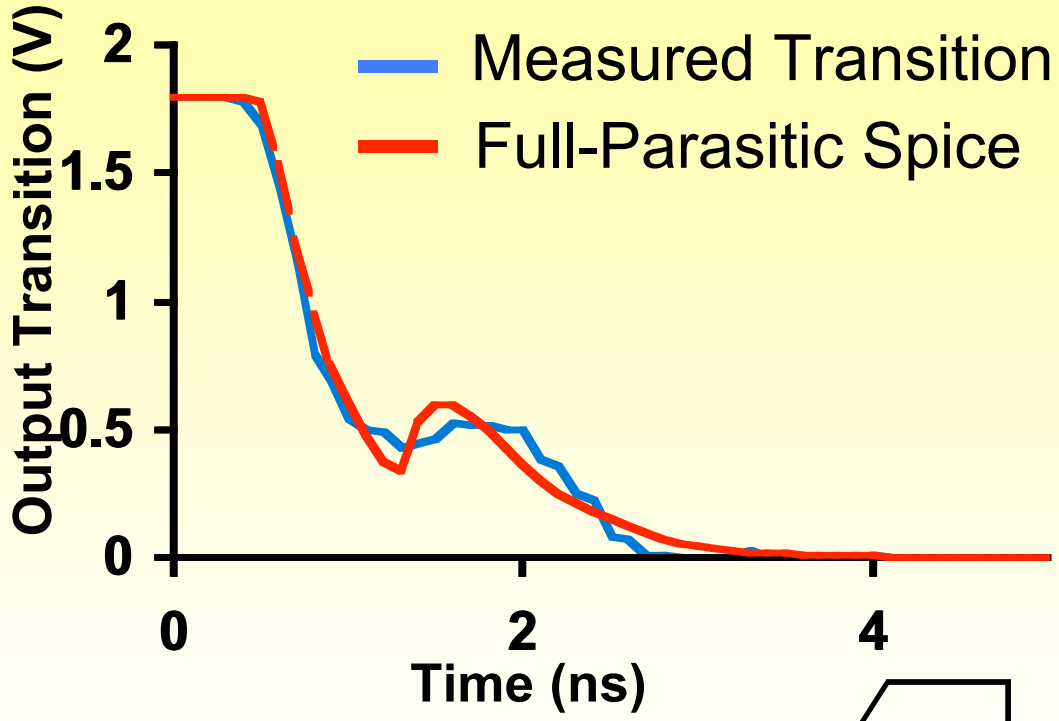
(M. Hafed & G. Roberts CICC 2003)



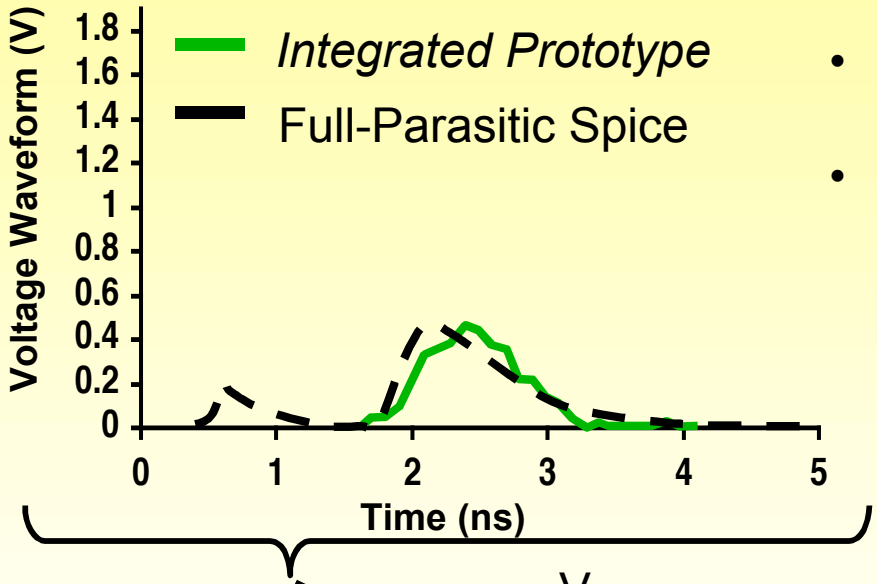
Area per DIG: 0.044 mm^2 (8-Bit Sampler)

10-GHz TDT Experimental Results

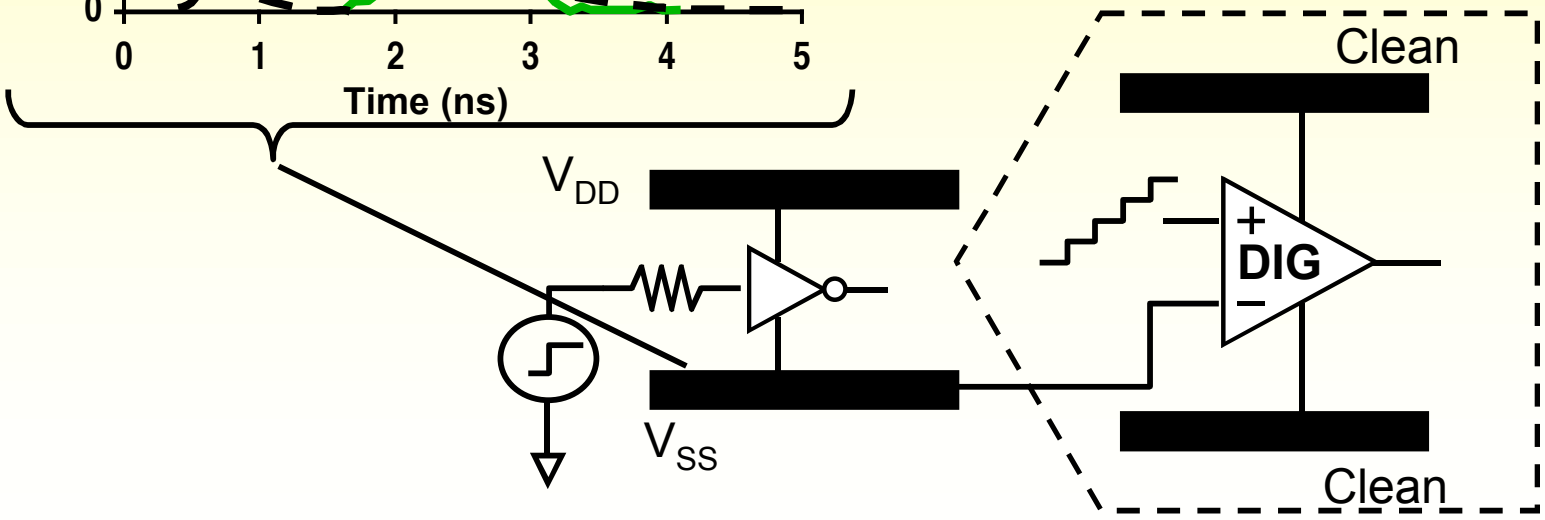
- Complete in situ digitization
- 6-bit resolution
- 10 GHz sample rate
- Other signal-integrity tests demonstrated



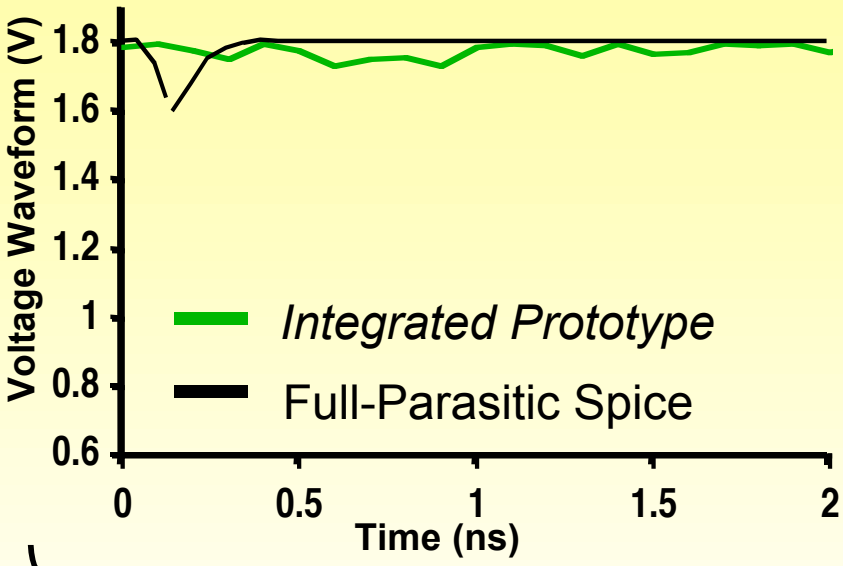
Substrate Noise



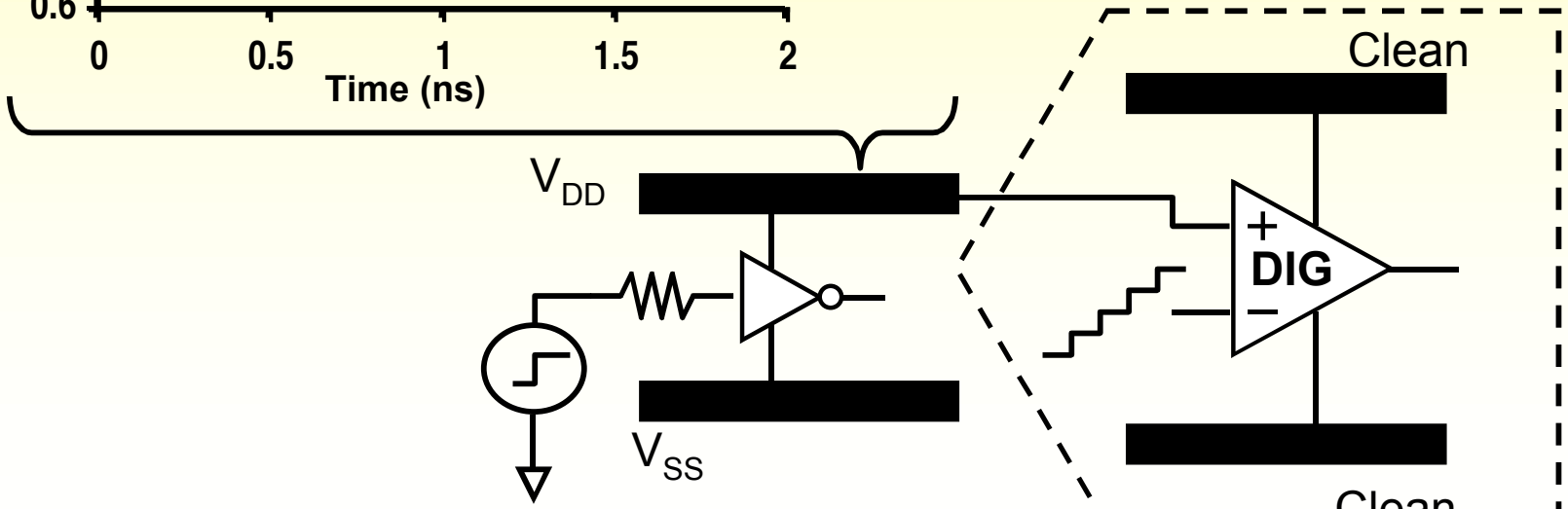
- Example of bounce on high resistance ground path
- Need to investigate improved sampling techniques



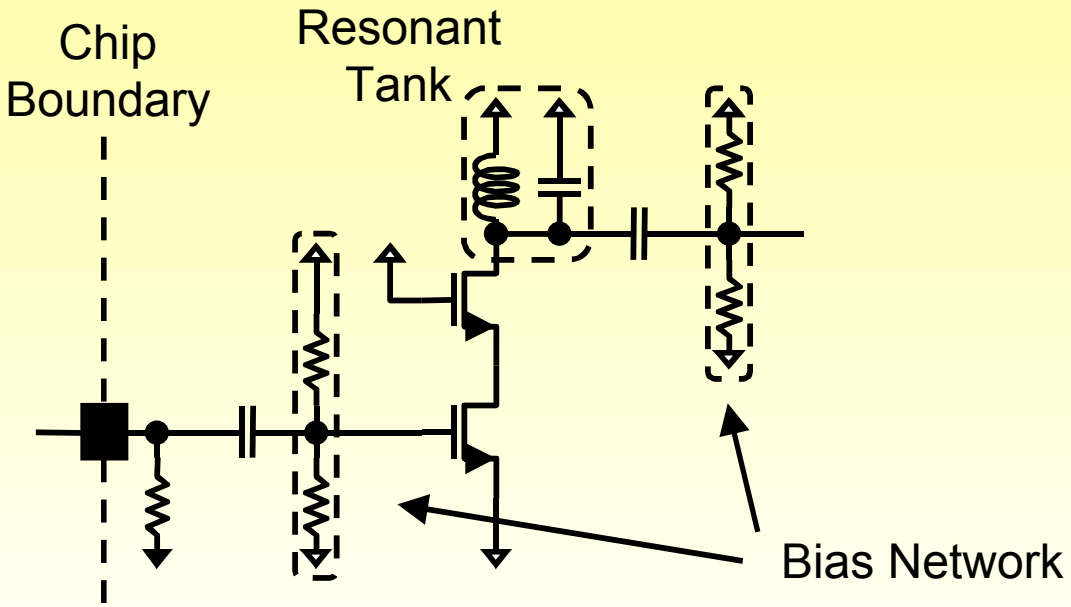
Power Supply Noise



- Other integrity issues successfully demonstrated
- Translation into frequency domain possible because of digitization

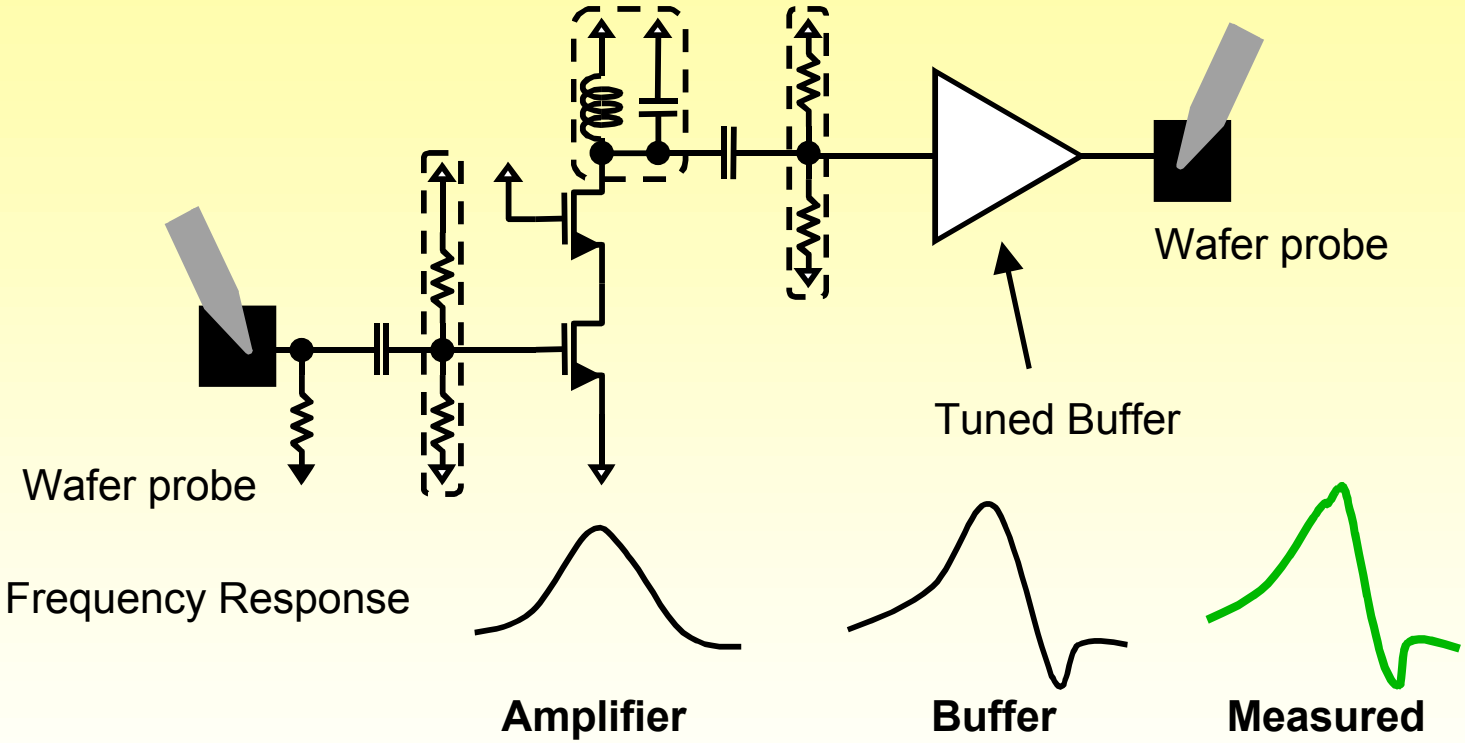


High-Frequency Tuned Amplifier



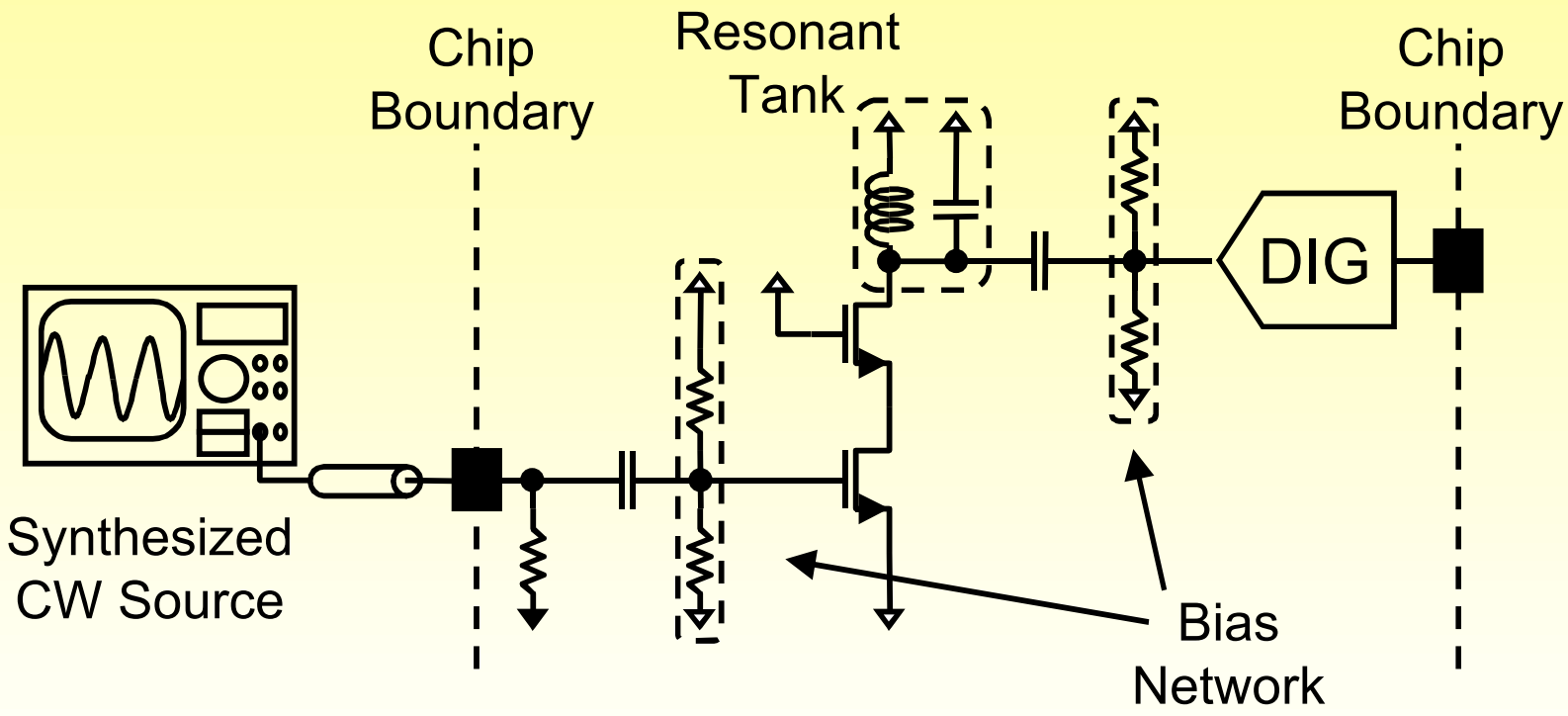
- Simple circuit for illustration purposes. Similar to a LNA, although not optimized for noise considerations
- **Output Signal not expected to be driven off-chip in "mission" environment**
- Conventional measurement requires buffer insertion

Buffer Insertion for Probe Test



- Even wafer probing presents too large a load
- Inserted buffer is typically also tuned in frequency (depending on termination)
- Measured spectrum influenced by buffer characteristics

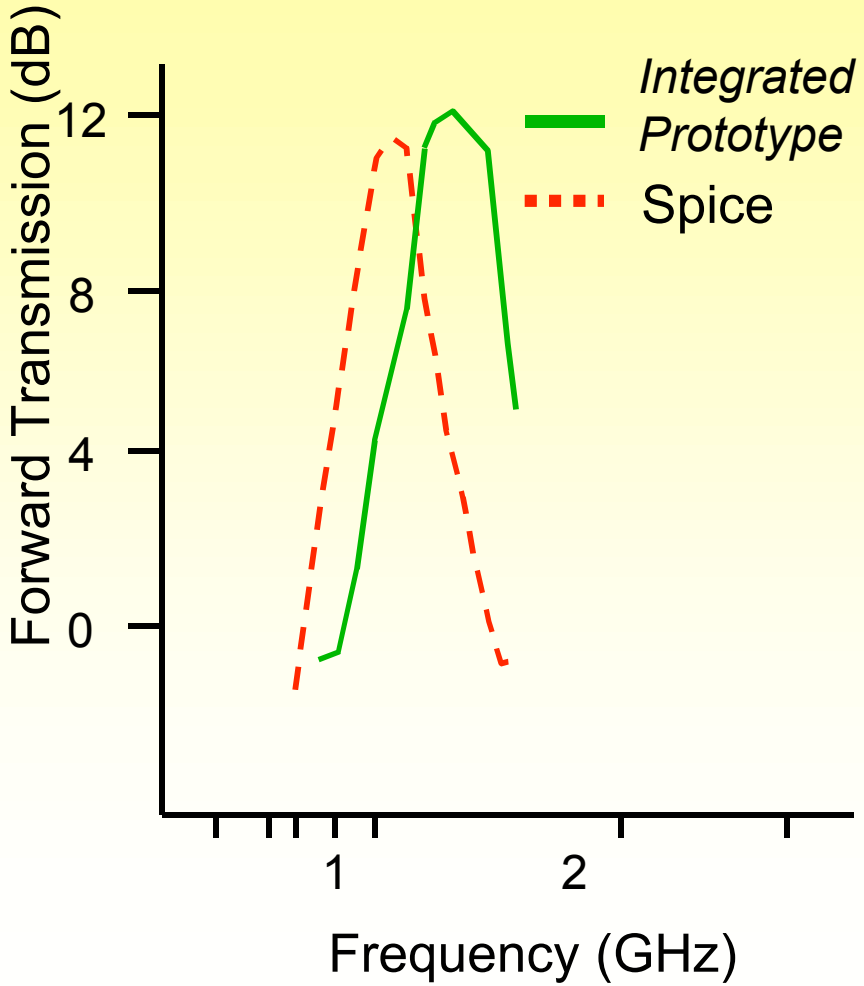
Proposed Test Vehicle



- Amplifier output directly sampled on-chip
- Flat response of DIG ensures proper extraction of spectral characteristics
- Offset/gain errors, and noise need to be investigated

Experimental Results

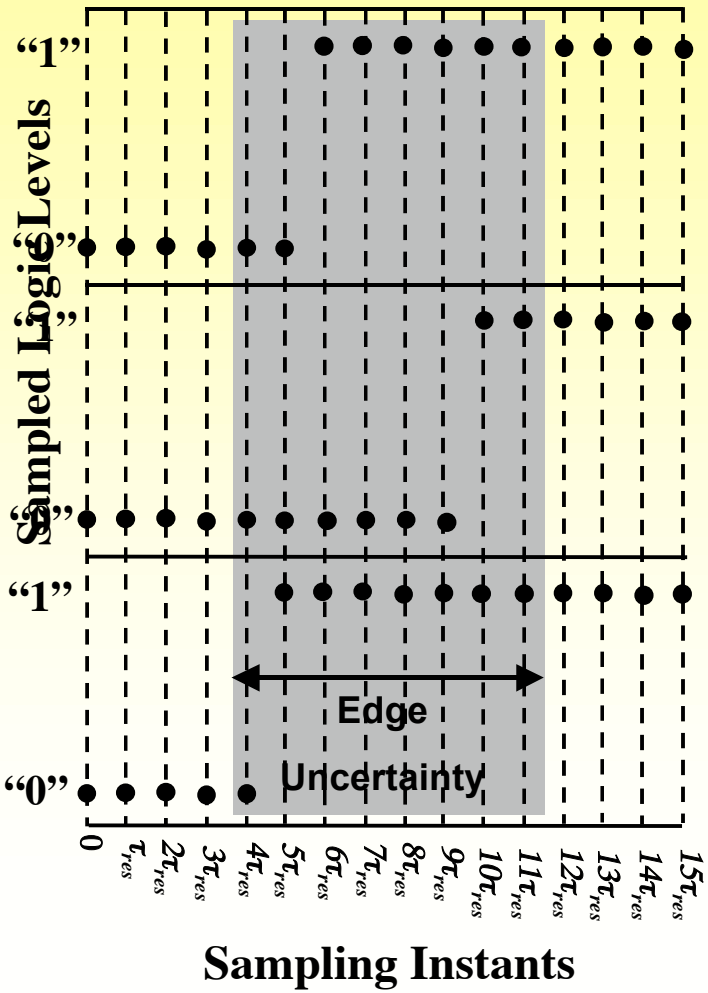
- *Embedded test* technology used to implement same DSP-based solution
- LNA resonance frequency slightly offset from simulation
- Investigate correlation with simulation



Outline

- Introduction
- On-Chip Instruments
  - Signal Generators
  - Sampling Oscilloscopes
  - Coherent Sampling Test System
  - Time Domain Reflectometry & Transmission
  - Timing Analyzers
- Conclusions

Measuring Jitter

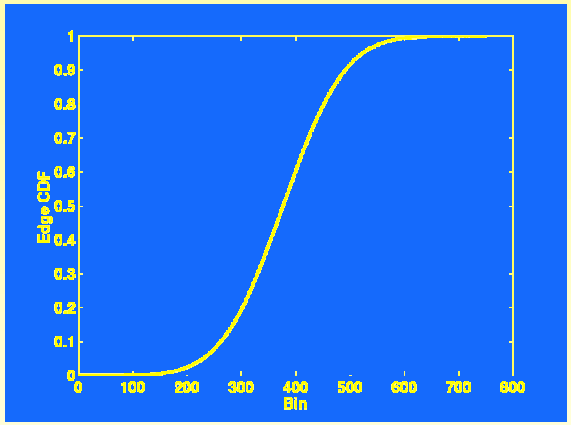


Edge 1

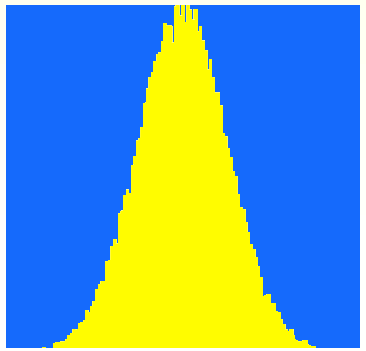
Edge 2

Edge 3

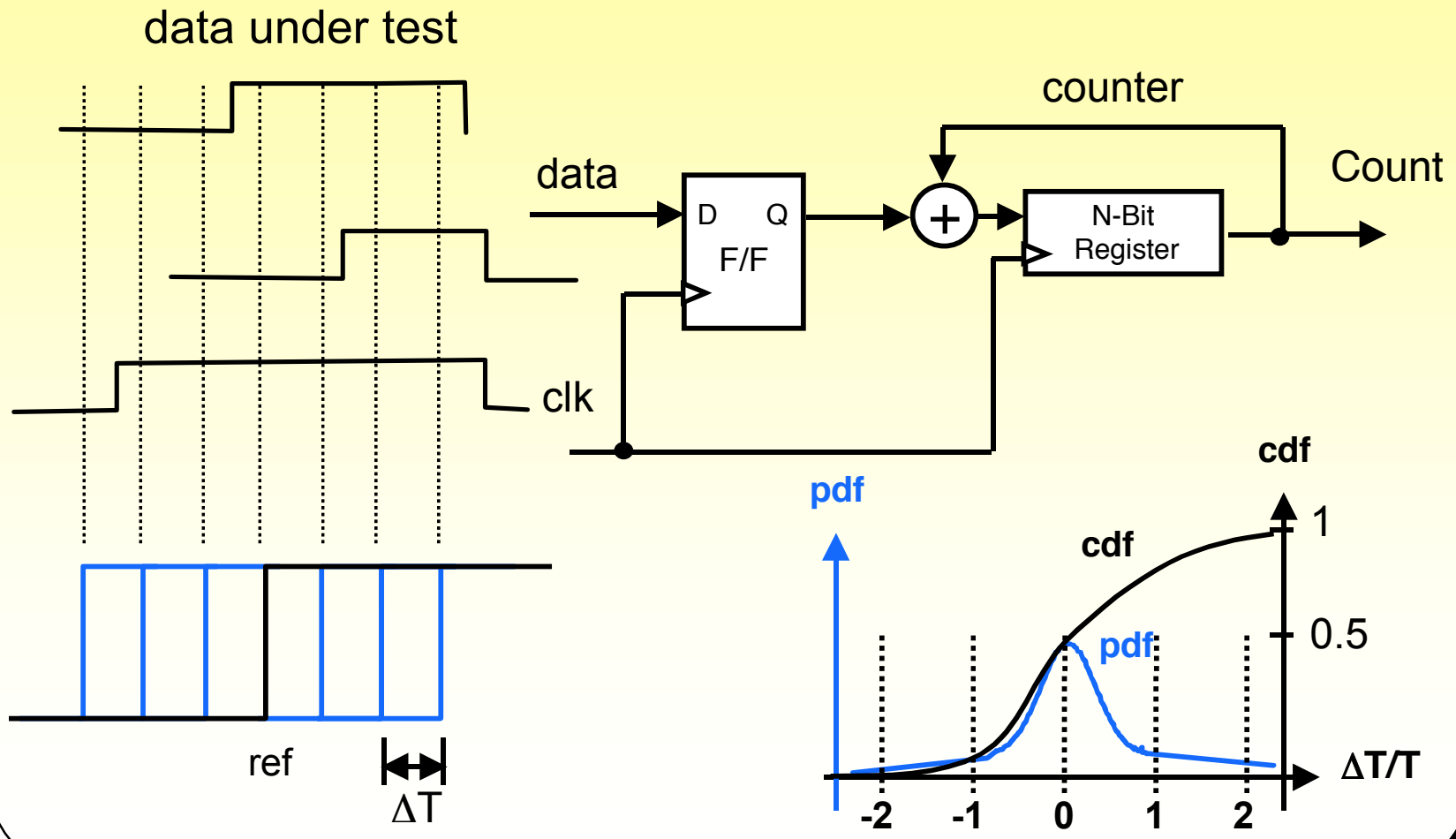
Edge Density (Jitter CDF)



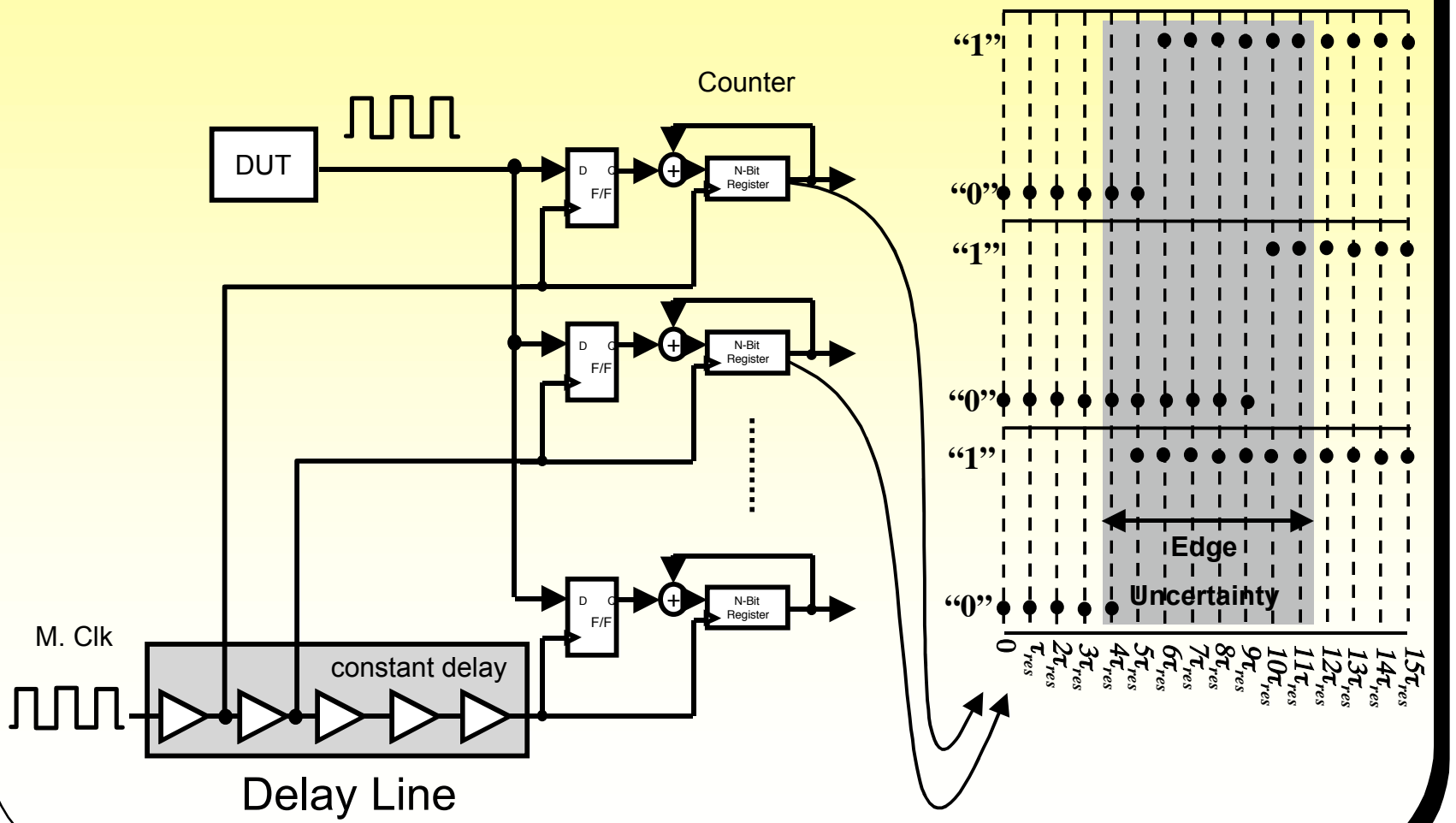
Edge Histogram (Jitter PDF)



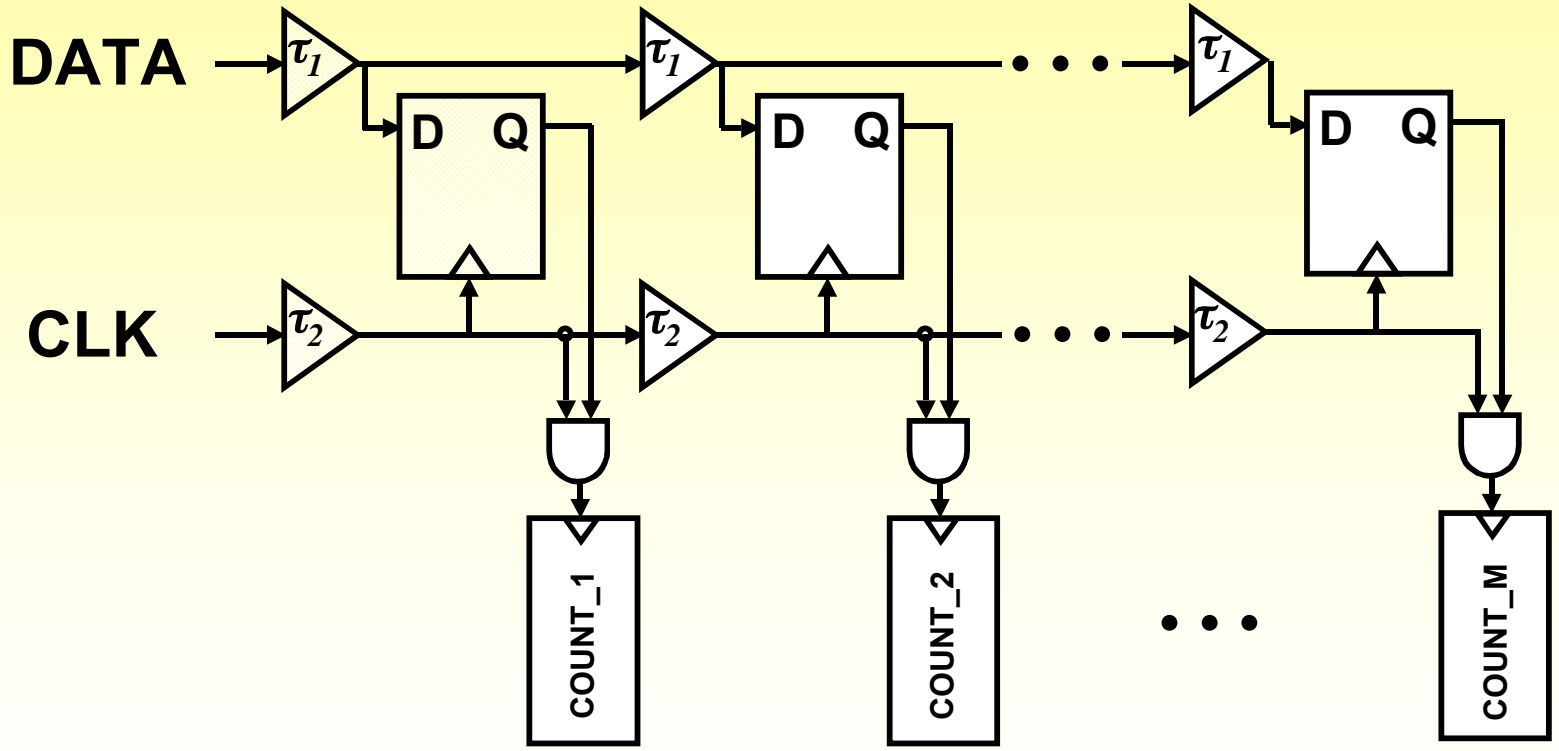
RMS-Jitter Measurement



RMS-Jitter Measurement



Jitter Measurement Device Using A Venier Delay Line



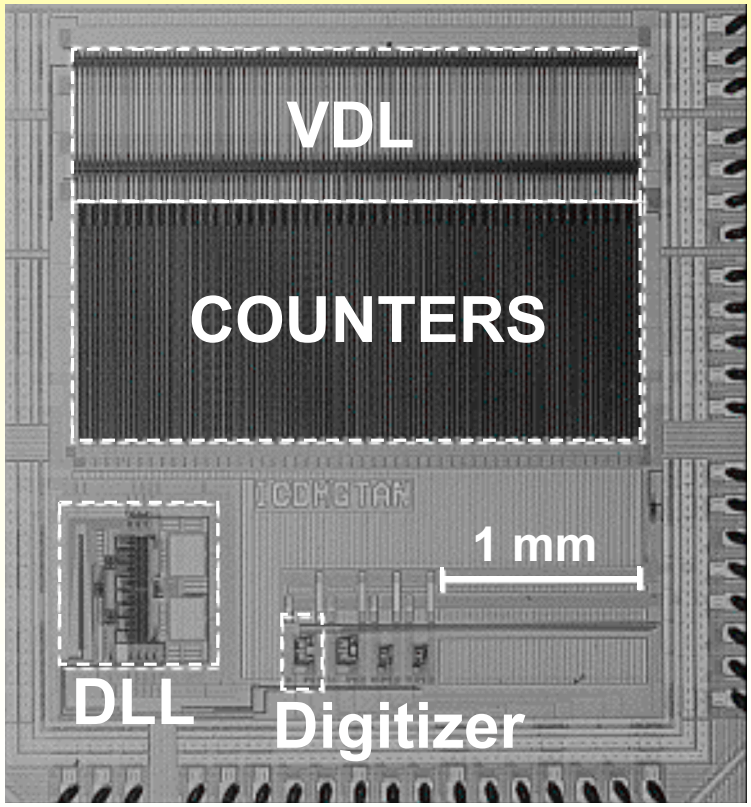
- Sub-gate delays can be realized using a VDL structure: $\tau_2 > \tau_1$, $\tau_{res} = \tau_2 - \tau_1$

Chip Micrograph

N. Abaskharoun & G. Roberts CICC'2001

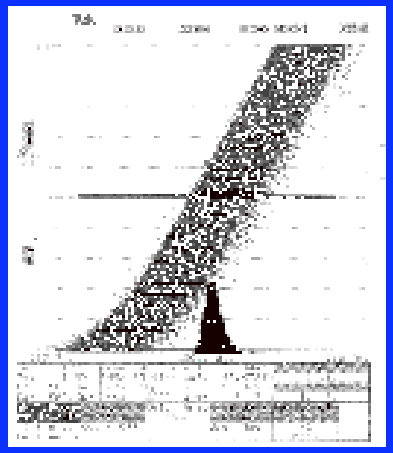
- 101 Stage VDL in a 0.35um CMOS
- VDL: 2.4 mm^2
- Counters: 3.1 mm^2

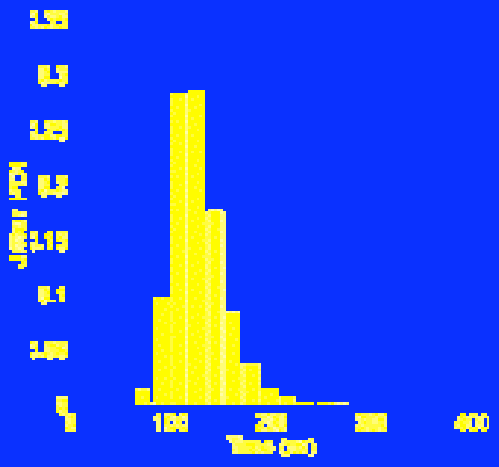
- BIG Circuit!!



Jitter Measurement
Guassian and Sinusoidal Distributions

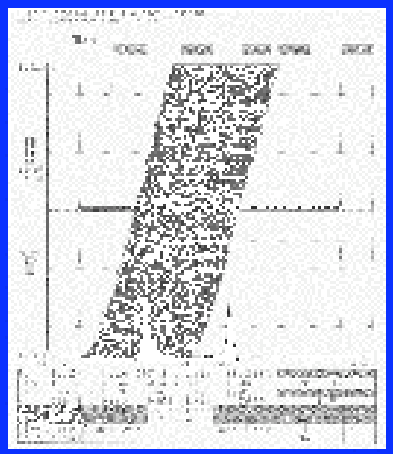
Pk-Pk = 310 ps
RMS = 30.41 ps

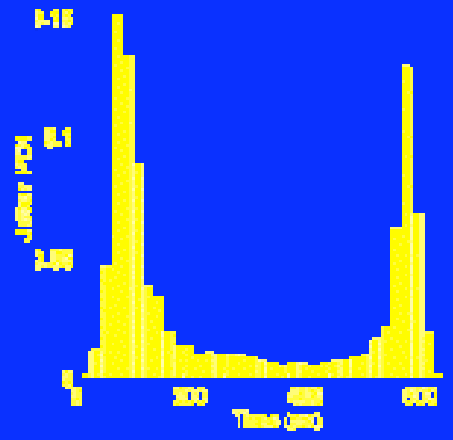




Pk-Pk = 324 ps
RMS = 27.61 ps

Pk-Pk = 644 ps
RMS = 230.4 ps



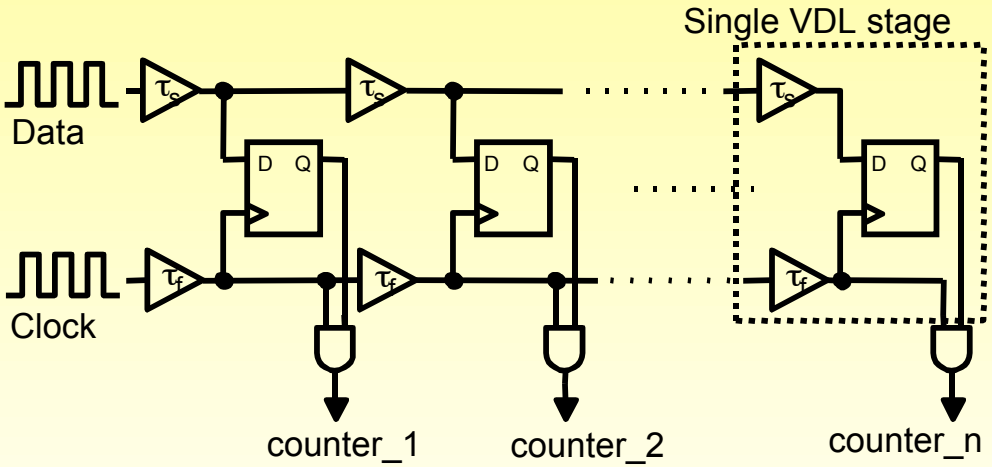


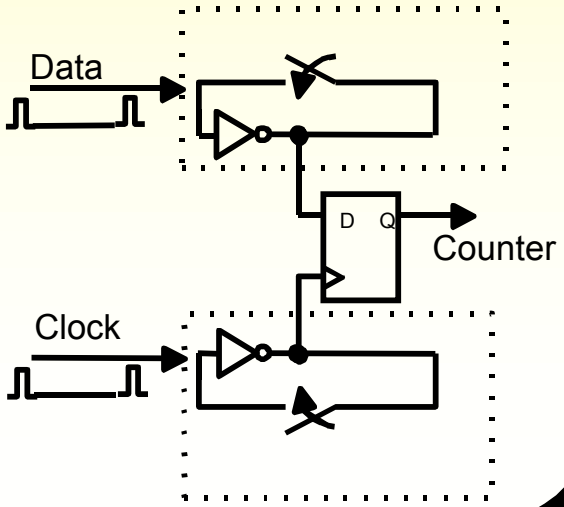
Pk-Pk = 666 ps
RMS = 220.2 ps

τ_{res} = 18 ps

Vernier Delay Line (VDL)

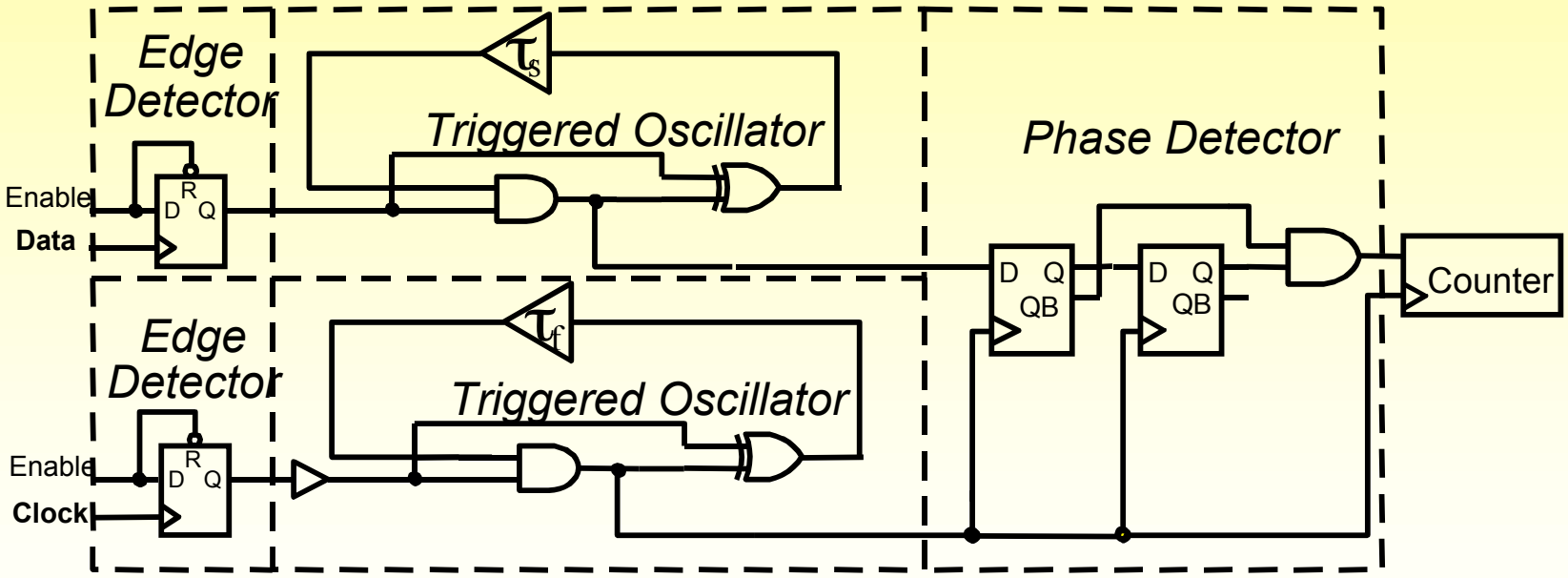
Overcome Drawbacks





Component-Invariant VDL

Complete Circuit

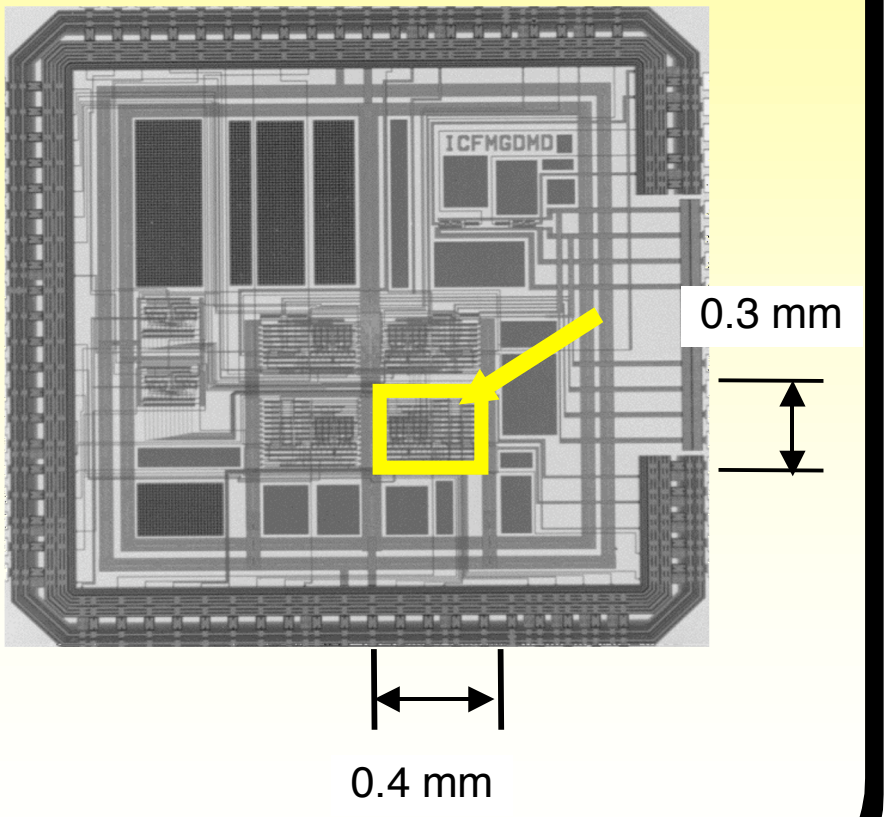


US & Canada Patent Pending

55 ps (19 ps) Timing Analyzer

A. Chan & G. W. Roberts, CICC'2002

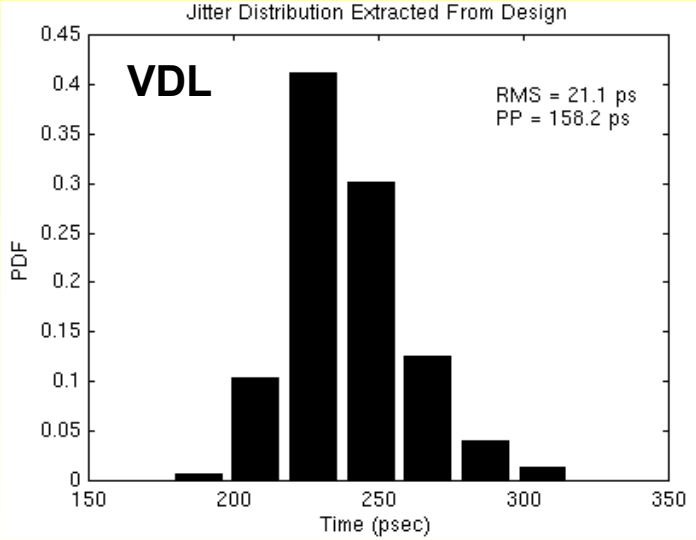
- 0.18 μm TSMC CMOS process
- 0.12 mm^2 per component-invariant VDL
- Expected resolution: ~ 10 ps
- Measured resolution: 19 ps
- Highest clock input frequency: 5 GHz
- Test time: ~ 150 ns/sample (6.66 MHz sampling rate)

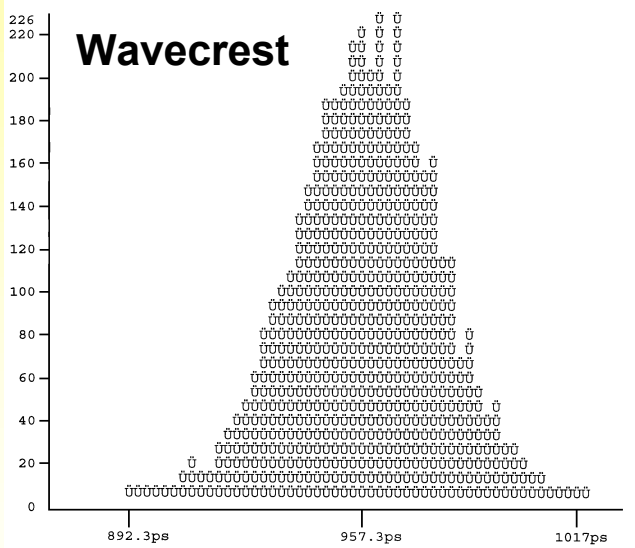


Experimental Results

IC Implementation – Pseudo Gaussian Distribution

VDL Timing resolution = 19 ps



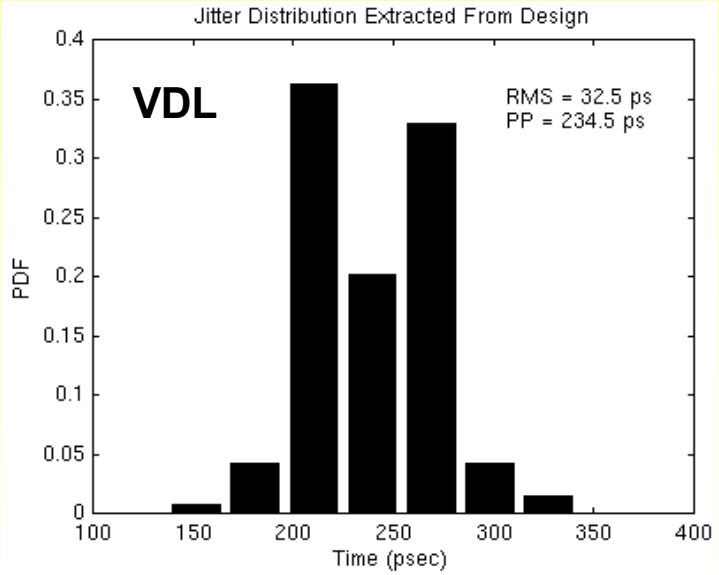


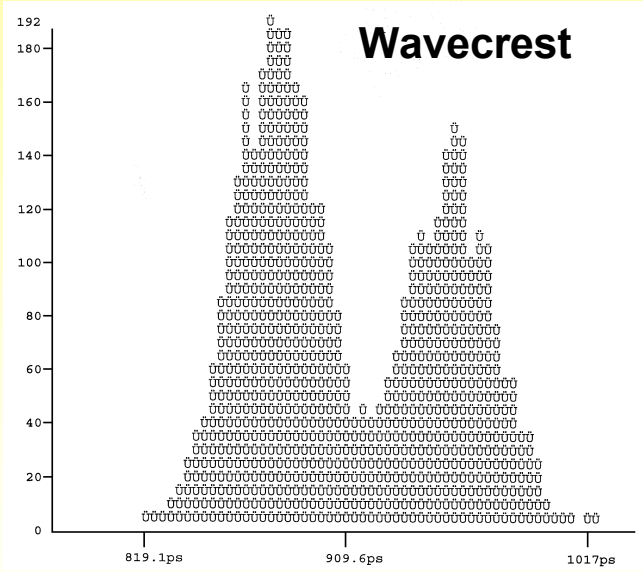
	VDL	Wavecrest
RMS Jitter	21.1 ps	18.68 ps
Peak to peak Jitter	158.2 ps	124.5 ps

Experimental Results

IC Implementation – Pseudo Sinusoidal Distribution

VDL Timing resolution = 19 ps

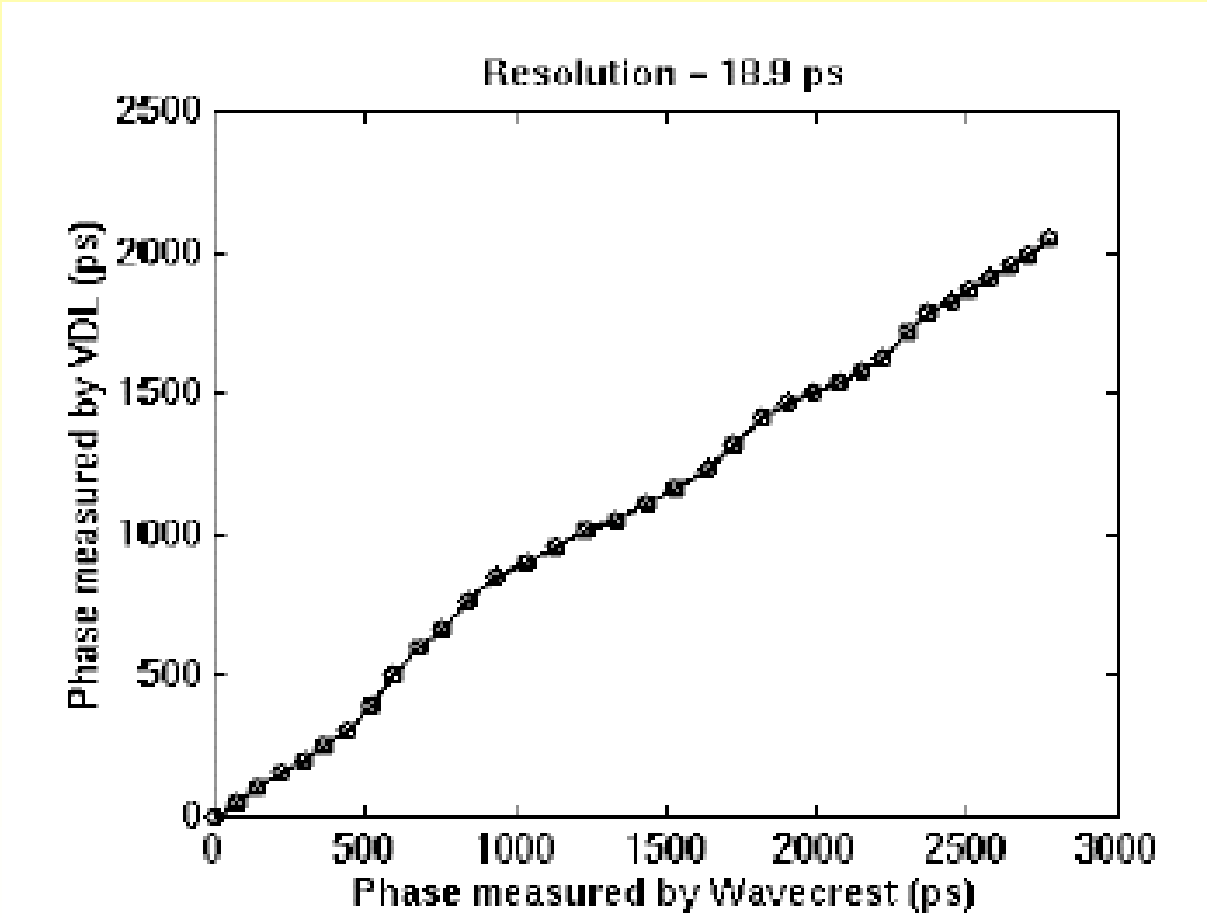




	VDL	Wavecrest
RMS Jitter	32.5 ps	41.94 ps
Peak to peak Jitter	234.5 ps	197.8 ps

Experimental Results

Mean Value of VDL Jitter Distribution Vs. Wavecrest



Conclusions

- Present and future SOC will require some form of Design-For-Test (DFT) to aid the test process.
  - Embedded cores can be accessed externally with an analog test bus and ATE
  - On-chip digitizer is essential for high-speed and low noise measurements.
  - Signal generator + digitizer provides full tester capability on chip.
- Numerous test instruments have been fabricated directly on-chip and can serve as a foundation for the engineering laboratory of the future.