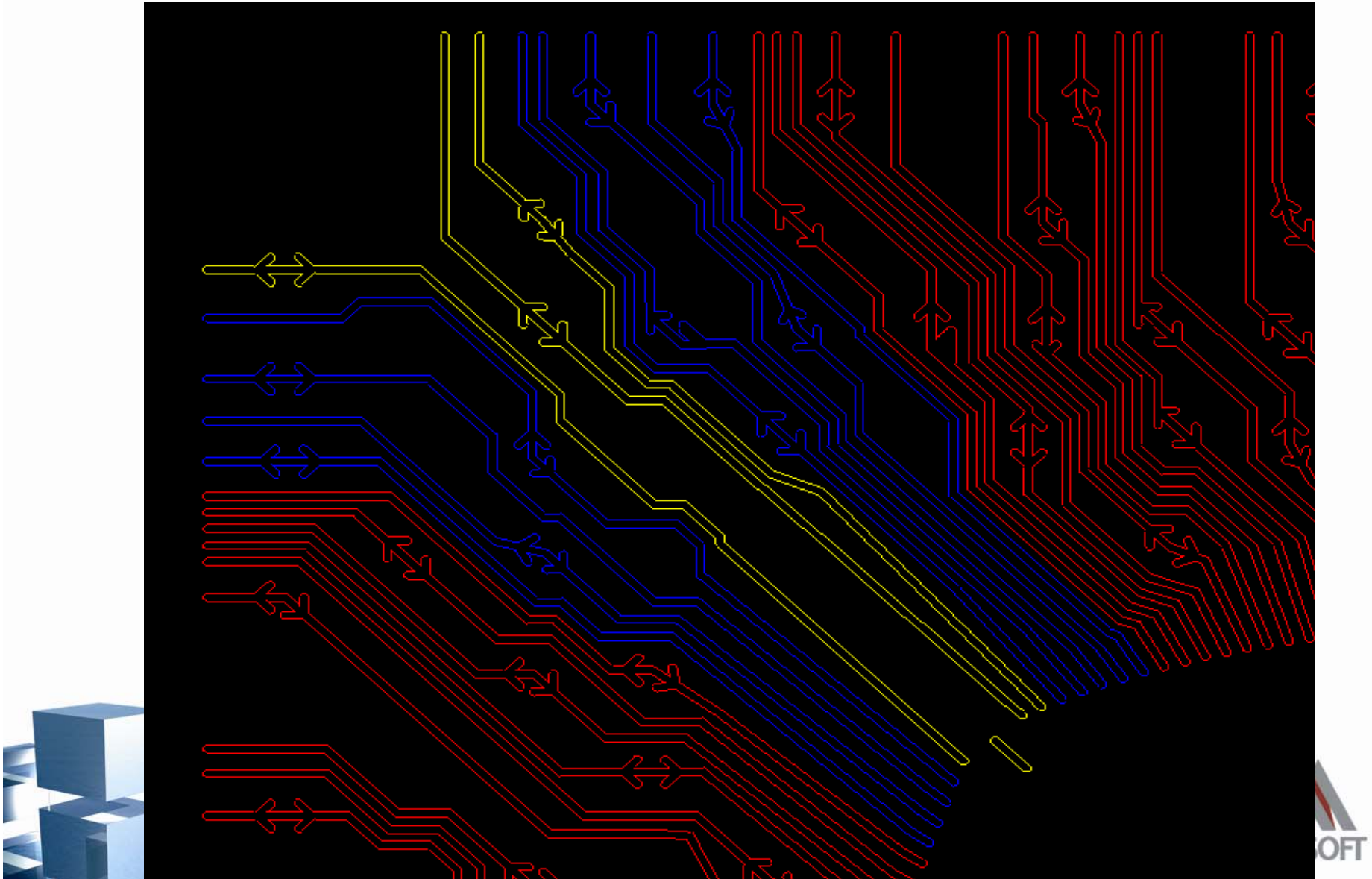
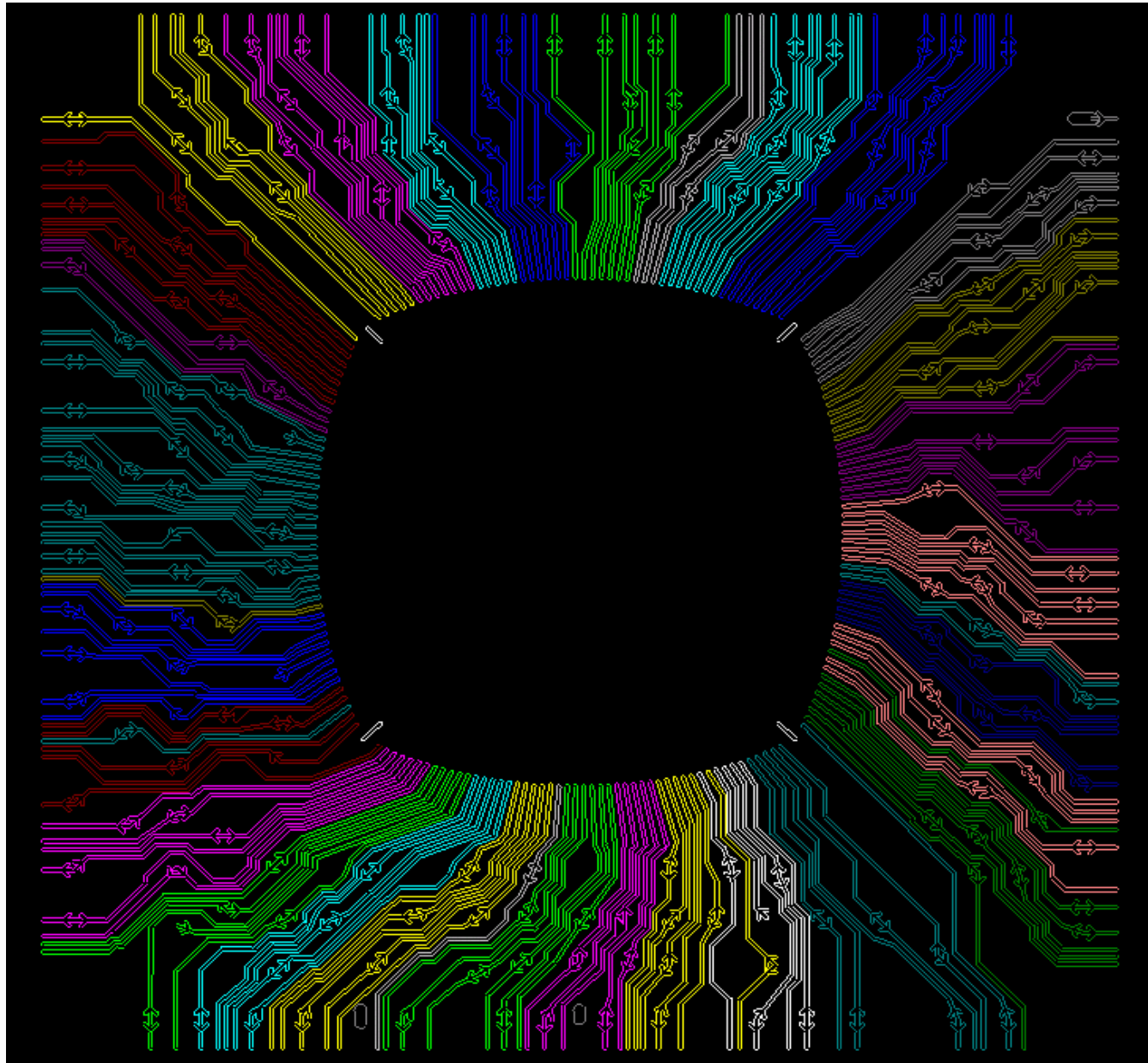


Package Net Group Creation

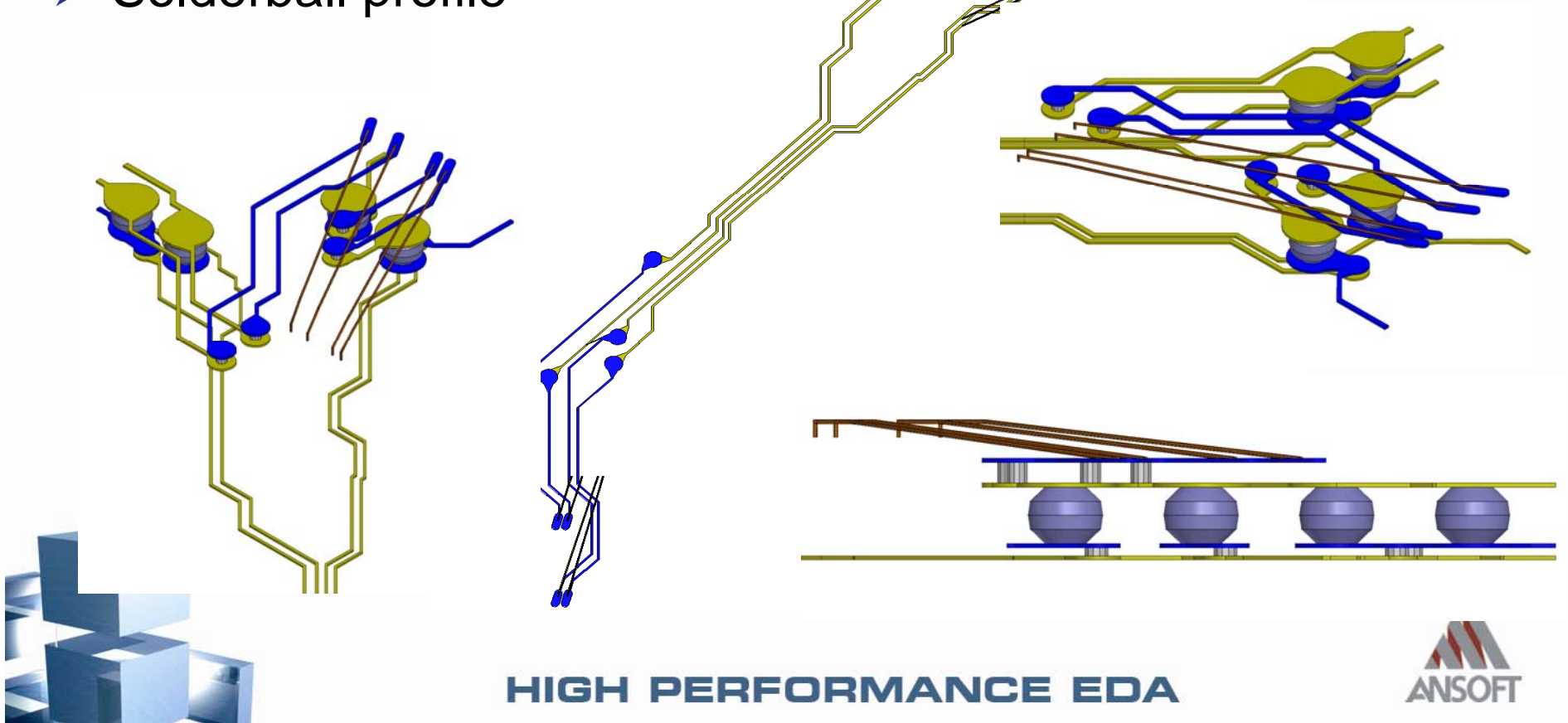


TPA Example Net Groupings

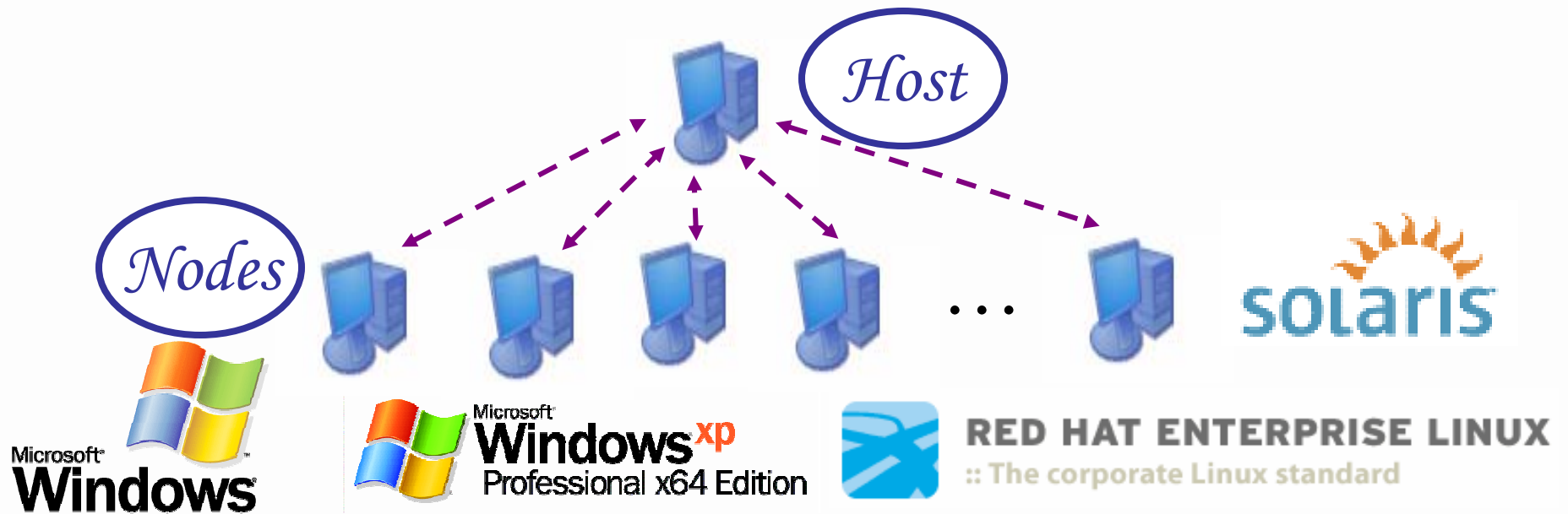


Parametric Variations

- Routing (width and spacing)
- Bondwire profile
- Solderball profile



DSO – Distributed Solve Option



Paradigm shift:

Old: 1 computer to 1 engineer

New: n number of CPU's to 1 engineer

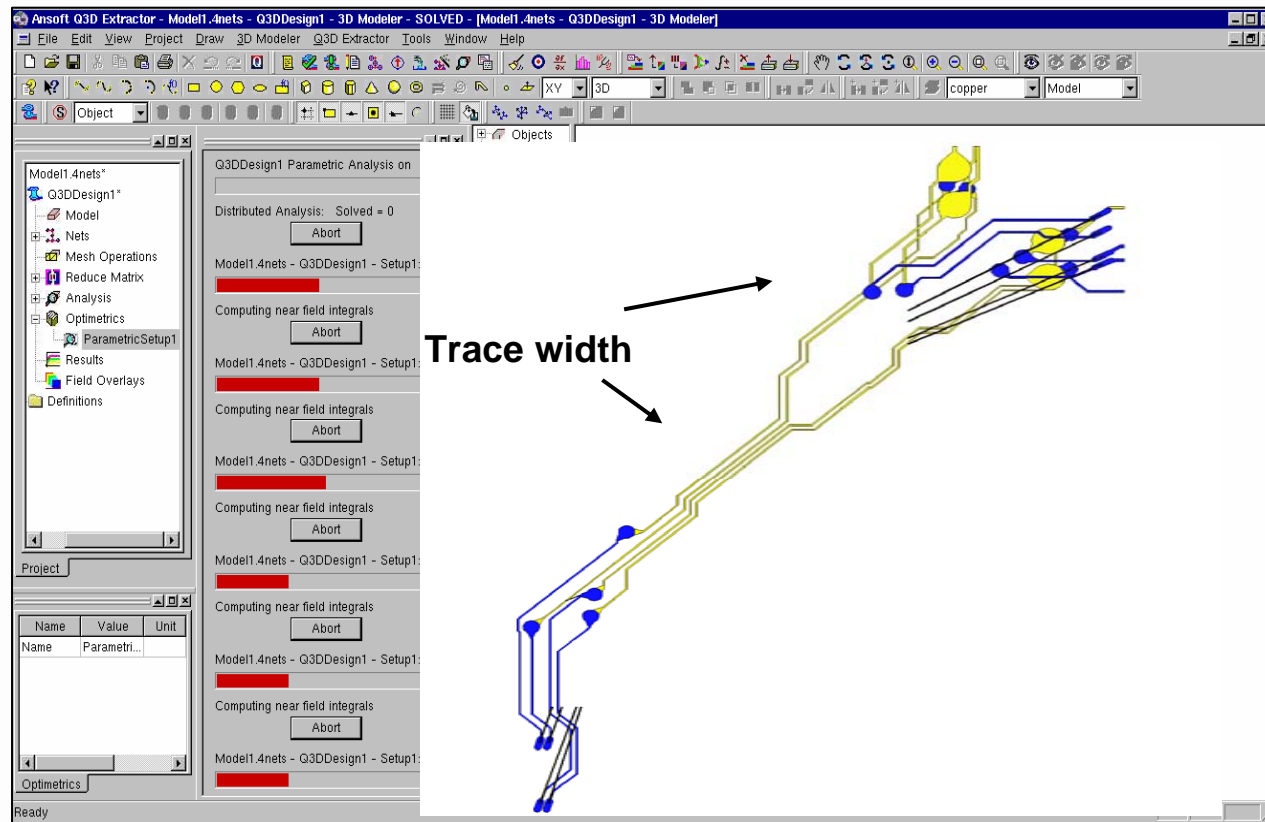


HIGH PERFORMANCE EDA



Optimize Performance

- Parametric Q3D Extractor[®] project
 - Trace width and spacing changing

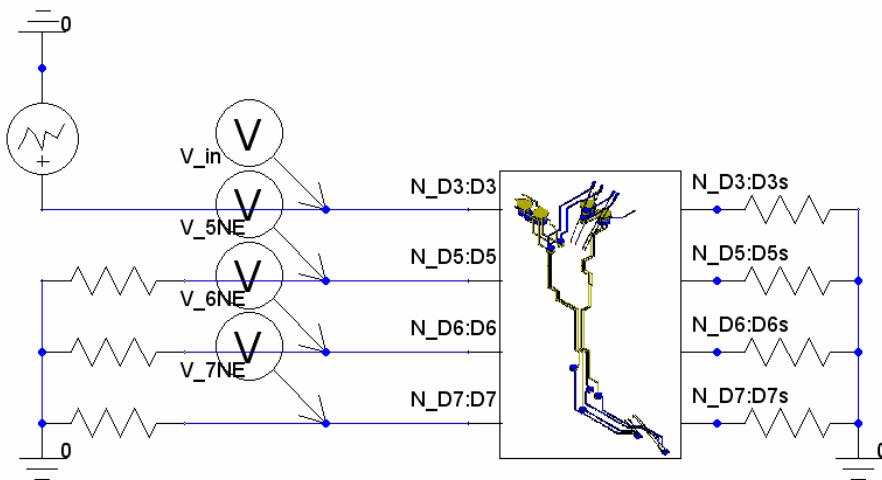


HIGH PERFORMANCE EDA

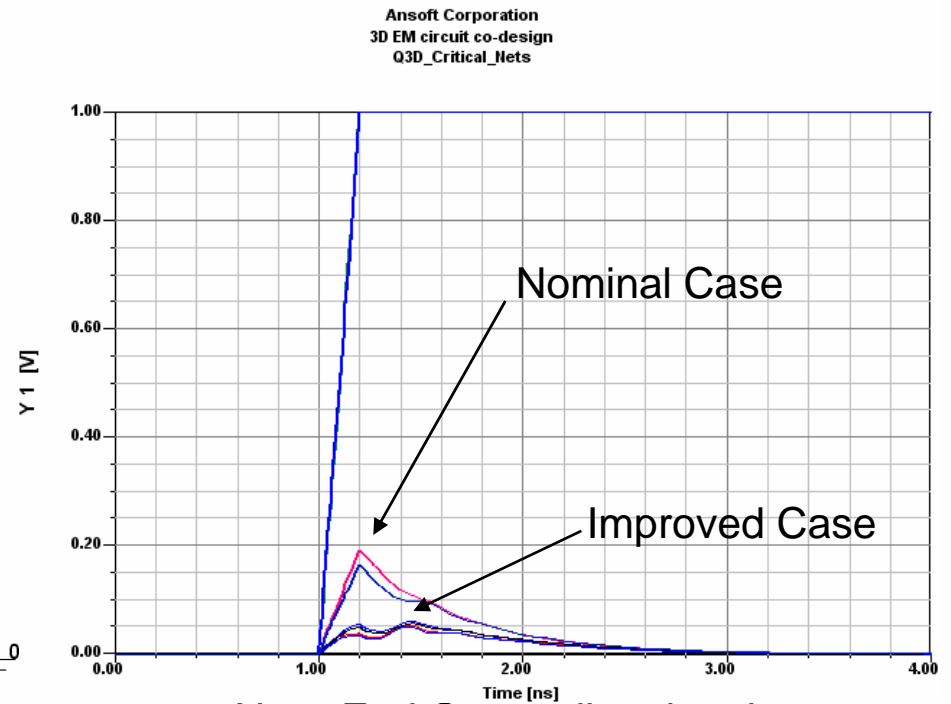


Optimize Performance

- 3D EM Based circuit co-design
 - Changed Routing
 - Trace length and spacing
 - Crosstalk analysis



DesignerSI™/Nexxim®
Schematic view



Near-End Crosstalk noise data
Tr=200ps



HIGH PERFORMANCE EDA



Optimize Simulation Run Times

- DSO Setup
 - 25 Parametric Case
 - 7 nodes used
 - 2.6 GHz Opteron 8 GB of RAM

- Without DSO
 - 7 hr 2 min

- Using DSO Time
 - 1hr 2 min

**** Linear Speed Increase ****
~ 7X speed up with 7 nodes

Post Analysis Display

ParametricSetup1

Result Profile

Q3D Extractor version 7.1.1 started on ansolf-dso at 09-05-2006 20:45:56

Variation	BFRD	BMR	H1	UR	WS	Start	Stop	Elapsed
1	170um	180...	125um	100um	-7.5um	20:46:03	21:13:51	00:27:48
2	170um	180...	150um	100um	-7.5um	20:46:08	21:13:56	00:27:48
3	170um	180...	125um	100um	7.5um	20:46:06	21:13:57	00:27:51
4	170um	180...	125um	100um	15um	20:46:05	21:14:54	00:28:49
5	170um	180...	150um	100um	-15um	20:46:07	21:14:54	00:28:47
6	170um	180...	100um	100um	15um	20:46:00	21:15:48	00:29:48
7	170um	180...	125um	100um	-15um	20:46:02	21:16:01	00:29:59
8	170um	180...	100um	100um	-15um	20:45:57	21:16:26	00:30:29
9	170um	180...	100um	100um	0um	20:45:59	21:17:43	00:31:44
10	170um	180...	100um	100um	-7.5um	20:45:58	21:18:11	00:32:13
11	170um	180...	125um	100um	0um	20:46:04	21:18:13	00:32:09
12	170um	180...	100um	100um	7.5um	20:46:01	21:18:46	00:32:45
13	170um	180...	150um	100um	0um	20:46:10	21:19:10	00:33:00
14	170um	180...	150um	100um	7.5um	21:13:56	21:38:11	00:24:15
15	170um	180...	150um	100um	15um	21:13:51	21:38:22	00:24:31
16	170um	180...	50um	100um	-15um	21:13:57	21:43:03	00:29:06
17	170um	180...	50um	100um	-7.5um	21:14:54	21:43:52	00:28:58
18	170um	180...	50um	100um	0um	21:14:54	21:43:52	00:28:58
19	170um	180...	75um	100um	15um	21:18:13	21:44:14	00:26:01
20	170um	180...	50um	100um	7.5um	21:16:01	21:44:23	00:28:22
21	170um	180...	50um	100um	15um	21:15:48	21:44:55	00:29:07
22	170um	180...	75um	100um	-15um	21:16:26	21:47:42	00:31:16
23	170um	180...	75um	100um	-7.5um	21:17:43	21:48:05	00:30:22
24	170um	180...	75um	100um	0um	21:18:11	21:48:20	00:30:09
25	170um	180...	75um	100um	7.5um	21:18:46	21:48:42	00:29:56

Export...
Solver Profile...

Finished at 09-05-2006 21:48:42 (Total Time : 01:02:46) **7hr 2 min**

DSO Solution Time

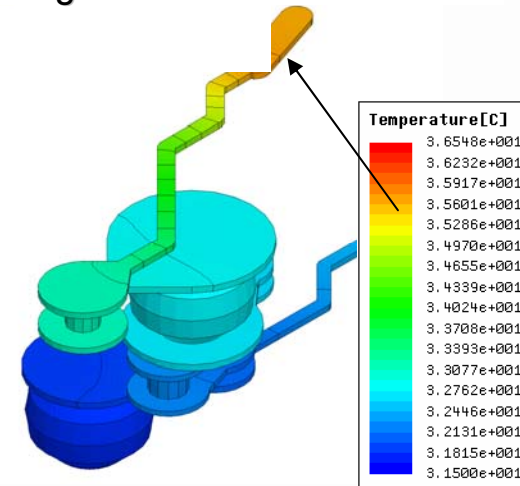
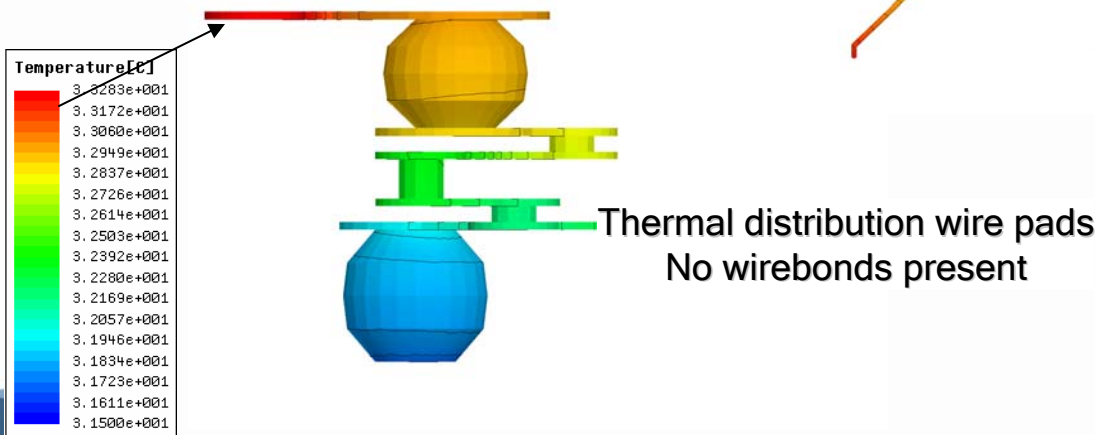
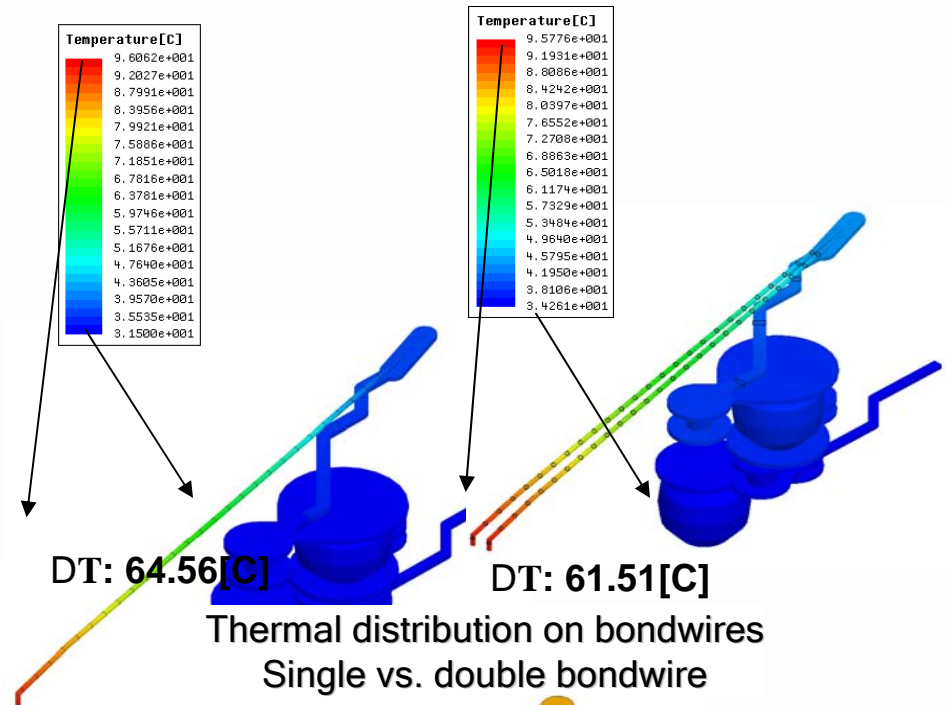
HIGH PERFORMANCE EDA



SI Thermal Effects

➤ ePhysics™

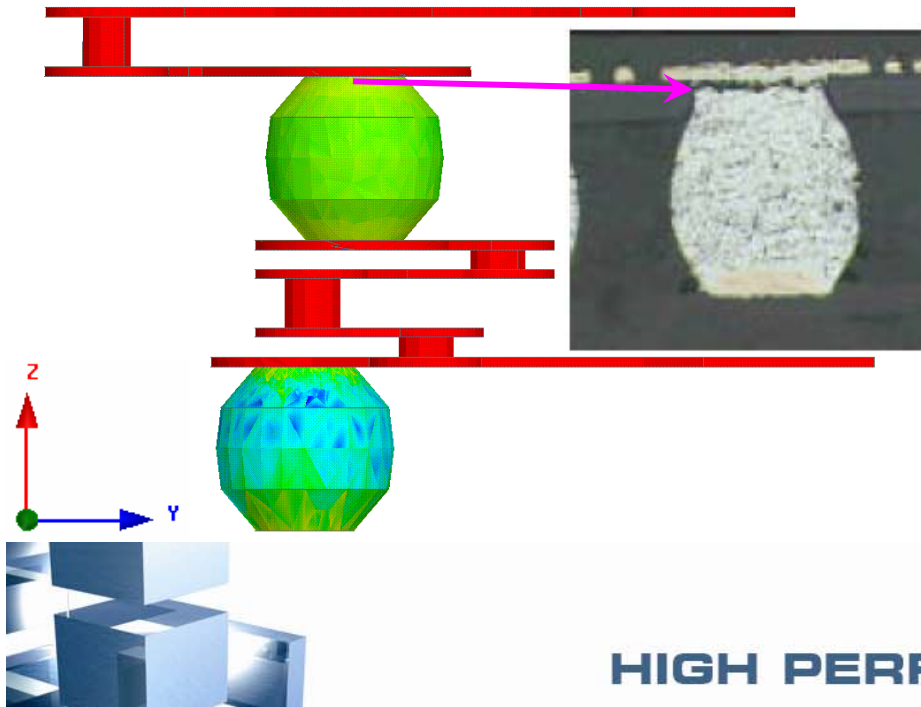
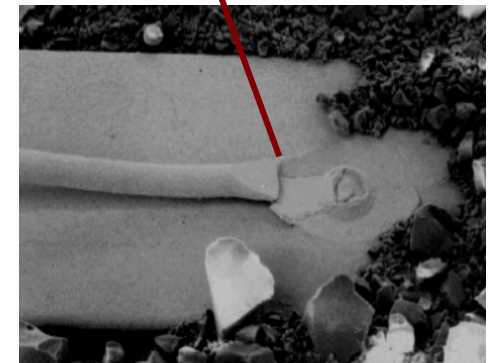
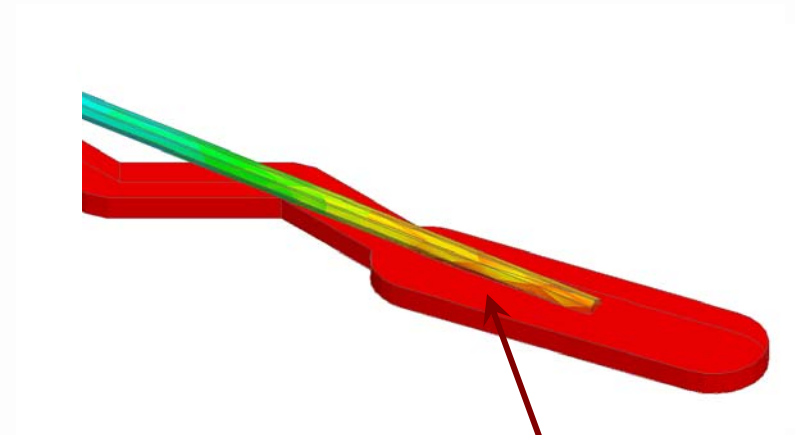
- Critical 3D Thermal and stress analysis
- Solderball interconnect reliability
- Stress induced strains in solder joints



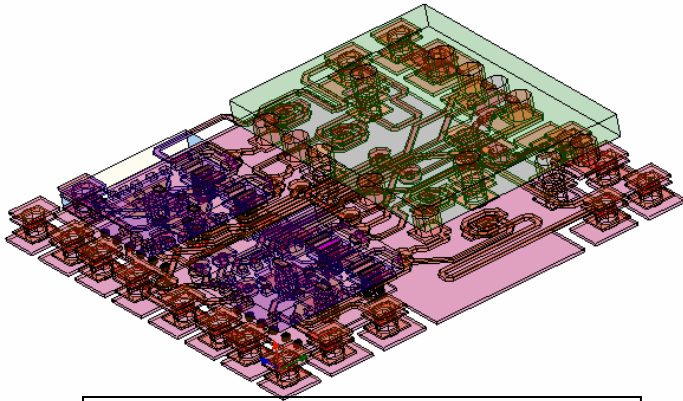
SI Mechanical Effects

➤ ePhysics™

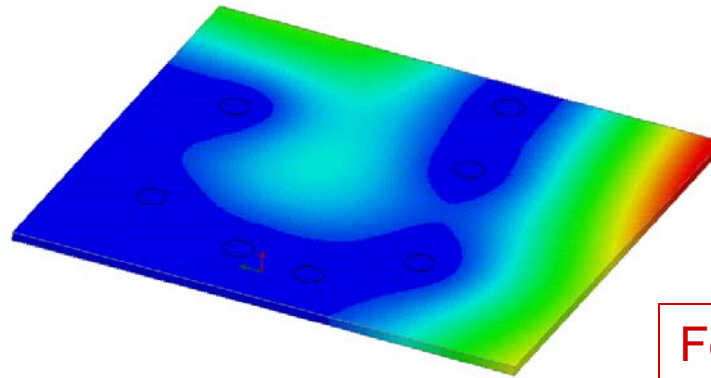
- Reduced design cycle time limits the use of testing to evaluate reliability.
- Stress induced strains in solder joints



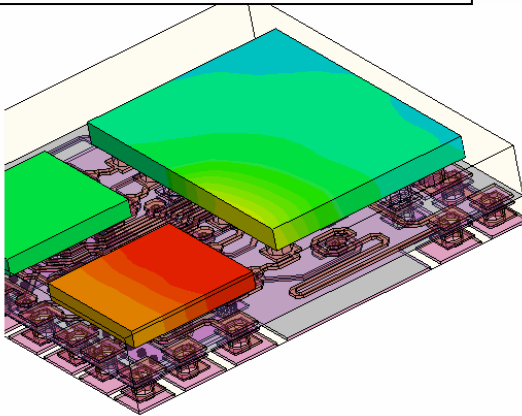
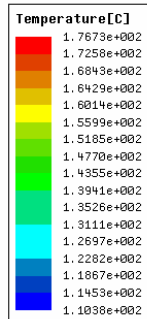
PCB Thermal and Stress Analysis



Thermal PCB simulation



"Bed of pins" stress simulation



Forced convection model

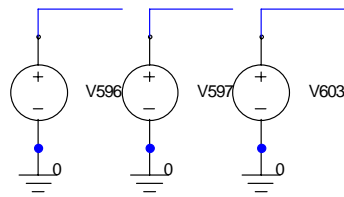
Features:

- Complex geometry;
- Anisotropic thermal material properties;
- Anisotropic stress material properties;
- Large thermal / stress FEM models



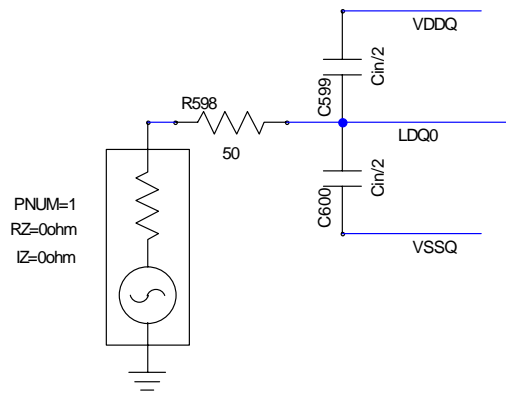
DDR2 Memory Channel

8Bit DQ Bus Channel



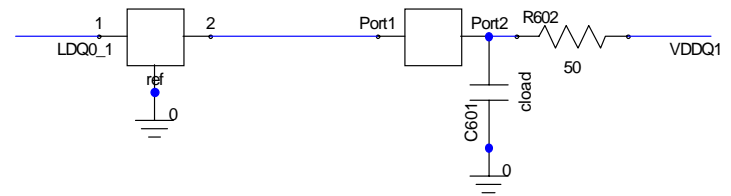
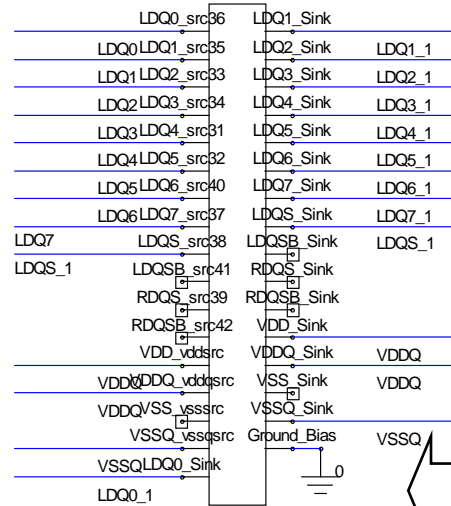
S-parameter model
TRL line

S-parameter model
FBGA model



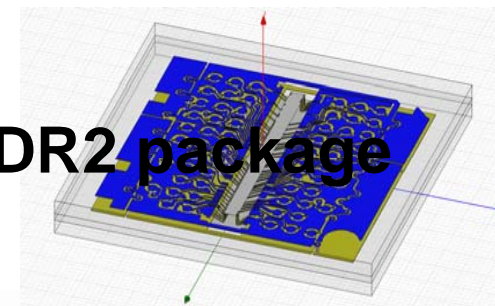
Digital Source

Unique Bit sequence source
for jitter analysis



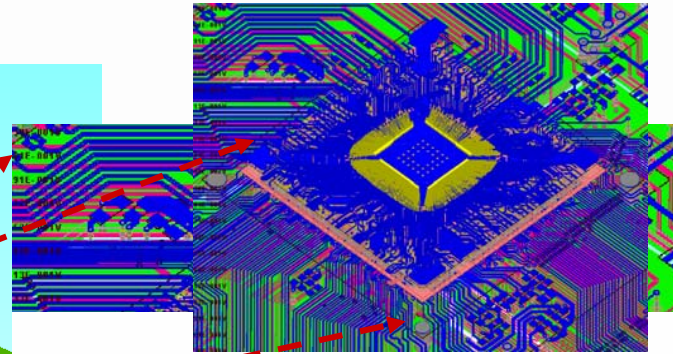
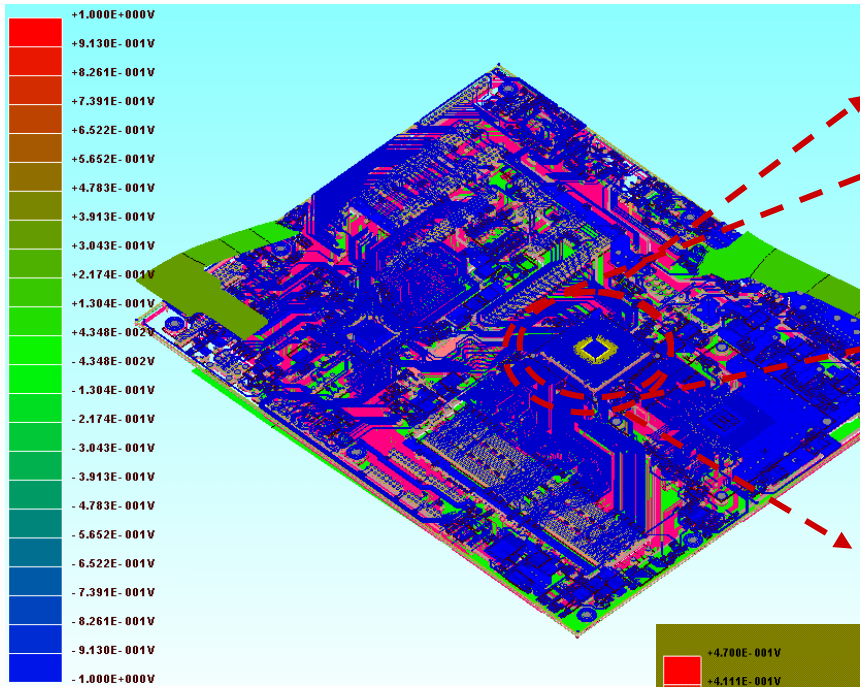
Direct import function keeps
track of connections

DDR2 package

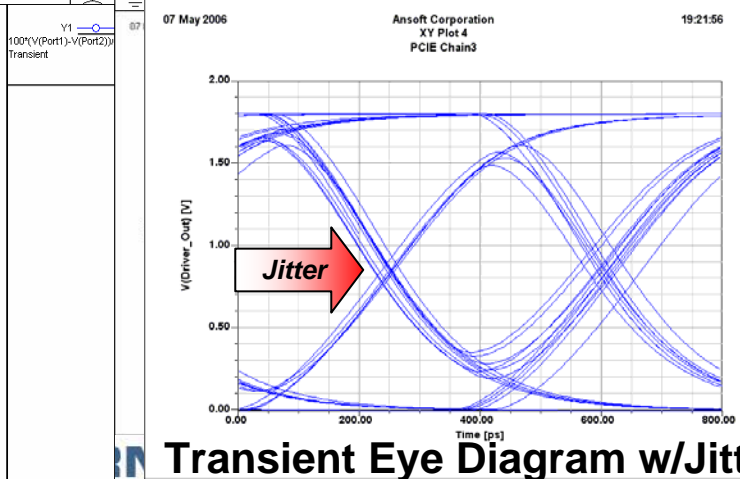
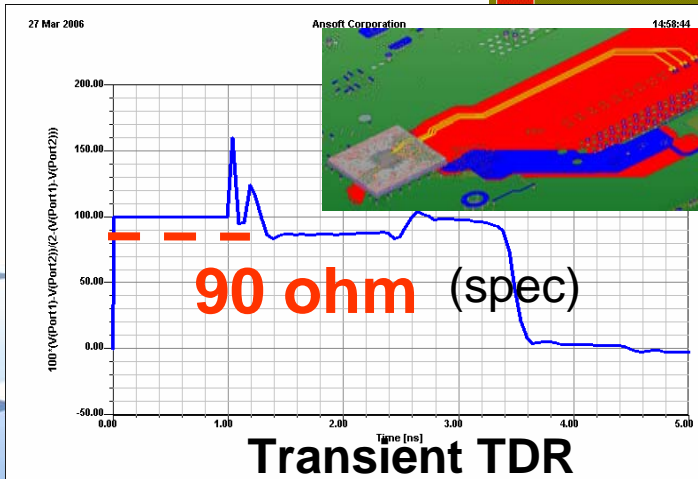
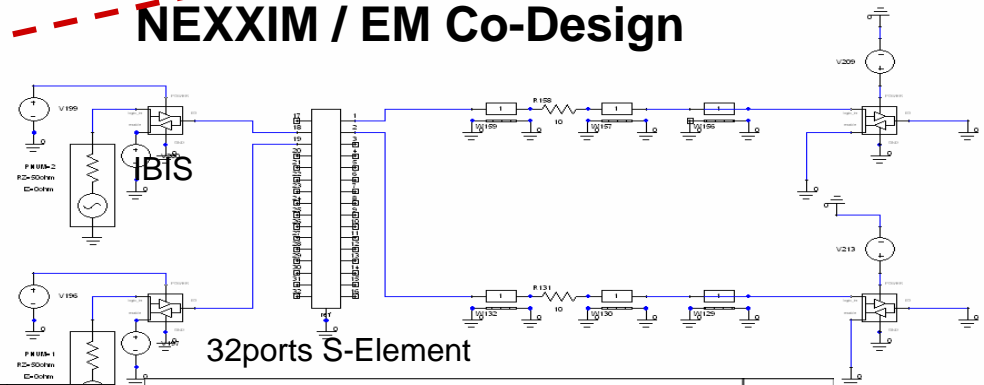


10/31/2006

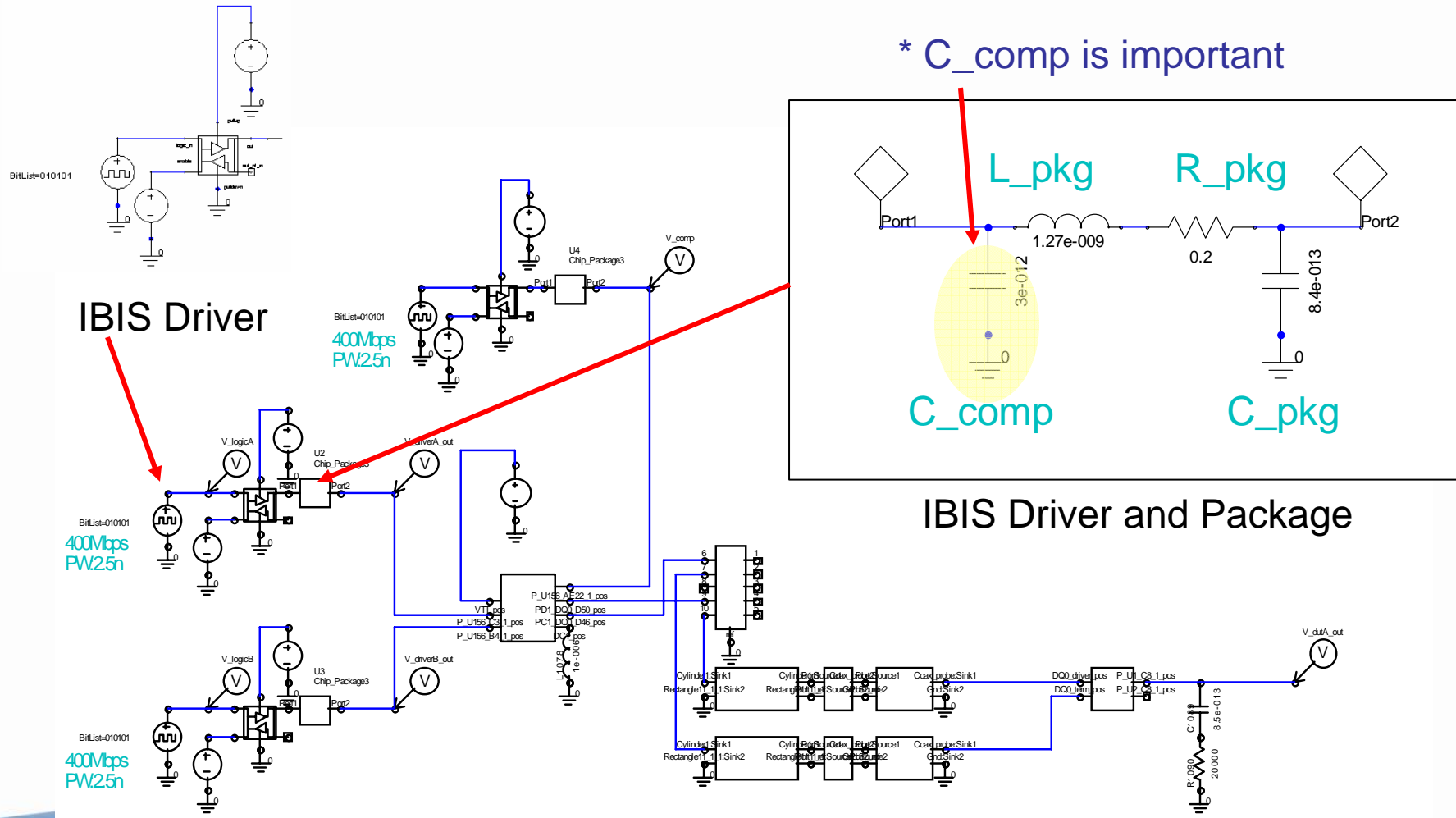
DDR2 Package on PCB



NEXXIM / EM Co-Design



DDR Memory Test System



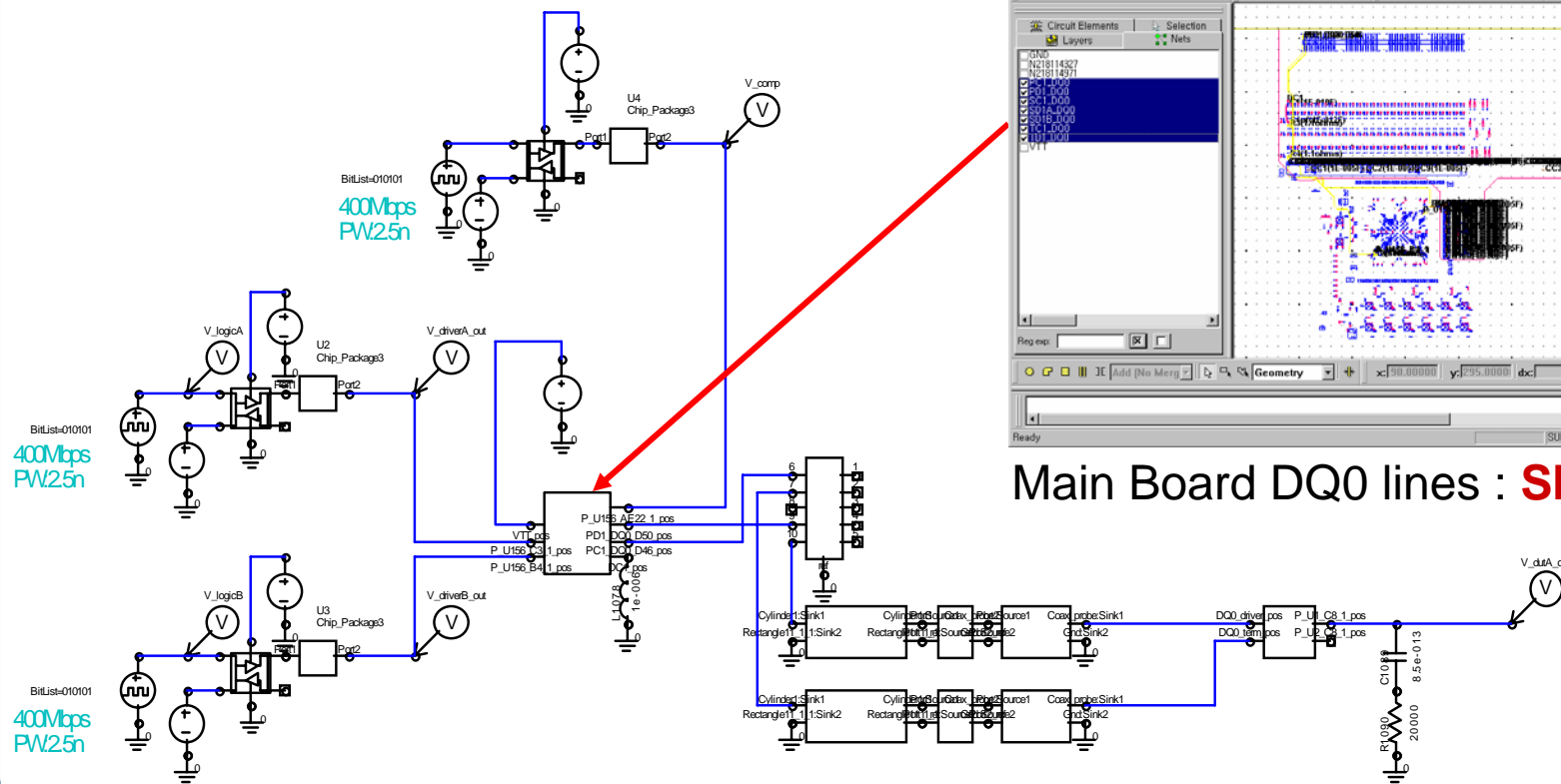
HIGH PERFORMANCE

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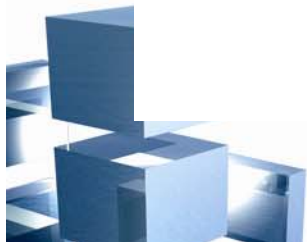
ANSOFT

DDR Memory Test System

* Series R and Swt. Included in DQ line



Main Board DQ0 lines : **Slwave**

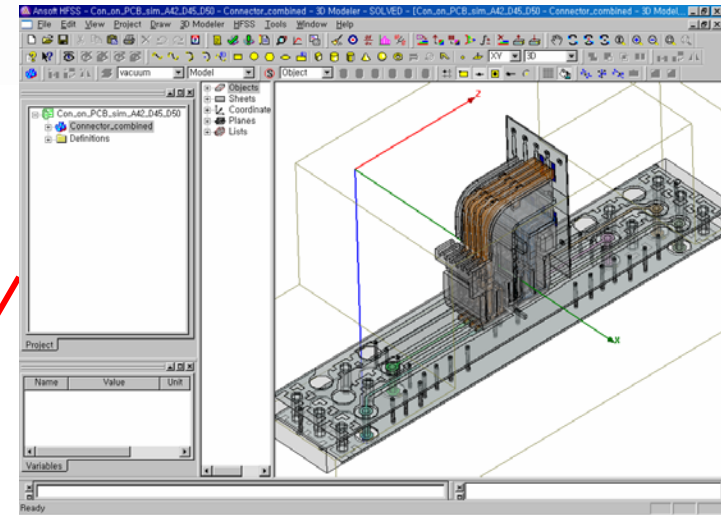
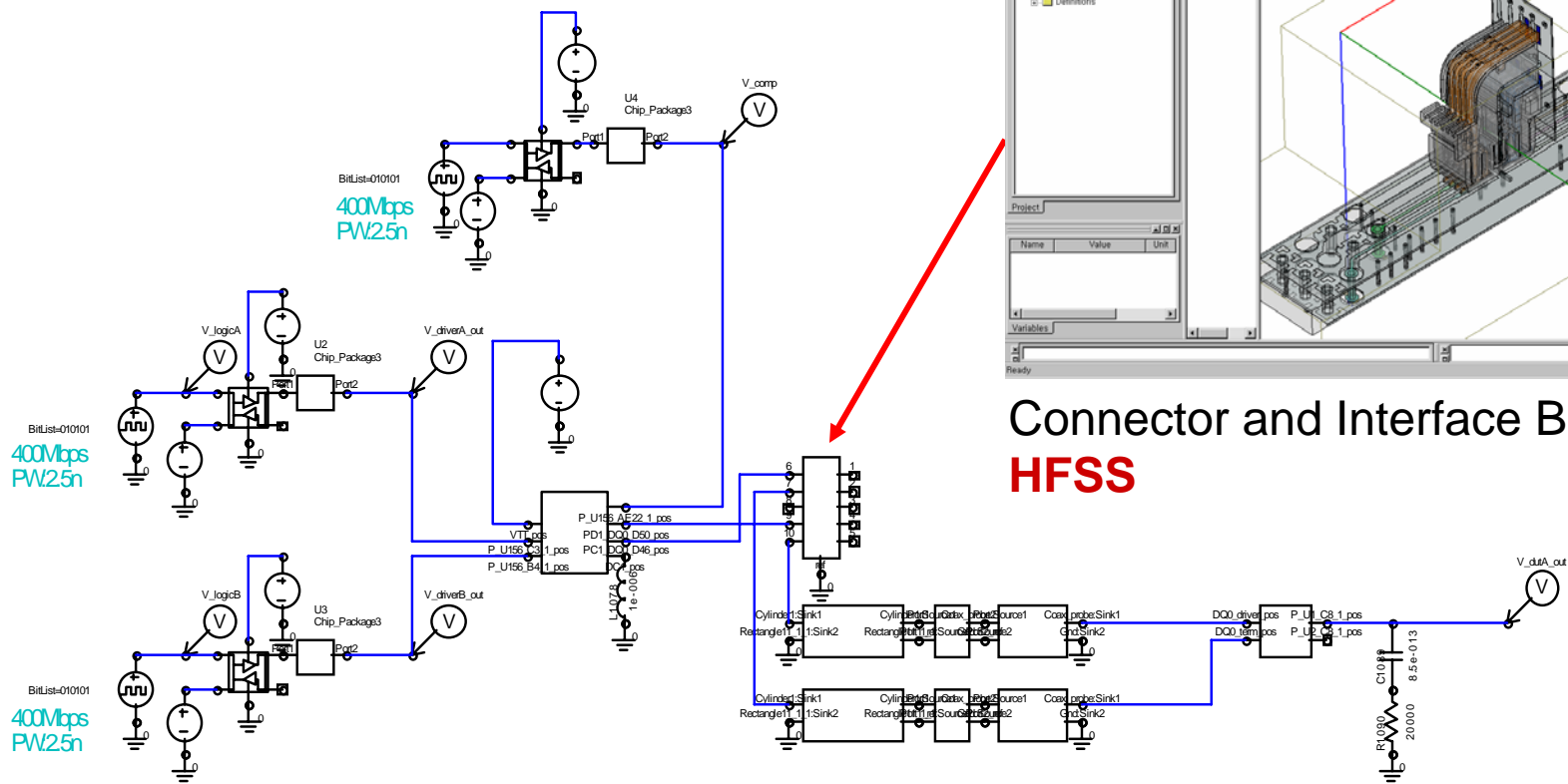


HIGH PERFORMANCE

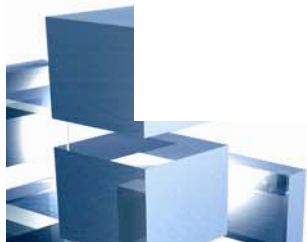
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DDR Memory Test System



Connector and Interface Board :
HFSS

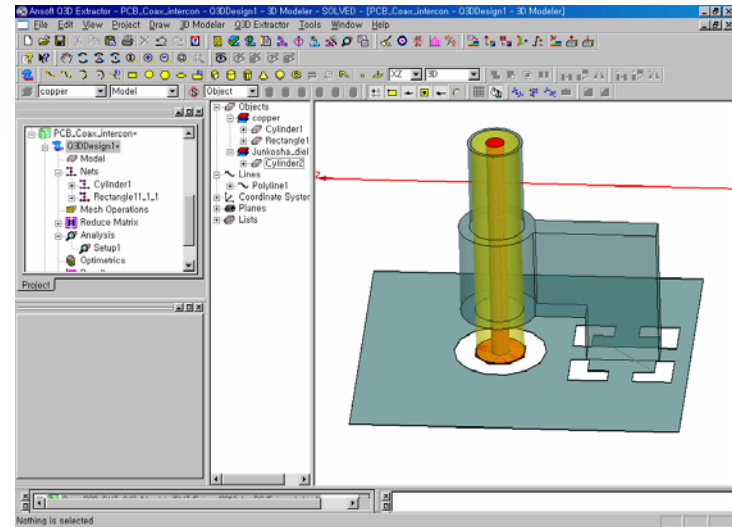
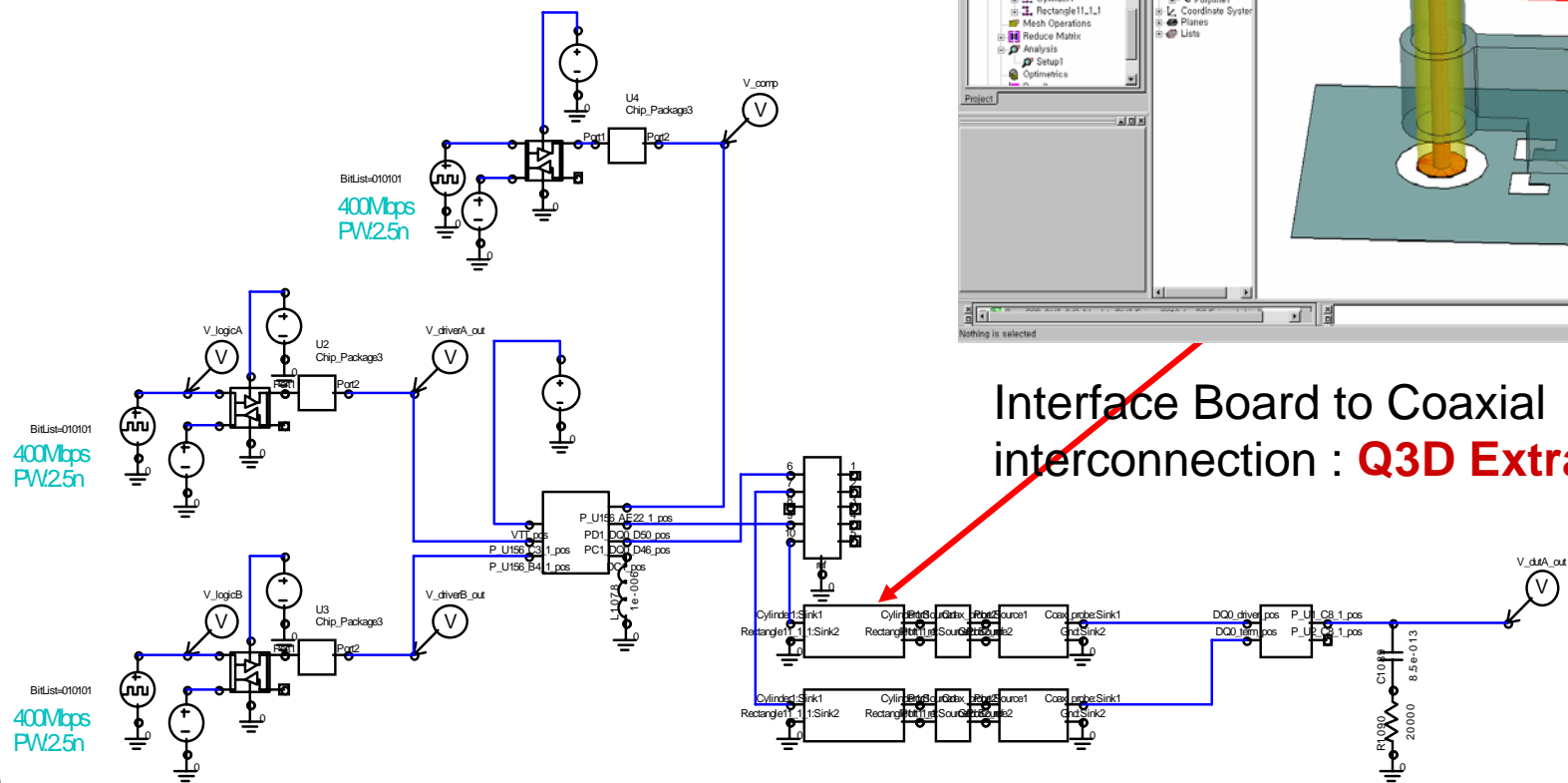


HIGH PERFORMANCE

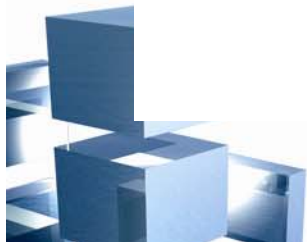
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DDR Memory Test System



Interface Board to Coaxial interconnection : **Q3D Extractor**



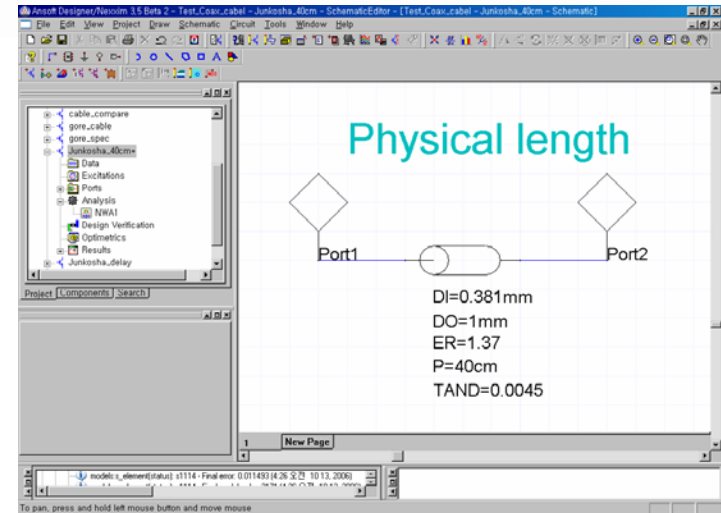
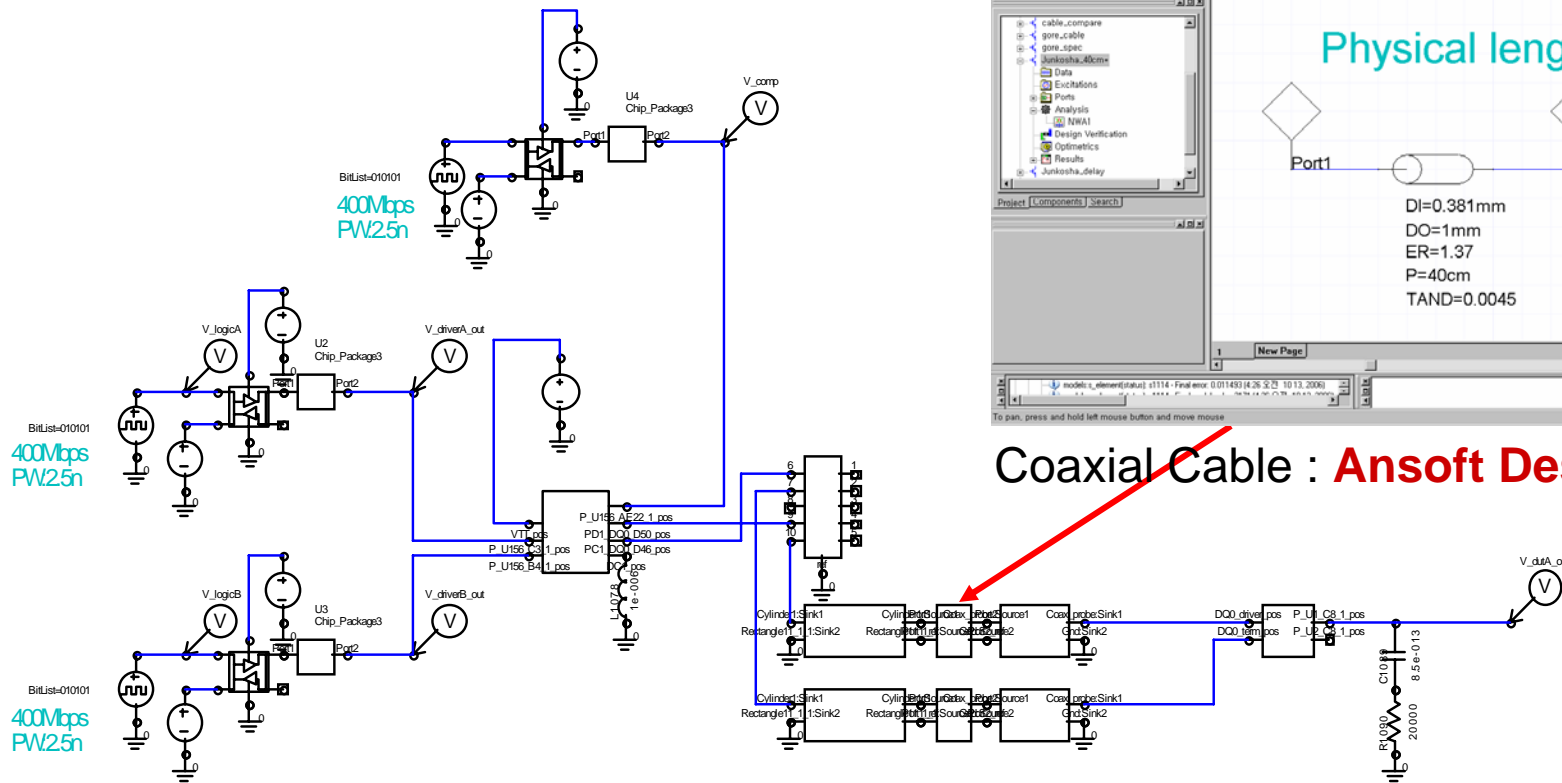
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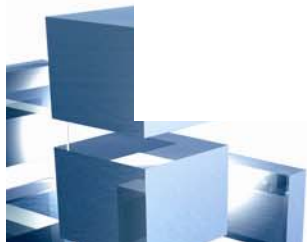
ANSOFT

DDR Memory Test System

* Er and TAND Optimized from Data Sheet (Delay and Attenuation)



Coaxial Cable : **Ansoft Designer**

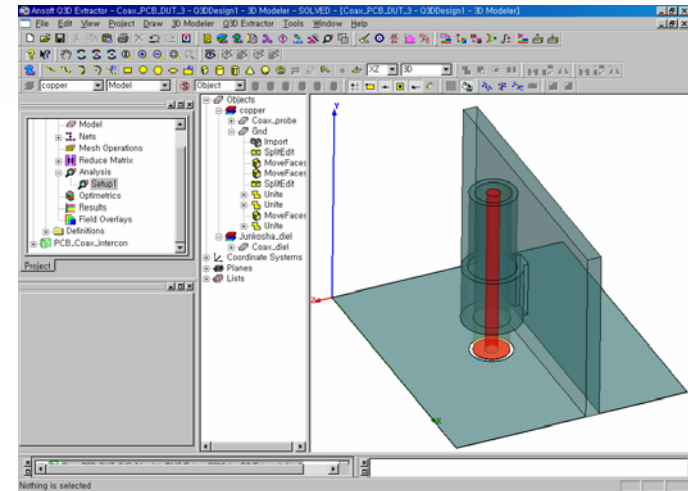
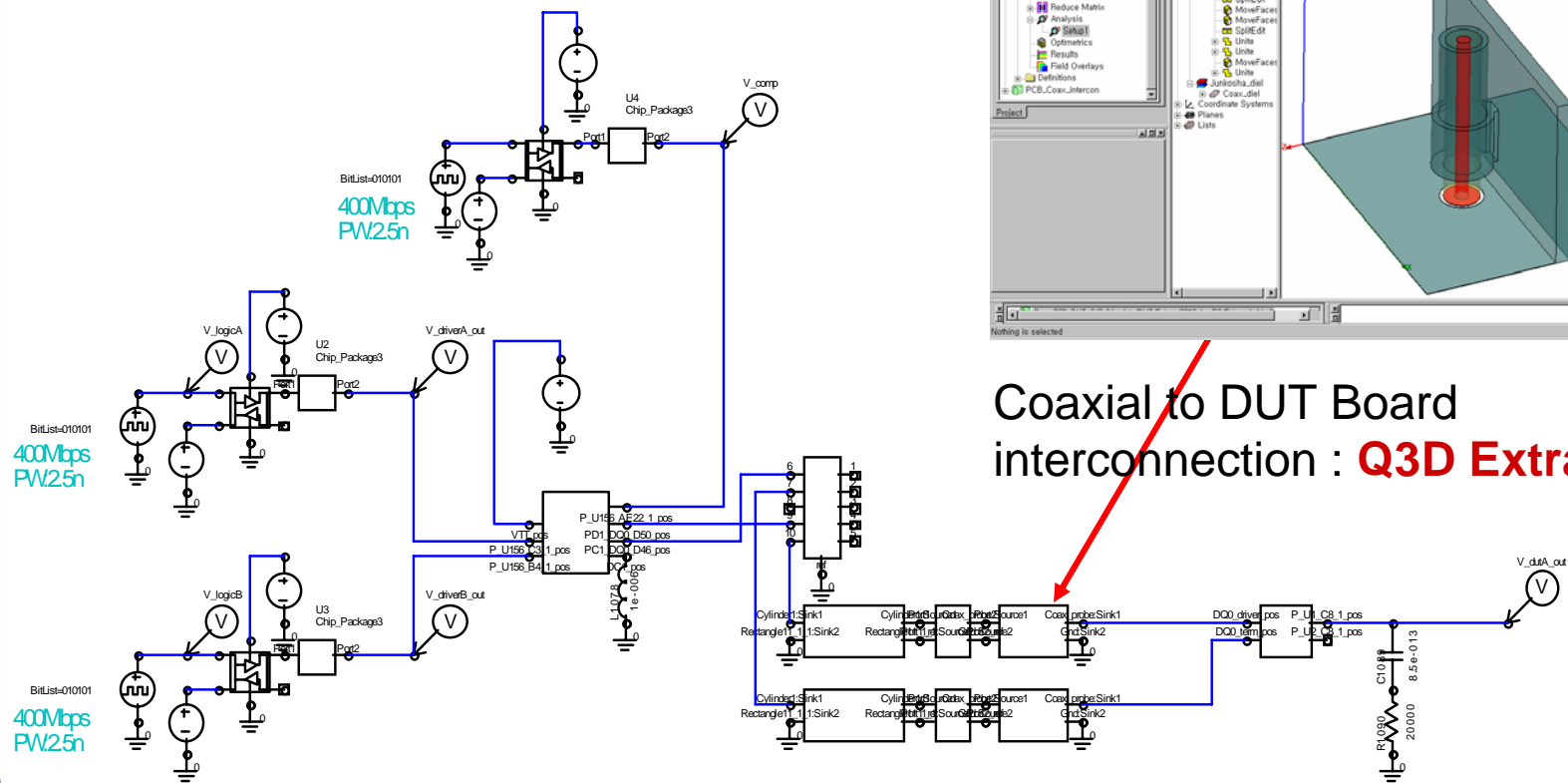


HIGH PERFORMANCE

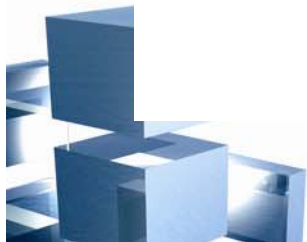
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DDR Memory Test System



Coaxial to DUT Board
interconnection : **Q3D Extractor**

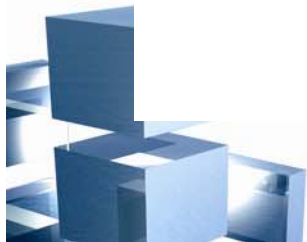
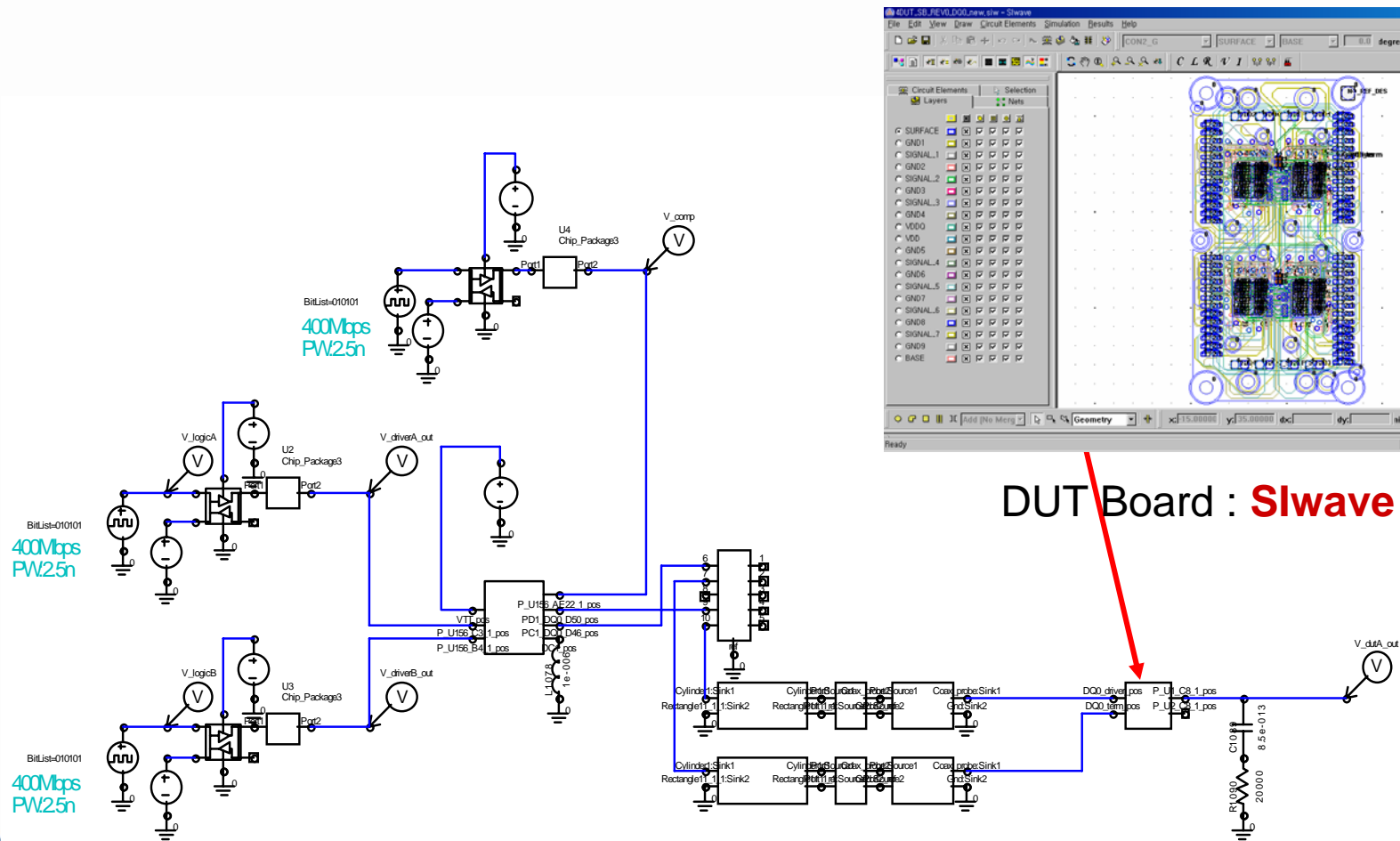


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DDR Memory Test System

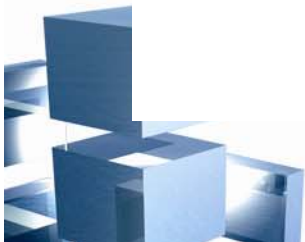
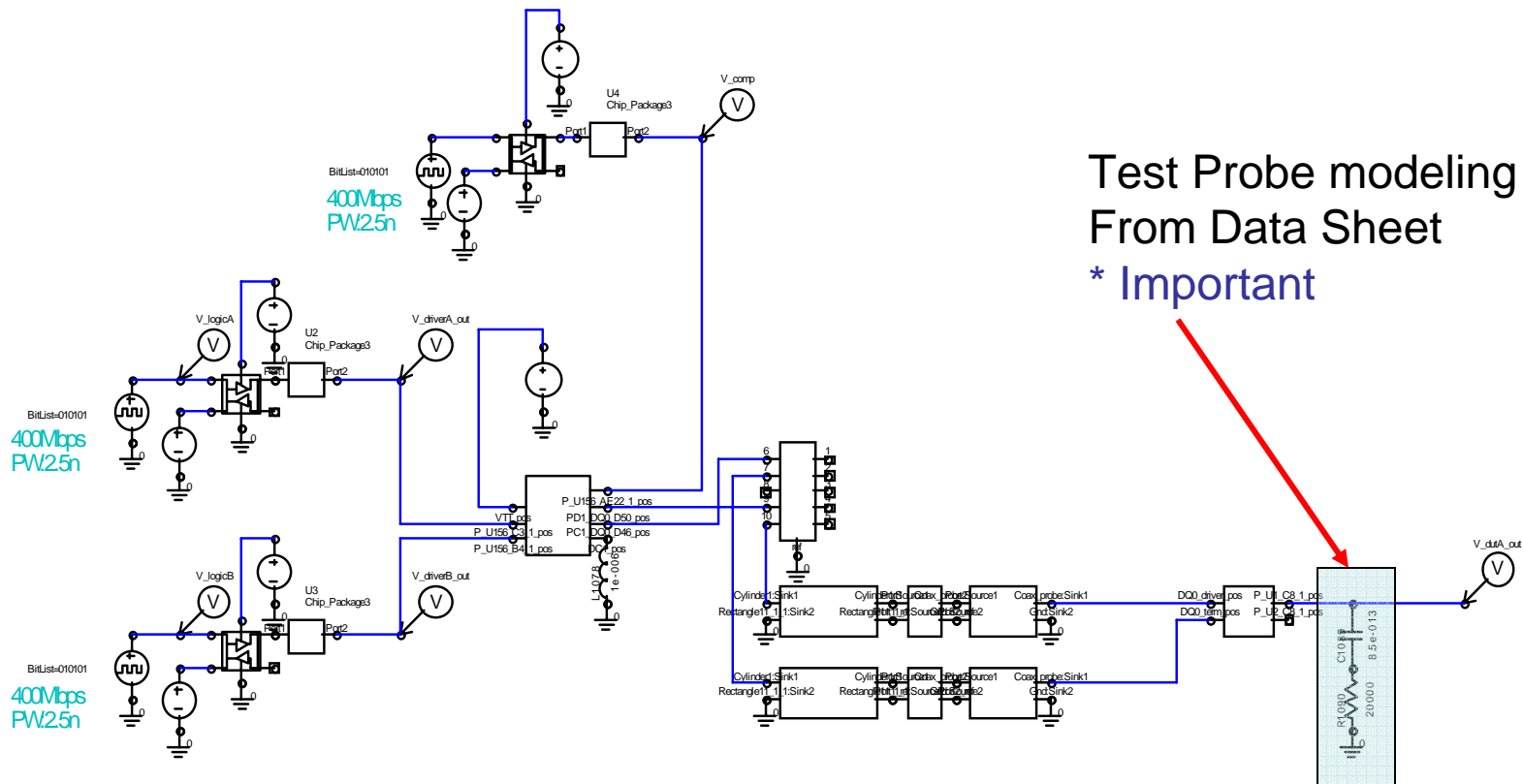


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DDR Memory Test System

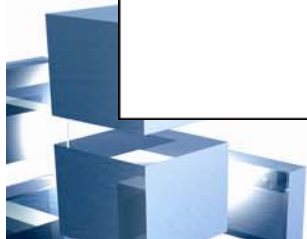
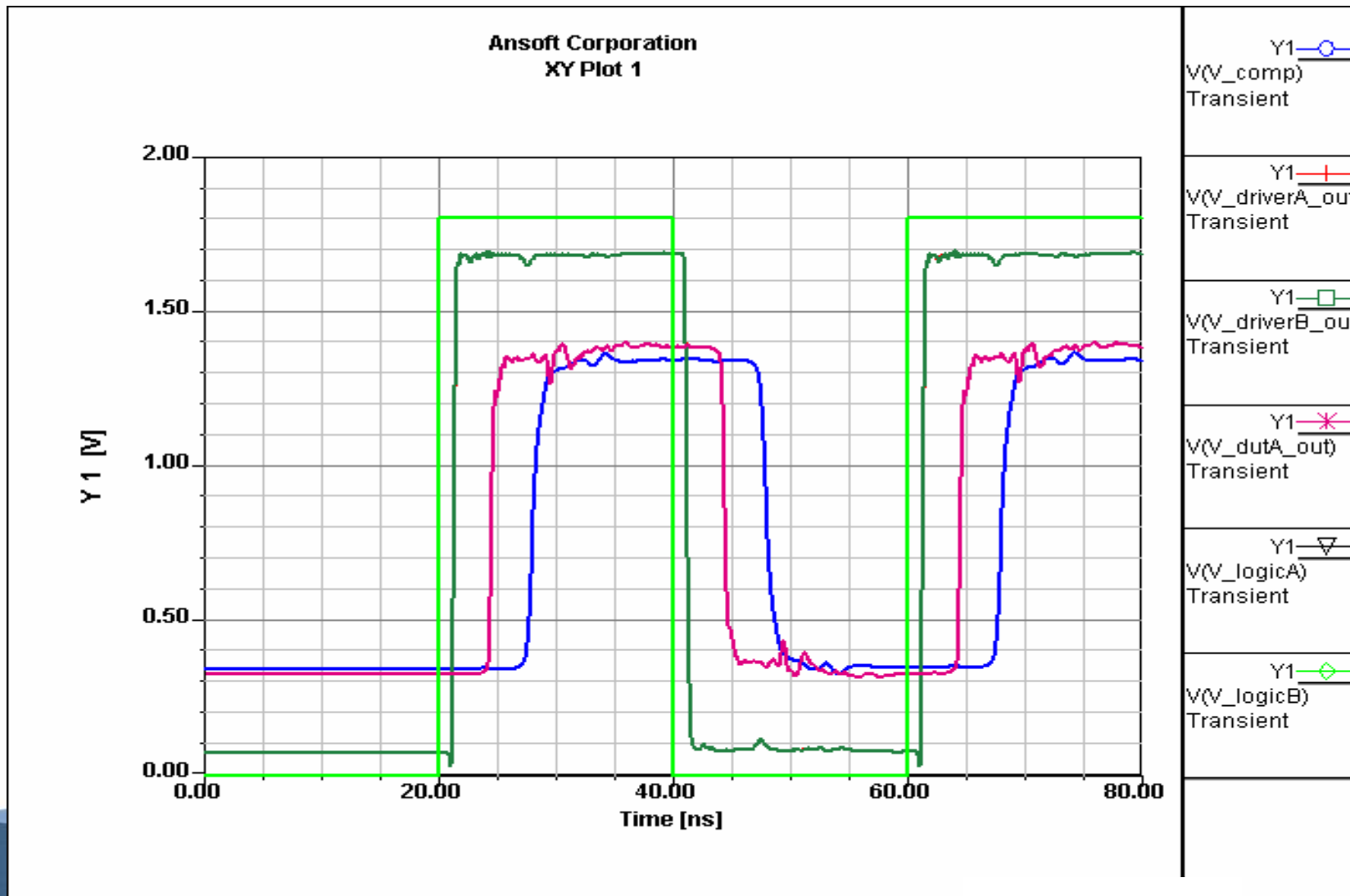


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Ansoft Results : 50Mbps DQ0

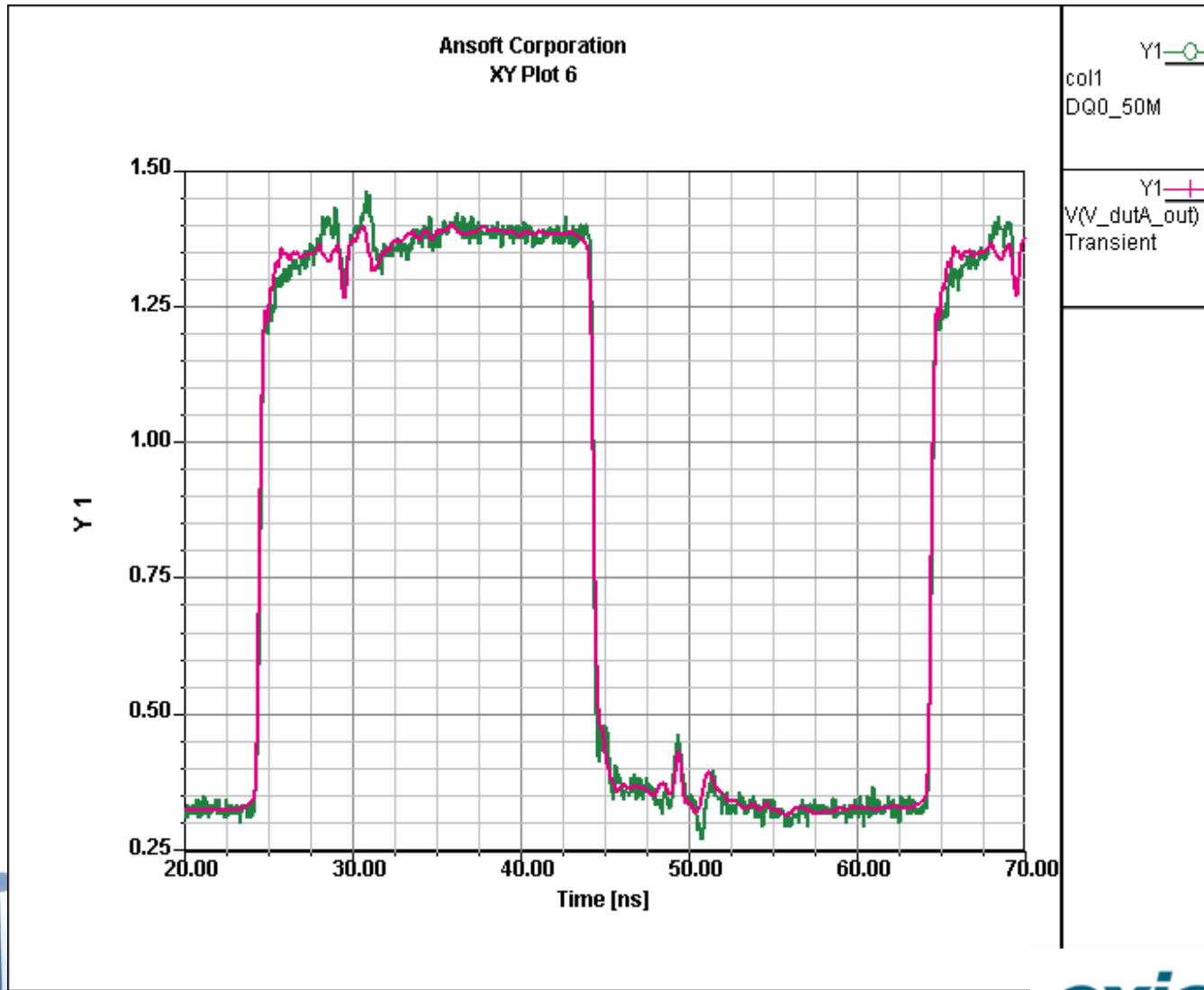


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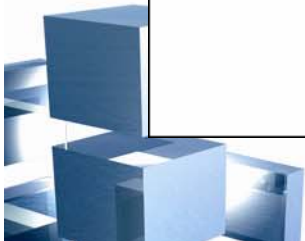
Measurement and Ansoft Results



: Measurement

: Ansoft

50Mbps DQ0

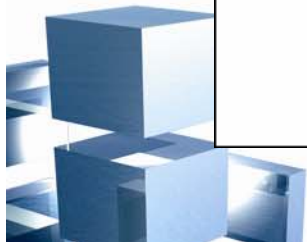
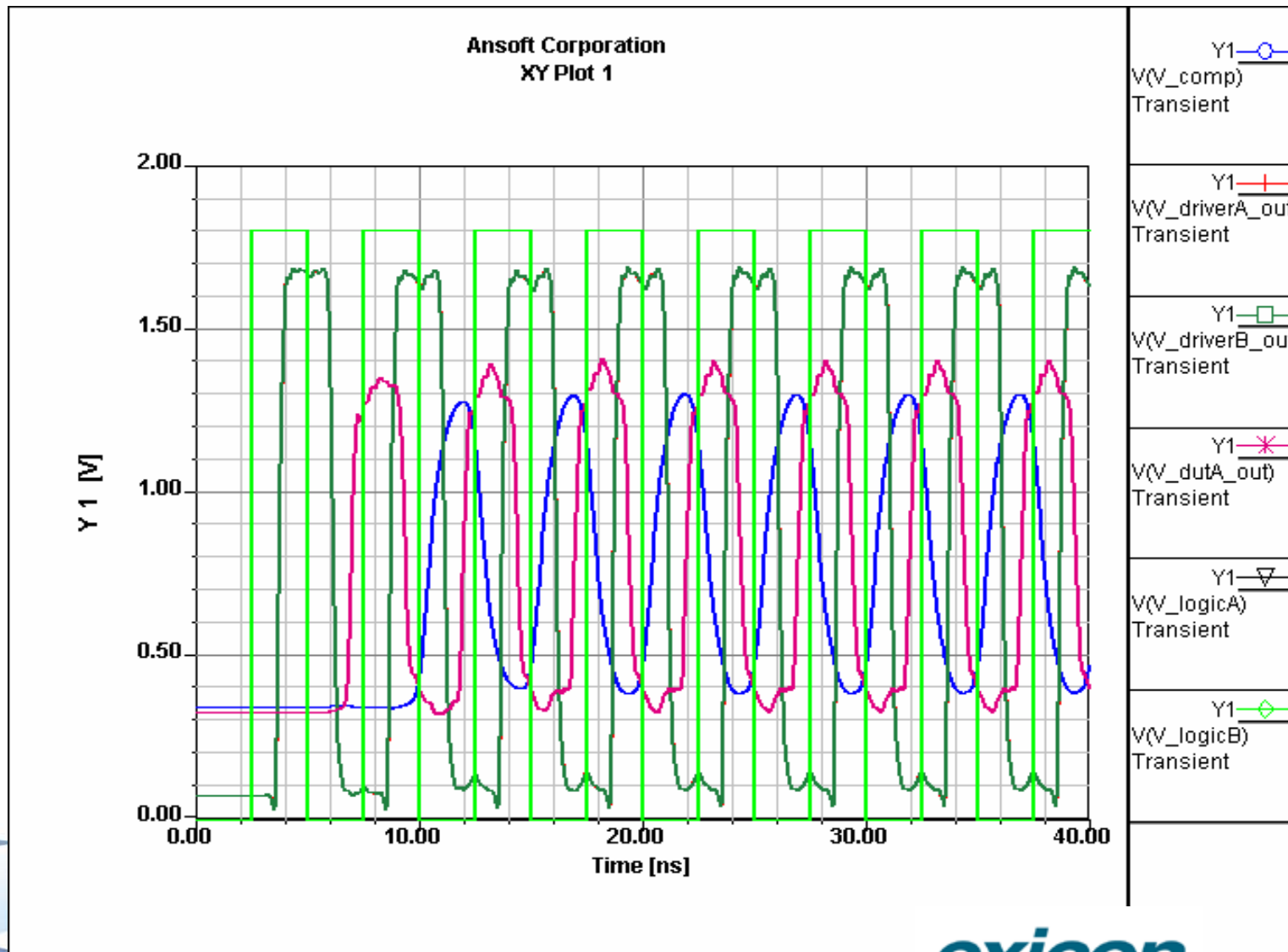


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Ansoft Results : 400Mbps DQ0

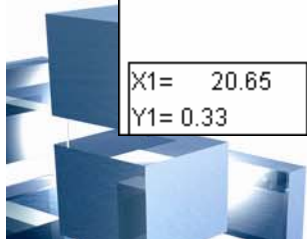
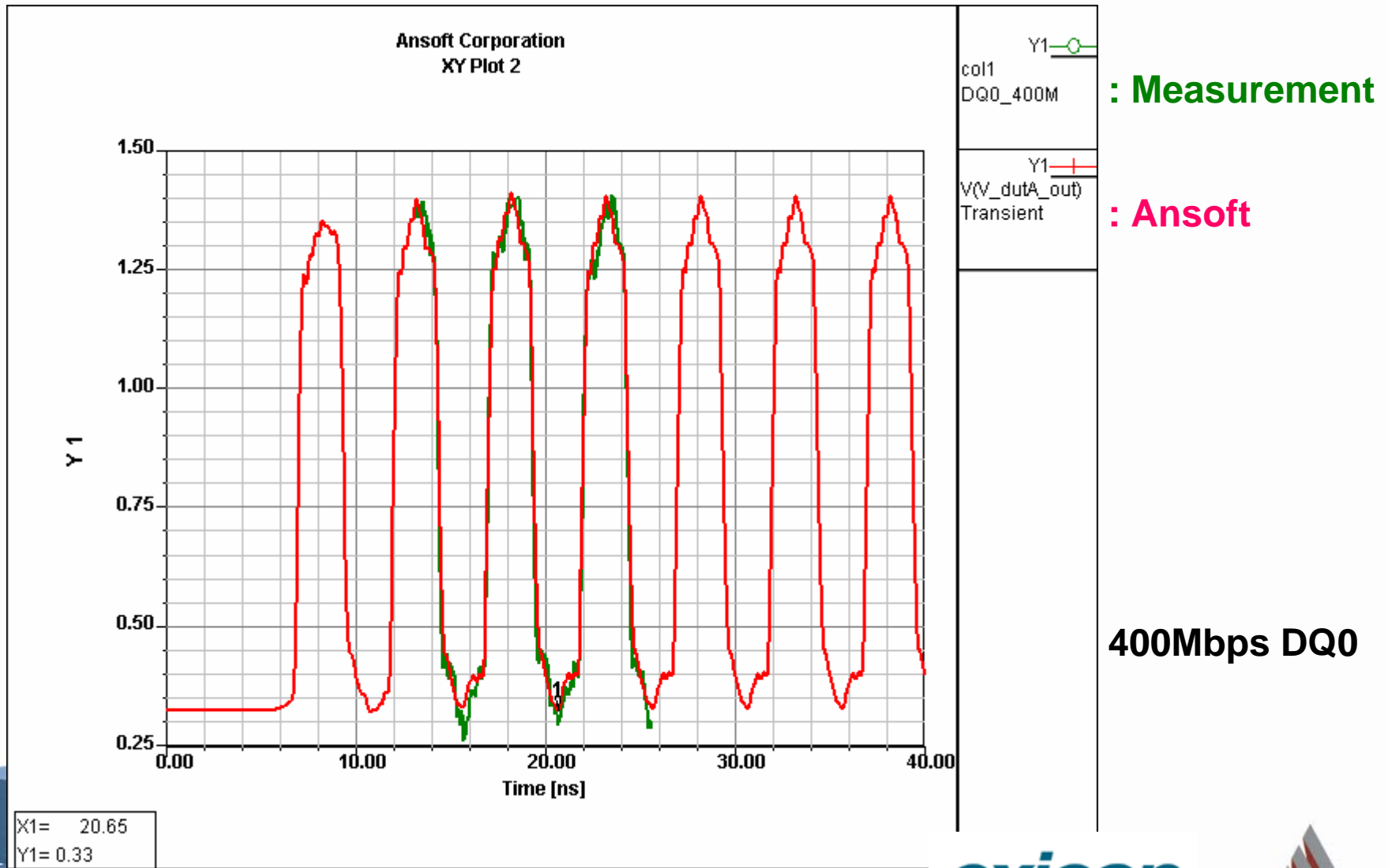


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Measurement and Ansoft Results

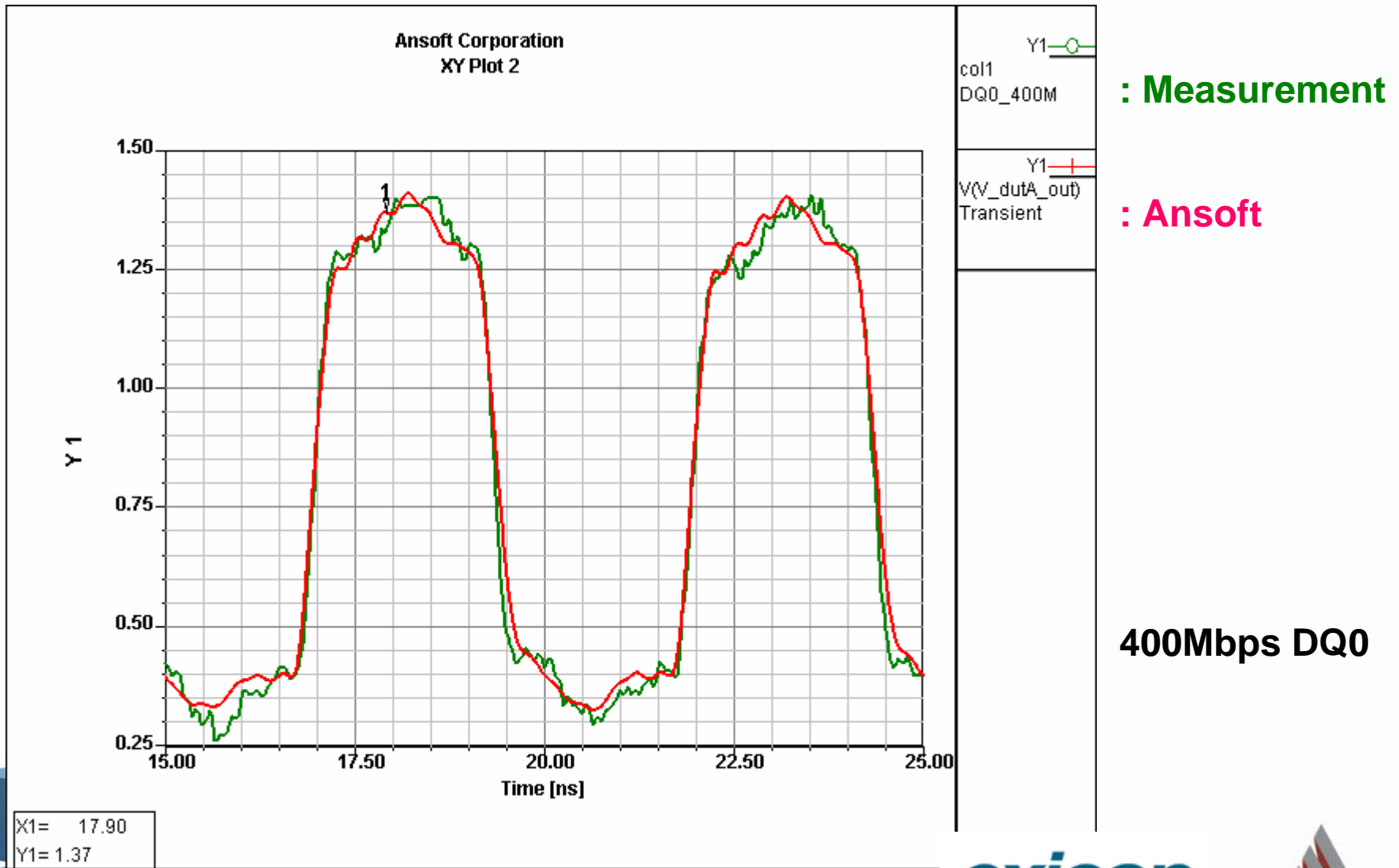


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Measurement and Ansoft Results

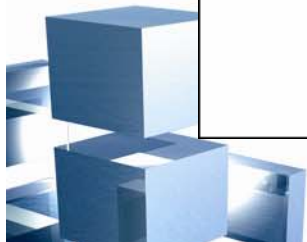
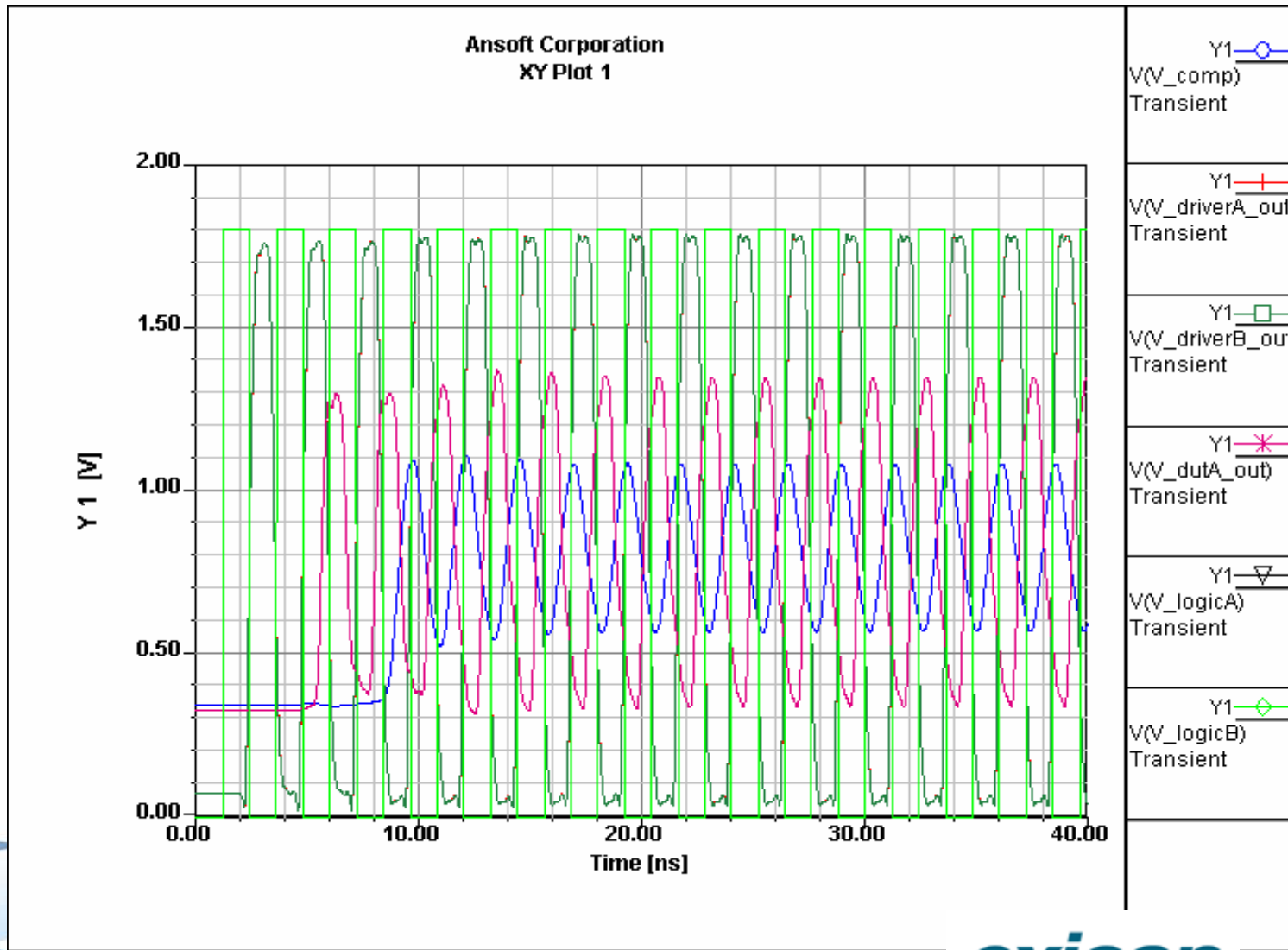


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ANSOFT

Ansoft Results : 830Mbps DQ0

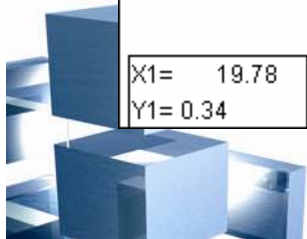
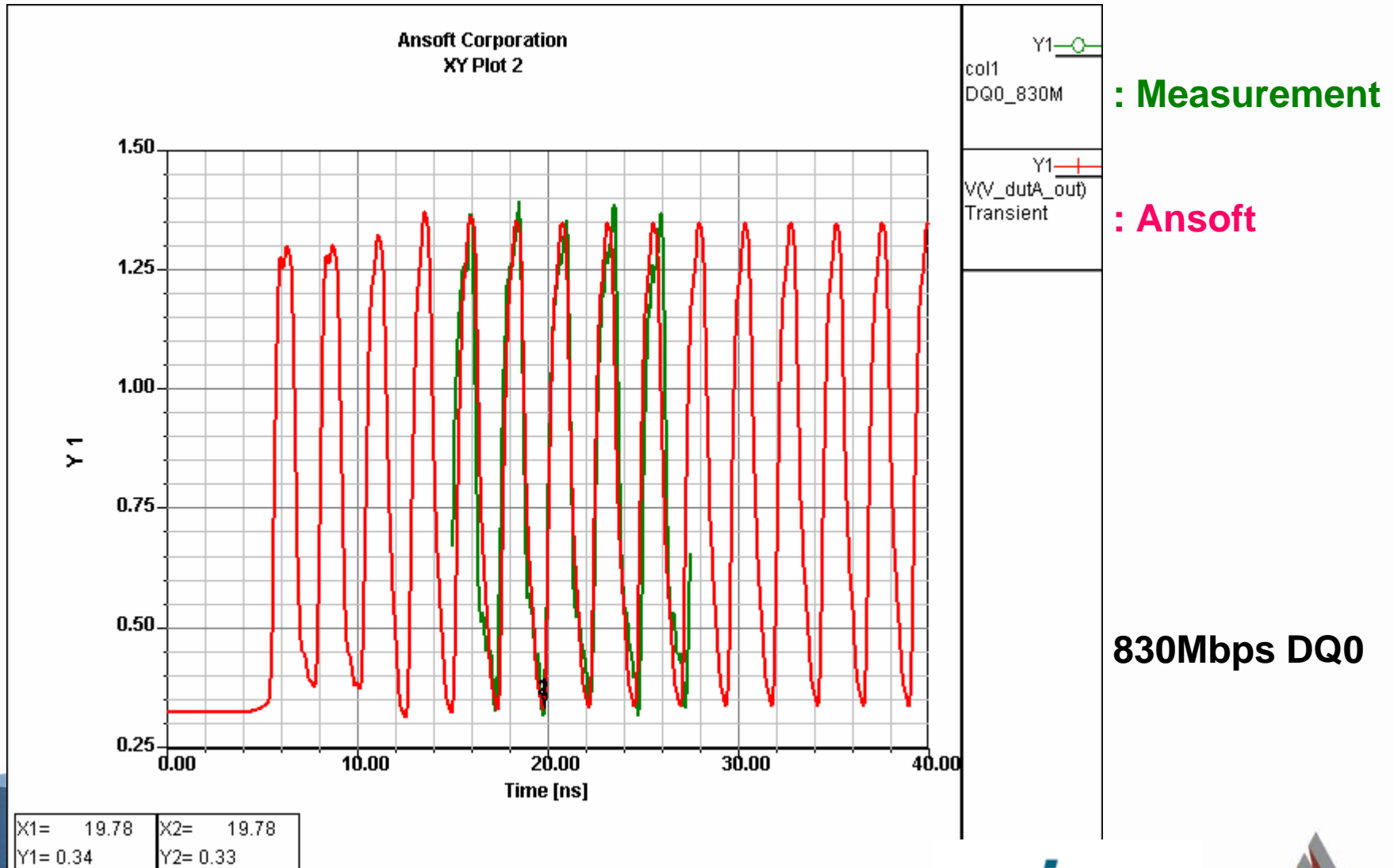


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Measurement and Ansoft Results

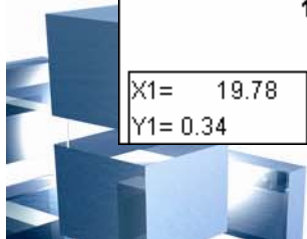
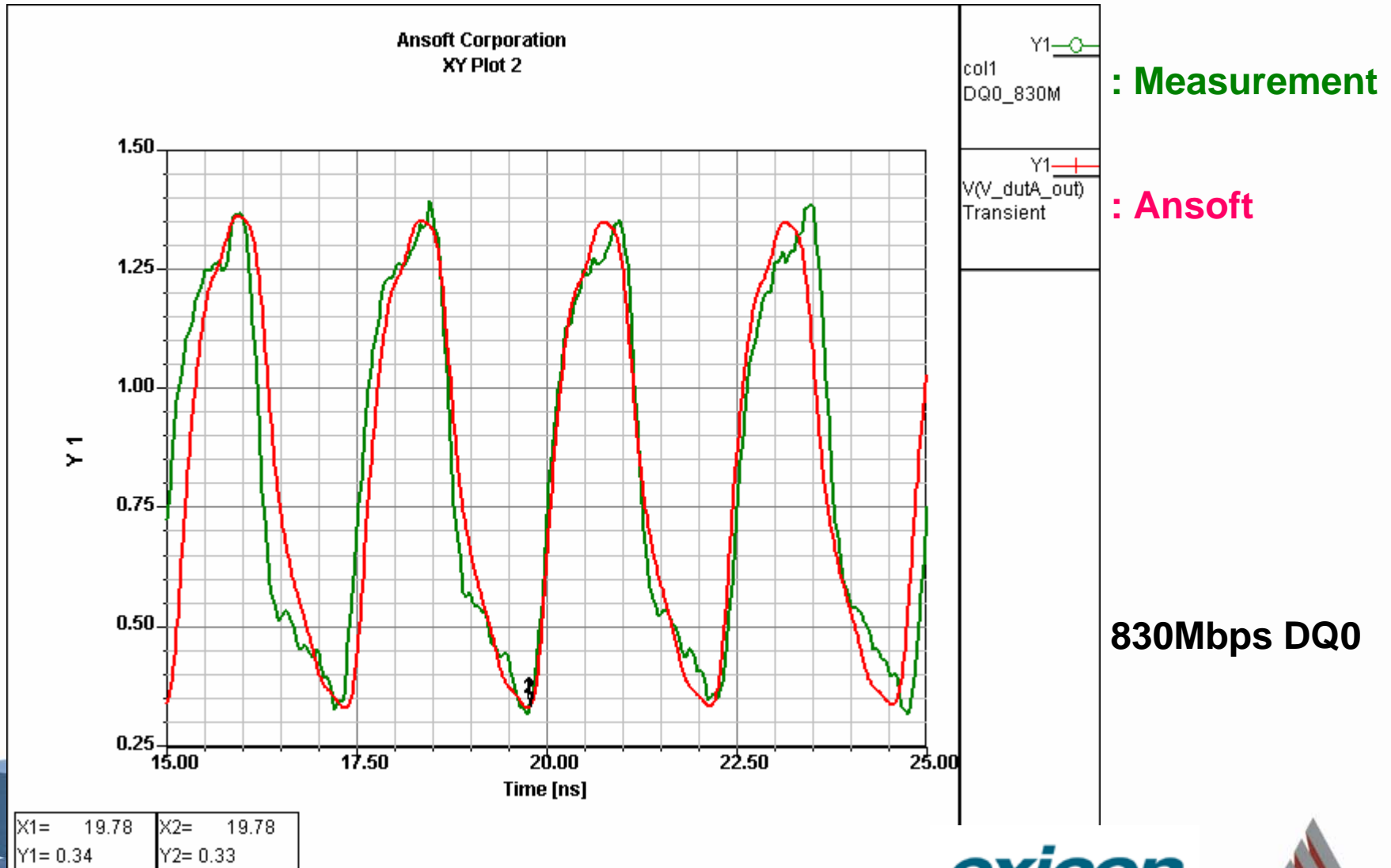


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Measurement and Ansoft Results



HIGH PERFORMANCE

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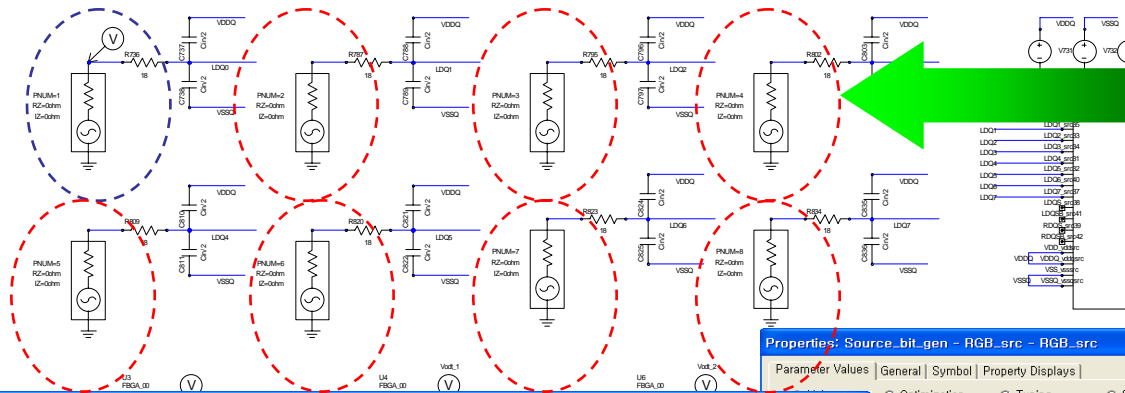


Bit Pattern

1. - Jitter noise analysis (time domain)

Eye diagram is useful for jitter analysis for DQ Bus.
1 DQ pin is Victim, another pin is Aggressor.

Source is text file.
(voltage profile)



Source Selection

Voltage Power

Name: Piecewise1

Type: Piecewise Linear

Parameters | Diagram |

Property	Value	Unit	Description
List			List of waveform points
tone	0	GHz	Frequency for HB analysis
ACMAG			
ACPHASE			
noise			

Piecewise Waveform List

Link to file

"E:/Project/AD3/Hynix_silm/vb_02_ts_0p1" Browse...

Enter time/value points

Time Value

Cancel

Properties: Source_bit_gen - RGB_src - RGB_src

Parameter Values | General | Symbol | Property Displays |

Value Optimization Tuning Sensitivity Statistics

Name	Value	Unit	Evaluated
BIT_PATTERN	10101001010111001100001100111110000111000111010101101010001100111100110000011100011111000111000		
PERIOD	104	104	104
NB	832	832	832
BR	800	MHz	800MHz
T	1.8	V	1.8V
F	0	V	0V

Victim

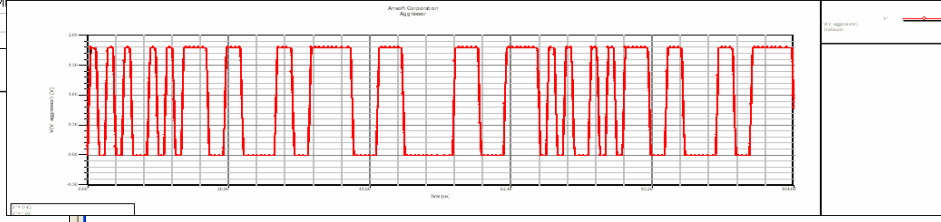
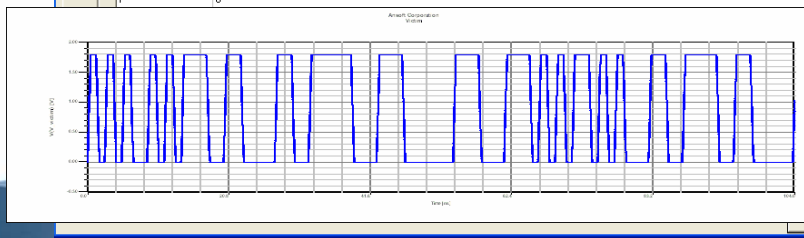
Properties: Source_bit_gen - RGB_src - RGB_src

Parameter Values | General | Symbol | Property Displays |

Optimization Tuning Sensitivity Statistics

Name	Value	Unit	Evaluated
BIT_PATTERN	10101001010111001100001100111110000111000111010101101010001100111100011000001110001111000111000		
PERIOD	104	104	104
NB	832	832	832
BR	800	MHz	800MHz
T	1.8	V	1.8V
F	0	V	0V

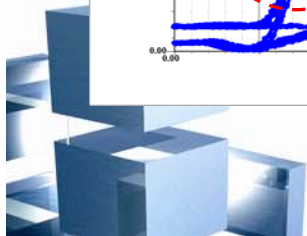
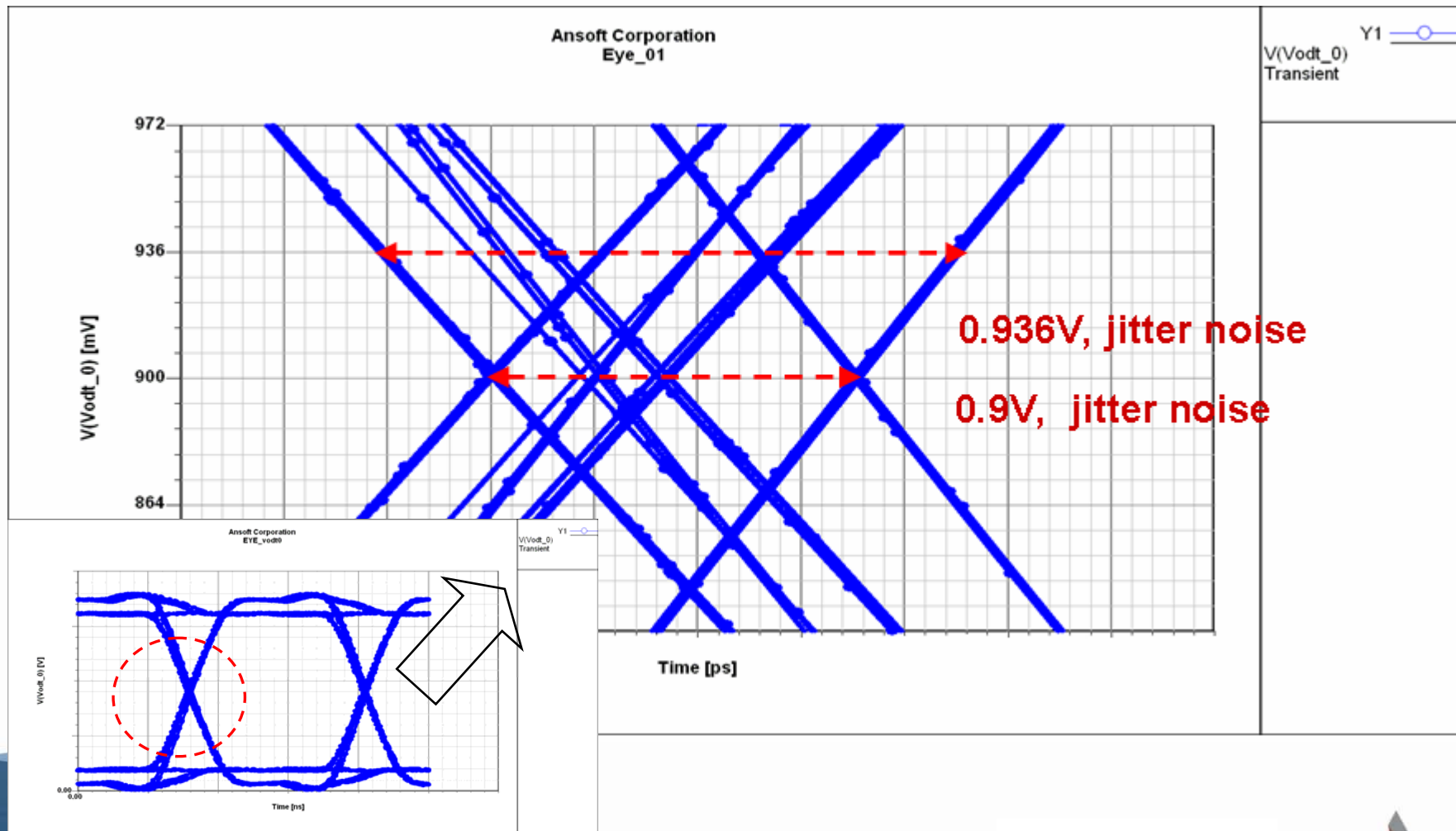
Aggressor



10/31/2006

DDR2 Channel Jitter Analysis

Jitter Noise analysis in Vodt pin (Within 2 % signal voltage)

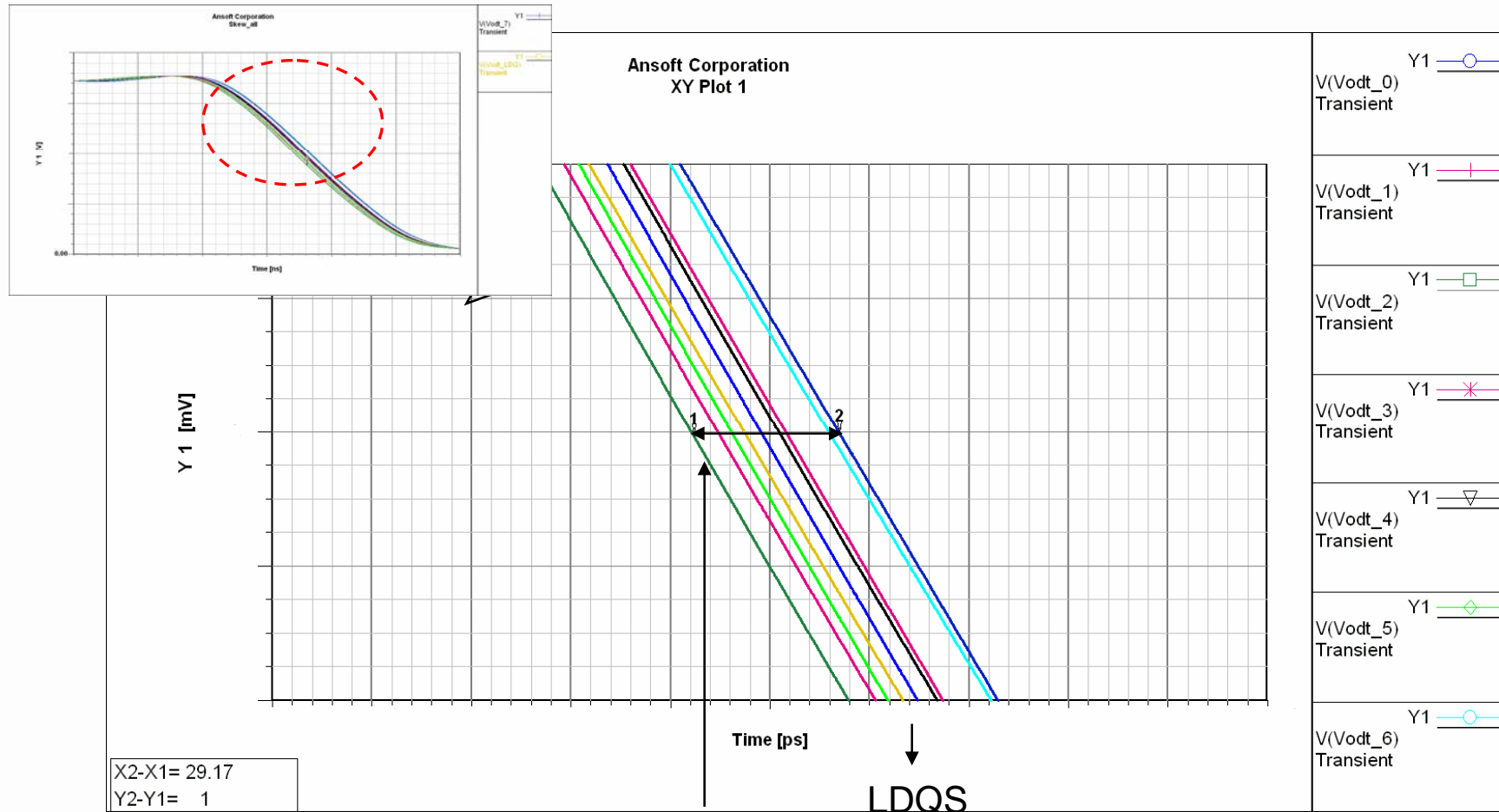


HIGH PERFORMANCE

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Skew Analysis (LDQ Bus vs. LDQS)



Maximum Skew value

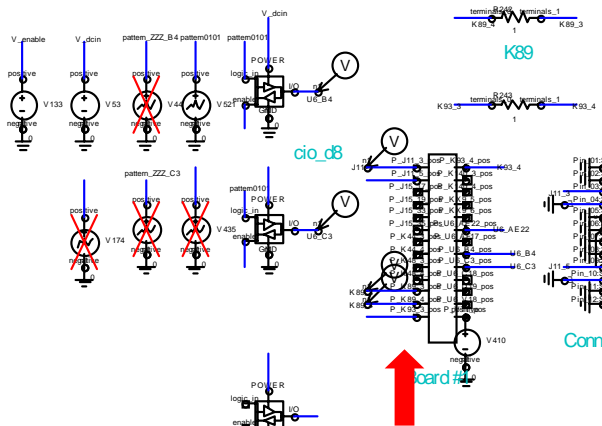
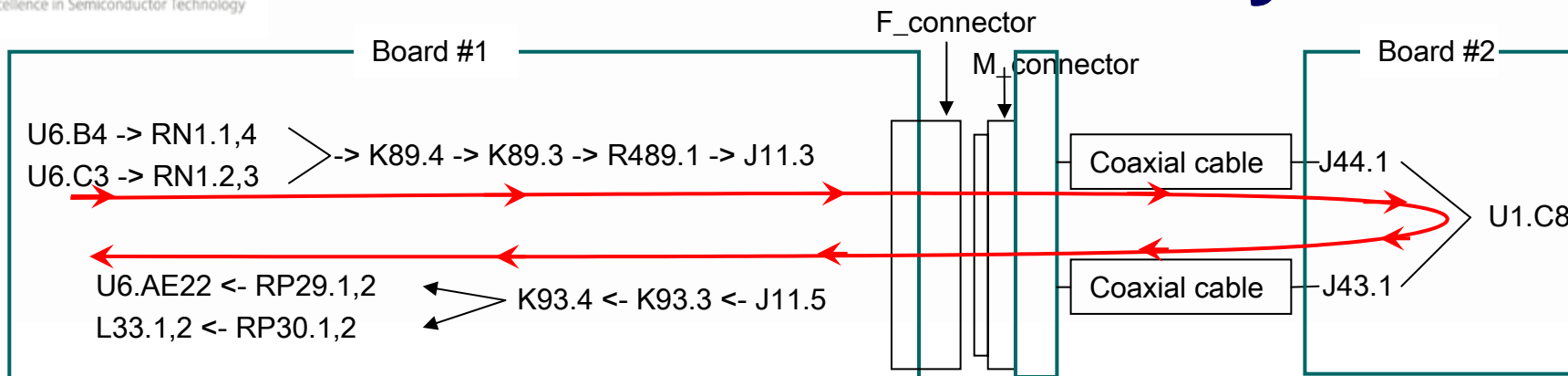


HIGH PERFORMANCE

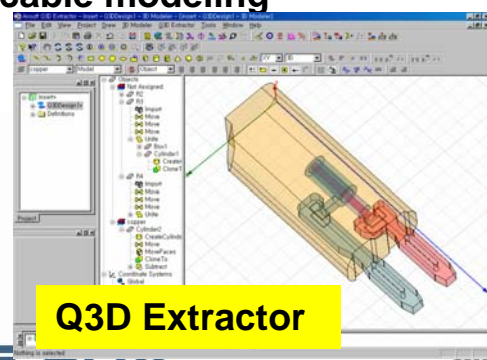
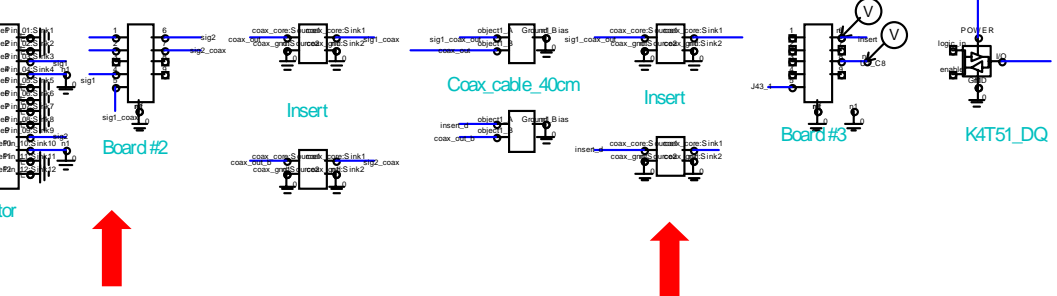
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Full Channel Analysis



=> Need Nexxim ++



Conclusions

- **Electromagnetics is key to chip/package/board simulation**



- **Model order reduction is key to bringing electromagnetics into circuit tools**

APPLICATION: PCI FB DIMMS

- **The new methodology provides an effective environment for chip/package/board co-design**

3D MODEL EXTRACTION

